CX20437

Codec

Data Sheet

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CONEXANT™

Revision Notice

Revision	Date	Comments
A	5/22/2002	Initial release.

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1 Introduction

1.1 Summary

The Conexant™ CX20437 Codec is an Integrated Analog (IA) circuit providing modem digital-to-analog and analog-to-digital conversion. It is packaged in a 32-pin LQFP. Ordering information is listed in Table 1-1.

The CX20437 Codec can serve as a line interface device between a Conexant Modem Data Pump (MDP) and the PSTN. It can also serve as a voice interface between the MDP and a microphone and speaker.

The MDP communicates with the CX20437 Codec via a serial interface. The CX20437 Codec has an 8-bit register that is used to configure the device. This register may be written to or read from via the serial interface.

The CX20437 Codec receive path consists of a microphone gain stage, line-input and mic-input anti-aliasing filters, a second order delta-sigma ADC, and a third-order sinc decimation filter. The transmit path consists of a third-order interpolation filter, a second-order delta-sigma DAC, a first-order lowpass switched capacitor filter, a second order lowpass continuous-time filter, a line-output driver, and a speaker-output driver. It has its own control registers, timing logic, serial interface, references, and microphone bias circuit.

The device is designed to run at a clock rate of 1.9584 MHz. Adjustable oversampling ratios (OSRs) are provided to allow for other master clock frequencies. Local and remote loopbacks are available for functionality and ease of testing.

The CX20437 Codec has separate digital supply (VDD) and analog supply (AVDD) pins to operate with any of the following three supply configurations: VDD and AVDD = 3.3 V, VDD and AVDD = 5 V, or VDD = 3.3 V and AVDD = 5 V. Optimum performance is obtained in the VDD = 3.3 V and AVDD = 5 V configuration.

Table 1-1. Ordering Information

Order No./Part No.	Package
20437-11	32-Pin LQFP
Note: For ordering purposes, the CX prefix may not be included in the part number. Also, the CX prefix may not appear in the part number as branded on the device.	

1.2 Features

- Line Codec
  - Delta-sigma ADC/DAC with dynamic range >70 dB
  - Line input and output for a 600 Ω PSTN interface
  - Single-ended speaker driver capable of a 150 Ω load
  - Differential line driver capable of a 600 Ω load
  - Single-ended microphone input with internal gain and filtering
  - Analog and digital filtering in both directions
  - Input/output mode selection and control
- Digital power supply (VDD) and analog power supply (AVDD) voltage
  - VDD and AVDD = 3.3 V,
  - VDD and AVDD = 5 V, or
  - VDD = 3.3 V and AVDD = 5 V
- Package
  - 32-pin LQFP

2 Hardware Interface

2.1 Hardware Interface Signals

The CX20437 Codec hardware signal interface for a typical line interface application using the CX20437 Codec is shown in Figure 2-1.

The CX20437 Codec hardware signal interface for a typical voice interface application using the CX20437 Codec is shown in Figure 2-2.

The CX20437 Codec pin assignments are shown in Figure 2-3 and are listed in Table 2-1.

The CX20437 Codec hardware interface signals are described in Table 2-2.

Figure 2-1. CX20437 Codec Hardware Interface Signals for Typical Line Interface Application

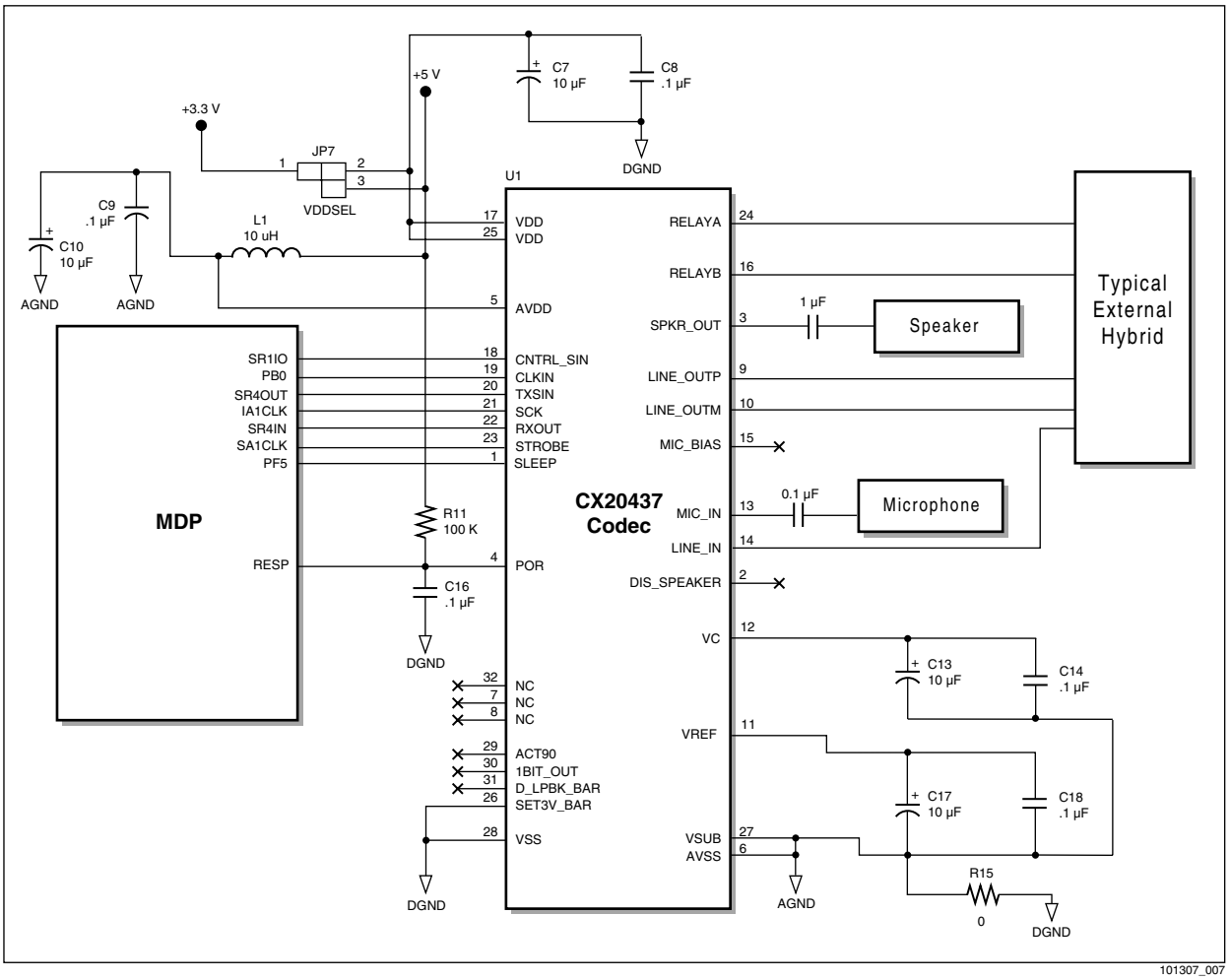


Figure 2-2. CX20437 Codec Hardware Interface Signals for Typical Voice Interface Application

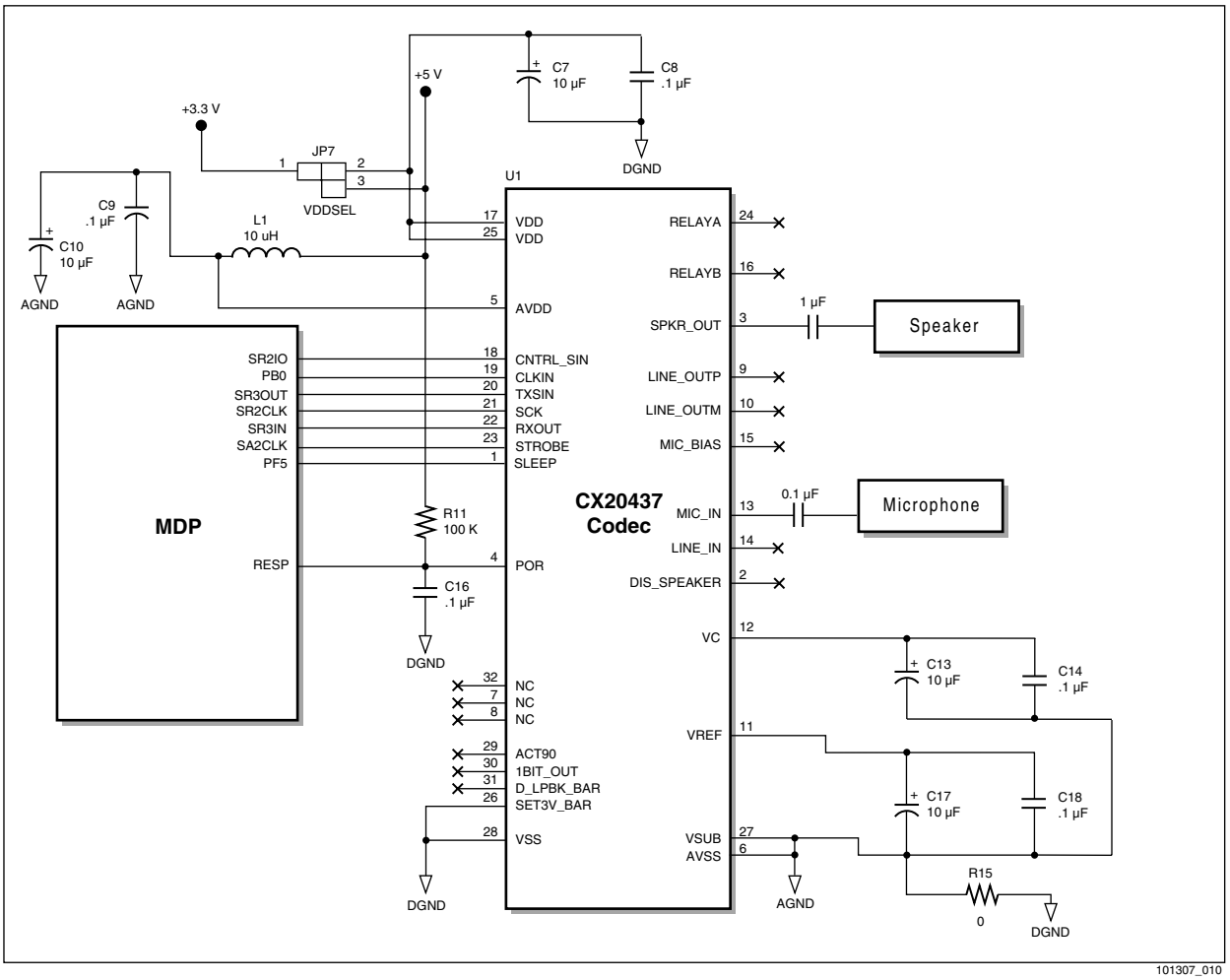


Figure 2-3. CX20437 Codec Pin Assignments for 32-Pin LQFP

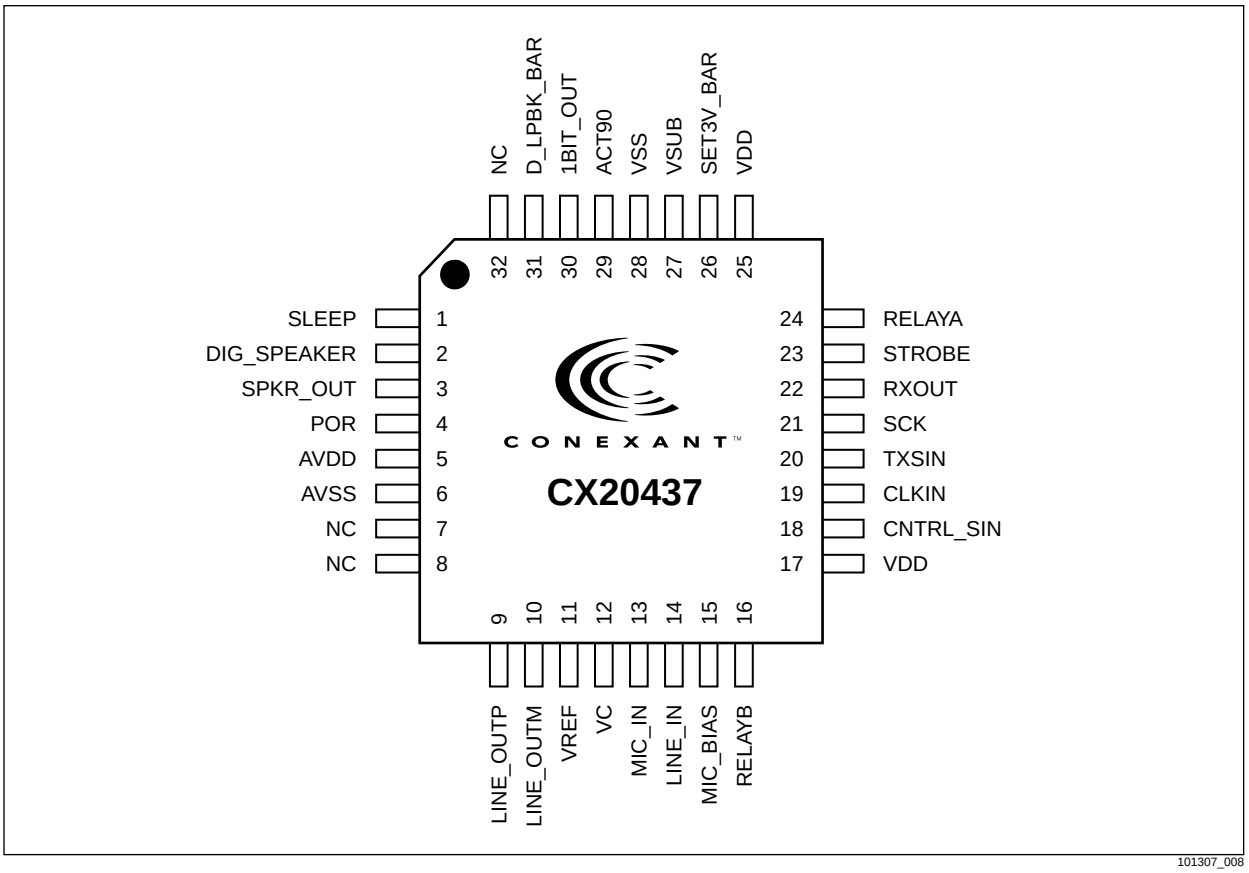


Table 2-1. CX20437 Codec Pin Signals – 32-Pin LQFP

Pin No.	Signal Name	Pin No.	Signal Name
1	SLEEP	17	VDD
2	DIG_SPEAKER	18	CNTRL_SIN
3	SPKR_OUT	19	CLKIN
4	POR	20	TXSIN
5	AVDD	21	SCK
6	AVSS	22	RXOUT
7	NC	23	STROBE
8	NC	24	RELAYA
9	LINE_OUTP	25	VDD
10	LINE_OUTM	26	SET3V_BAR
11	VREF	27	VSUB
12	VC	28	VSS
13	MIC_IN	29	ACT90
14	LINE_IN	30	1BIT_OUT
15	MIC_BIAS	31	D_LPBK_BAR
16	RELAYB	32	NC

Table 2-2. CX20437 Codec Pin Signal Definitions

Signal Name	Pin No.	I/O Type	Signal Description
Power and Ground			
VDD	17, 25	PWR	**Digital Power Supply.** Connect VDD to 5 V or 3.3 V and to digital circuits power supply filter.
AVDD	5	PWR	**Analog Power Supply.** Connect AVDD to 5 V or 3.3 V and analog circuits power supply filter.
VSS	28	GND	**Digital Ground.** Connect to GND.
AVSS	6	AGND	**Analog Ground.** Connect to AGND.
Control			
ACT90	29	I_{PU}	**10490 Control Register Format.** High = 10490 format; low = 10485 format.
1BIT_OUT	30	O	**1-bit ADC Output.** Used for factory test only. Leave open for normal operation.
D_LPBK_BAR	31	I_{PU}	**Digital Loopback Control.** Active low input asserted to loopback DAC to SINC. Used for factory test only. Leave open for normal operation.
SET3V_BAR	26	I_{PU}	**Set 5 V Analog Operation.** Sets VREF and VC levels. High = +5V operation; low = +3.3V operation.
NC	7, 8, 32	—	**No Internal Connection.** Leave open.
Host Interface			
CNTRL_SIN	18	I_{PD}	**Control Serial In.** Connect to the MDP M_CNTL (SR1IO) for line interface or to MDP V_CTRL (SR2IO) for voice interface.
TXSIN	20	I_{PD}	**Transmit Data Serial In.** Connect to the MDP M_TXSIN (SR4OUT) for line interface or to V_TXSIN (SR3OUT) for voice interface.
SCK	21	O	**Shift Clock Out.** Connect to the MDP M_SCLK (IA1CLK) for line interface or to MDP V_SCLK (SR2CLK) for voice interface.
RXOUT	22	O	**Receive Data Serial Out**. Connect to the MDP M_RXOUT (SR4IN) for line interface or to MDP V_RXOUT (SR3IN) for voice interface.
STROBE	23	O	**Strobe Out.** Connect to the MDP M_STROBE (SA1CLK) for line interface or to MDP V_STROBE (SA2CLK) for voice interface.
CLKIN	19	I_{PD}	**Clock In.** Connect to the MDP CLK (PB0).
POR	4	I_{PU}	**Power-On Reset In.** Active low reset input. Connect to MDP RESP.
SLEEP	1	I_{PD}	**Sleep Control In.** Active low input asserted to power down the CX20437 Codec. Connect to MDP PF5.
Line Interface			
RELAYA	24	O_D	**Relay A Control.** Leave open if not used.
RELAYB	16	O_D	**Relay B Control.** Leave open if not used.
LINE_OUTP	9	O_A	**Line Output Plus.** Single-ended analog data output to the telephone handset circuit. The output can drive a 300 Ω load.
LINE_OUTM	10	O_A	**Line Output Minus.** Single-ended analog data output to the telephone handset circuit. The output can drive a 300 Ω load.
LINE_IN	14	I_A	**Line Input.** Single-ended analog data input from the telephone handset circuit.
MIC_IN	13	I_A	**Microphone Input.** Single-ended analog data input from the microphone circuit.
MIC_BIAS	15	O_A	**Microphone Bias Voltage Output.** Nominal 2.2 V output. Leave open if not used.
SPKR_OUT	3	O_A	**Analog Speaker Output.** The SPKR_OUT analog output reflects the selected analog signal. When the speaker is turned off, the SPKR_OUT output is clamped to the voltage at the VC pin. The SPKR_OUT output can drive an impedance as low as 150 Ω.
DIG_SPEAKER	2	O	**Hard limited Speaker Output for PCMCIA.** Leave open.

Table 2-2. CX20437 Codec Pin Signal Definitions (Continued)

Signal Name	Pin No.	I/O Type	Signal Description
Reference			
VREF	11	O_A	**Analog Reference Voltage.** 4.10 V nom. for AVDD = 5 V; 2.35 V nom. for AVDD = 3.3 V. Connect to VC through 10 µF (polarized, + terminal to VREF) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VREF pin.
VC	12	O_A	**Analog Reference Voltage.** 2.5 V nom. for AVDD = 5 V; 1.35 V nom. for AVDD = 3.3 V. Connect to AGND through 10 µF (polarized, + terminal to VC) and 0.1 µF (ceramic) in parallel. Ensure a very close proximity between these capacitors and VC pin. Use a short path and a wide trace to AGND pin.
VSUB	27	GND	**Digital Substrate Pin.** Connect to AGND.

NOTES:

1. I/O types*:

I	Digital Input: CMOS receiver, I_{PD} = 75 kΩ pull-down, I_{PU} = 75 kΩ pull-up
O	Digital Output: CMOS driver, 2 mA, 120 Ω
O_D	Digital Output: CMOS driver, open drain
I_A	Analog Input: Analog receiver
O_A	Analog Output: Analog driver
PWR	Power
AGND	Analog ground
GND	Digital ground
AGND	Analog Ground
GND	Digital Ground

*See DC Electrical Characteristics (Table 2-3) and Analog Electrical Characteristics (Table 2-4).

Table 2-3. DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	0.4 * VDD	VDD + 0.3	V
Input low voltage	V_{IL}	-0.3	0.2 * VDD	V
Output high voltage	V_{OH}	0.8 * VDD	VDD	V
Output low voltage	V_{OL}	—	0.4	V
Input leakage current	I_{IN}	—	±10	µA
Output leakage current	I_{OUT}	—	±10	µA

Notes:

Applies to types I and O unless otherwise indicated.

All voltages referenced to ground (VSS). Currents are positive when flowing into the device.

Table 2-4. Analog Electrical Characteristics

Parameter	Symbol	Min		Max	Unit
DAC to Line Driver output at -10 dBm, 600 Ω	SNR	—	—	83 (modem) 74 (voice)	dB
Line input to ADC at –6 dBm	SNR	—	—	80	dB
Input leakage current	I_{IN}	—	—	± 10	µA
Output leakage current	I_{OUT}	—	—	± 10	µA

2.2 Electrical Characteristics

The CX20437 Codec device's recommended operating conditions, absolute maximum ratings, and current requirements are listed in Table 2-6 through Table 2-7, respectively.

Table 2-5. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
Digital supply voltage	VDD	5 ± 0.5 or 3.3 ± 0.3	V
Analog supply voltage	AVDD	5 ± 0.5 or 3.3 ± 0.3	V
Operating ambient temperature range	T_A	0 to +70	°C
Note: Voltages referenced to ground (Vss).			

Table 2-6. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Analog supply voltage (+3.3 V operation)	AVDD	-0.3 to +4.6	V
Digital supply voltage (+3.3 V operation)	VDD	-0.3 to +4.6	V
Analog supply voltage (+5 V operation)	AVDD	-0.3 to +7.0	V
Digital supply voltage (+5 V operation)	VDD	-0.3 to +7.0	V
Digital inputs	V_{IN}	–0.3 to (VDD + 0.3)	V
Analog inputs	V_{IN}	–0.3 to + (AVDD + 0.3)	V
DC input clamp current	I_{IK}	±10	mA
DC output clamp current	I_{OK}	±10	mA
Static discharge voltage (25 °C)	V_{ESD}	±2500	V
Latch-up current (25 °C)	I_{TRIG}	±150	mA
Operating temperature range	T_A	0 to +70	°C
Storage temperature range	T_{STG}	–55 to +150	°C
Relative humidity	H_{REL}	Up to 90% non-condensing, or a wet bulb temperature up to 35 °C, whichever is less.	
Note: Voltages referenced to ground (VSS).			

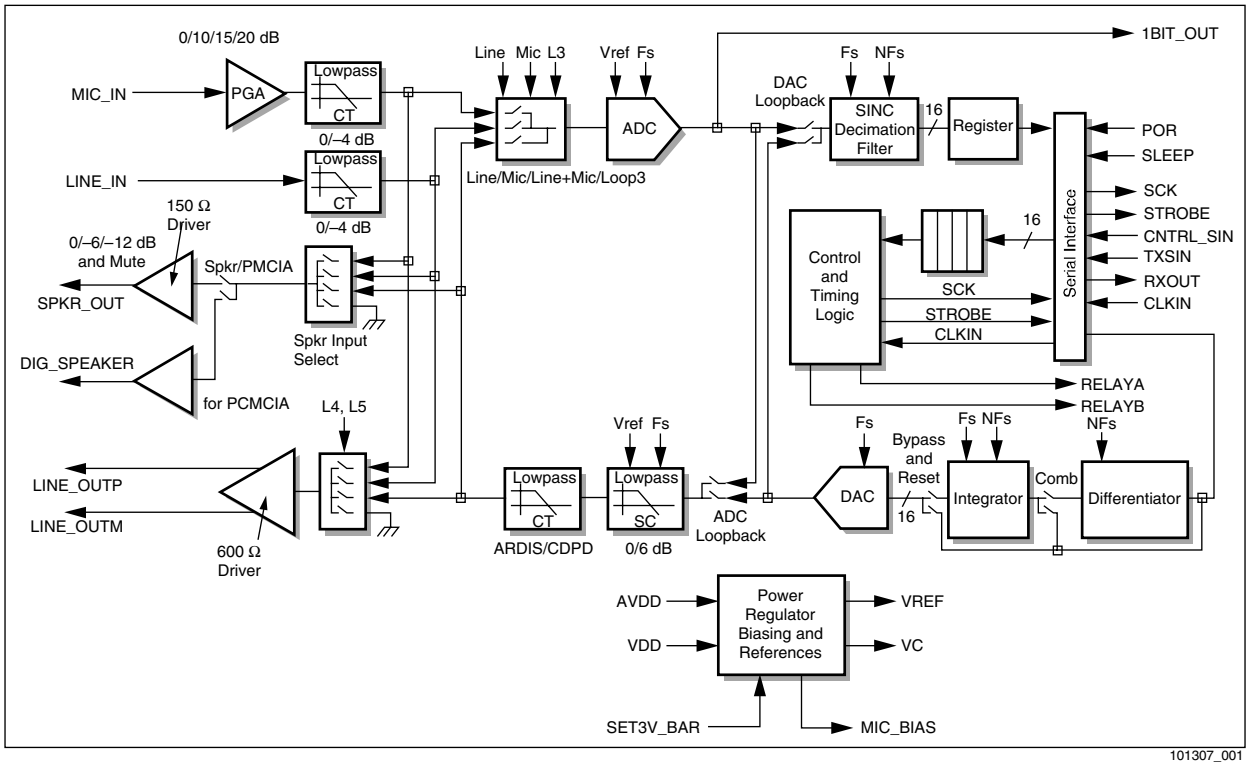
Table 2-7. Current Requirements

Mode	Typical Current @ 25 °C			
	VDD = 3.3V	VDD = 5V	AVDD = 3.3V	AVDD = 5V
Operating	0.2 mA	0.6 mA	2.3 mA	3.8 mA
Sleep	< 0.1 µA	16 µA	0.5 µA	0.5 µA

3 Functional Description

A block diagram of the CX20437 Codec is shown in Figure 3-1.

Figure 3-1. CX20437 Codec Block Diagram



3.1 Microphone Input

This input provides programmable gain for a microphone signal and low pass filtering to avoid aliasing before the signal is converted into a digital format. The microphone can be connected to this device as single-ended. A programmable gain amplifier provides four selectable gain settings from 0 to 20 dB, in steps of 5 dB. The gain in the LPF is selectable at 0 dB or –4 dB. The input impedance is 150 kΩ minimum.

3.2 Line Input

This input provides low pass filtering to avoid aliasing before the signal is converted into a digital format. The line input is single-ended and must be AC coupled into the device. The filter structure realizes a two-pole LPF filter. The gain in the LPF is selectable at 0 dB or –4 dB. The input impedance is 150 kΩ minimum. Either Line input or Microphone input or both can be selected.

3.3 A/D Converter

The ADC is a second order sigma-delta type ADC which samples at a rate between 1.024 MHz and 2.048 MHz to produce a programmable baseband sample, depending on the decimation ratio programmed in the decimation filter and the clock value.

3.4 D/A Converter

The incoming digital signal from the MDP is fed to a low-pass interpolation filter and then to a second order delta-sigma type DAC. The DAC analog output drives a switched capacitor analog filter.

The output of this filter is passed to a passive continuous-time second order low pass filter that removes signal images around the switched capacitor clock frequency.

3.5 Speaker Output

The SPKR_OUT output signal can drive a 150 Ω resistive load.

The speaker driver is intended to buffer and drive the low impedance speaker load with the signal selected on its input. The microphone input, or the line input, or the transmit output signal can be selected to be the speaker output.

The speaker driver output can be attenuated or muted. It also has a power down mode.

3.6 Line Output

The main purpose of the line output stage is to buffer the signal and drive the low impedance line load with the signal selected on its input. The microphone input, or the line input, or the transmit output signal can be selected to be the line output.

The line driver provides a 600 Ω differential output.

3.7 Power Up Condition

Upon application of both AVDD and VDD power, the power up sequence consists of:

1. The internal reset circuit becoming activated.
2. The VREF and VC generators powering up.

This power-on sequence takes approximately 50 ms.

4 Serial Interface Registers and Timing

4.1 Modes and Formats

The CX20437 Codec has two timing modes (10485 and 10490) and two format modes (10485 and 10490).

Bit D9 of Control Register 10 controls the timing mode.

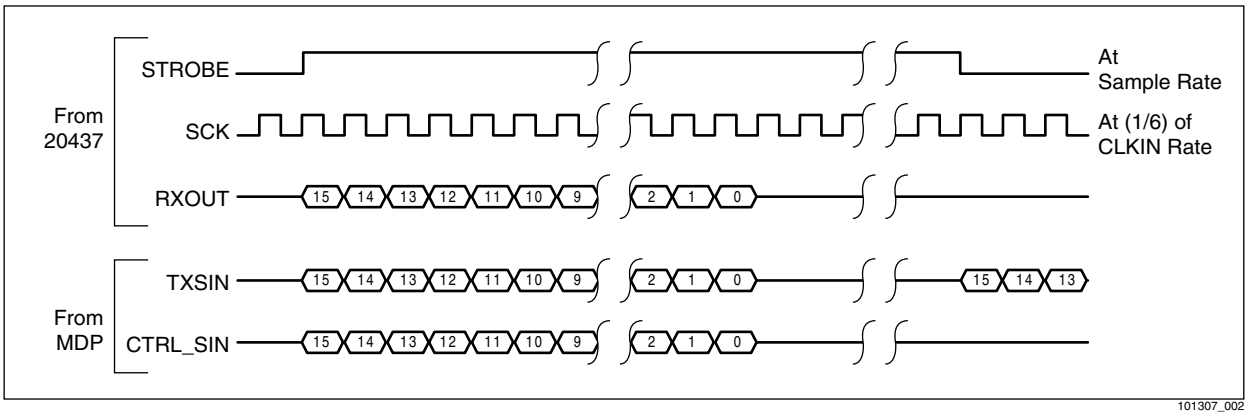
The ACT90 pin controls the format used by the control serial interface. ACT90 high (default with ACT90 open due to internal pullup) selects the 10490 Control Register format. ACT90 low selects the 10485 Control Register format.

4.1.1 10485 Timing Mode

The serial bit stream for the 10485 Timing Mode (selected by default) is illustrated in Figure 4-1.

- The SHIFT CLOCK (SCK) runs continuously at one sixth the MASTER CLOCK rate (CLKIN).
- The RX DATA output of the ADC (RXOUT) is available at the SAMPLE RATE on the rising edge of STROBE (STROBE).
- The TX DATA input (TXSIN) is read at twice the sampling rate on both edges of STROBE (STROBE).

Figure 4-1. Serial Interface Bit Stream - 10485 Timing Mode (Default)



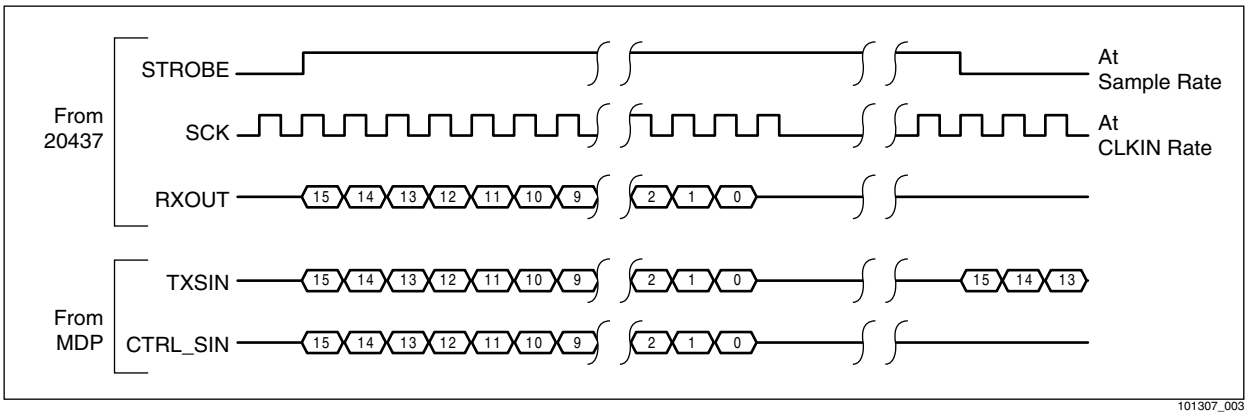
4.1.2 10490 Timing Mode

The serial bit stream for the 10490 Timing Mode is illustrated in Figure 4-2.

When the CX20437 Codec is in the 10490 Control Register Format, the 10490 Timing Mode may be selected by setting bit D9 of Control Register 10. This differs from the 10485 Timing Mode in that the shift clock runs at the master clock rate (instead of one-sixth the rate), and in burst mode: 18 pulses, 16 for the 16 data bits, plus one leading and one lagging guard pulse.

- The SHIFT CLOCK (SCK) runs in burst mode and at the MASTER CLOCK rate (CLKIN).
- The RX DATA output of the ADC (RXOUT) is available at the SAMPLE RATE on the rising edge of STROBE (STROBE).
- The TX DATA input (TXSIN) is read at twice the sampling rate on both edges of STROBE (STROBE).

Figure 4-2. Serial Interface Bit Stream - 10490 Timing Mode



4.2 10490 Control Register Format

In the 10490 Control Register Format (selected by ACT90 pin high), all of the control bits are available to the MDP. The control serial input (CNTRL_SIN) bit stream is interpreted as a 2-bit address, followed by a write/read bit, followed by 13 bits of control register data, as shown in the following sections.

4.2.1 Control Serial In Bit Order

MSB LSB

AD1	AD0	W/R	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Control Register numbers are defined in bits AD1 (MSb) and AD0 (LSb).

4.2.2 Control Register 00 (AD1 = 0; AD0 = 0)

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF	TL	TS	O7	O6	O5	O4	O3	O2	O1	O0	V2	V1

TF TL	Select source for DAC input		0 0 default
0 0	DAC interpolator bypass and reset		
0 1	Selects bits [37:22] from the interpolator		
1 0	Selects bits [36:21] from the interpolator		
1 1	Selects bits [35:20] from the interpolator		
TS	Analog transmit SC filter gain control		0 default
0	0 dB gain		
1	6 dB gain		
O[7:0]	Oversampling Ratio (OSR). OSR selection bits O[7:0] are interpreted differently in the two timing modes. The 10485 Timing Mode cannot support the full OSR range available, only O[5:0] are supported. In 10490 Timing Mode, bits O[7:6] are ignored, and bits O[5:0] are interpreted the same as in the 10485 Control Register Format.		0000000 default
11111111	N=255 OSR = 2N + 34 = 544		
|	|		
00000000	N=0 OSR = 2N + 34 = 34		
V2 V1	Speaker gain		0 0 default
0 0	Squelch (force to VC)		
1 0	0 dB		
0 1	–6 dB		
1 1	–12 dB		

4.2.3 Control Register 01 (AD1 = 0; AD0 = 1)

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LBadc	Test	M1	M0	Dth	Ctrl_A	Ctrl_E	L5	L3	L4	Ra	Dt	Rb

LBadc	ADC Loop Back—Loop back enable (ADC -> SCF)	1 active	0 default
Test	1-bit ADC output to test pad	1 active	0 default
M1 M0 0 0 0 1 1 0 1 1	Microphone gain 0 dB 10 dB 15 dB 20 dB		0 0 default
Dth	Apply dither to ADC	1 active	0 default
Ctrl_A	4 dB line input attenuation at ADC	1 active	0 default
Ctrl_E	Line input into ADC	0 active	0 default
L4 L5 0 0 0 1 1 0 1 1	Select Line Driver input TX filter Mic input Line input Line input		0 0 default
L3	Loop 3—loop back enable Local Analog Loop Back (DAC -> SCF -> CTF -> ADC -> RxOUT)	1 active	0 default
Ra	Off-hook relay (RelayA)	1 active	0 default
Dt	Line Driver squelch (force to VC)	1 active	0 default
Rb	Talk/data relay (RelayB) (ANDed with PORbar at pad)	1 active	0 default

4.2.4 Control Register 10 (AD1 = 1; AD0 = 0)

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MicA	Ctrmic	Osr90	T90/85	S_Mic	Spk1	Spk0	LBdac	Pd_ln	Pd_sk	ardis	cdpd	Tst_cr

MicA	Microphone input attenuation at ADC input	1 active	0 default
0	0 dBm Microphone input attenuation at ADC input		
1	4 dBm Microphone input attenuation at ADC input		
Ctrmic	Microphone input into ADC	1 active	0 default
0	Microphone input disabled into ADC		
1	Microphone input enabled into ADC		
Osr90	Bit selection for 10485 decimator	1 active	0 default
0	Disables dynamic range of decimators to track the OSR even in 10485 mode		
1	Enables dynamic range of decimators to track the OSR even in 10485 mode		
T90/85	Select 10490 Timing Mode		0 default
0	10485 Timing		
1	10490 Timing		
S_Mic	Toggle Mic Bias		0 default
0	Mic Bias = 2.2V		
1	Mic Bias = VC		
Spk1 Spk0	Speaker Driver input		0 0 default
0 0	Line		
0 1	Line		
1 0	TX filter		
1 1	Microphone		
LBdac	DAC Loop Back—Loop back enable (DAC -> SINC)	1 active	0 default
Pd_ln	Line Driver power down		0 default
0	Line Driver ON		
1	Line Driver OFF		
Pd_sk	Speaker Driver power down		1 default
0	Speaker Driver ON		
1	Speaker Driver OFF		
Cdpd ardis	TX Lowpass Filter pole location		0 0 default
0 0	8 kHz		
0 1	12 kHz		
1 0	25 kHz		
1 1	25 kHz		
Tst_cr	Control register contents to RXOUT	1 active	0 default
0	Disable Control register contents to RXOUT.		
1	Enable Control register contents to RXOUT.		

4.2.5 Control Register 11 (AD1 = 1; AD0 = 1)

D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Out2	Comb	M_Slv	D_spk									

Out2	2X serial output rate—enable Forces output on both clock edges, and thus OSR -> OSR/2	1 active	0 default
Comb	Bypass the differentiators in DAC interpolator	1 active	0 default
M_Slv	Master / Slave mode—enable	1 active	0 default
D_spk	Digital speaker output for PCMCIA—enable (forces Speaker Driver to power off when activated)	1 active	0 default

4.3 10485 Control Register Format

The 10485 Control Register Format (selected by ACT90 pin low) provides only a 16-bit subset of all the control bits provided to the MDP. The control serial input (CNTRL_SIN) bit stream consists of 16 bits as shown below.

4.3.1 Control Serial In Bit Order

MSB LSB

TF	TL	O6	O5	O4	O3	O2	O1	TS	L3	V2	V1	L4	Ra	Dt	Rb

TF TL 0 0 0 1 1 0 1 1	Select source for DAC input DAC interpolation filter bypass and reset Selects bits 38:23 from the interpolator Selects bits 37:22 from the interpolator Selects bits 36:21 from the interpolator		0,0 default
O[6:1] 111111 | 000000	Oversampling Ratio (OSR) {O[6:1] = B1, B2 ...B6 of 10485} N=63 OSR=2N+192 = 318 | N=0 OSR=2N+192 = 192		000000 default
TS 0 1	Analog transmit SC filter gain control 0 dB gain 6 dB gain		0 default
L3	Loop 3—loop back enable Local Analog Loop Back (DAC -> SCF -> CTF -> ADC -> RxOUT)	1 active	0 default
V2 V1 0 0 1 0 0 1 1 1	speaker gain squelch (force to VC) 0 dB –6 dB –12 dB		0 0 default
L4	Loop 4—loop back enable Remote Analog Loop Back (line in -> AAF -> line out)	1 active	0 default
Ra	Off-hook relay (RelayA)	1 active	0 default
Dt	Line Driver squelch (force to VC)	1 active	0 default
Rb	Talk/Data relay (RelayB) (ANDed with PORbar at pad)	1 active	0 default

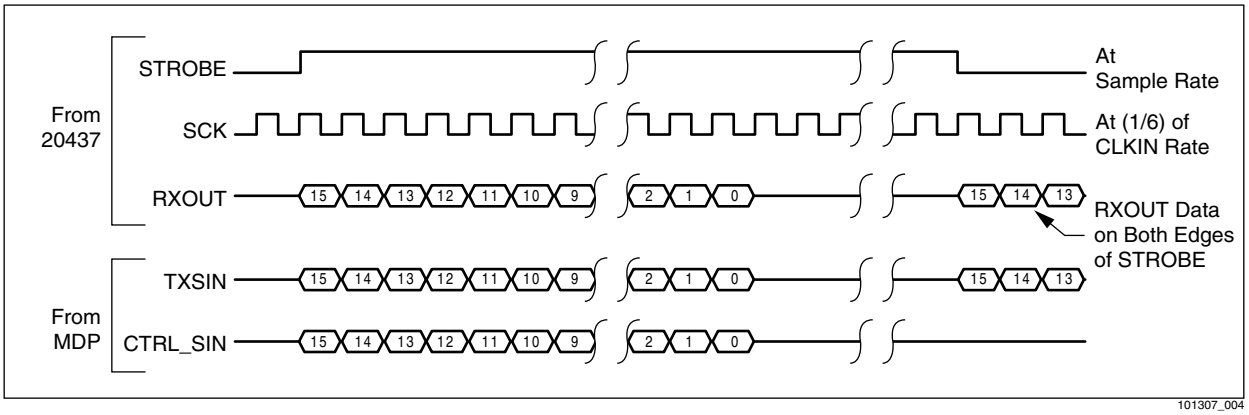
4.4 Double-Rate RX Data Output

In the 10490 Control Register Format mode, RX data may be output at double its usual rate by setting bit D12 of Control Register 11 to HIGH. RX data is then available on both edges of STROBE (versus on the rising edge only).

This feature is available for both 10485 and 10490 Timing Modes.

The Double-Rate RXOUT Data Mode bit stream for the 10485 Timing Mode is illustrated in Figure 4-3.

Figure 4-3. Double-Rate RXOUT Data Mode Bit Stream - 10485 Timing Mode



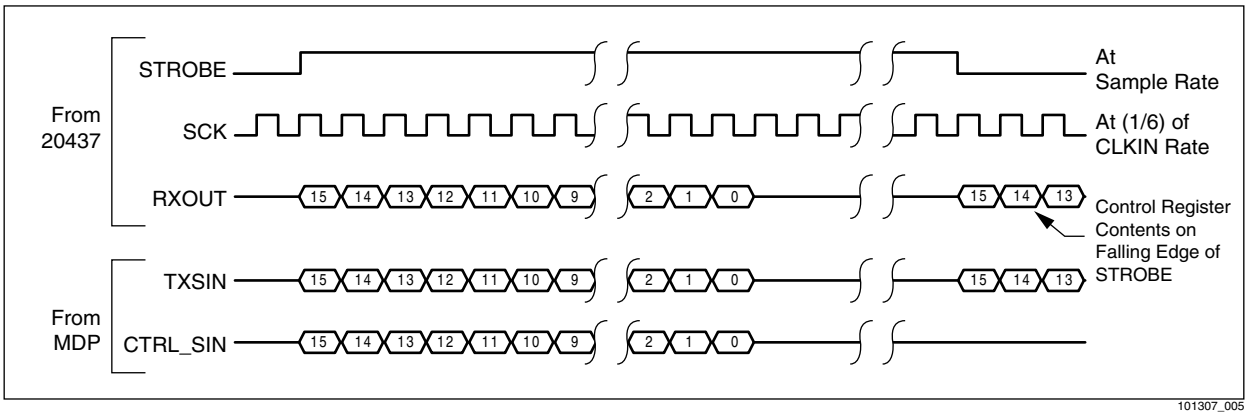
4.5 Control Register Readout

In the 10490 Control Register Format mode, the contents of any control register can be read out. Two conditions must be met: first, set bit D0 of Register 10 to HIGH, second, send the two-bit register address and set the Write/Read bit LOW (Read) in the CTRLSIN bit stream. The contents of the register will appear on the falling edge of STROBE. The output bit order is identical to the input: address, Write/Read, and register contents.

This feature is available for both 10485 and 10490 Timing Modes.

The Control Register Readout Mode bit stream for the 10485 Timing Mode is illustrated in Figure 4-4.

Figure 4-4. Control Register Readout Mode Bit Stream – 10485 Timing Mode



4.6 Serial Interface Timing

Interface timing relationship between serial interface signals and the master clock (CLKIN) are shown in Figure 4-5 and are listed in Table 4-1.

Figure 4-5. Serial Interface Waveforms

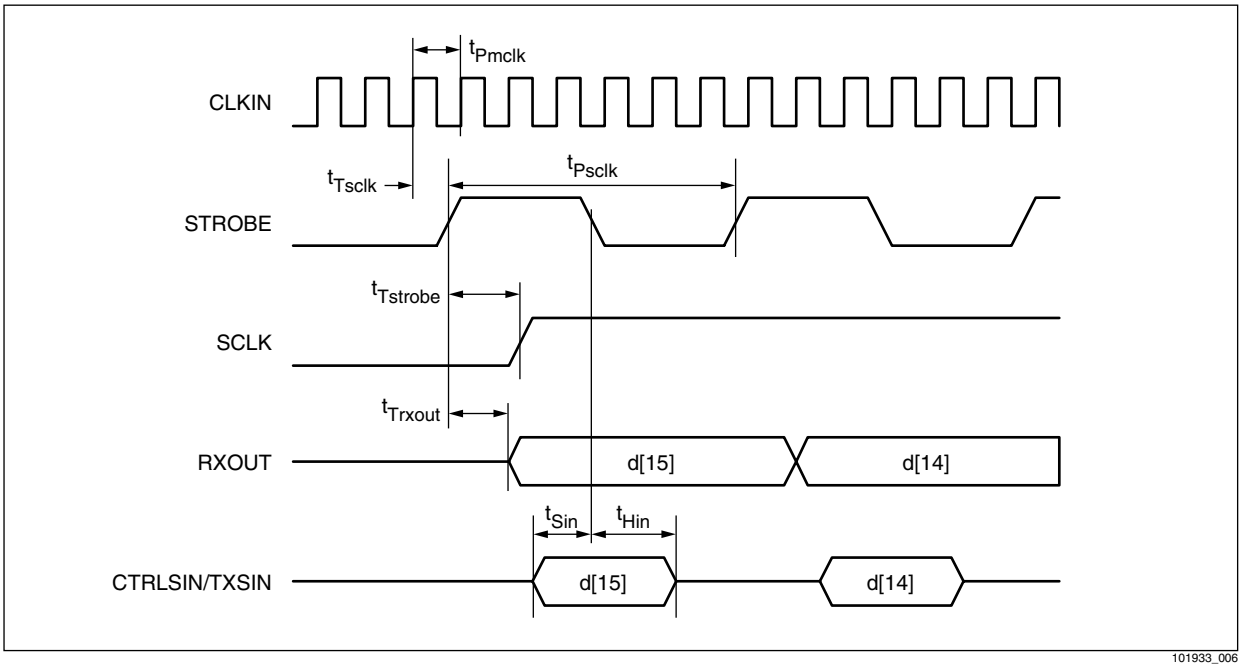


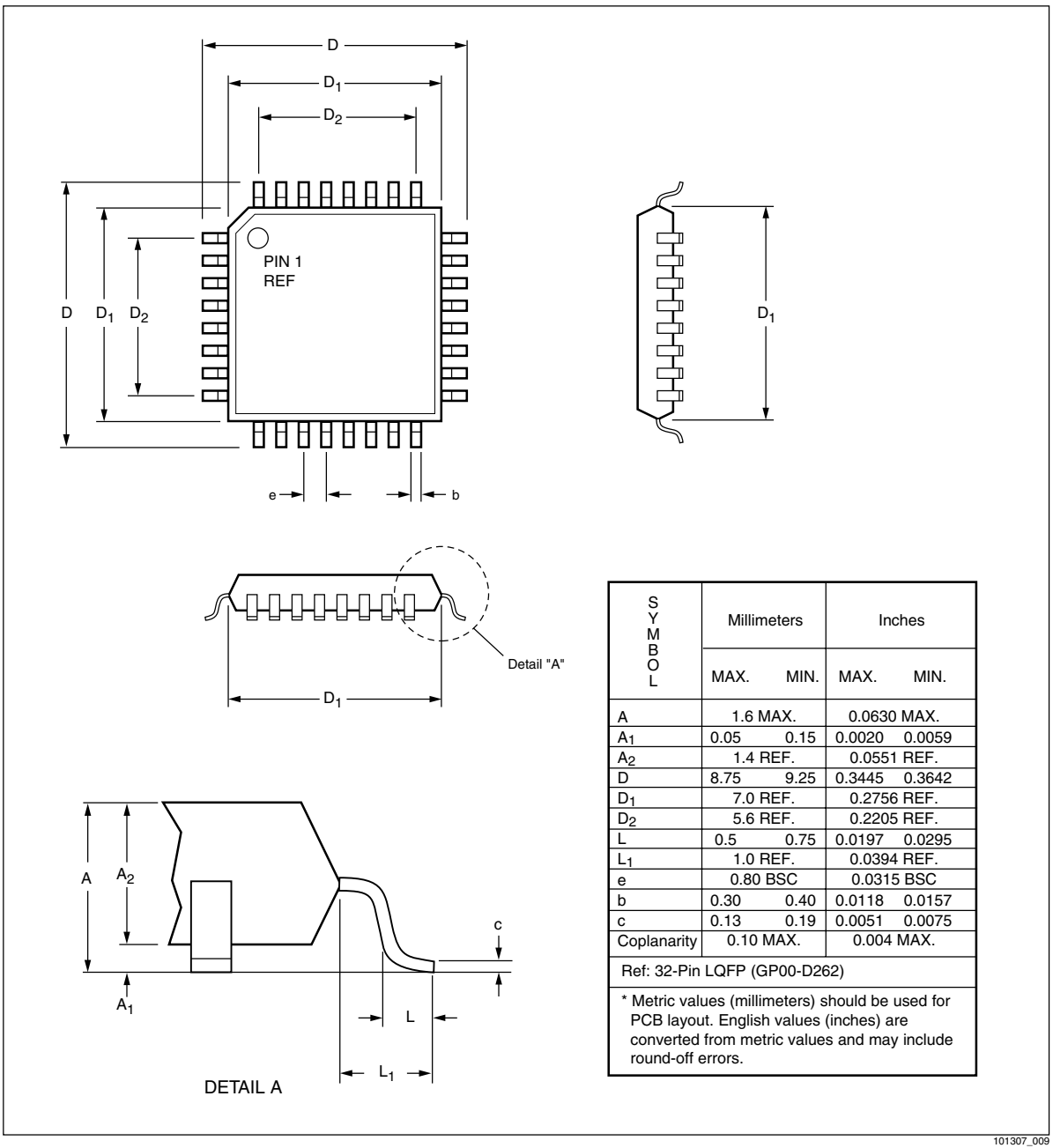
Table 4-1. Serial Interface Timing

Parameter	Description	Minimum	Typical	Maximum
t_{Pmclk}	Master clock period		1/1.9 MHz	
t_{Tsclk}	MCLK rising edge to SCLK change	0 ns	$t_{Pmclk}/6$	20 ns
t_{Psclk}	SCLK period		6x t_{Pmclk}	
$t_{Tstrobe}$	SCLK rising edge to strobe change	2 ns		20 ns
t_{Trxout}	SCLK rising edge to RXOUT valid	2 ns		20 ns
t_{Sin}	CTRLSIN/TXSIN setup before falling edge of SCLK	10 ns		
t_{Hin}	CTRLSIN/TXSIN hold after falling edge of SCLK	10 ns		

5 Package Dimensions

Package dimensions for the CX20437 Codec device are shown in Figure 5-1.

Figure 5-1. Package Dimensions—32-Pin LQFP



SYMBOL	Millimeters		Inches	
	MAX.	MIN.	MAX.	MIN.
A	1.6 MAX.		0.0630 MAX.	
A_1	0.05	0.15	0.0020	0.0059
A_2	1.4 REF.		0.0551 REF.	
D	8.75	9.25	0.3445	0.3642
D_1	7.0 REF.		0.2756 REF.	
D_2	5.6 REF.		0.2205 REF.	
L	0.5	0.75	0.0197	0.0295
L_1	1.0 REF.		0.0394 REF.	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX.		0.004 MAX.	
Ref: 32-Pin LQFP (GP00-D262)				
* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.				

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NOTES

www.conexant.com
General Information:
U.S. and Canada: (800) 854-8099
International: (949) 483-6996
Headquarters – Newport Beach
4311 Jamboree Rd.
Newport Beach, CA 92660-3007

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