Single-Chip FaxEngine Codec

Integrated Analog Device (CX20415)

The Conexant™ Single-Chip FaxEngine Integrated Analog (IA) device (CX20415) is packaged in a 32-pin TQFP package and provides the analog functionality of the modem. It serves as a voice/line codec and line interface device between the CX9450 DSP and the PSTN. The DSP communicates with the integrated analog device via a serial interface. The IA has an 8-bit register that is used to configure the device. This register may be written to or read from via the serial interface.

Codec

The voice/line codec is a monolithic CMOS integrated circuit operating off a regulated analog 5V ±10% power supply. It consists of an A/D and D/A converter path, with digital filtering and analog signal processing circuits to realize a complete ITU G.714-compatible voice frequency linear coder/decoder.

The codec is intended as a low power general purpose voice codec and line interface for applications like fax, telephony, mobile telephony, etc. A block diagram is shown in Figure 1. The diagram shows the principal functional sections of the codec and double serial interfaces to the Conexant family of DSPs.

Features

- Voice/Line Codec
  - Delta-sigma ADC/DAC with dynamic range >70 dB
  - Line input and output for 600Ω PSTN interface
  - Differential speaker driver capable of a 150 Ω load
  - Single-ended line driver capable of a 350 Ω load
  - Differential microphone input with internal gain and filtering
  - Analog and digital filtering in both directions
  - Input/output mode selection and control
- Power Requirements
  - Analog power supply: 5 V
  - Digital power supply: 3.3 V
- Package
  - Codec: 32-pin TQFP

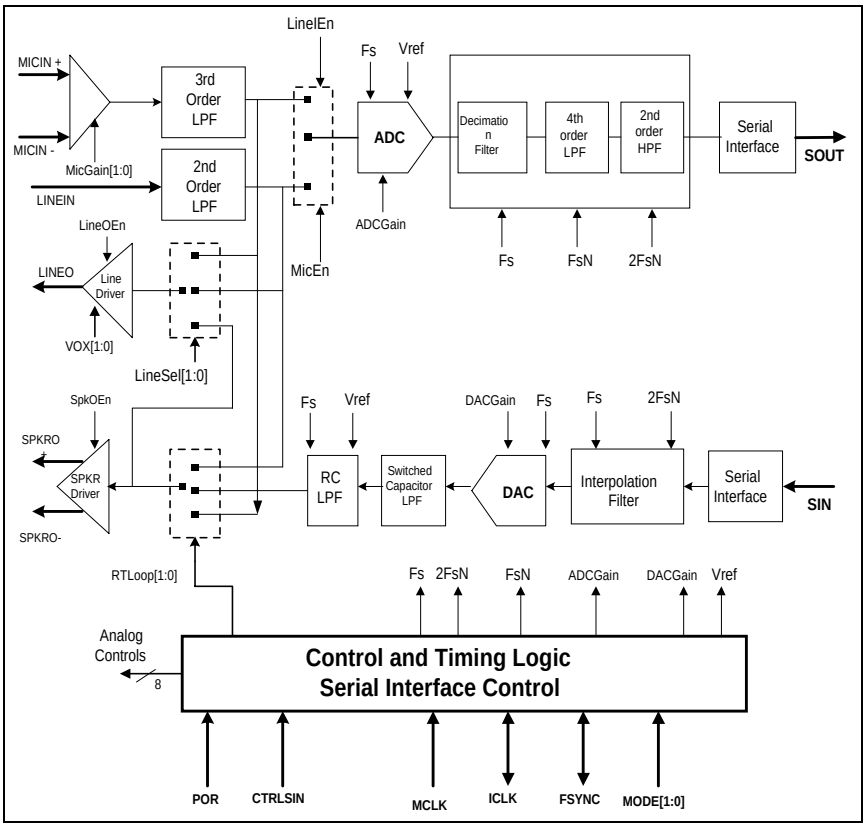

Figure 1. Integrated Analog Device Block Diagram

Single-Chip FaxEngine Family Characteristics and Ordering Information

Device Set Number	Description	Marketing Abbreviation	Single-Chip FaxEngine	Integrated Analog Device	Full-Duplex Speakerphone	DTAM Support
DSFE-L400-011	9600 Single-Chip FaxEngine	SCE109	CXD9450-25	20415-11 (one)	No	No
DSFE-L400-001	9600 Single-Chip FaxEngine with DTAM	SCE109-V	CXD9450-24	20415-11 (one)	No	Yes
DSFE-L400-021	9600 Single-Chip FaxEngine with DTAM and Speakerphone Support	SCE109-VS	CXD9450-23	20415-11 (two)	Yes	Yes
DSFE-L410-001	14400 Single-Chip FaxEngine	SCE114	CXD9450-15	20415-11 (one)	No	No
DSFE-L410-011	14400 Single-Chip FaxEngine with DTAM	SCE114-V	CXD9450-14	20415-11 (one)	No	Yes
DSFE-L410-021	14400 Single-Chip FaxEngine with DTAM and Speakerphone Support	SCE114-VS	CXD9450-13	20415-11 (two)	Yes	Yes

Revision History

Revision	Date	Comments
223DS (100550A)	08/25/99	Initial limited release of document
100550B	03/31/00	Reformat, new product name, add order info

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Microphone Input

This input provides programmable gain for a microphone signal and low pass filtering to avoid aliasing before the signal is converted into a digital format. The microphone can be connected to this device either differentially or single-ended. A programmable gain amplifier provides four selectable gain settings from 0 to 30 dB.

Line Input

This input provides low pass filtering to avoid aliasing before the signal is converted into a digital format. The line input is single-ended and is AC coupled into the device. The filter structure realizes a two pole LPF filter. The gain on the line input is fixed to 0 dB. The input impedance is 150K ohm minimum. Either Line input or Microphone input or both can be selected by using the LineIEn and MicEn control signals.

A/D Converter

The signal level out of the anti-aliasing filters can be as high as 3.2V pp. To avoid a potential overload problem, 4 dB of attenuation can be provided at the ADC input. This can be enabled using the ADC Gain control.

The ADC is a second order sigma-delta type ADC which samples at a rate between 1.024 MHz and 2.048 MHz to produce a programmable baseband sample, depending on the decimation ratio programmed in the decimation filter and the clock value. An option exists to disable the HPF biquad filter and in this case the output is available at a 16 KHz sample rate. The LPF biquad filter can also be enabled or disabled.

D/A Converter

The incoming digital signal from the DSP is fed to a low-pass interpolation filter and then to a second order delta-sigma type DAC. The DAC gain is controlled by the DACGn control signal. The DAC analog output drives a switched capacitor analog filter.

The output of this filter is a differential 2V pp or 4V pp signal depending on DAC Gain status. It is passed to a passive continuous-time second order low pass filter which removes signal images around the switched capacitor clock frequency.

Speaker Output

The SPKR+ and SPKR- signals form a differential output capable of driving a 150 Ω resistive load or a highly capacitive (100 nF) ceramic receiver via dual 75 Ω series resistors. This output is used to drive either the PSTN or a handset earpiece.

The speaker driver is intended to buffer and drive the low impedance speaker load with the signal selected on its input. The microphone input, or the line input, or the transmit output signal can be selected to be the speaker output.

The speaker driver is enabled by using the SpkOEn signal. The speaker driver has a very high input impedance, while the line driver has a moderate input impedance. Thus , the speaker driver does not introduce gain loss when interfaced to a nominal load.

Line Output

The main purpose of the line output stage is to buffer the signal and drive the low impedance line load with the signal selected on its input. The microphone input, or the line input, or the speaker output can be selected to be the output.

The line driver provides a single-ended output. Since all internal signals are differential, the line driver provides differential to single-ended conversion.

The load attenuation for the line driver output is controlled by the VOX [1:0] lines in steps of -6 dB. The line driver output can be tri-stated using the control signal LineOEn.

Serial Interface

The codec provides two serial digital interfaces for communication with the DSP. Depending upon the configuration used to communicate with the DSP, all clock signals are either provided by the DSP or by the IA.

Two modes of serial interface are available: Primary and Secondary. The first mode is used with the Primary IA which utilizes the line codec and the second mode is used with the Secondary IA which utilizes the voice codec. Both modes are used in support of the speakerphone option. Mode selection is made as follows:

IA Type	Mode 1	Mode 0
Primary	0	0
Secondary	0	1

Hardware Interface

A hardware interface diagram of a typical system design using the 32-pin package is shown in Figure 2. The 32-pin codec pin assignment diagram is shown in Figure 3.

The 32-pin codec signals are described in detail in Table 1.

Electrical Characteristics

The Integrated Analog device's absolute maximum ratings, recommended operating conditions, current and power requirements, and digital interface electrical characteristics are listed in Table 2 through Table 5, respectively.

Package Dimensions

Package dimensions for the Integrated Analog device are shown in Figure 4.

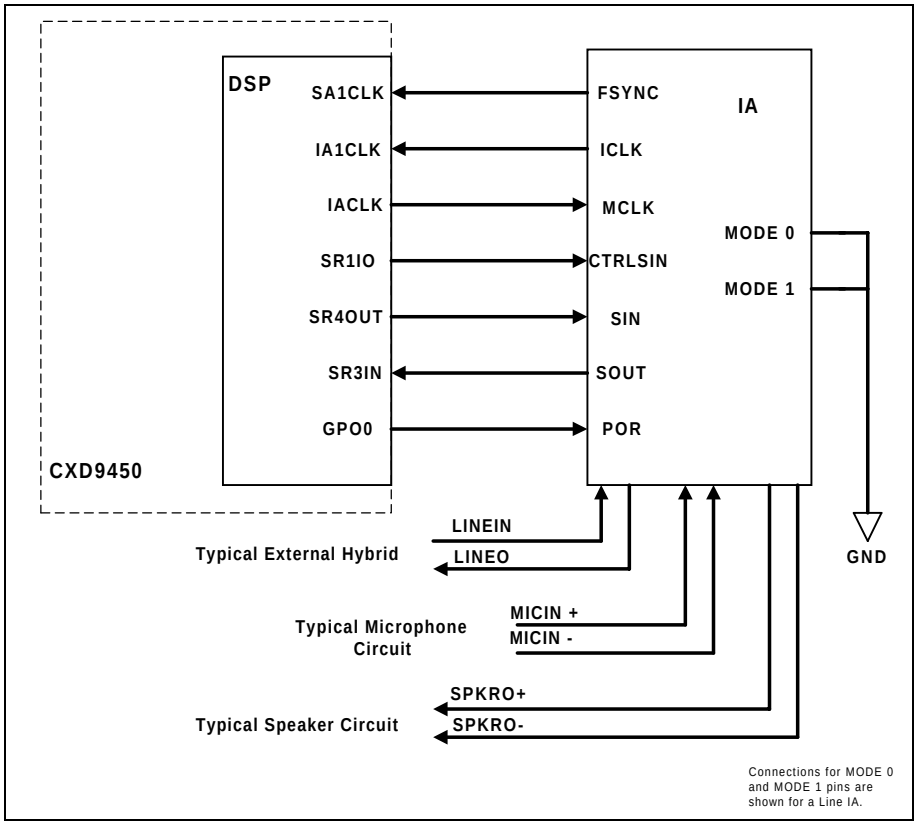


Figure 2. Hardware Interface Diagram

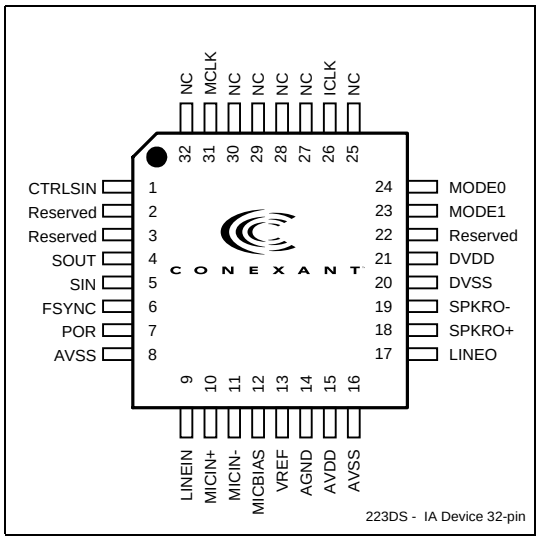


Figure 3. 32-Pin Integrated Analog Device - Pin Assignments

Table 1. Integrated Analog Device Signal Description – 32-pin TQFP

Pin #	Pin Name	Type (Note 1)	Description
1	CTRLSIN	I	Serial control data input
2	Reserved	—	No connection allowed
3	Reserved	—	No connection allowed
4	SOUT	O	Serial data output
5	SIN	I	Serial data input
6	FSYNC	I/O	Frame sync
7	POR	I	Reset input, active low
8	AVSS	I	Analog Ground
9	LINEIN	I-A	Analog input to line pre-amp, ADC channel.
10	MICIN+	I	Positive differential analog input to microphone preamplifier
11	MICIN-	I	Negative differential analog input to microphone preamplifier
12	MICBIAS	O	2.2 V nominal DC bias source for microphone
13	VREF	O-A	Analog reference voltage output. Bypass to AVSS with 0.1µF capacitor
14	AGND	I-A	Analog ground bias output. Bypass to AVSS with 0.1µF capacitor
15	AVDD	I-A	Analog power supply
16	AVSS	I-A	Analog ground
17	LINEO	O-A	Line driver output, DAC channel or filtered LINEIN, or filtered MICIN
18	SPKRO+	O-A	Positive speaker driver output, DAC channel, or filtered LINEIN, or filtered MICIN
19	SPKRO-	O-A	Negative speaker driver output, DAC channel, or filtered LINEIN, or filtered MICIN
20	DVSS	I	Digital ground
21	DVDD	I	Digital power supply
22	Reserved	—	No connection allowed
23	MODE1	I	Serial interface mode selection
24	MODE0	I	Serial interface mode selection
25	Reserved	—	No connection allowed
26	ICLK	I	Bit clock input/output for digital serial interface
27-30	NC	—	No connect
31	MCLK	I	Main clock input
32	NC	—	No connect

Note 1:

I	Digital	Input: CMOS receiver
O	Digital	Output: 4 mA driver
I-A	Analog	Input: Analog receiver
O-A	Analog	Output: Analog driver

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply voltage			V
Analog	AVDD	+7.0	
Digital	DVDD	+3.6	
Digital inputs	VIN	–0.3 ≤ VIN < DVDD + 0.3 V	V
Analog inputs	VIN	–0.3 ≤ VIN < AVDD + 0.3 V	V
DC input clamp current	IIK	±10	mA
DC output clamp current	IOK	±10	mA
Static discharge voltage (25 °C)	VESD	±2500	V
Latch-up current (25 °C)	ITRIG	±150	mA
Operating temperature range	TA	0 to +70	°C
Storage temperature range	TSTG	–55 to +150	°C
Relative humidity	HREL	Up to 90% non-condensing, or a wet bulb temperature up to 35 °C, whichever is less.	

Note: Voltages referenced to ground (Vss).

Table 3. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
Supply voltage			V
Analog	AVDD	5 ±10%	
Digital	DVDD	3.3 ± 10%	
Operating ambient temperature range	Ta	0 to +70	°C

Note: Voltages referenced to ground (Vss).

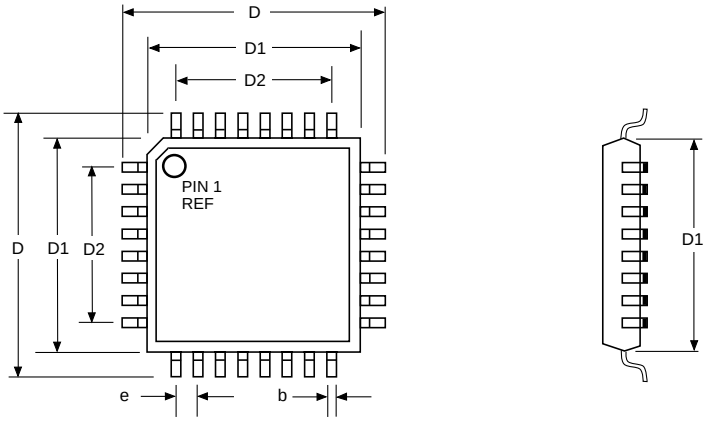
Table 4. Current Requirements

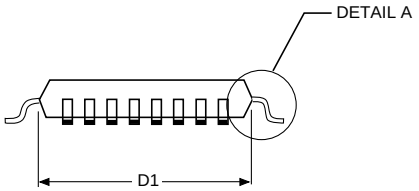
Mode	Typical Current @ 25ºC (mA)	
	3.3V	5V
Operating	4.6	6 mA
Sleep	< 0.5	10 µA

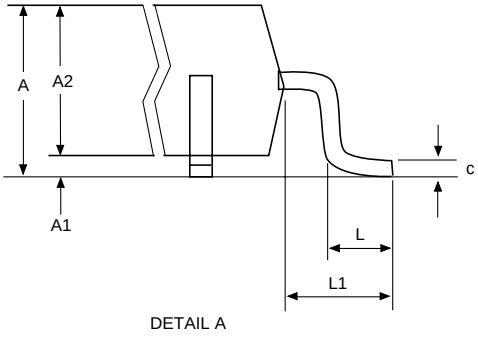
Table 5. Digital Interface Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input high voltage (Logic 1)	Vih	DVDD = 3.3 V	2.2		V
Input low voltage (Logic 0)	Vil	DVDD = 3.3 V		1.1	V
Output high voltage (Logic 1)	Voh	DVDD = 3.3 V	2.5		V
Output low voltage (Logic 0)	Vol	DVDD = 3.3 V		0.4	V
Input leakage current	Iin	DVDD = 3.3 V		±10	µA

Notes:
1. Applies to types: I and O unless otherwise indicated.
2. All voltages referenced to ground (VSS). Currents are positive when flowing into the device.







Dim.	Millimeters Min.	Millimeters Max.	Inches Min.	Inches Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	8.75	9.25	0.3445	0.3642
D1	7.0 REF		0.2756 REF	
D2	5.6 REF		0.2205 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.80 BSC		0.0315 BSC	
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity	0.10 MAX		0.004 MAX	

Ref: 32-PIN TQFP (GP00-D262)

Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-32 (040395)

Figure 4. Integrated Analog (IA) Device Package Dimensions – 32-Pin TQFP

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