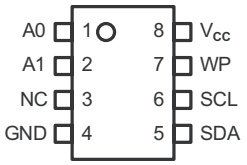
128Kbit and 256Kbit Serial I²C Bus EEPROM

DESCRIPTION

The CW24C128/256 is Electrically Erasable PROM. The device is organized as one block of 16384/32768 x 8-bit memory with 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1μA and 1mA respectively. The CW24C128/256 also has a page write capability for up to 64 bytes of data.

PIN CONFIGURATION



(Top View)

FEATURES

- Wide Voltage Operation V_{CC}= 1.8V to 5.5V
- Low-power technology
  - 1mA Active Current (Typical)
  - 1μA Standby Current (Typical)
- Internally Organized:
  - CW24C128, 16384x8 (128K bits)
  - CW24C256, 32768x8 (256K bits)
- Two-wire Serial Interface, Fully I²C Bus Compatible
- 400kHz (1.8V, 2.7V, 5V) Compatibility
- Schmitt Trigger Inputs for Noise Suppression
- Write Protect Pin for Hardware Data Protection
- Self-timed Write Cycle (5 ms max)
- Byte and Multi-byte Write
- Page Write, 64-byte Page(CW24C128/256)
- Byte, Random and Sequential Read Mode
- Automatic Address Increment
- ESD protection > 2.5kV
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- DIP8L，SOP8L Packages
- Pb-free finish available, RoHS compliant

APPLICATIONS

- Intelligent Instrument
- Industrial Controller
- Household Appliance
- Automotive Electronics
- Computer/Notebook
- Communication

ORDERING INFORMATION

Temperature Range	Package		Orderable Device	Package Qty.
-40°C to +85°C	DIP8L	Pb-Free	CW24CXXP	50 Units/Tube
	SOP8L		CW24CXXD	100 Units/Tube
			CW24CXXDR	3000 Units/R&T

XX = 128/256

BLOCK DIAGRAM

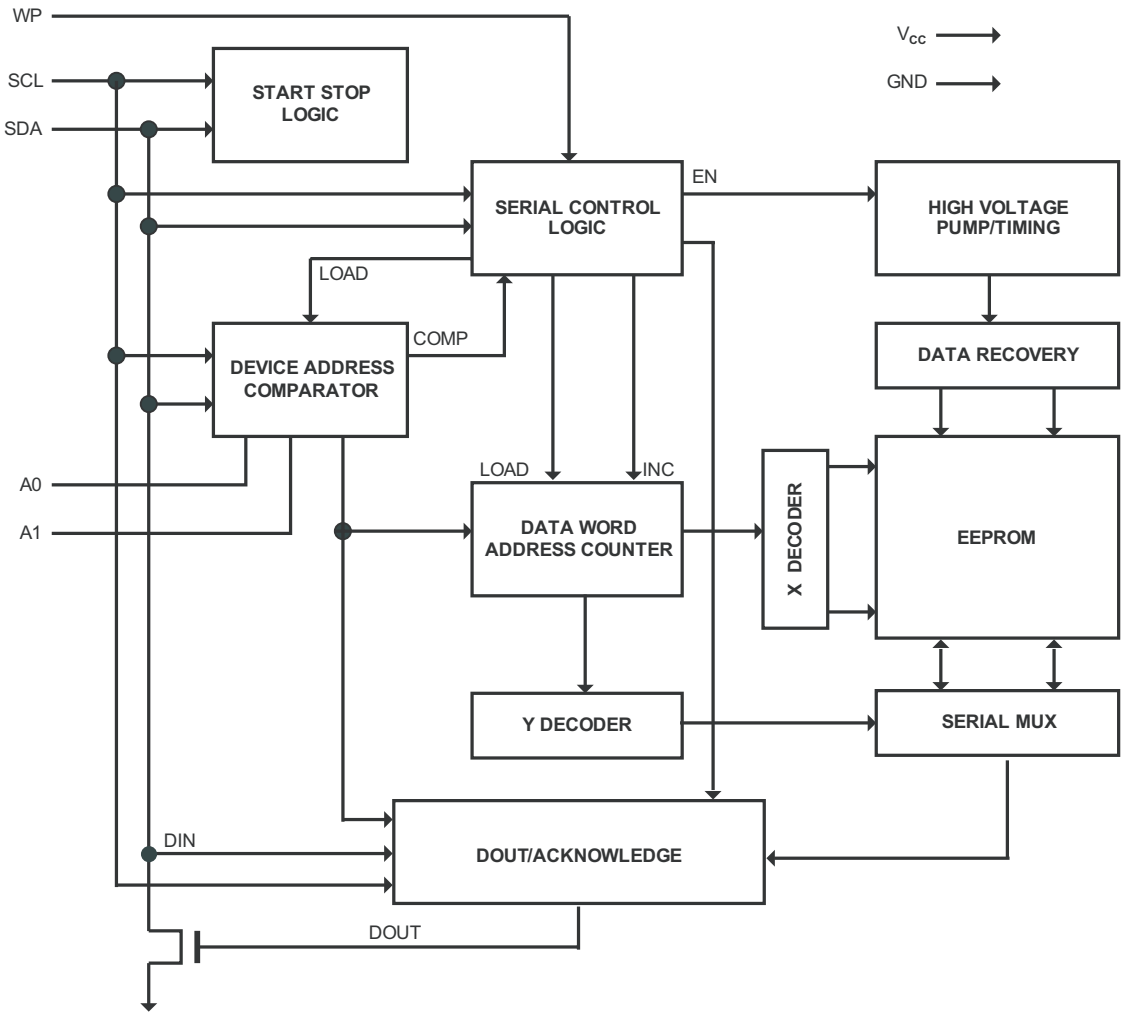


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS

(Maximum Ratings are those values beyond which damage to the device may occur.)

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	-0.3 to +6.5	V
DC Input Voltage	V_{IN}	-0.3 to V_{CC} +0.3	V
DC Output Voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V
Storage Temperature	T_{STG}	-55 to +125	°C
Electrostatic Discharge Voltage (Human Body model)	V_{ESD}	2500	V
Electrostatic Discharge Voltage (Machine model)		200	V

RECOMMENDED OPERATING CONDITIONS

(Functional operation should be restricted to the Recommended Operating Conditions.)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	1.8	5.5	V
Operating Temperature	T_A	-40	+85	°C

CAPACITANCE

(Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input/Output Capacitance (SDA)	$C_{I/O}$	$V_{I/O}$ = 0V		8	pF
Input Capacitance (A0, A1, SCL)	C_{IN}	V_{IN} = 0V		6	pF

DC ELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from: T_A = -40°C to +85°C,
V_{CC} = +1.8V to +5.5V,unless otherwise noted)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Supply Current	I_{CC}	V_{CC} =5V	Read at 400kHz		0.4	1.0	mA
			Write at 400kHz		2.0	3.0	mA
Standby Current	I_{SB}	V_{IN} = V_{CC} or GND				1.0	μA
Input Leakage Current	I_{LI}	V_{IN} = V_{CC} or GND				3.0	μA
Output Leakage Current	I_{LO}	V_{OUT} = V_{CC} or GND			0.05	3.0	μA
Input Low Level	V_{IL}			-0.6		V_{CC}×0.3	V
Input High Level	V_{IH}			V_{CC}×0.7		V_{CC}+0.5	V
Output Low Level	V_{OL3}	V_{CC} =5.0V, I_{OL} = 3.0 mA				0.4	V
	V_{OL2}	V_{CC} =3.0V, I_{OL} = 2.1 mA				0.4	V
	V_{OL1}	V_{CC} =1.8V, I_{OL} = 0.15 mA				0.2	V

AC ELECTRICAL CHARACTERISTICS

(Applicable over recommended operating range from T_A = -40°C to +85°C,
V_{CC} = +1.8V to +5.5V, C_L = 100 pF,unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Frequency, SCL	f_{SCL}	V_{CC} = 1.8V			400	kHz
		V_{CC} = 5V			400	
Clock Pulse Width Low	t_{LOW}	V_{CC} = 1.8V	1.2			μs
		V_{CC} = 5V	0.6			
Clock Pulse Width High	t_{HIGH}	V_{CC} =1.8V	0.6			μs
		V_{CC} = 5V	0.4			
Noise Suppression Time	t_I	V_{CC} = 1.8V			50	ns
		V_{CC} = 5V			50	
Clock Low to Data Out Valid	t_{AA}	V_{CC} = 1.8V	0.1		0.9	μs
		V_{CC} = 5V	0.05		0.9	
Time the bus must be free before a new transmission can start	t_{BUF}	V_{CC} = 1.8V	1.2			μs
		V_{CC} = 5V	0.5			
Start Hold Time	$t_{HD.STA}$	V_{CC} = 1.8V	0.6			μs
		V_{CC} = 5V	0.25			
Start Setup Time	$t_{SU.STA}$	V_{CC} = 1.8V	0.6			μs
		V_{CC} = 5V	0.25			
Data In Hold Time	$t_{HD.DAT}$		0			μs
Data In Setup Time	$t_{SU.DAT}$		100			ns
Inputs Rise Time	t_R				300	ns
Inputs Fall Time	t_F	V_{CC} = 1.8V			300	ns
		V_{CC} = 5V			300	
Stop Setup Time	$t_{SU.STO}$	V_{CC} = 1.8V	0.6			μs
		V_{CC} = 5V	0.25			
Data Out Hold Time	t_{DH}		50			ns
Write Cycle Time	t_{WR}				5	ms

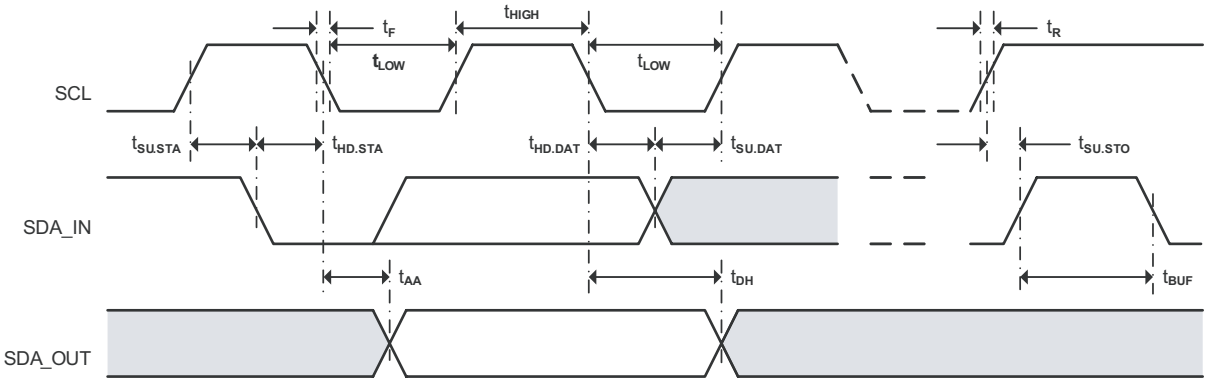
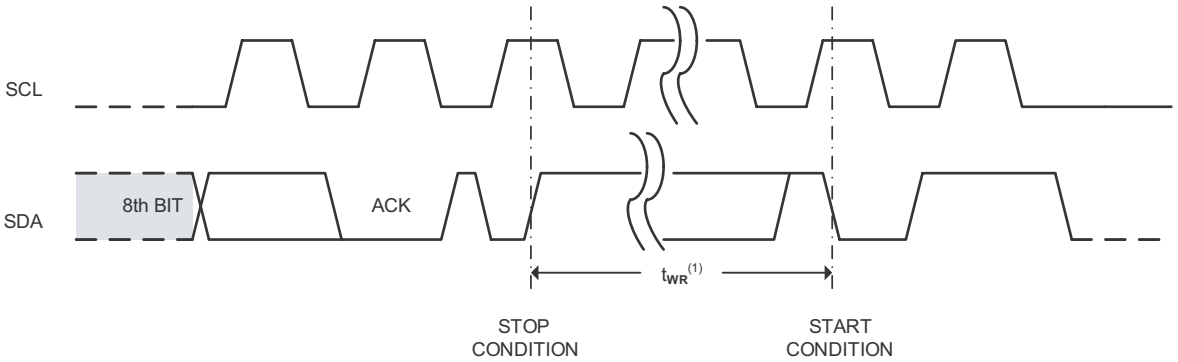


Figure 2. Bus Timing



NOTE 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 3. Write Cycle Timing

PIN DESCRIPTION

No.	Name	Function Description
1	A0	Address input. The A1 and A0 pins are device address inputs for hard wire addressing and a total of eight CW24C128/256 devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).
2	A1	
3	NC	
5	SDA	Serial address and data I/O. The SDA pin is bi-directional for serial data transfer. It is an open-drain pin, therefore the SDA bus requires a pull-up resistor to V_{CC} (typical 10kΩ).
6	SCL	Serial clock input. The SCL input is used to synchronize the data transfer to and from each EEPROM device. It's positive edge clock data into the device and negative edge clock data out of the device.
7	WP	Write protect. The WP pin that provides hardware data protection. The WP pin allows normal read/write operations when connected to ground (GND). When the WP pin is connected to V_{CC}, the write protection feature is enabled and read only.
4	GND	Circuit ground pin.
8	V_{CC}	Positive supply voltage.

MEMORY ORGANIZATION

Device	Total bits	Total pages	Bytes per page	Word address
CW24C128	128K	256	64	14-bit
CW24C256	256K	512	64	15-bit

DETAILED OPERATING INFORMATION

I²C DATA BUS AND TRANSMISSION PROTOCOL

I²C-Bus Interface

The CW24CXX supports I²C-bus transmission protocol. The I²C-bus is a bidirectional, two-line communication interface. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. A typical bus configuration using this 2-wire protocol is show in Figure 4.

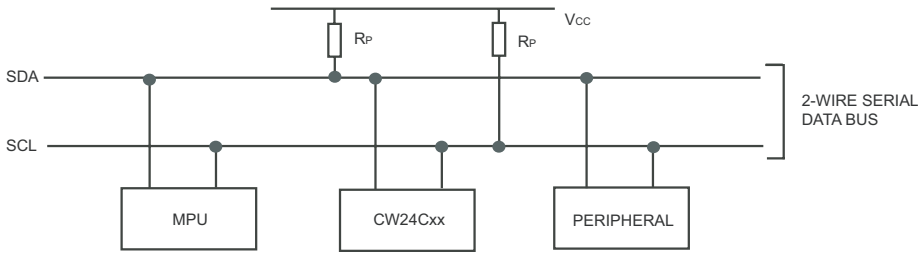


Figure 4. Typical 2-Wire Bus Configuration

DETAILED OPERATING INFORMATION(CONTINUED)

A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The master device generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The CW24CXX operates as a slave on the I²C-bus.

Data transfer may be initiated only when the bus is not busy (Both data and clock lines remain HIGH). Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Start and Stop Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition(S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P), see Figure 5.

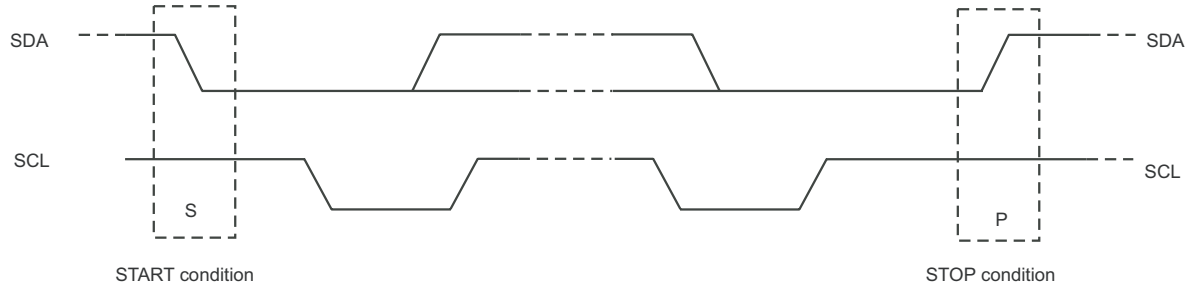


Figure 5. Definition of Start and Stop Condition

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal, as shown in Figure 6.

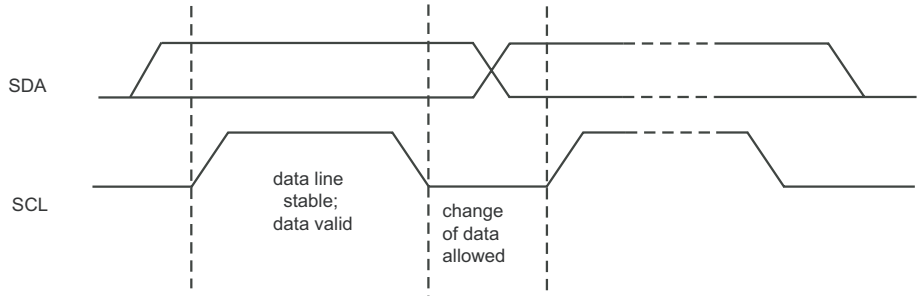


Figure 6. Bit Transfer

DETAILED OPERATING INFORMATION(CONTINUED)

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledgement after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit (see Figure 7).

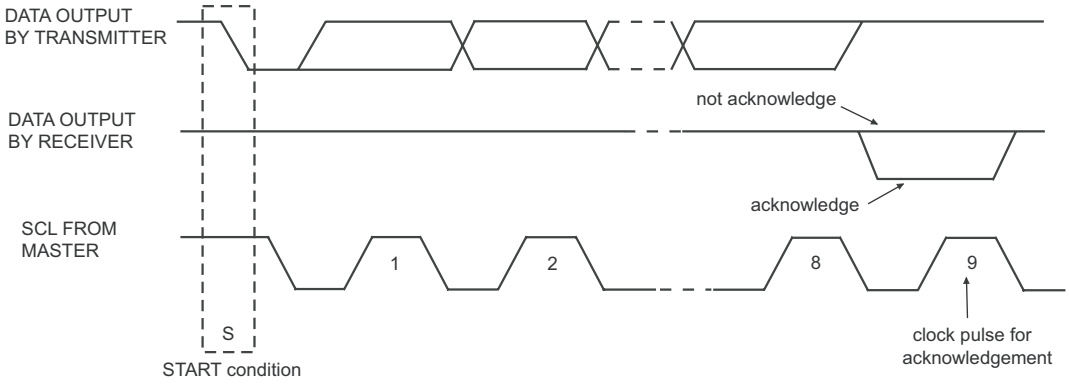


Figure 7. Acknowledge on the I2C bus

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledgement on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

DEVICE ADDRESSING

The EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 8).

The device address word consists of a mandatory "1", "0" sequence for the first five most significant bits as shown. This is common to all the Serial EEPROM devices.

The next 2 bits are the A1 and A0 device address bits for the CW24C128/256. These 2 bits must compare to their corresponding hardwired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

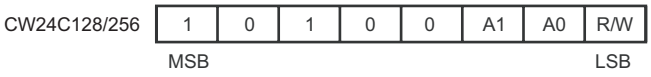


Figure 8. Device Address

DETAILED OPERATING INFORMATION(CONTINUED)

DEVICE OPERATION

Standby Mode

The EEPROM features a low-power standby mode which is enabled: (1) upon power-up and (2) after the receipt of the STOP bit and the completion of any internal operations.

Memory Reset

After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:
(1) Clock up to 9 cycles.
(2) Look for SDA high in each cycle while SCL is high.
(3) Create a start condition.

Write Operation

1. Byte Write

A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 9).

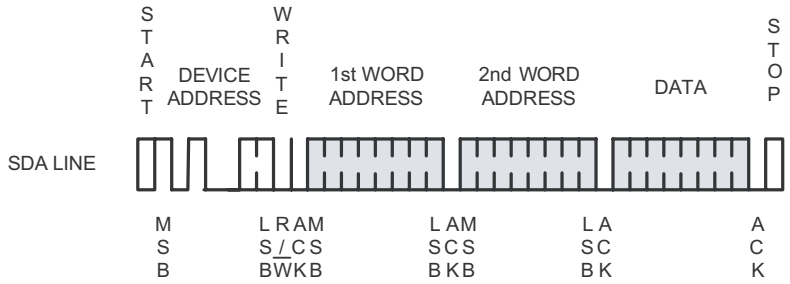


Figure 9. Byte Write

2. Page Write

The CW24C128/256 devices is capable of 64-byte page write.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 (CW24C128/256) more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 10).

The data word address lower 6 (CW24C128/256) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 (CW24C128/256) data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

DETAILED OPERATING INFORMATION(CONTINUED)

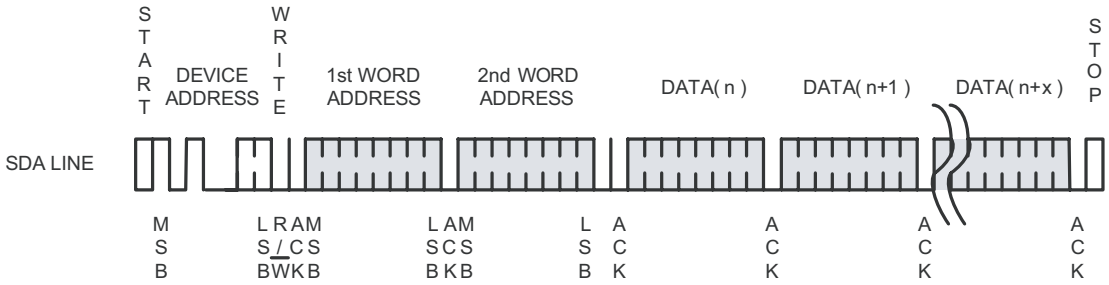


Figure 10. Page Write

3. Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.See Figure 11 for flow diagram.

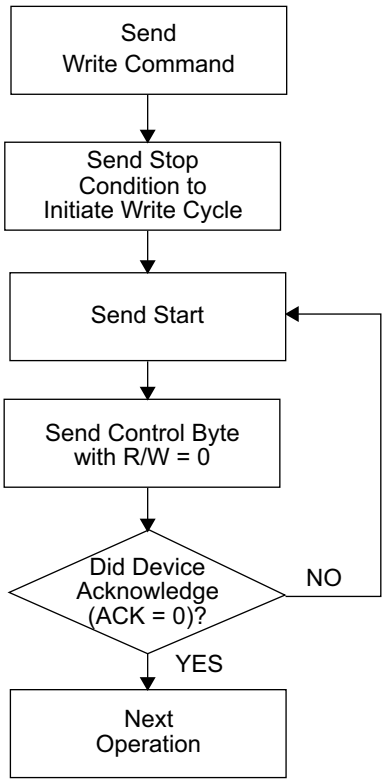


Figure 11. Acknowledge Polling Flow

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

DETAILED OPERATING INFORMATION(CONTINUED)

1. Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 12).

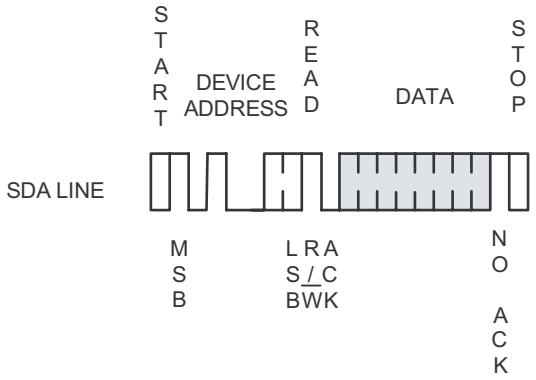


Figure 12. Current Address Read

2. Random Read

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 13).

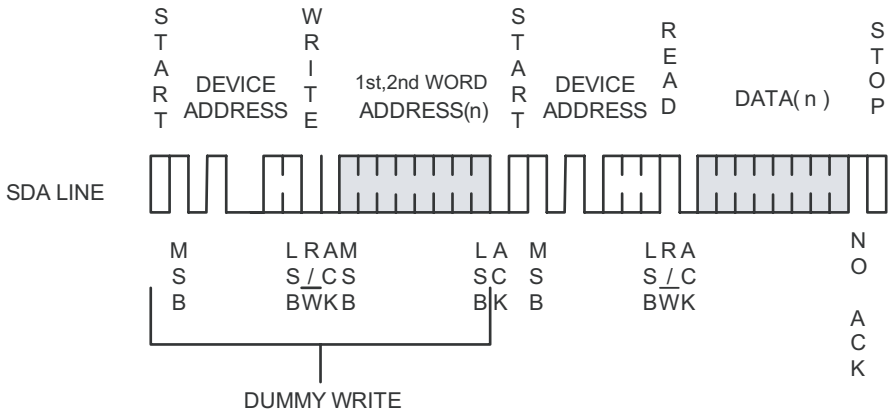


Figure 13. Random Read

DETAILED OPERATING INFORMATION(CONTINUED)

3. Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 14).

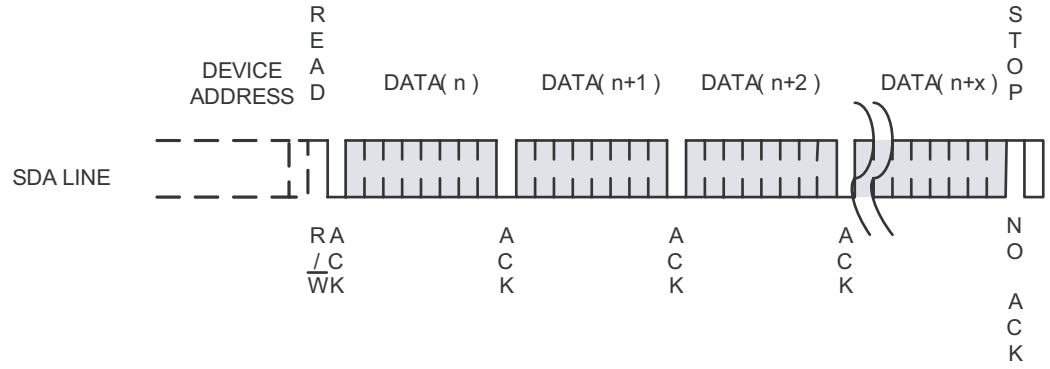


Figure 14. Sequential Read

TYPICAL APPLICATION

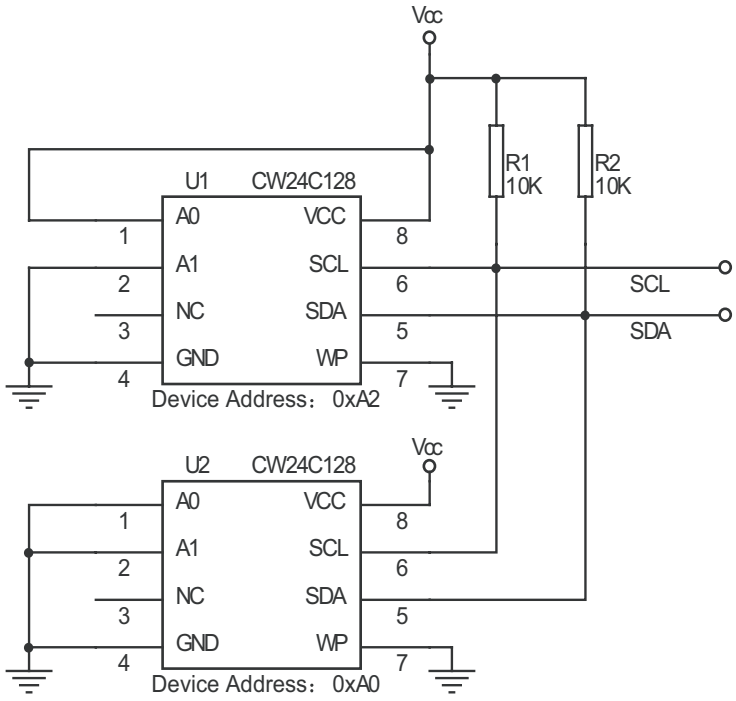
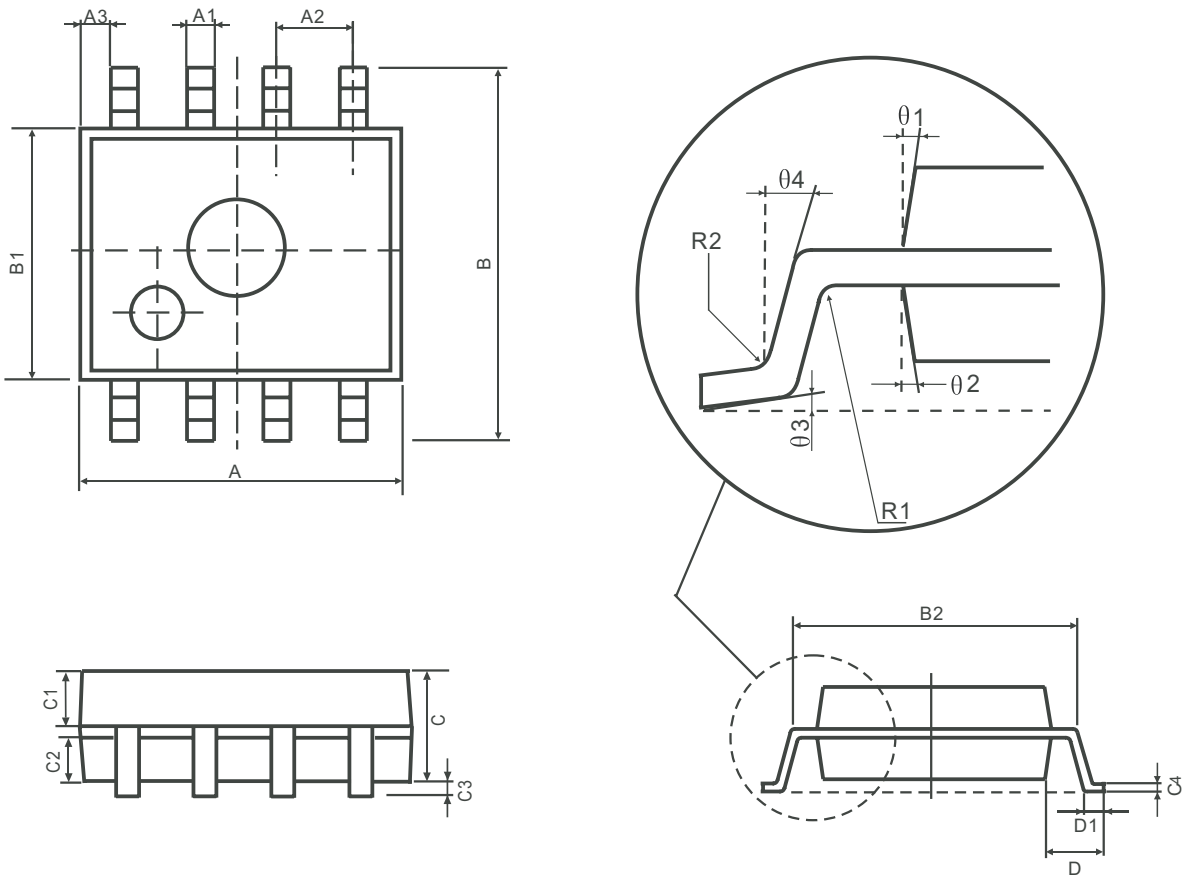


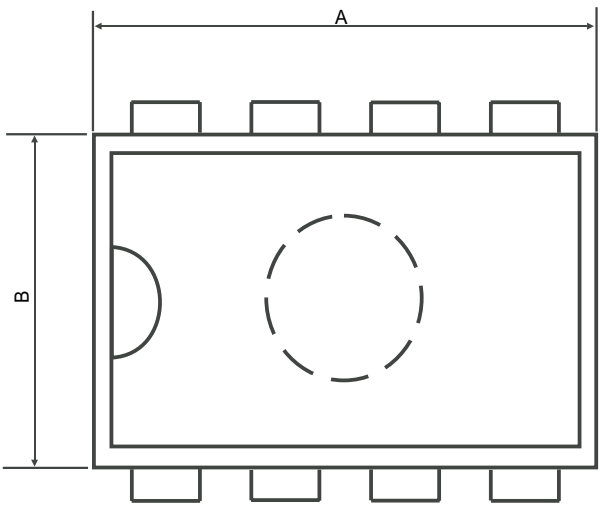
Figure 15. Cascades of Two EEPROM

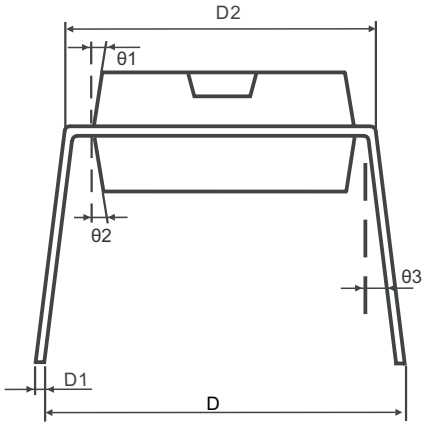
PHYSICAL DIMENSIONS
SOP8L

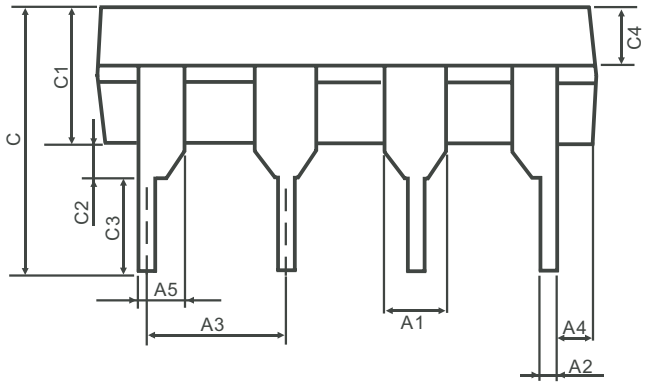


Symbol	Dimension(mm)		Symbol	Dimension(mm)	
	Min	Max		Min	Max
A	4.95	5.15	C3	0.05	0.20
A1	0.37	0.47	C4	0.20(TYP)	
A2	1.27(TYP)		D	1.05(TYP)	
A3	0.41(TYP)		D1	0.40	0.60
B	5.80	6.20	R1	0.07(TYP)	
B1	3.80	4.00	R2	0.07(TYP)	
B2	5.0(TYP)		θ1	17°(TYP)	
C	1.30	1.50	θ2	13°(TYP)	
C1	0.55	0.65	θ3	4°(TYP)	
C2	0.55	0.65	θ4	12°(TYP)	

DIP8L







Symbol	Dimension(mm)		Symbol	Dimension(mm)	
	Min	Max		Min	Max
A	9.30	9.50	C2	0.5(TYP)	
A1	1.524(TYP)		C3	3.3(TYP)	
A2	0.39	0.53	C4	1.57(TYP)	
A3	2.54(TYP)		D	8.20	8.80
A4	0.66(TYP)		D1	0.20	0.35
A5	0.99(TYP)		D2	7.62	7.87
B	6.3	6.5	θ1	8°(TYP)	
C	7.20(TYP)		θ2	8°(TYP)	
C1	3.30	3.50	θ3	5°(TYP)	