



深圳市矽源特科技有限公司
ShenZhen ChipSourceTek Technology Co., Ltd.

CS8571E

AB/D switch, 5.5W mono audio power amplifier

overview

CS8571E is a FM interference-free, Class AB amplifier and Class D amplifier with two modes Switchable 5.5W mono audio amplifier. CS8571E adopts original AERC (Adaptive Edge Rate Control) technology can provide excellent Full bandwidth EMI suppression capability, without any auxiliary design, in FCC Part15 Class B standard still has more than 20dB margin.

CS8571E does not require a filter for PWM modulation structure and gain built-in mode to reduce This reduces external components, PCB area, and system cost, and simplifies the design. Up to 90% efficiency, fast start-up time and small package size make CS8571E becomes an excellent choice for portable audio products.

CS8571E has built-in over-current protection, short-circuit protection and over-heat protection, which can effectively protect Protect the chip from being damaged under abnormal working conditions.

CS8571E provides ESOP8 package with heat sink for customers to choose The rated operating temperature range is -40°C to 85°C.

describe

Output Power

PO at 10% THD+N, VDD = 5V

RL = 4 Ω 3.40W (typical)

RL = 2 Ω 5.50W (typical)

PO at 10% THD+N, VDD = 3.6V RL = 4 Ω 1.70W

(typ.)

RL = 2 Ω 2.42W (typical)

Class AB/Class D working mode switching

function Original AERC technology provides excellent full-bandwidth EMI

suppression capability Excellent "pop-noise" noise suppression

capability Excellent low-noise

suppression function Operating voltage

range: 2.5V to 5.5V Class-D structure

without filtering Up to

90% efficiency High power supply rejection ratio (PSRR): 72dB at

217Hz Fast start-up time (35ms) Low

quiescent current (3mA) Low

shutdown current (0.1μA)

Overcurrent protection, short circuit protection and

overheating protection Lead-free packaging compliant with Rohs standards

Encapsulation

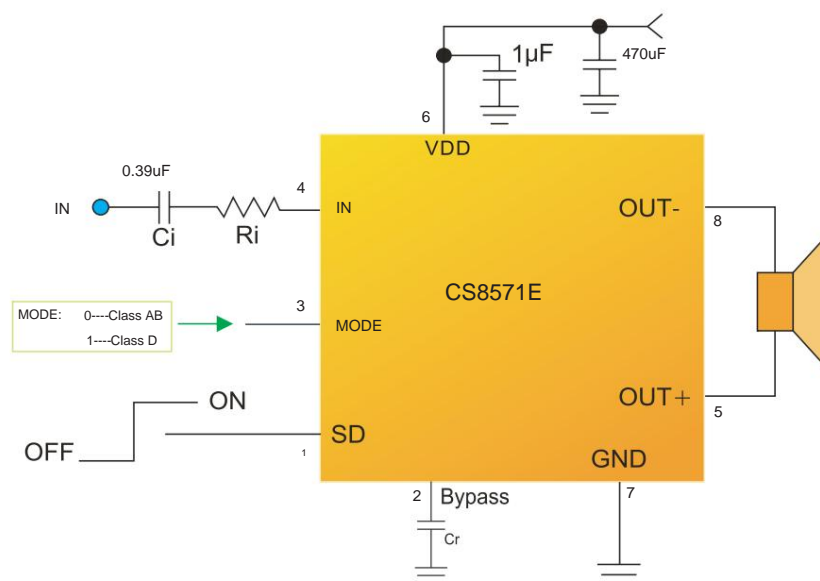
ESOP8

application

USB Speaker/Bluetooth

Speaker Amplifier

Typical application diagram



CS8571 application circuit diagram

TEL: +86-0755-27595155 27595165

FAX: +86-0755-27594792

WEB: [Http://www.ChipSourceTek.com](http://www.ChipSourceTek.com)

Email: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Oct, 2012 Rev. 1.0

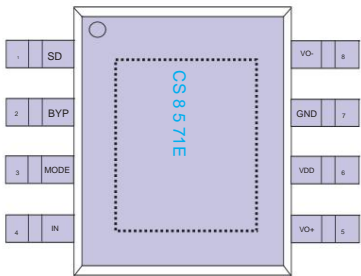


深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co. ,Ltd.

CS8571E

Pin arrangement and definition



ESOP_8L
(Top View)

Serial number	symbol	describe
1	SD	Power-off control pin, high level is effective
2	BYP	Analog reference voltage
3	MODE	Class AB/Class D switch selection, low level selects Class AB mode, high level selects Class D mode
4	IN	Audio input
5	VO+	Positive phase audio output
6	VDD	power supply
7	GND	land
8	VO-	Inverted audio output



深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co., Ltd.

CS8571E

Limit parameter table

parameter	describe	Numeric	unit
	Power supply when there is no signal input to VDD	7	V
	VI input voltage	-0.3 to VDD+0.3	V
	TJ Junction Operating Temperature Range Lead	-40 to 150	°C
T _{SDR}	Temperature (Soldering 10 Seconds)	260	°C
T _{STG}	Storage Temperature Range	-65 to 150	°C

Recommended working environment

parameter	describe	Numeric	unit
VDD	Input voltage	2.5~6.5	V
T _{AMB}	Ambient temperature range	-40~85	°C
T _J	Junction temperature range	-40~125	°C

Thermal Effects Information

parameter	describe	Numeric	unit
θ_{JA} (ESOP8) Package thermal resistance --- chip to ambient thermal resistance		40	°C/W

Ordering Information

Product Model	Package	Device Marking	Packaging Type	quantity
CS8571E	ESOP-8L	CS8571E XXXX	Tube	100 units

ESD Range

ESD range HBM (Human Body Model) _____ ±4kV

ESD range MM (machine electrostatic mode) ----- ±400V

- The above parameters are only the limit values of the device. It is not recommended that the device's operating conditions exceed these limit values, otherwise it will affect the reliability and life of the device. impact, or even cause permanent damage.
- The place where the CS8571E is placed on the PCB needs to have a heat dissipation design. The heat sink at the bottom of the CS8571E is connected to the heat dissipation area of the PCB and connected through vias. Connected to the ground.



深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co., Ltd.

CS8571E

Electrical parameters (Class D mode)

TA = 25°C (unless otherwise specified)

parameter	describe	Test Conditions Min Typ Max Unit			
FLIGHT	Output offset voltage	VIN=0V, Off=2V/V VDD=2.5V to 6.5V	5	25 mV	
PSRR	Power supply ripple rejection ratio	VDD=2.5V to 5.5V,217Hz	-70		dB
CMRR	Common Mode Rejection Ratio	Input pin short-circuit VDD = 2.5V to 5.5V	-72		dB
IDD	Quiescent Current	VDD=5.5V, no load, no filter	5		mA
		VDD=3.6V, no load, no filter	4		
ISD shutdown current			0.1		μA
rDS(ON)	Source-drain on-resistance	VDD=6.5V	210		mΩ
		VDD=3.6V	280		
	Output impedance in shutdown state	V(SHUTDOWN)=0.35V	2		kΩ
f(SW)	Modulation frequency	VDD=2.7V to 5.5V	500		KHz

Working characteristics

TA=25°C, RL = 4 Ω (unless otherwise specified)

Parameter	Description	Test	Min.	Typ.	Max.	Unit
AFTER	Output Power	conditions: VDD=5.0V, THD=10%, f=1KHz, RL=2Ω (Class AB)			5.50	W
		VDD=5.0V, THD=10%, f=1KHz, RL=2Ω (Class D)			4.90	
		VDD=5.0V, THD=10%, f=1KHz, RL=4Ω (Class AB)			3.50	
		VDD=5.0V, THD=1%, f=1KHz, RL=4Ω (Class D)			3.15	
THD+N Total	Harmonic Distortion + Noise	VDD=5.0V, Po=3.0W, f=1KHz, RL=2Ω			0.07	%
		VDD=5.0V, Po=1.0W, f=1KHz, RL=4Ω			0.04	
or	efficiency	VDD=5.0V, Po=0.6W, f=1KHz, RL=4Ω (Class D)			90	%
SNR	Signal-to-Noise Ratio	VDD=5.0V, Po=0.5W, f=1KHz, RL=2Ω			85	dB

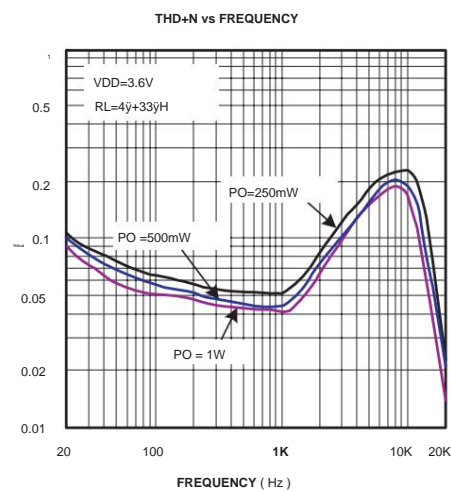
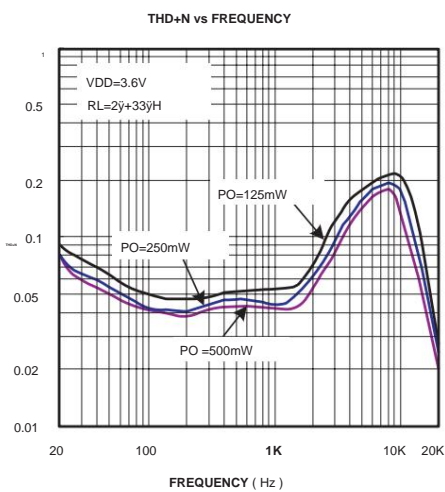
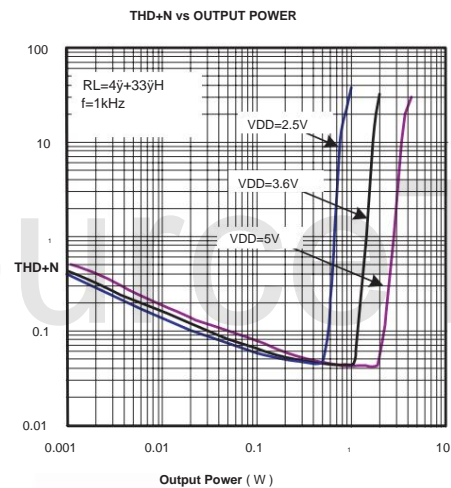
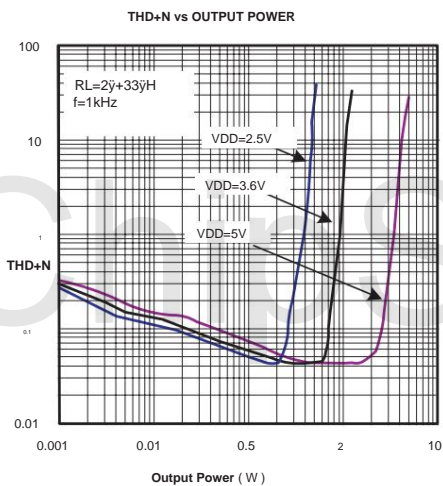
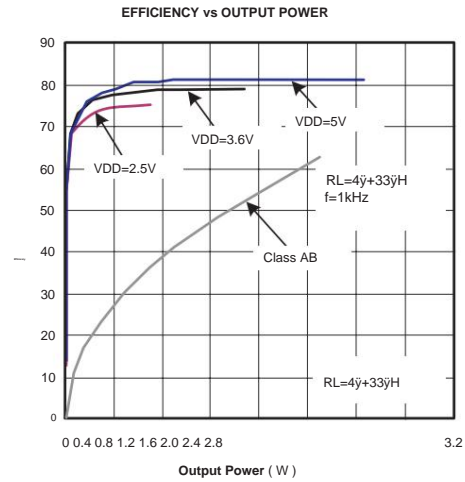
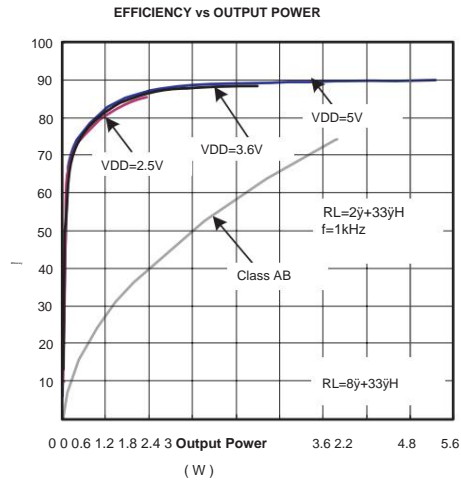


深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co., Ltd.

CS8571E

Typical characteristic curves $T_A=25^{\circ}\text{C}$, $R_L = 4\ \Omega$ (unless otherwise specified)



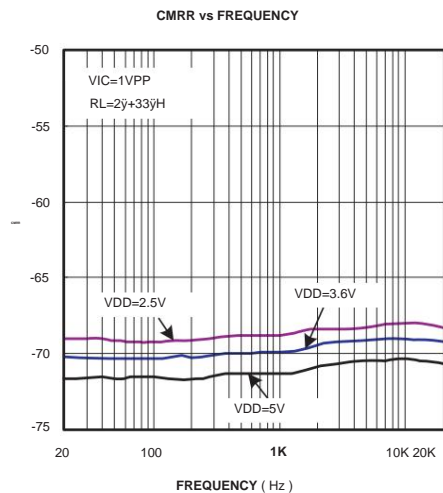
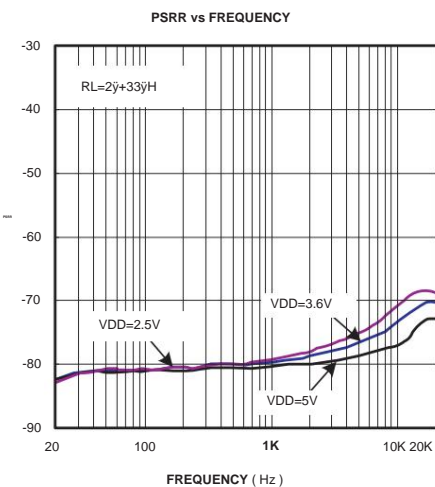
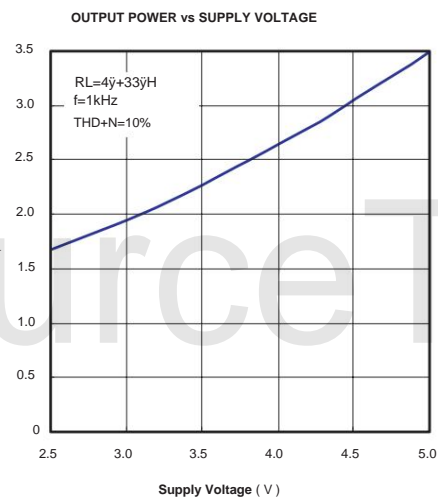
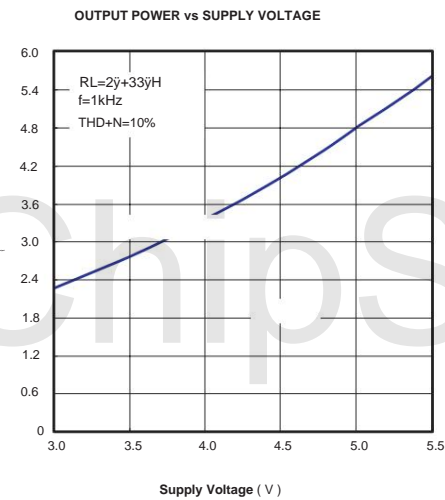
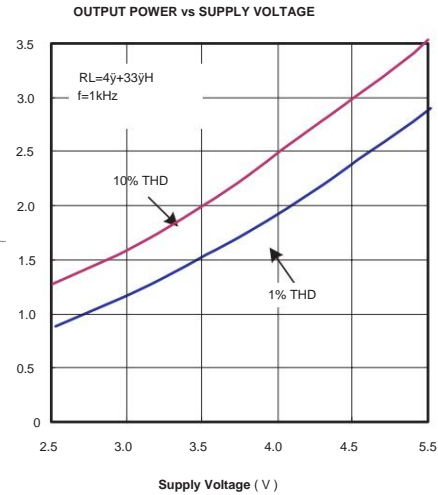
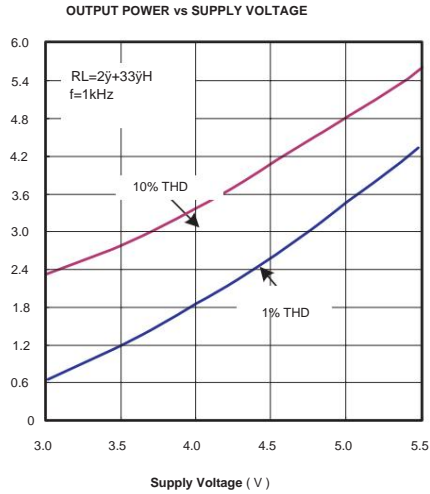


深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co., Ltd.

CS8571E

Typical characteristic curves $T_A=25^{\circ}\text{C}$, $R_L = 4\ \Omega$ (unless otherwise specified)



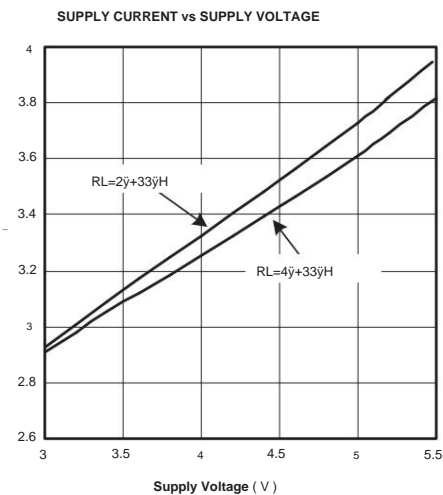
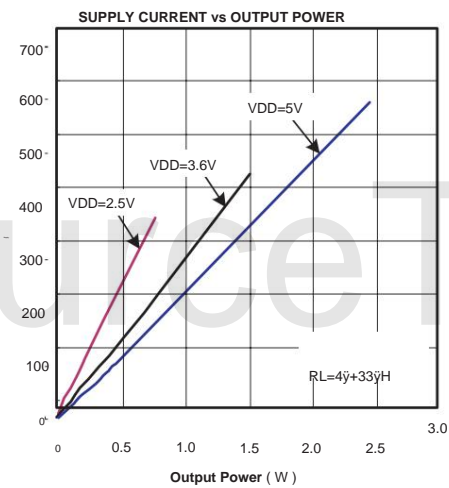
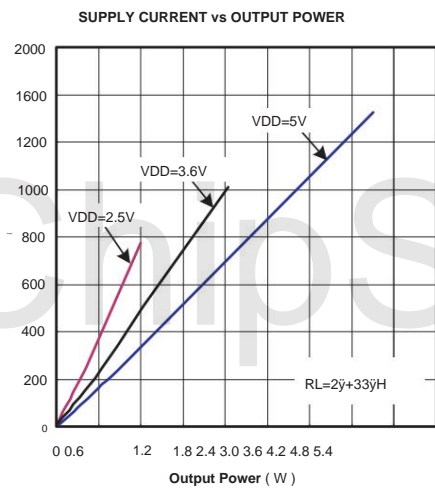
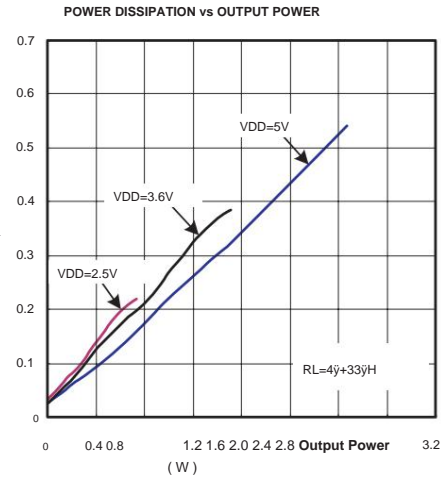
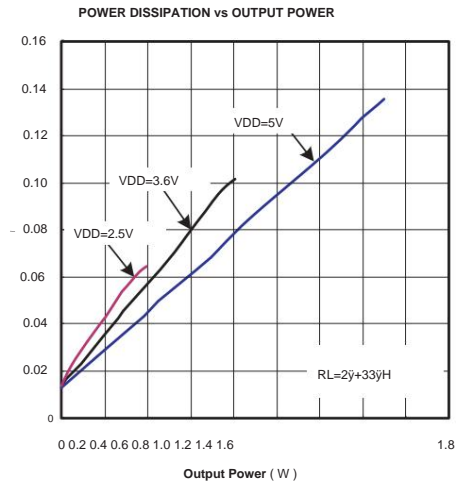


深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co., Ltd.

CS8571E

Typical characteristic curves $T_A=25^{\circ}\text{C}$, Gain = 2 V/V, $R_L = 4\ \Omega$ (unless otherwise specified)





深圳市矽源特科技有限公司
ShenZhen ChipSourceTek Technology Co., Ltd.

CS8571E

Product Features

CS8571ECS8571E is a 5.5W mono audio amplifier with FM interference-free, Class AB and Class D modes. It can provide 5.5W output power to a 2 Ω load at 5V power supply and has an efficiency of up to 90%.

CS8571E adopts proprietary AERC (Adaptive Edge Rate Control) technology, which greatly reduces EMI interference within the full audio bandwidth, and has a margin of more than 20dB under FCC standards for 60cm audio lines.

The PWM modulation structure of CS8571E in Class D mode without filter reduces the number of external components, PCB area and system cost, and simplifies the design. The chip has built-in over-current protection, over-heat protection and under-voltage protection functions, which ensure that the chip is shut down under abnormal working conditions, effectively protecting the chip from damage. When the abnormal conditions are eliminated, CS8571E has a self-recovery function to make the chip work again.

The

switching operation of the output transistor determines the high efficiency of the CS8571E Class D amplifier. In Class D mode, the output transistor acts like a current regulating switch, and the additional power consumed during the switching process is basically negligible. The power loss associated with the output stage is mainly caused by the IR generated by the MOSFET on-resistance and the power supply current. The efficiency of the CS8571E can reach 90%.

The CS8571E's Class D

mode uses a filter-free PWM modulation method, eliminating the LC filter of traditional Class D amplifiers, improving efficiency and providing a smaller, lower-cost implementation solution for the audio subsystem of portable devices.

Pop & Click Suppression The

CS8571E has a built-in proprietary timing control circuit to achieve comprehensive Pop & Click suppression, which can effectively eliminate transient noise that may occur during system power-on, power-off, wake up and shutdown operations.

Protection Circuit

During the application of CS8571E, when the chip output pin and power supply or ground short circuit occurs, or short circuit fault occurs between outputs, the overcurrent protection circuit will shut down the chip to prevent the chip from being damaged. After the short circuit fault is eliminated, CS8571E automatically resumes work. When the chip temperature is too high, the chip will also be shut down. After the temperature drops, CS8571E can continue to work normally. When the power supply voltage is too low, the chip will also be shut down. After the power supply voltage is restored, the chip will start again.

The MODE mode class

AB and class D switching control function is controlled by the MODE pin. When the MODE pin is set high, the CS8571E works in class D mode; when the MODE pin is set low, the CS8571E works in class AB mode.

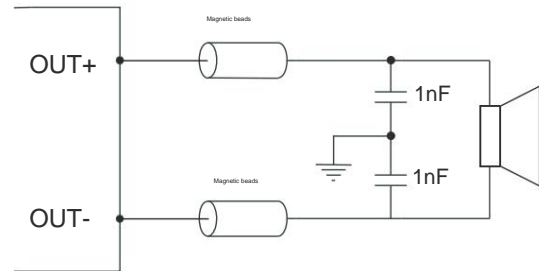
Decoupling capacitor (Cs)

CS8571E is a high-performance Class AB/Class D integrated audio amplifier. Appropriate power supply decoupling capacitors are required at the power supply end to ensure high efficiency and optimal total harmonic distortion. At the same time, in order to obtain good high-frequency transient performance, the ESR value of the capacitor is expected to be as small as possible. Generally, a typical value of 1 μ F capacitor is selected to bypass the ground. The decoupling capacitor should be placed as close to the chip VDD as possible in the layout. Placing the decoupling capacitor close to the CS8571E is very important for improving the efficiency of the CS8571E. Because any resistance or self-inductance between the device and the capacitor will lead to a decrease in efficiency. If you want to better filter out low-frequency noise, you need to add a 10 μ F or larger decoupling capacitor according to the specific application.

Application Information

Ferrite beads and

capacitors CS8571E can still meet the FCC standard for a 60cm audio line without ferrite beads and capacitors. When the output audio line is too long or the device layout is close to EMI sensitive devices, it is recommended to use ferrite beads and capacitors. The ferrite beads and capacitors should be placed as close to the CS8571E as possible, as shown in the figure below.



Input capacitor (C_{in}) A high

pass filter is formed between the input resistor and the input capacitor, and its cut-off frequency is as follows:

$$f_c = \frac{1}{2\pi R_{in} C_{in}}$$

The value of the input capacitor is very important. It is generally believed that it directly affects the low-frequency performance of the circuit. The speaker in the wireless phone usually does not respond well to low-frequency signals. In the application, a relatively large f_c can be selected to filter out the interference introduced by 217Hz noise. Good matching between capacitors is helpful to improve the overall performance of the chip and the suppression of Pop & Click, so it is required to select capacitors with an accuracy of 10% or less.



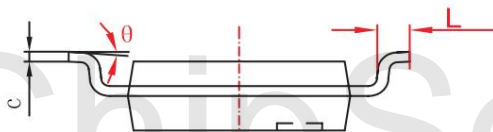
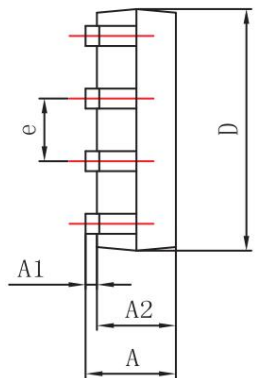
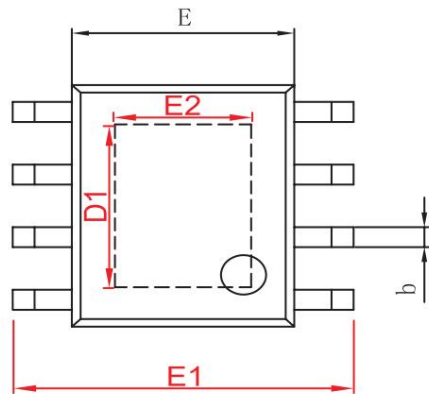
深圳市矽源特科技有限公司

ShenZhen ChipSourceTek Technology Co. ,Ltd.

CS8571E

Packaging information

CS8571E ESOP_8L



character	Dimensions In Millimeters Min Max				Dimensions In Inches	
	1.350	1.750	0.050	0.150	1.350	My Max
A	1.550	0.330	0.510	0.170	0.250	0.053 0.069
A1	4.700	5.100	3.202	3.402	3.800	0.004 0.010
A2	4.000	5.800	6.200	2.313	2.513	0.053 0.061
b	1.270(BSC)	1.270				0.013 0.020
c						0.006 0.010
D						0.185 0.200
D1						0.126 0.134
AND						0.150 0.157
E1						0.228 0.244
E2						0.091 0.099
and						0.050(BSC)
L	0.400	0°				0.016 0.050
i			8°		0°	8°

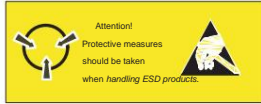
Notes:

- (1) All dimensions are in millimeters
(2) Refer to JEDEC MO-187 standard



深圳市矽源特科技有限公司
ShenZhen ChipSourceTek Technology Co. ,Ltd.

CS8571E



MOS circuit operation precautions: Static electricity

can be generated in many places. Taking the following precautions can effectively prevent MOS circuits from being damaged by electrostatic discharge:

- Operators must be grounded using an anti-static wrist strap.
- The equipment casing must be grounded.
- Tools used during assembly must be grounded.
- Conductive packaging or antistatic materials must be used for packaging or transportation.

ChipSourceTek