CapStone

CS5801 Datasheet

HDMI2.0b to DisplayPort1.4 converter

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1 Introduction

The CS5801 is a HDMI2.0b to DP1.4a converter. CS5801 has a HDMI2.0b input and the maximum bandwidth is up to 18Gbps. It supports the highest resolutions of 4k@60Hz. For DP1.4 output, it consists of 4 data lanes, supporting 1.62Gbps, 2.7Gbps, 5.4Gbps link rate. The build-in optional SSC function reduces EMI effect.

The embedded MCU is based on a 32-bit RISC-V core with internal serial flash.

The CS5801 is suitable for multiple market segments and display applications, such as monitor, Dongles, Mobile systems, and embedded applications.

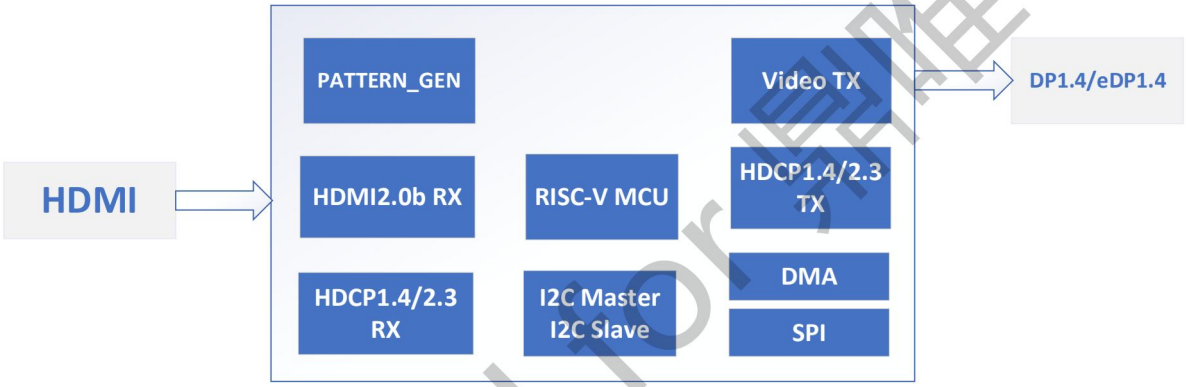


Figure 1-1 CS5801 Block Diagram

2 Features

General

- HDMI specification v2.0b compliant receiver, data rate up to 6-Gbps per channel
- VESA DisplayPort™ (DP) v1.4 compliant transmitter
- VESA embedded DisplayPort™ (eDP) v1.4 compliant transmitter
- Support both HDCP 1.4 & HDCP2.3 with on-chip keys
- Support RGB 4:4:4 8/10bit bpc and YCbCr 4:4:4, 4:2:2, 8/10bit bpc
- AUX channel, I2C host interface for chip control
- Embedded EDID
- Embedded 32-bit RISC-V with SPI flash controller
- Require only one crystal to generate all timing

HDMI Digital Input

- HDMI 2.0b compliant
- Support 6, 8, 10bpc
- Support DVI mode
- Support HDCP 1.4/2.3
- Max data rate up to 6-Gbps per channel
- Support up to 3840 x 2160@60Hz or 4096x2160@60Hz

eDP/DP Output

- VESA embedded DisplayPort™ (eDP) v1.4. Support 4-lane up to HBR2(5.4Gbps) output
- Support 6, 8, 10bpc, RGB output
- Support ASSR
- Support 1Mbps AUX channel

Embedded MCU

- 32-bit RISC-V core
- Support I2C Master and Slave up to 400-KHz.
- Support SPI controller for internal serial flash
- Support one UART for debug purpose

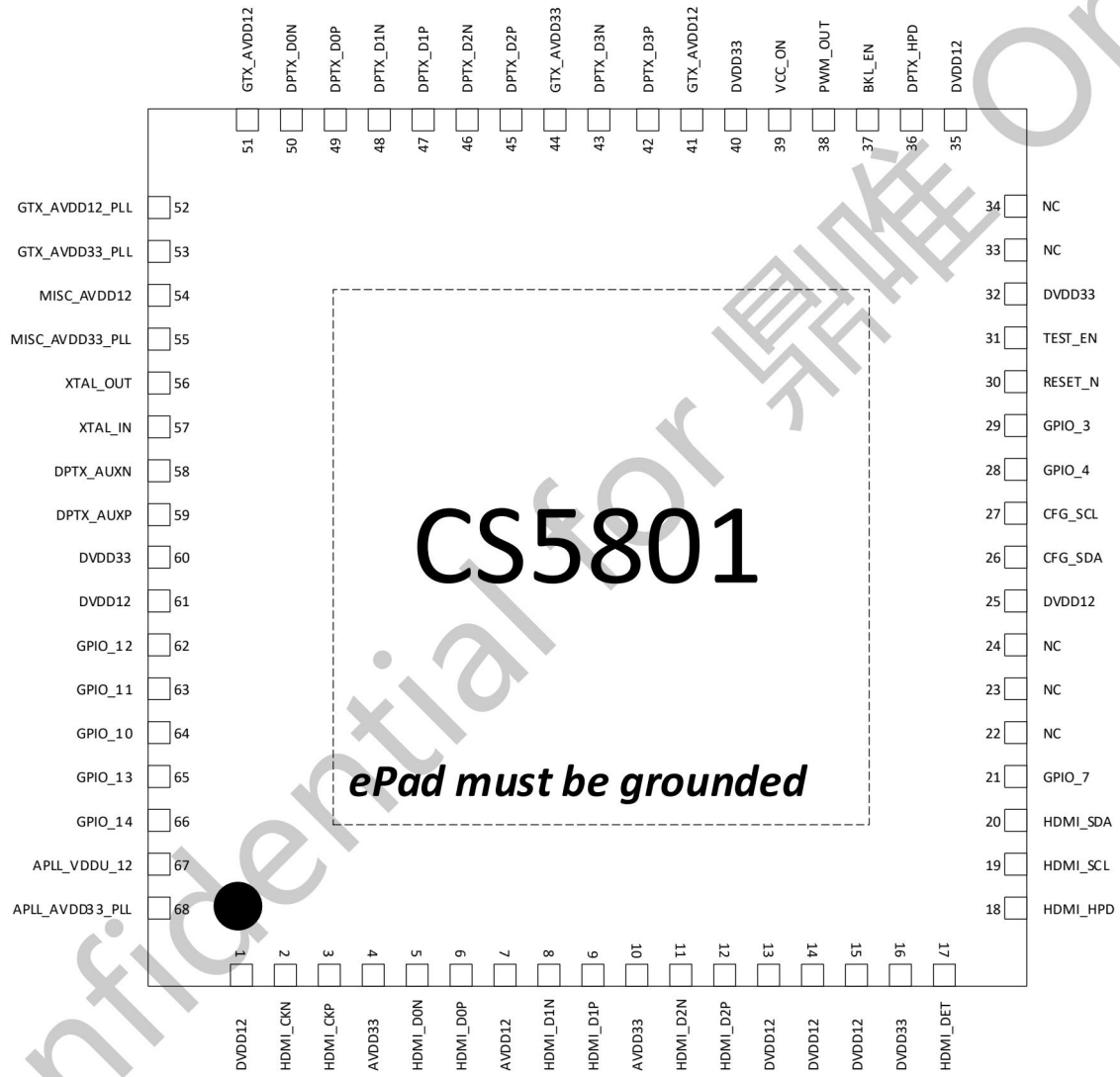
Power & Technology

- 3.3V/1.2V power supply
- HBM 6-KV for all pins

3 Pin Definition

3.1 Pin Assignments

Figure 3-1 CS5801 Pin Layout



3.2 Pin Description

Table 3-1 CS5801 Pin Definitions

Pin #	Description	Type	PU/PD	Note
1	HDMI_DVDD12_A	P		1.2V power input
2	HDMI_CKN	AI		HDMI clock differential pair N input
3	HDMI_CKP	AI		HDMI clock differential pair P input
4	HDMI_AVDD33_A	P		3.3V power input
5	HDMI_D0N	AI		HDMI data channel 0 different pair N input
6	HDMI_D0P	AI		HDMI data channel 0 different pair P input
7	HDMI_AVDD12_A	P		1.2V power input
8	HDMI_D1N	AI		HDMI data channel 1 different pair N input
9	HDMI_D1P	AI		HDMI data channel 1 different pair P input
10	HDMI_AVDD33_B	P		3.3V power input
12	HDMI_D2N	AI		HDMI data channel 2 different pair N input
12	HDMI_D2P	AI		HDMI data channel 2 different pair P input
13	HDMI_DVDD12_B	P		1.2V power input
14	DVDD12	P		1.2V power input
15	DVDD12	P		1.2V power input
16	DVDD33	P		3.3V power input
17	HDMI_DET(5T)	I/O	PD	HDMI Hot Plug detect (5V Tolerance)
18	HDMI_HPD(5T)	I/O		General input output (5V Tolerance)
19	HDMI_SCL(5T)	I/O	PU	HDMI DDC clock (5V Tolerance)
20	HDMI_SDA(5T)	I/O	PU	HDMI DDC data (5V Tolerance)
21	GPIO_7/UART_TX	I/O		General input output/MCU UART TX
22	NC	-		Reserved pin
23	NC	-		Reserved pin
24	NC	-		Reserved pin
25	DVDD12	P		1.2V power input
26	CFG_SDA	I/O	-	I2C slave DATA pin for debug
27	CFG_SCL	I/O	-	I2C slave CLOCK pin for debug
28	GPIO_4	I/O		GPIO4
29	GPIO_3	I/O		GPIO3
30	RESET_N	I	PU	1: Reset mode. 0: Normal mode.
31	TEST_EN	I	PD	1: Test mode. 0: Normal mode.
32	DVDD33	P		3.3V power input
33	NC	-		Reserved pin

34	NC	-		Reserved pin
35	DVDD12	P		1.2V power input
36	DPTX_HPD	I		DP TXHPD input
37	BKL_EN	O		LCD panel back light enable signal for eDP panel.
38	PWM_OUT	O		PWM output for backlight brightness control for eDP panel.
39	VCC_ON	O		LCD panel VCC enable signal for eDP panel.
40	DVDD33	P		3.3V power input
41	GTX_AVDD12	P		1.2V power input
42	DPTX_D3P	AO		Differential pair for DPTX port data lane
43	DPTX_D3N	AO		Differential pair for DPTX port data lane
44	GTX_AVDD33	P		3.3V power input
45	DPTX_D2P	AO		Differential pair for DPTX port data lane
46	DPTX_D2N	AO		Differential pair for DPTX port data lane
47	DPTX_D1P	AO		Differential pair for DPTX port data lane
48	DPTX_D1N	AO		Differential pair for DPTX port data lane
49	DPTX_D0P	AO		Differential pair for DPTX port data lane
50	DPTX_D0N	AO		Differential pair for DPTX port data lane
51	GTX_AVDD12	P		1.2V power input
52	GTX_AVDD12_PLL	P		1.2V power input
53	GTX_AVDD33_PLL	P		3.3V power input
54	MISC_AVDD12	P		1.2V power input
55	MISC_AVDD33_PLL	P		3.3V power input
56	XTAL_OUT	O		27MHz Crystal output.
57	XTAL_IN	I		27MHz Crystal input.
58	DPTX_AUXN	AIO		DisplayPort TX AUX channel negative
59	DPTX_AUXP	AIO		DisplayPort TX AUX channel positive
60	DVDD33	P		3.3V power input
61	DVDD12	P		1.2V power input
62	GPIO_12	I/O		General input output
63	GPIO_11	I/O		General input output
64	GPIO_10	I/O		General input output
65	GPIO_13	I/O		General input output
66	GPIO_14	I/O		General input output
67	APLL_VDDU_12	P		1.2V power input
68	APLL_AVDD33_PLL	P		3.3V power input

4 Electrical Specifications

4.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 4.2 for functional operating limits.

Table 4-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	3.3V power input	-0.3	—	3.96	V
VDD12	1.2V power input	-0.3	—	1.44	V
T_A	Junction temperature	-40	—	125	°C
Q_{JA}	Storage temperature1	-65	—	150	°C
ESD_{HBM}	ESD protection (Human body model)	—	—	±6	KV
ESD_{CDM}	ESD protection (Charge Device model)	—	—	700	V

1. Max 260°C can be guaranteed with max 8 sec soldering time.

4.2 Operating Conditions

Table 4-2 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	3.3V power input	3.0	3.3	3.6	V
VDD12	1.2V power input	1.10	1.2	1.30	V
T_A	Ambient temperature	0		70	°C
Q_{JA}	Package thermal resistance, no air flow	—	39.3	—	°C/W

4.3 Electrical Specification

Table 4-3 DC Electrical Specification

Symbol	Parameter	For 3.3V I/O		
		Min	Typ	Max
V_{il} (V)	Input low voltage	—	—	0.8
V_{ih} (V)	Input high Voltage	2.0	—	—
V_{ol} (V)	Output low voltage	0	—	0.4
V_{oh} (V)	Output high voltage[1]	2.4	—	—
I_{in} (uA)	Input leakage current	-10	—	+10
I_{hiz} (uA)	Output tri-state leakage current	-10	—	+10

5 Package Specification

Figure 5-1 CS5268AN Package Outline (QFN68 Leads 8x8mm2)

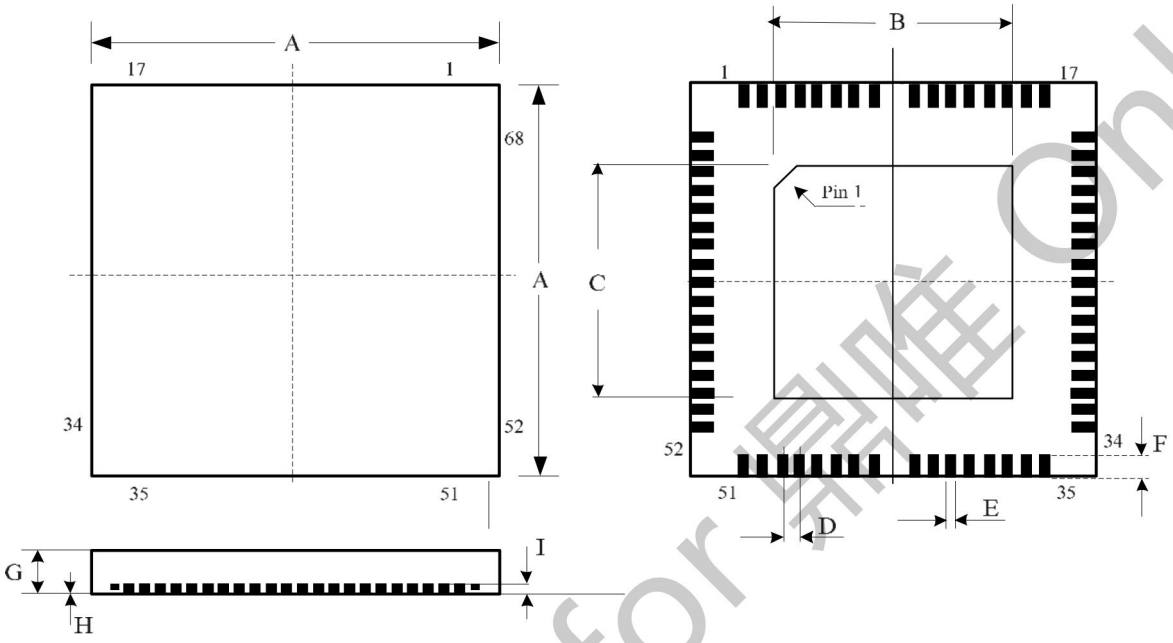


Table 5-1 Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	Min	Normal	Max	Min	Normal	Max
A	7.9	8.0	8.1	0.311	0.314	0.319
B	5.50	5.70	5.90	0.217	0.224	0.232
C	5.50	5.70	5.90	0.217	0.224	0.232
D		0.40 BSC			0.016 BSC	
E	0.15	0.20	0.25	0.006	0.008	0.010
F	0.30	0.40	0.50	0.012	0.016	0.020
G	0.80	0.85	0.90	0.031	0.033	0.035
H	0	0.02	0.05	0	0.001	0.002
I		0.20 REF			0.008 REF	

6 Ordering Information

The CS5801 can be ordered using the part numbers in Table 6-1. Please consult sales for further details.

Table 6-1 CS5801 Ordering Information

Part No.	Description	Temperature Range	MSL	Environment Compliance	Packing Type
CS5801AN	68 Pin (QFN) Lead-free package	Commercial: 0 to 70 degree C	Level 3	Green	Tray

Table 6-2 CS5801 Marking Information

Line No.	Description	Temperature Range
Line1	CS5801	Product Name
Line2	XXXXXX	Lot #
Line3	YYWW	YYWW: Date code
Line4	PIN1 indicator	

Figure 6-1 CS5801 Marking

7 Revision History

Table 7-1 Document Revision History

Revision	Date	Changes
V0.1	Dec. 2021	Initial version
V0.2	Jan. 2022	Change some typo.