CS5394

117 dB, 48 kHz Audio A/D Converter

Features

- 24-Bit Conversion
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates
  - including 32 kHz, 44.1 kHz and 48 kHz
- 117 dB Dynamic Range (A-Weighted)
- -103 dB THD + N
- Differential Analog Circuitry
- Internal 64× Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - with >117 dB Stopband Attenuation
- Single +5 V Power Supply
- Power Down Mode

Description

The CS5394 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 24-bit values for both left and right inputs in serial form. The output sample rate can be up to 50 kHz per channel.

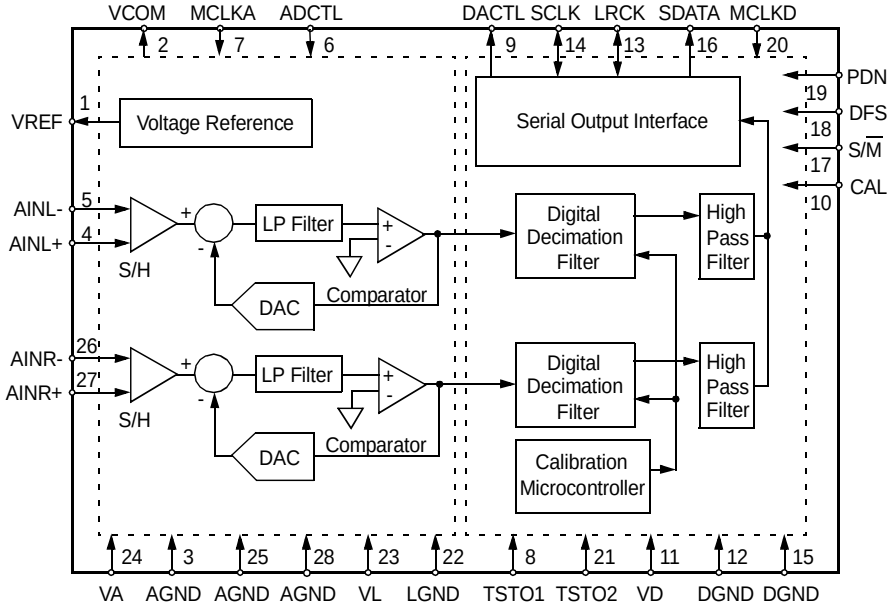
The CS5394 uses 7th-order, delta-sigma modulation with 64× oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5394 has a linear phase filter with passband of dc to 22.1 kHz, ± 0.005 dB passband ripple and >117 dB stopband rejection.

The CS5394 is targeted for the highest performance professional audio systems requiring wide dynamic range, negligible distortion and low noise.

ORDERING INFORMATION

CS5394-KS	-10° to 70° C	28-pin SOIC
CDB5394		Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25 °C; VA, VL, VD = 5 V; Full-scale Input Sinewave, 997 Hz; Fs = 48 kHz; SCLK = 3.072 MHz; Analog connections as shown in Figure 1; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Logic 0 = 0 V, Logic 1 = VD.)

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Performance							
Dynamic Range				TBD	114	-	dB
		A-weighted		TBD	117	-	
Total Harmonic Distortion + Noise		(Note 1)	THD+N				dB
	-1.0 dB			-	-103	TBD	
	-20 dB			-	-94	TBD	
	-60 dB			-	-54	TBD	
Total Harmonic Distortion	-1.0 dB	(Note 1)	THD	-	0.0007	TBD	%
Interchannel Phase Deviation				-	0.01	-	Degree
Interchannel Isolation				-	118	-	dB
dc Accuracy							
Interchannel Gain Mismatch				-	0.05	-	dB
Gain Error				-	±5	TBD	%
Gain Drift				-	100	-	ppm/°C
Bipolar Offset Error		with High Pass filter		-	0	-	LSB
Analog Input							
Full-scale Differential Input Voltage		(Note 2)	V_{IN}	TBD	4.0	TBD	V_{pp}
Input Impedance			Z_{IN}	-	4.5	-	kΩ
Common-Mode Rejection Ratio			CMRR	-	82	-	dB
Common mode bias Voltage			Vcom	-	2.5	-	V

Notes: 1. Referenced to typical full-scale differential input voltage (4.0 Vpp).

2. Specified for a fully differential input ±{(AINR+) - (AINR-)}. Full-scale outputs will be produced for differential inputs beyond V_{IN} and within VA and AGND.

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice

POWER AND THERMAL CHARACTERISTICS (T_A = 25 °C; VA, VL, VD = 5 V ±5%; Fs = 48 kHz; Master Mode.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current (Normal Operation)	(VA) + (VL)	I_A	-	85	TBD	mA
	VD	I_D	-	65	TBD	mA
Power Supply Current (Power-Down Mode)	(VA) + (VL)	I_A	-	2	-	mA
	VD	I_D	-	2	-	mA
Power Consumption	Normal Operation		-	750	TBD	mW
	Power-Down Mode		-	20	-	mW
Power Supply Rejection Ratio	1 kHz	PSRR	-	65	-	dB
Allowable Junction Temperature			-	-	135	°C
Junction to Ambient Thermal Impedance		θ_{JA}	-	45	-	°C/W

DIGITAL FILTER CHARACTERISTICS (T_A = 25 °C; VA, VL, VD = 5 V ±5%; Fs = 48 kHz)

Parameter			Symbol	Min	Typ	Max	Unit
Passband	-0.01 dB	(Note 3)		0	-	22.1	kHz
Passband Ripple				-	-	±0.005	dB
Stopband		(Note 3)		26.6	-	3050	kHz
Stopband Attenuation		(Note 4)		117	-	-	dB
Group Delay (Fs = Output Sample Rate)			t_{gd}	-	34/Fs	-	s
Group Delay Variation vs Frequency			Δt_{gd}	-	-	0.0	µs
High Pass Filter Characteristics							
Frequency Response	-3 dB	(Note 3)		-	1.8	-	Hz
	-0.036 dB			-	20	-	
Phase Deviation	@ 20 Hz	(Note 3)		-	5.3	-	Degree
Passband Ripple				-	-	0	dB

Notes: 3. Filter characteristic scales with sample rate.

4. The analog modulator samples the input at 3.072 MHz for Fs equal to 48 kHz. There is no rejection of input signals which are (n × 3.072 MHz) ±22.1 kHz, where n = 0, 1, 2, 3, ...

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA, VL, VD = 5 V ±5%)

Parameter		Symbol	Min	Max	Unit
High-Level Input Voltage		V_{IH}	2.4	-	V
	MCLKA/D only		3.0	-	V
Low-Level Input Voltage		V_{IL}	-	0.8	V
	MCLKA/D only		-	1.0	V
High-Level Output Voltage		V_{OH}	(VD) - 1.0	-	V
Low-Level Output Voltage		V_{OL}	-	0.4	V
Input Leakage Current		I_{in}	-	±10	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, All voltages with respect to ground.)

Parameter		Symbol	Min	Max	Unit
DC Power Supplies	Positive Analog	VA	-0.3	+6.0	V
	Positive Logic	VL	-0.3	+6.0	
	Positive Digital	VD	-0.3	+6.0	
	|VA - VD|		-	0.4	
	|VA - VL|		-	0.4	
	|VD - VL|		-	0.4	
Input Current	(Note 5)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 6)	V_{INA}	-0.7	(VA) + 0.7	V
Digital Input Voltage	(Note 6)	V_{IND}	-0.7	(VD) + 0.7	V
Ambient Operating Temperature (Power Applied)		T_A	-55	+100	°C
Storage Temperature		T_{stg}	-65	+150	°C

Notes: 5. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

6. The maximum over/under voltage is limited by the input current.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0 V, All voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Analog	VA	4.75	5.0	5.25	V
	Positive Logic	VL	4.75	5.0	5.25	
	Positive Digital	VD	4.75	5.0	5.25	
	|VA - VD|		-	-	0.4	

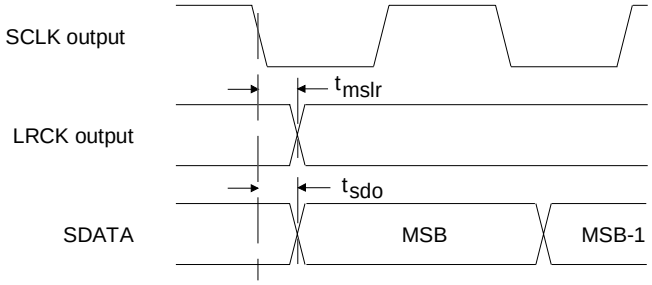
SWITCHING CHARACTERISTICS (T_A = -10 to 70 °C; VA = VL = VD = 5 V ±5%; Inputs: Logic 0 = 0 V, Logic 1 = VA = VL = VD; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Output Sample Rate	F_s	2	-	50	kHz
MCLK Period	t_{clkw}	78	-	1950	ns
MCLK Low	t_{clkl}	26	-	-	ns
MCLK High	t_{clkh}	26	-	-	ns
MCLK Fall Time		-	-	12	ns
Master Mode					
SCLK falling to LRCK	t_{mslr}	-20	-	+20	ns
SCLK falling to SDATA valid	t_{sdo}	-	-	20	ns
SCLK Duty Cycle		-	50	-	%
Slave Mode					
LRCK Period	$1/F_s$	20	-	500	µs
LRCK Duty Cycle		TBD	50	TBD	%
SCLK Period	t_{sclkw}	(Note 7)	-	-	ns
SCLK Pulse Width Low	t_{sclkl}	(Note 8)	-	-	ns
SCLK Pulse Width High	t_{sclkh}	60	-	-	ns
SCLK falling to SDATA valid	t_{dss}	-	-	(Note 9)	ns
LRCK edge to MSB valid	t_{lrdss}	-	-	(Note 9)	ns
SCLK rising to LRCK edge delay	t_{slr1}	(Note 9)	-	-	ns
LRCK edge to rising SCLK setup time	t_{slr2}	(Note 9)	-	-	ns

Notes: 7. $\frac{1}{128\ F_S}$

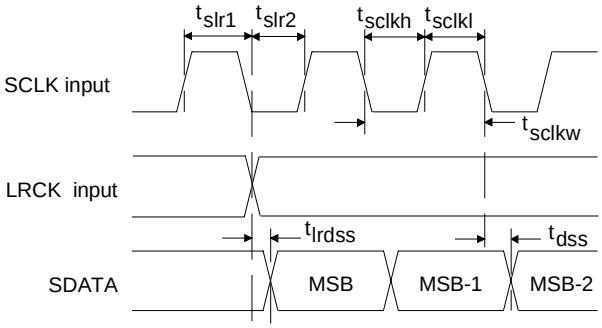
8. $\frac{1}{256\ F_S}$

9. $\frac{1}{512\ F_S} + 20$



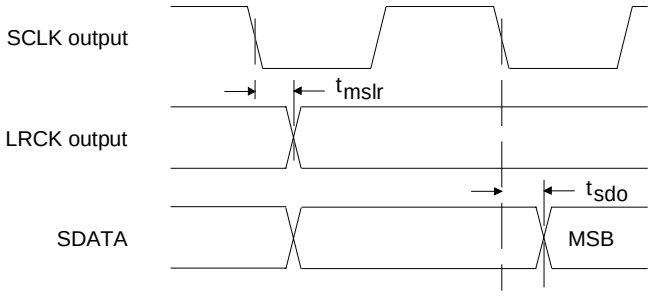
SCLK to SDATA & LRCK - MASTER Mode

Serial Data Format, DFS low



SCLK to LRCK & SDATA - SLAVE Mode

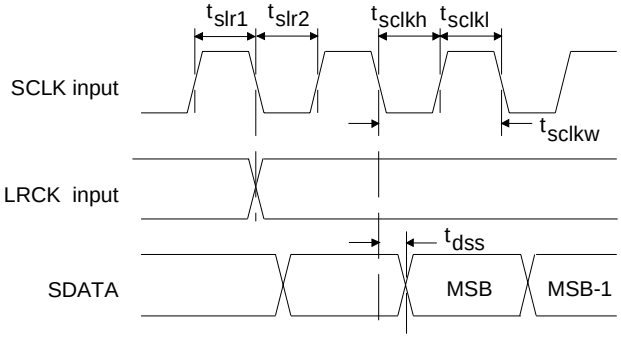
Serial Data Format, DFS low



SCLK to SDATA & LRCK - MASTER Mode

Serial Data Format, DFS high

I^2S compatible



SCLK to SDATA & LRCK - MASTER Mode

Serial Data Format, DFS high

I^2S compatible

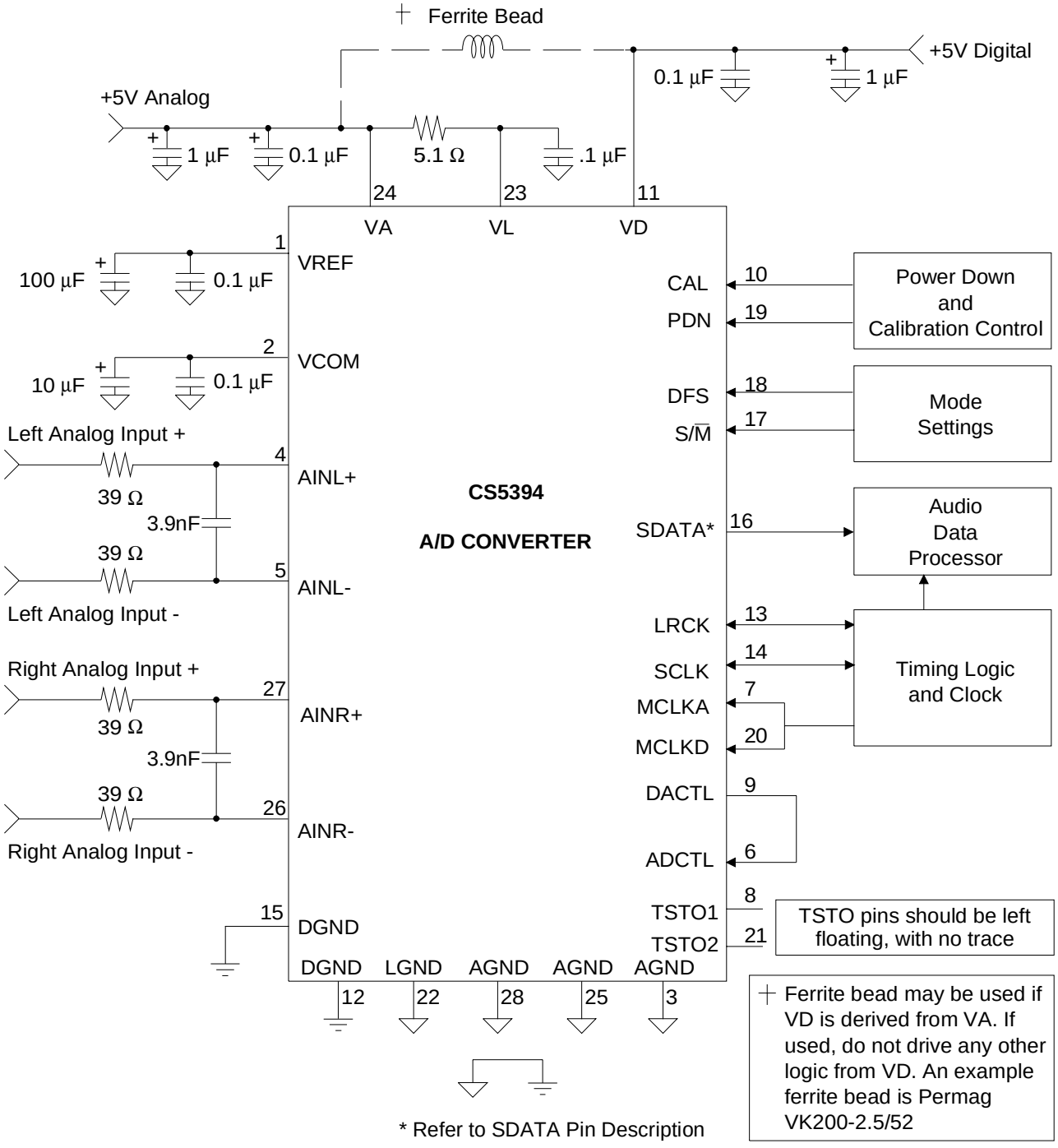


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5394 is a 24-bit, stereo A/D converter designed for stereo digital audio applications. The device uses a patented, 7th-order tri-level delta-sigma modulator to sample the analog input signals at 64 times the output sample rate (Fs) of the device. Sample rates of up to 50 kHz are supported. The analog input channels are simultaneously sampled by separate delta-sigma modulators. The resulting serial bit streams are digitally filtered, yielding pairs of 24-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters and it does not require external sample-and-hold amplifiers or voltage references.

An on-chip voltage reference provides for a differential input signal range of 4.0 Vpp. The device also contains a high pass filter, implemented digitally after the decimation filter, to completely eliminate any internal offsets in the converter or any offsets present at the input to the device. Output data is available in serial form, coded as 2's complement 24-bit numbers.

For more information on delta-sigma modulation techniques see the references at the end of this data sheet.

SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for isolation are all that's required, as shown in Figure 1.

Master Clock

The master clock is the clock source for the delta-sigma modulator (MCLKA) and digital filters (MCLKD). The required MCLKA/D frequencies are determined by the desired Fs and must be 256x Fs, as shown in Table 1.

LRCK (kHz)	MCLKA/D (MHz)	SCLK (MHz)
32	8.192	2.048
44.1	11.2896	2.822
48	12.288	3.072

Table 1. Common Clock Frequencies

SERIAL DATA INTERFACE

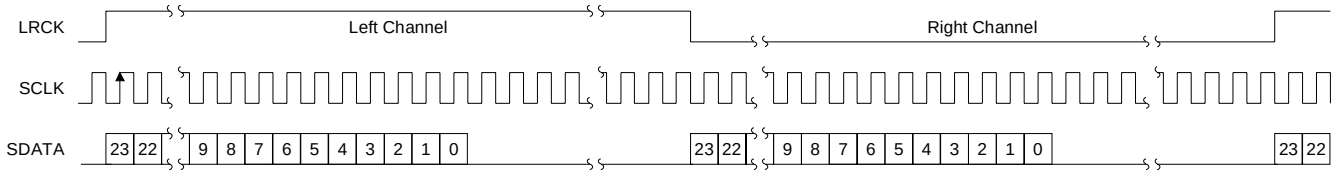
The CS5394 supports two serial data formats which are selected via the digital format select pin, DFS. The digital format determines the relationship between the serial data, left/right clock and serial clock. Figures 2 and 3 detail the interface formats. The serial data interface is accomplished via the serial data output, SDATA, serial data clock, SCLK, and the left/right clock, LRCK. The serial nature of the output data results in the left and right data words being read at different times. However, the samples within each left/right pair represent simultaneously sampled analog inputs.

Serial Data

The serial data block consists of 24 bits of audio data presented in 2's-complement format with the MSB-first. The data is clocked from SDATA by the serial clock and the channel is determined by the Left/Right clock.

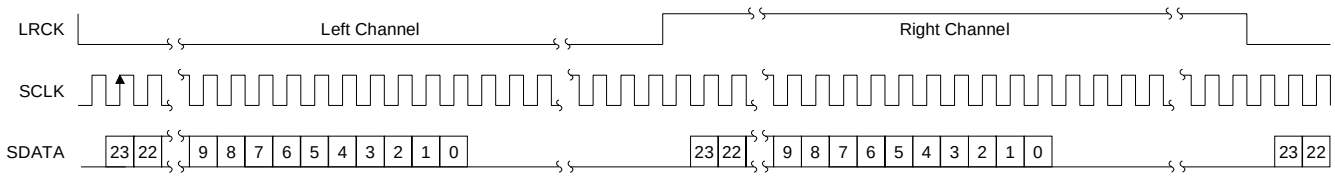
Serial Clock

The serial clock shifts the digitized audio data from the internal data registers via the SDATA pin. SCLK is an output in Master Mode where internal dividers will divide the master clock by 4 to generate a serial clock which is 64× Fs. In Slave Mode, SCLK is an input with a serial clock typically between 48× and 128× Fs. It is recommended that SCLK be equal to 64× Fs, though other frequencies are possible, to avoid potential interference effects which may degrade system performance.



MASTER	SLAVE
24-Bit Left Justified Data	24-Bit Left Justified Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x F_S	MCLK equal to 256x F_S

Figure 2. Serial Data Format, DFS Low



MASTER	SLAVE
I^2S 24-Bit Data	I^2S 24-Bit Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x F_S	MCLK equal to 256x F_S

Figure 3. Serial Data Format, DFS High (I^2S compatible)

Left / Right Clock

The Left/Right clock, LRCK, determines which channel, left or right, is to be output on SDATA. In Master Mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs and synchronous to MCLKA/D.

Master Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the master clock. Internal dividers will divide MCLKA/D by 4 to generate a SCLK which is 64× Fs and by 256 to generate a LRCK which is equal to Fs. The CS5394 is placed in the Master mode with the slave/master pin, S/$\overline{M}$, low.

Slave Mode

LRCK and SCLK become inputs in slave mode. LRCK must be externally derived from MCLKA/D and be equal to Fs. It is recommended that SCLK be equal to 64×. Other frequencies between 48× and 128× Fs are possible but may degrade system performance due to interference effects. The master clock frequency must be 256× Fs. The CS5394 is placed in the Slave mode with the slave/master pin, S/$\overline{M}$, high.

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented differentially to the modulators via the AINR+/- and AINL+/- pins. Each analog input will accept a maximum of 2.0 Vpp. The + and - input signals are 180° out of phase resulting in a differential input voltage of 4.0 Vpp. Figure 4 shows the input signal levels for

full scale. Input signals can be AC or DC coupled. The VCOM output is available to filter the internal common mode and it is recommended that this output be used to bias the analog input buffer to minimize distortion. However, this pin is not intended to supply significant amounts of current and is susceptable to noise coupling into the sampling circuits. Please refer to the CDB5394 for a suggested implementation.

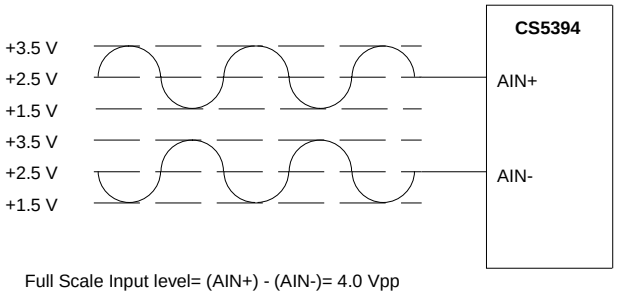


Figure 4. Full Scale Input Voltage

The CS5394 samples the analog inputs at 64× Fs, 3.072 MHz for a 48 kHz sample-rate. The digital filter rejects all noise above 26.6 kHz except for frequencies at 3.072 MHz ±22.1 kHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 39 Ω resistor in series with each analog input and a 3.9 nF capacitor across the inputs will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient must be avoided since these will degrade signal linearity. NPO and COG capacitors are recommended. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with sample rate.

The on-chip voltage reference is available at VREF for the purpose of decoupling only. The circuit traces attached to this pin must be minimal in length and no load current may be taken from VREF. The recommended decoupling scheme, Figure 1, is a 100 µF electrolytic capacitor and a 0.1 µF ceramic capacitor connected from VREF to AGND. The decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF and pin 3, AGND, on the printed circuit board.

High Pass Filter

The CS5394 includes a high pass filter after the decimator to remove the indeterminate DC offsets introduced by the analog buffer stage and the CS5394 analog modulator. The first-order high pass filter are detailed in the Digital Filter specifications table. The filter response scales linearly with sample rate.

Power-up and Calibration

Reliable power-up can be accomplished by withholding the MCLKA/D until the 5 Volt power and configuration pins are stable. It is also recommended that the MCLKA/D be removed if the supplies drop below 4.75 Volt to prevent power glitch related issues.

The delta-sigma modulators settle in a matter of microseconds after the analog section is powered, either through the application of power or by exiting the power-down mode. However, the voltage reference will take much longer to reach a final value due to the presence of external capacitance on the VREF pin.

A calibration of the tri-level delta-sigma modulator should always be initiated following power-up and after allowing sufficient time for the voltage on the external VREF capacitor to settle. This is required to minimize noise and distortion. Calibration is activated on a rising edge applied to the CAL pin and requires 4100 LRCK cycles. It is also advised that the CS5394 be calibrated after the device has reached thermal equilibrium to maximize performance.

Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. It is recommended that the rising edge of the CAL signal be timed with a falling edge of MCLK to ensure that all devices will initiate a calibration and synchronization sequence on the same rising edge of MCLK. The absence of re-timing of the CAL signal can result in a sampling difference of one MCLK period.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA and VL connected to a clean +5 V supply. VD, which powers the digital filter, may be run from the system +5 V logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. The VREF decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from VREF and pin 3, AGND. The CDB5394 evaluation board demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

PERFORMANCE

Digital Filter

Figures 5-8 show the performance of the digital filter included in the ADC. All plots are normalized to Fs. Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with Fs.

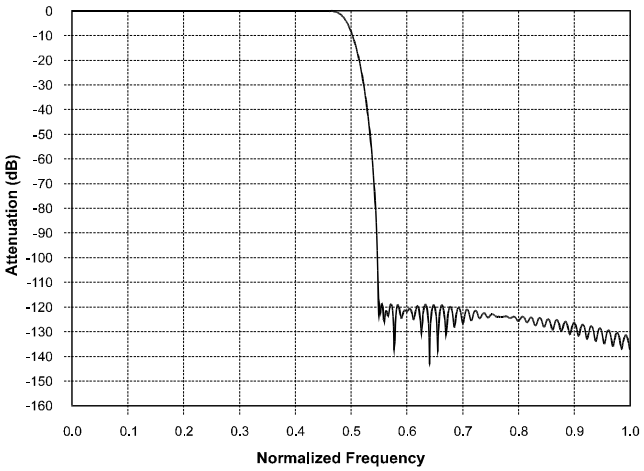


Figure 5. CS5394 Stopband Attenuation

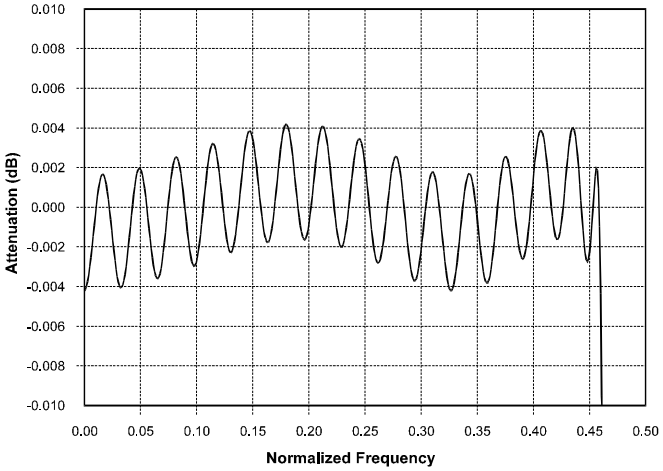


Figure 6. CS5394 Passband Ripple

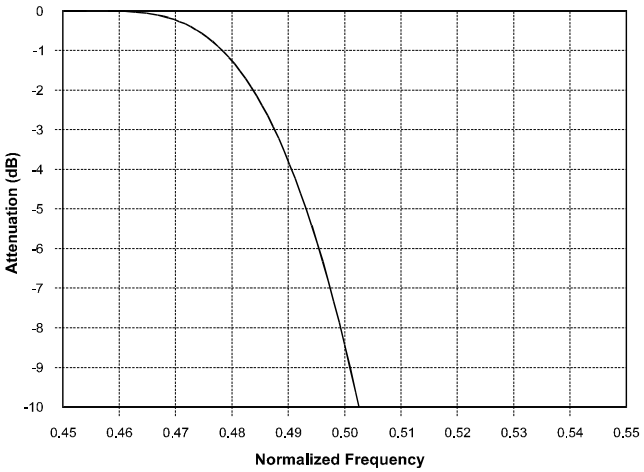


Figure 7. CS5394 Transition Band

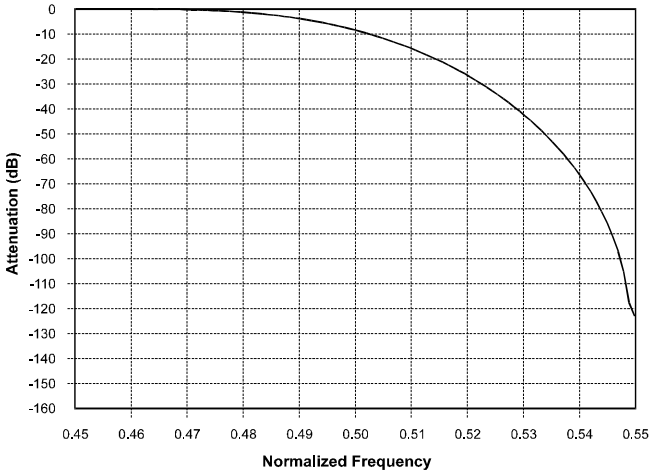
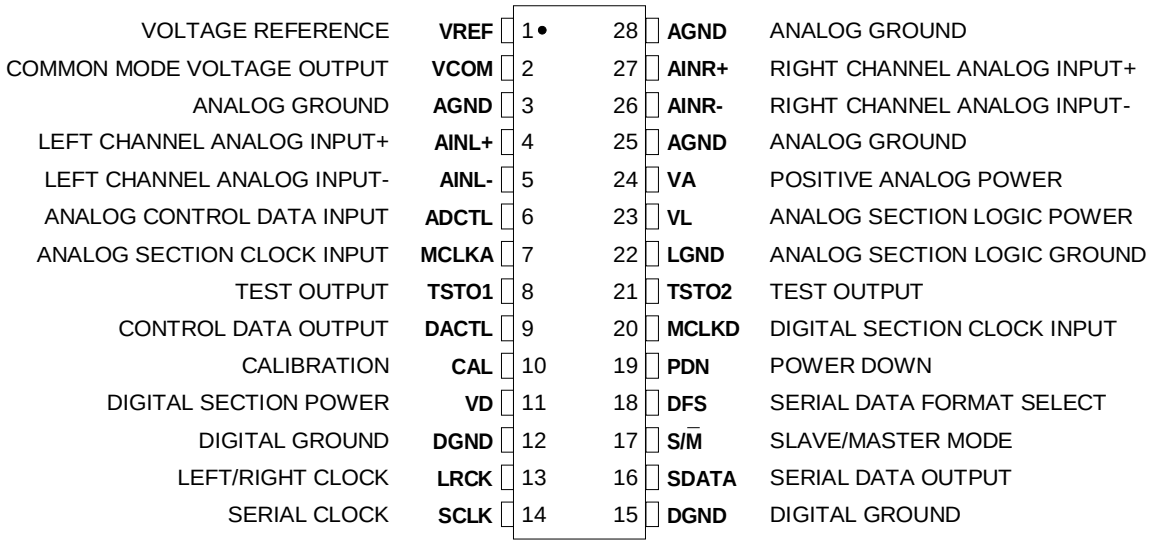


Figure 8. CS5394 Transition Band

PIN DESCRIPTIONS



Power Supply Connections

VA - Analog Power, Pin 24.

Positive analog supply. Nominally +5 volts.

VL - Logic Power, Pin 23.

Positive logic supply for the analog section. Nominally +5 volts.

AGND - Analog Ground, Pins 3, 25, and 28.

Analog ground reference.

LGND - Logic Ground, Pin 22.

Ground reference for the logic portions of the analog section.

VD - Digital Power, Pin 11.

Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, Pins 12 and 15.

Digital ground reference for the digital section.

Analog Inputs

AINR-, AINR+ - Differential Right Channel Analog Inputs, Pins 26 and 27.

Analog input connections for the right channel differential inputs. Nominally 4.0 Vpp differential for full-scale digital output.

AINL-, AINL+ - Differential Left Channel Analog Inputs, Pins 4 and 5.

Analog input connections for the left channel differential inputs. Nominally 4.0 Vpp differential for full-scale digital output.

Analog Outputs

VCOM - Common Mode Voltage Output, Pin 2.

Nominally +2.5 volts. Requires a 10 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor for decoupling to AGND. Caution is required if this output be used to bias the analog input buffer circuits. Refer to the CDB5394 as an example.

VREF - Voltage Reference Output, Pin 1.

Nominally +4 volts. Requires a 100 µF electrolytic capacitor in parallel with 0.1 µF ceramic capacitor for decoupling to AGND.

Digital Inputs

ADCTL - Analog Control Input, Pin 6.

Must be connected to DACTL. This signal enables communication between the analog and digital circuits.

DFS - Digital Format Select, Pin 18.

The relationship between LRCK, SCLK and SDATA is controlled by the DFS pin. When high, the serial output data format is I^2S compatible. The serial data format is left-justified when low.

CAL - Calibration, Pin 10.

Activates the calibration of the tri-level delta-sigma modulator on the rising edge of the CAL input.

MCLKA - Analog Section Input Clock, Pin 7.

This clock is internally divided and controls the delta-sigma modulators. An MCLKA frequency of 12.288 MHz sets a modulator sampling rate of 3.072 MHz and a output sample rate of 48 kHz. MCLKA must be connected to MCLKD.

MCLKD - Digital Section Input Clock, Pin 20.

MCLKD clocks the digital filter and must be connected to MCLKA. The required MCLKD frequency is determined by the desired sample rate. A MCLKD of 12.288MHz corresponds to Fs equal to 48 kHz. MCLKA must be connected to MCLKD.

PDN - Power Down, Pin 19.

When high, the device enters power down. Upon returning low, the device enters normal operation and issues commands to initialize the voltage reference and synchronize the analog and digital sections of the device.

S/$\overline{M}$ - Slave or Master Mode, Pin 17.

When high, the device is configured for Slave mode where LRCK and SCLK are inputs. The device is configured for Master mode where LRCK and SCLK are outputs when S/M is low.

Digital Outputs

DACTL- Digital to Analog Control Output, Pin 9.

Must be connected to ADCTL. This signal enables communication between the digital and analog circuits.

SDATA - Digital Audio Data Output, Pin 16.

The 24-bit audio data is presented MSB first, in 2's complement format. This pin has a internal pull-down resistor and must remain low during the power-up sequence to avoid accessing a test mode.

Digital Inputs or Outputs

LRCK - Left/Right Clock, Pin 13.

LRCK determines which channel, left or right, is to be output on SDATA. The relationship between LRCK, SCLK and SDATA is controlled by the Digital Format Select (DFS) pin. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. In master mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to Fs.

SCLK - Serial Data Clock, Pin 14.

Clocks the individual bits of the serial data from SDATA. The relationship between LRCK, SCLK and SDATA is controlled by the Digital Format Select (DFS) pin. In master mode, SCLK is an output clock at 64× Fs. In slave mode, SCLK is an input which requires a continuously supplied clock at any frequency from 48× to 128× Fs (64× is recommended).

Miscellaneous

TSTO1, TSTO2 - Test Outputs, Pins 8 and 21.

These pins are intended for factory test outputs. They must not be connected to any external component or any length of circuit trace.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

REFERENCES

1) "Techniques to Measure and Maximize the Performance of a 120 dB, 96 kHz A/D Comveter Integrated Circuit" by Steven Harris, Steven Green and Ka Leung. Presented at the 103rd Convention of the Audio Engineering Society, September 1997.

2) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

3) "The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

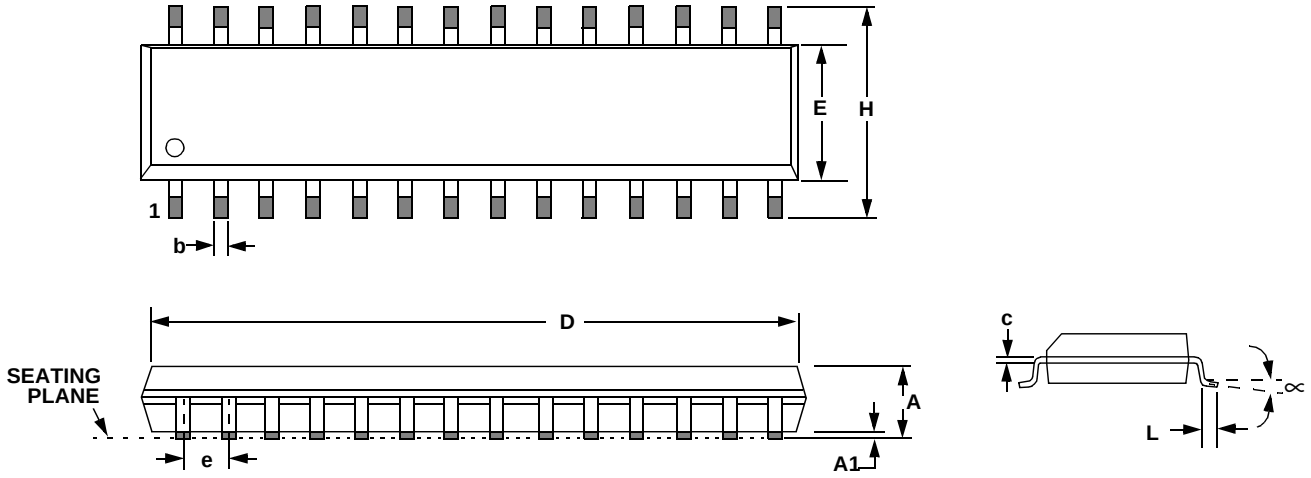
4) "An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

5) "How to Achieve Optimum Performance from Delta-Sigma A/D and D/A Converters" by Steven Harris. Presented at the 93rd Convention of the Audio Engineering Society, October 1992.

6) "A Fifth-Order Delta-Sigma Modulator with 110dB Audio Dynamic Range" by I. Fujimori, K. Hamashita and E.J. Swanson. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

PACKAGE DIMENSIONS

28L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
E	0.291	0.299	7.40	7.60
e	0.040	0.060	1.02	1.52
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°