

FEATURES

- ❑ World's first cost-effective, high-performance 32-bit DSP that is solely dedicated to enable Audyssey Laboratories audio processing technologies for today's high-volume consumer electronic products
- ❑ Features: Audyssey Dynamic Volume™, Audyssey Dynamic EQ™, Audyssey EQ™ & Audyssey BassXT™/BassXT-TV™
- ❑ Audyssey Dynamic Volume eliminates the need for constant volume adjustments
- ❑ Audyssey Dynamic EQ enables a reference playback experience at any desired playback level
- ❑ Audyssey EQ removes much of the distortion caused by speaker enclosures and the typical room environment producing greatly improved sound compared to similar products without correction
- ❑ Audyssey BassXT and BassXT-TV are specifically calibrated to enhance the physical bass response of each product model
- ❑ Configurable Serial Audio Inputs/Outputs
 - Maximum 32-bit @ 192 kHz
(Note: Audyssey Laboratories algorithms support 48 kHz, 44.1 kHz and 32 kHz)
 - Integrated 192 kHz capable S/PDIF transmitter
- ❑ Integrated Clock Manager/PLL
 - Can operate from external crystal, external oscillator
- ❑ Input Fs Auto Detection & Coefficient Loading
- ❑ Host Control & Boot via Serial Interface
- ❑ Support for Master (Self) Boot via Serial EEPROM for single Fs applications (i.e. 48 kHz only via ADC input)
- ❑ Configurable GPIOs and External Interrupt Input
- ❑ 1.8V Core and a 3.3V I/O that is tolerant to 5V input
- ❑ Low-power Mode
 - "Energy Star® Ready" via low-power mode, 268 µW in standby

The brand new CS48AU2B device is still based on the same high-performance 32-bit fixed point Digital Signal Processor core but instead is equipped with much less memory, tailoring it for more cost-effective applications which feature Audyssey Laboratories audio processing technologies. Target applications are:

- Digital Televisions
- iPod® Docking Stations
- Automotive Head Units (OEM and Aftermarket)
- Automotive Outboard Amplifiers (OEM and Aftermarket)
- Blu-ray® Disc Receivers
- Soundbars / Sound Projectors

The following Audyssey Laboratories algorithms are currently supported on the CS48AU2B and more are in development:



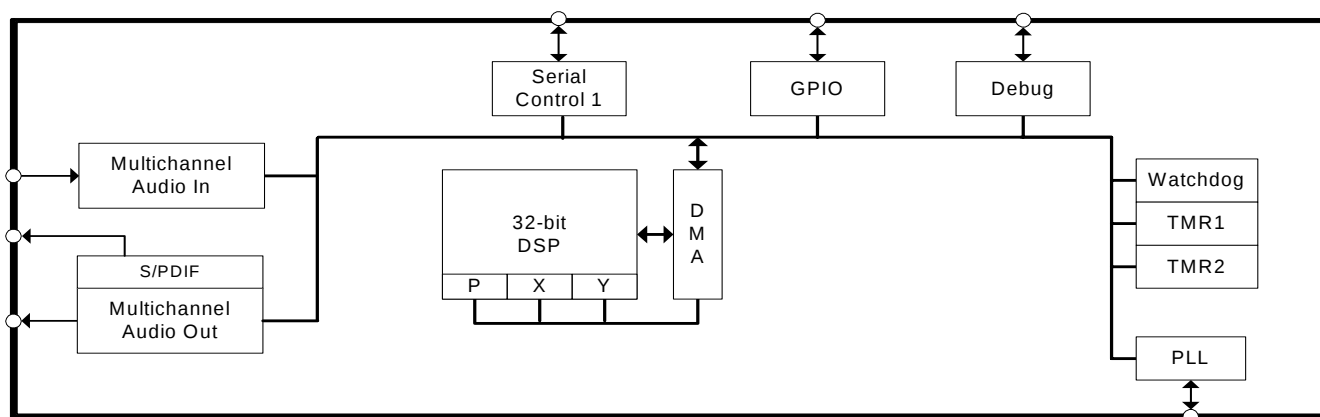
While the individual Audyssey processing algorithms have already been implemented on this DSP, the CS48AU2B is programmed using the Cirrus proprietary DSP Composer™ GUI development tool.

Processing chains combining both standard signal processing blocks (Tone Control, Bass Management, etc.) in combination with any combination of Audyssey Laboratories technology algorithm blocks may be designed using a simple drag-and-drop interface to create a custom signal flow specific to your product model. The end result of this is a software image that is down-loaded to the DSP via serial host (I²C® or SPI™) or via a serial master (self) boot.

Support for loading of the various Audyssey Laboratories algorithm coefficient files supplied by Audyssey Laboratories is easily supported via DSP Composer, enabling the OEM/ODM to quickly be able to generate the necessary files for the system microcontroller which have been custom tailored for each specific model based on the measurement and analysis performed by Audyssey Laboratories.

Ordering Information:

See [page 21](#) for ordering information



Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com.

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1. Documentation Strategy

The *CS48AU2B Data Sheet* describes the CS48AU2B audio processor. This document should be used in conjunction with the following documents when evaluating or designing a system around the CS48AU2B of processors.

Table 1. CS48AU2B Related Documentation

Document Name	Description
<i>CS48AU2B Data Sheet</i>	This document
<i>CS485xx Hardware User's Manual</i>	Includes detailed system design information including Typical Connection Diagrams, Boot-Procedures, Pin Descriptions, etc.
<i>AN298 - CS485xx Firmware User's Manual</i>	Includes detailed firmware design information including signal processing flow diagrams and control API information for the operating system.
<i>DSP Composer™ User's Manual</i>	Includes detailed configuration and usage information for the GUI development tool.
<i>AN298PPMQ, Audyssey Dynamic Volume™ Audyssey Dynamic EQ™ Firmware Module Application Note</i>	Contains description of API used to control Audyssey Dynamic Volume and Audyssey Dynamic EQ firmware.
<i>AN298PPMR, Audyssey EQ™ Firmware Module Application Note</i>	Contains description of API used to control Audyssey EQ firmware.
<i>AN298PPMS, Audyssey BassXT™ Firmware Module Application Note</i>	Contains description of API used to control Audyssey BassXT firmware.

The scope of the *CS48AU2B Data Sheet* is primarily the hardware specifications of the CS48AU2B of devices. This includes hardware functionality, characteristic data, pinout, and packaging information.

The intended audience for the *CS48AU2B Data Sheet* is the system PCB designer, MCU programmer, and the quality control engineer.

2. Overview

The CS48AU2B DSP is designed to provide high-performance post-processing and mixing of digital audio. The low-power standby preserves battery life for applications which are always on, but not necessarily processing audio, such as automotive audio systems. The CS48AU2B is available in a 48-pin QFP package. Please refer to [Table 2 on page 7](#) for the input, output and suggested applications for this device.

2.1 Licensing

Licenses are required for any of the Audyssey Laboratories algorithms listed in [Section 3](#). Please contact Audyssey Laboratories at sales@audyssey.com for more information on licensing their technology. Please send e-mail to trademark@audyssey.com for more information on Audyssey trademarks.

3. Code Overlays

The suite of software available for the CS48AU2B consists of an operating system (OS) and a library of overlays. The overlays have been divided into three main groups called Matrix-processors, Virtualizer-processors, and Post-processors. All software components are defined below:

1. **OS/Kernel** - Encompasses all non-audio processing tasks, including loading data from external memory, processing host messages, calling audio-processing subroutines, error concealment, etc.
2. **Matrix-processor** - Any Module that performs a matrix decode on PCM data to produce more output channels than input channels ($2 \Rightarrow n$ channels). Generally speaking, these modules increase the number of valid channels in the audio I/O buffer.
3. **Virtualizer-processor** - Any module that encodes PCM data into fewer output channels than input channels ($n \Rightarrow 2$ channels) with the effect of providing “phantom” speakers to represent the physical audio channels that were eliminated. Generally speaking, these modules reduce the number of valid channels in the audio I/O buffer.
4. **Post-processors** - Any module that processes audio I/O buffer PCM data in-place after the matrix- or virtualizer-processors. Examples are bass management, audio manager, tone control, Audyssey Dynamic Volume, Audyssey Dynamic EQ, Audyssey EQ, Audyssey BassXT, delay, & customer-specific effects, etc.

The certified DSP firmware or application codes provided by Cirrus Logic (under a license to you from Audyssey Laboratories) may enable some or all of the Audyssey Laboratories algorithms. These licensed processing blocks can be used in combination with a host standard post-processing signal blocks (tone control, Bass Management, delays, etc.) or lower level primitives such as a filter or math function.

A product-specific signal flow is generated by the designer using DSP Composer.

Once all of the custom coefficient files supplied by Audyssey Laboratories have been loaded and the signal flow has been set, the user can perform a “generate deliverables” inside DSP Composer.

This generates a collection of files that can be easily converted to .c or .h files by the designer for storage inside the host controller OR can be converted into a small image that can either be stored in an external serial FLASH/EEPROM, or downloaded via a host controller through the SPI™/I²C® serial port.

The overlay structure reduces the time required to reconfigure the DSP when a processing change is requested. Each overlay can be reloaded independently without disturbing the other overlays. For example, when a new matrix-processor is selected, the OS, virtualizer-, and post-processors do not need to be reloaded — only the new matrix-processor (the same is true for the other overlays).

[Table 2](#) below lists the firmware available based on device selection. Please refer to AN298, *CS485xx Firmware User's Manual* for the latest listing of application codes and Cirrus Framework™ modules available.

Table 2. Device and Firmware Selection Guide

Device	Suggested Application	Channel Count Input/Output	Package
CS48AU2B-CQZ	Digital TV Portable Audio Docking Station Portable DVD DVD Mini / Receiver Multimedia PC Speakers 8 Channel Car Audio DVD Receiver High-end Digital TV 12 channel Car Audio	Up to 12 channel in /12 channel out	48-pin QFP

4. Hardware Functional Description

4.1 DSP Core

The CS48AU2B DSP is a single-core DSP with separate X and Y data and P code memory spaces. The DSP core is a high-performance, 32-bit, fully user-programmable, fixed-point DSP that is capable of performing two multiply-and-accumulate (MAC) operations per clock cycle. The DSP core has eight 72-bit accumulators, four X- and four Y-data registers, and 12 index registers.

The DSP core is coupled to a flexible DMA engine. The DMA engine can move data between peripherals such as the serial control port (SCP), digital audio input (DAI) and digital audio output (DAO), or any DSP core memory, all without the intervention of the DSP. The DMA engine off loads data move instructions from the DSP core, leaving more MIPS available for signal processing instructions.

CS48AU2B functionality is controlled by DSP firmware or application codes that are downloaded to the CS48AU2B from a host controller or external serial FLASH/EEPROM.

Users can develop their applications using DSP Composer to create the processing chain and then compile the image into a series of commands that are sent to the CS48AU2B through the SCP. The processing application can either load modules (matrix-processors, virtualizers, post-processors) from the DSPs on-board ROM, or custom firmware can be downloaded through the SCP.

4.1.1 DSP Memory

The DSP core has its own on-chip data and program RAM and ROM and does not require external memory for post-processing applications.

The Y-RAM and P-RAM share a single block of memory that can be configured to make Y and P equal in size, or more memory can be allocated for Y-RAM in 2kword blocks.

4.1.2 DMA Controller

The powerful 8-channel DMA controller can move data between 8 on-chip resources. Each resource has its own arbiter: X, Y, and P RAMs/ROMs and the peripheral bus. Modulo and linear addressing modes are supported, with flexible start address and increment controls. The service intervals for each DMA channel, as well as up to 6 interrupt events, are programmable.

4.2 On-chip DSP Peripherals

4.2.1 Digital Audio Input Port (DAI)

The DAI port supports a wide variety of data input formats at sample rates (F_s) as high as 192 kHz. Up to 32-bit word lengths are supported. The DAI also supports a time division multiplexed (TDM) one-line data mode, that packs PCM audio on a single data line the total number possible depends on the ratio of SCLK to LRCLK. The CS48AU2B supports up to 8.

The port has two independent slave-only clock domains. Each data input can be independently assigned to a clock domain. The sample rate of the input clock domains can be determined automatically by the DSP, off-loading the task of monitoring the SPDIF receiver from the host. A time-stamping feature allows the input data to be sample-rate converted via software.

4.2.2 Digital Audio Output Port (DAO)

DAO port supports PCM resolutions of up to 32-bits. The port supports sample rates (F_s) as high as 192 kHz. The port can be configured as an independent clock domain mastered by the DSP, or as a clock slave if an external MCLK or SCLK/LRCLK source is available. One of the serial audio pins can be re-configured as a SPDIF transmitter that drives a bi-phase encoded S/PDIF signal (data with embedded clock on a single line).

The DAO also supports a time division multiplexed (TDM) one-line data mode, that packs multiple channels of PCM audio on a single data line.

4.2.3 Serial Control Port (I²C® or SPI™)

The on-chip serial control port is capable of operating as master or slave in either SPI™ or I²C® modes. Master/Slave operation is chosen by mode select pins when the CS48AU2B comes out of Reset. The serial clock pin can support frequencies as high as 25 MHz in SPI mode (SPI clock speed must always be $\leq (F_{clk}/2)$). The CS48AU2B serial control port also includes a pin for flow control of the communications interface (SCP_BSY) and a pin to indicate when the DSP has a message for the host (SCP_IRQ).

4.2.4 GPIO

Many of the CS48AU2B peripheral pins are multiplexed with GPIO. Each GPIO can be configured as an output, an input, or an input with interrupt. Each input-pin interrupt can be configured as rising edge, falling edge, active-low, or active-high.

4.2.5 PLL-based Clock Generator

The low-jitter PLL generates integer or fractional multiples of a reference frequency which are used to clock the DSP core and peripherals. Through a second PLL divider chain, a dependent clock domain can be output on the DAO port for driving audio converters. The CS48AU2B defaults to running from the external reference frequency and is switched to use the PLL output after overlays have been loaded and configured, either through master boot from an external FLASH or through host control. A built-in crystal oscillator circuit with a buffered output is provided. The buffered output frequency ratio is selectable between 1:1 (default) or 2:1.

4.2.6 Hardware Watchdog Timer

The CS48AU2B has an integrated watchdog timer that acts as a “health” monitor for the DSP. The watchdog timer must be reset by the DSP before the counter expires, or the entire chip is reset. This peripheral ensures that the CS48AU2B will reset itself in the event of a temporary system failure. In stand-alone mode (that is, no host MCU), the DSP will reboot from external FLASH. In slave mode

(that is, host MCU present) a GPIO will be used to signal the host that the watchdog has expired and the DSP should be rebooted and re-configured.

4.3 DSP I/O Description

4.3.1 Multiplexed Pins

Many of the CS48AU2B pins are multi-functional. For details on pin functionality please refer to the *CS485xx Hardware User's Manual*.

4.3.2 Termination Requirements

Open-drain pins on the CS48AU2B must be pulled high for proper operation. Please refer to the *CS485xx Hardware User's Manual* to identify which pins are open-drain and what value of pull-up resistor is required for proper operation.

Mode select pins in the CS48AU2B are used to select the boot mode upon the rising edge from reset. A detailed explanation of termination requirements for each communication mode select pin can be found in the *CS485xx Hardware User's Manual*.

4.3.3 Pads

The CS48AU2B I/Os operate from the 3.3 V supply and are 5 V tolerant.

4.4 Application Code Security

The external program code may be encrypted by the programmer to protect any intellectual property it may contain. A secret, customer-specific key is used to encrypt the program code that is to be stored external to the device. Please contact your local Cirrus representative for details.

5. Characteristics and Specifications

Note: All data sheet minimum and maximum timing parameters are guaranteed over the rated voltage and temperature. All data sheet typical parameters are measured under the following conditions: $T = 25^{\circ}\text{C}$, $C_L = 20\text{ pF}$, $V_{DD} = V_{DDA} = 1.8\text{ V}$, $V_{DDIO} = 3.3\text{ V}$, $G_{NDD} = G_{NDIO} = G_{NDA} = 0\text{ V}$.

5.1 Absolute Maximum Ratings

($G_{NDD} = G_{NDIO} = G_{NDA} = 0\text{ V}$; all voltages with respect to 0V)

Parameter	Symbol	Min	Max	Unit
DC power supplies:				
Core supply	VDD	-0.3	2.0	V
PLL supply	VDDA	-0.3	3.6	V
I/O supply	VDDIO	-0.3	3.6	V
VDDA – VDDIO		-	0.3	V
Input pin current, any pin except supplies	I_{in}	-	+/-10	mA
Input voltage on PLL_REF_RES	V_{filt}	-0.3	3.6	V
Input voltage on I/O pins	V_{inio}	-0.3	5.0	V
Storage temperature	T_{stg}	-65	150	$^{\circ}\text{C}$

Caution: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5.2 Recommended Operating Conditions

($G_{NDD} = G_{NDIO} = G_{NDA} = 0\text{ V}$; all voltages with respect to 0V)

Parameter	Symbol	Min	Typ	Max	Unit
DC power supplies:					
Core supply	VDD	1.71	1.8	1.89	V
PLL supply	VDDA	3.13	3.3	3.46	V
I/O supply	VDDIO	3.13	3.3	3.46	V
VDDA – VDDIO			0		V
Ambient operating temperature	T_A		-		$^{\circ}\text{C}$
- CQZ		0		+70	
- DQZ		-40		+85	

Note: It is recommended that the 3.3 V IO supply come up ahead of or simultaneously with the 1.8 V core supply.

5.3 Digital DC Characteristics

(Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	V_{IH}	2.0	-	-	V
Low-level input voltage, except XTl	V_{IL}	-	-	0.8	V
Low-level input voltage, XTl	V_{ILXTl}	-	-	0.6	V
Input Hysteresis	V_{hys}		0.4		V
High-level output voltage ($I_O = -2\text{ mA}$), except XTl	V_{OH}	$V_{DDIO} * 0.9$	-	-	V
Low-level output voltage ($I_O = 2\text{ mA}$), except XTl	V_{OL}	-	-	$V_{DDIO} * 0.1$	V
Input leakage XTl	I_{LXTl}	-	-	5	μA
Input leakage current (all digital pins with internal pull-up resistors enabled)	I_{LEAK}	-	-	70	μA

5.4 Power Supply Characteristics

(Measurements performed under operating conditions)

Parameter	Min	Typ	Max	Unit
Operational Power Supply Current:				
VDD: Core and I/O operating ¹	-	203	-	mA
VDDA: PLL operating	-	8	-	mA
VDDIO: With most ports operating	-	27	-	mA
Total Operational Power Dissipation:		480		mW
Standby Power Supply Current:				
VDD: Core and I/O not clocked	-	100	-	μA
VDDA: PLL halted	-	1	-	μA
VDDIO: All connected I/O pins 3-stated by other ICs in system	-	50	-	μA
Total Standby Power Dissipation:	-	348	-	μW

1. Dependent on application firmware and DSP clock speed.

5.5 Thermal Data (48-Pin LQFP)

Parameter	Symbol	Min	Typ	Max	Unit
Junction Temperature	T_j	-	-	125	°C
Thermal Resistance (Junction to Ambient)					
Two-layer Board ¹	θ_{ja}	-	63.5	-	°C / Watt
Four-layer Board ²		-	54	-	
Thermal Resistance (Junction to Top of Package)					
Two-layer Board ³	ψ_{jt}	-	0.70	-	°C / Watt
Four-layer Board ⁴		-	0.64	-	

1. Two-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20 % of the top & bottom layers.

2. Four-layer board is specified as a 76 mm X 114 mm, 1.6 mm thick FR-4 material with 1-oz. copper covering 20 % of the top & bottom layers and 0.5-oz. copper covering 90 % of the internal power plane & ground plane layers.

3. To calculate the die temperature for a given power dissipation

$$T_j = \text{Ambient Temperature} + [(\text{Power Dissipation in Watts}) * \theta_{ja}]$$

4. To calculate the case temperature for a given power dissipation

$$T_c = T_j - [(\text{Power Dissipation in Watts}) * \psi_{jt}]$$

5.6 Switching Characteristics— RESET

Parameter	Symbol	Min	Max	Unit
RESET minimum pulse width low	T_{rstl}	1	-	ms
All bidirectional pins high-Z after RESET low	T_{rst2z}	-	100	ns
Configuration pins setup before RESET high	T_{rstsu}	50	-	ns
Configuration pins hold after RESET high	T_{rsthld}	20	-	ns

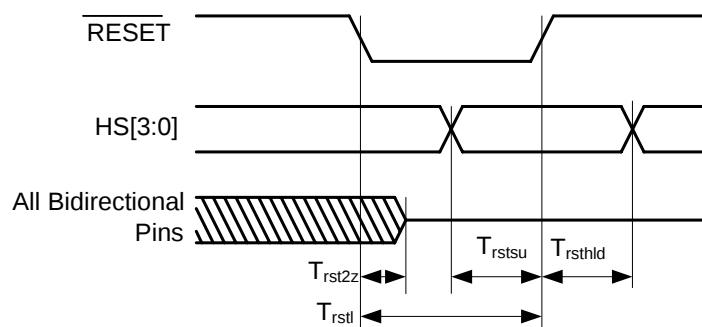


Figure 1. RESET Timing

5.7 Switching Characteristics — XTI

Parameter	Symbol	Min	Max	Unit
External Crystal operating frequency ¹	F_{xtal}	11.2896	27	MHz
XTI period	T_{clki}	33.3	100	ns
XTI high time	T_{clkih}	13.3	-	ns
XTI low time	T_{clkil}	13.3	-	ns
External Crystal Load Capacitance (parallel resonant) ²	C_L	10	18	pF
External Crystal Equivalent Series Resistance	ESR	-	50	Ω

1. Part characterized with +/- 50 PPM Crystal with the following frequency values: 11.2896, 12.288, 18.432, 24.576, and 27 MHz.
2. C_L refers to the total load capacitance as specified by the crystal manufacturer. Crystals that require a C_L outside this range should be avoided. The crystal oscillator circuit design should follow the crystal manufacturer's recommendation for load capacitor selection.

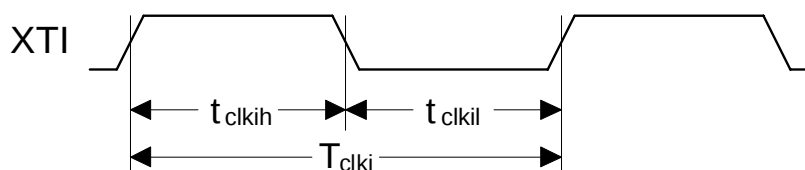


Figure 2. XTI Timing

5.8 Switching Characteristics — Internal Clock

Parameter	Symbol	Min	Max	Unit
Internal DCLK frequency ¹ CS48AU2B-CQZ	F_{dclk}	- F_{xtal}	150	MHz
Internal DCLK period ¹ CS48AU2B-CQZ	DCLKP	- 6.7	$1/F_{\text{xtal}}$	ns

1. After initial power-on reset, $F_{\text{dclk}} = F_{\text{xtal}}$. After initial kickstart commands, the PLL is locked to max F_{dclk} and remains locked until the next power-on reset.

5.9 Switching Characteristics — Serial Control Port - SPI Slave Mode.

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency ¹	f_{spisck}	-		25	MHz
SCP_CS falling to SCP_CLK rising	t_{spicss}	24		-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MOSI input	t_{spidsu}	5		-	ns
Hold time SCP_MOSI input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MISO output valid	t_{spidov}	-		11	ns
SCP_CLK falling to SCP_IRQ rising	t_{spiirqh}	-		20	ns
SCP_CS rising to SCP_IRQ falling	t_{spiirql}	0			ns
SCP_CLK low to SCP_IRQ rising	t_{spicsh}	24		-	ns
SCP_CS rising to SCP_MISO output high-Z	t_{spicsdz}	-	20		ns
SCP_CLK rising to SCP_BSY falling	t_{spibsyf}	-	$3 \times \text{DCLKP} + 20$		ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the SCP_BSY pin should be implemented to prevent overflow of the input data buffer. At boot the maximum speed is $F_{\text{xtal}}/3$.

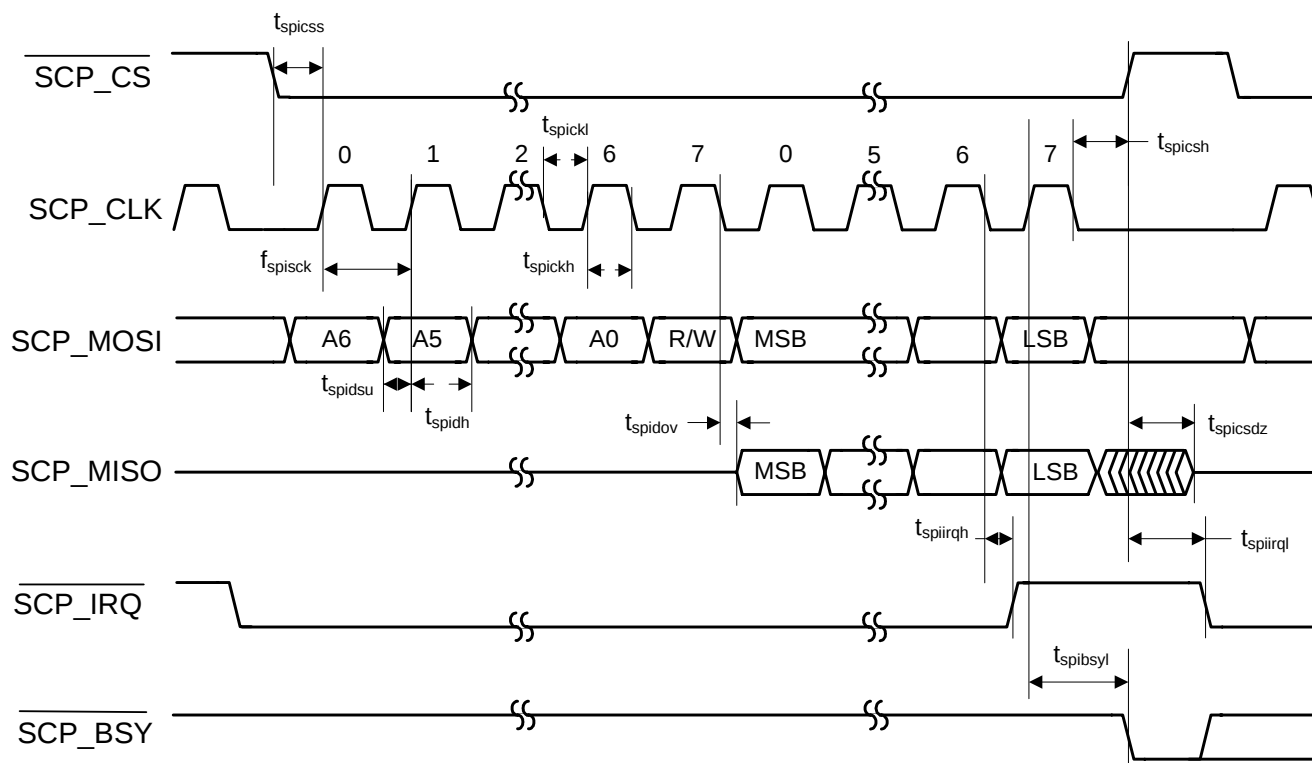


Figure 3. Serial Control Port - SPI Slave Mode Timing

5.10 Switching Characteristics — Serial Control Port - SPI Master Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency ¹	f_{spisck}	-		$F_{\text{xtal}}/2^2$	MHz
SCP_CS falling to SCP_CLK rising ³	t_{spicss}	-	$11 \cdot \text{DCLKP} + (\text{SCP_CLK PERIOD})/2$	-	ns
SCP_CLK low time	t_{spickl}	20		-	ns
SCP_CLK high time	t_{spickh}	20		-	ns
Setup time SCP_MISO input	t_{spidsu}	9		-	ns
Hold time SCP_MISO input	t_{spidh}	5		-	ns
SCP_CLK low to SCP_MOSI output valid	t_{spidov}	-		8	ns
SCP_CLK low to $\overline{\text{SCP_CS}}$ falling	t_{spicsl}	7		-	ns
SCP_CLK low to $\overline{\text{SCP_CS}}$ rising	t_{spicsh}	-	$11 \cdot \text{DCLKP} + (\text{SCP_CLK PERIOD})/2$	-	ns
Bus free time between active $\overline{\text{SCP_CS}}$	t_{spicsx}		$3 \cdot \text{DCLKP}$	-	ns
SCP_CLK falling to SCP_MOSI output high-Z	t_{spidz}	-		20	ns

1. The specification f_{spisck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.
2. See [Section 5.7](#).
3. SCP_CLK PERIOD refers to the period of SCP_CLK as being used in a given application. It does not refer to a tested parameter

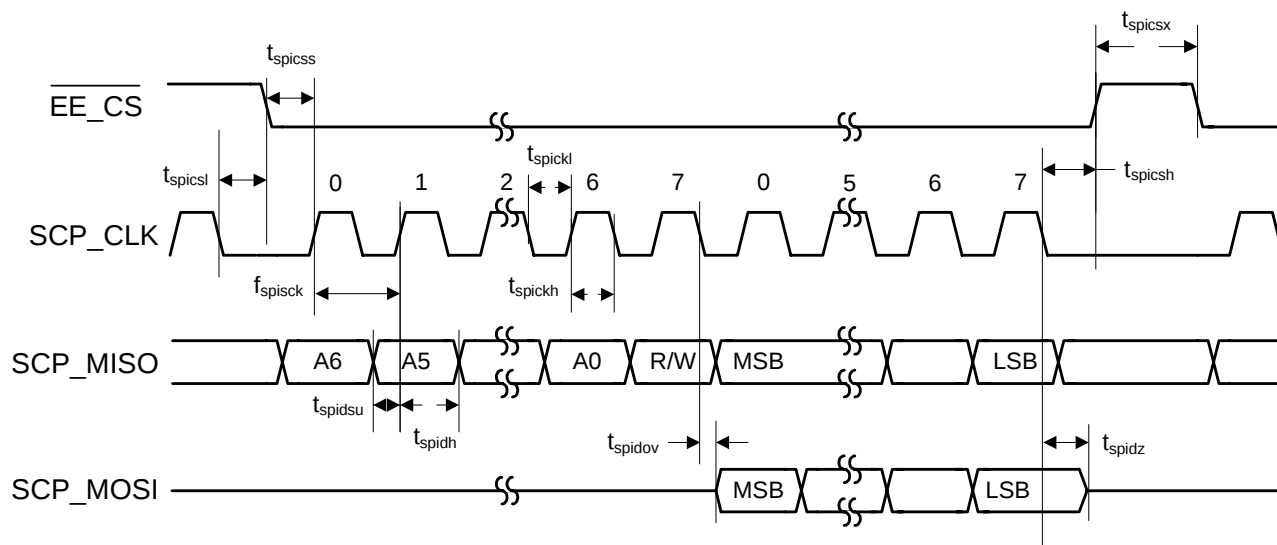


Figure 4. Serial Control Port - SPI Master Mode Timing

5.11 Switching Characteristics — Serial Control Port - I²C Slave Mode

Parameter	Symbol	Min	Typical	Max	Units
SCP_CLK frequency ¹	f_{iicck}	-		400	kHz
SCP_CLK low time	t_{iicckl}	1.25		-	μ s
SCP_CLK high time	t_{iicckh}	1.25		-	μ s
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25			μ s
START condition to SCP_CLK falling	$t_{iicstsc}$	1.25		-	μ s
SCP_CLK falling to STOP condition	t_{iicstp}	2.5		-	μ s
Bus free time between STOP and START conditions	t_{iicbft}	3		-	μ s
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100			ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20		-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-		18	ns
SCP_CLK falling to $\overline{\text{SCP_IRQ}}$ rising	$t_{iicirqh}$	-		$3 \cdot \text{DCLKP} + 40$	ns
NAK condition to $\overline{\text{SCP_IRQ}}$ low	$t_{iicirql}$		$3 \cdot \text{DCLKP} + 20$		ns
SCP_CLK rising to $\overline{\text{SCP_BSY}}$ low	$t_{iicbsyl}$	-	$3 \cdot \text{DCLKP} + 20$		ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application. Flow control using the $\overline{\text{SCP_BSY}}$ pin should be implemented to prevent overflow of the input data buffer.

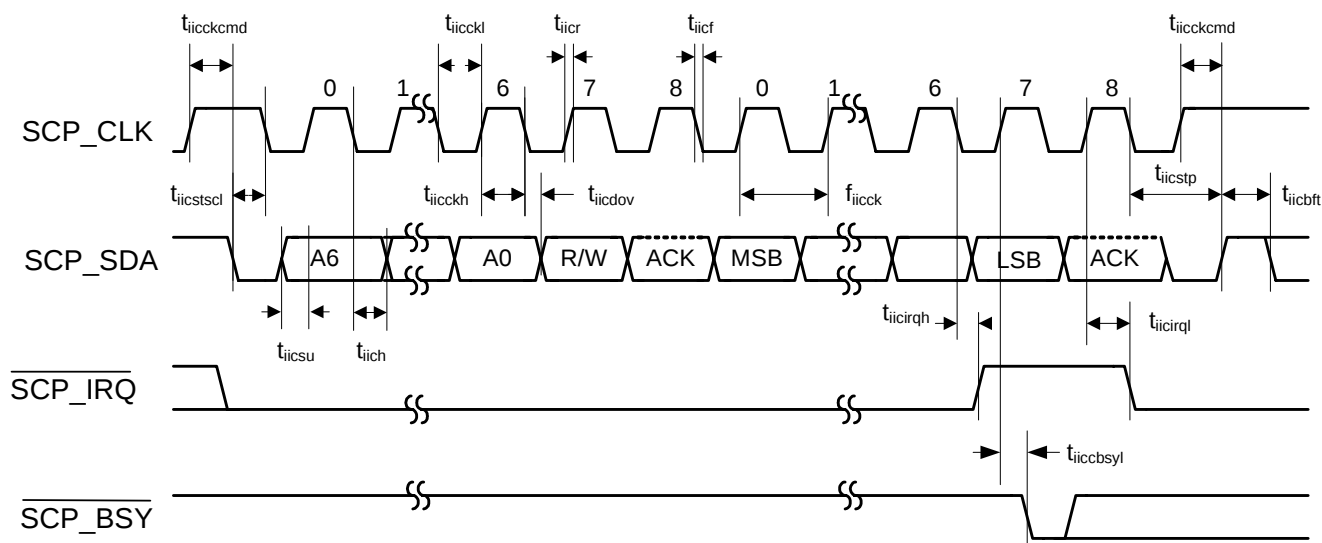


Figure 5. Serial Control Port - I²C Slave Mode Timing

5.12 Switching Characteristics — Serial Control Port - I²C Master Mode

Parameter	Symbol	Min	Max	Units
SCP_CLK frequency ¹	f_{iicck}	-	400	kHz
SCP_CLK low time	t_{iicckl}	1.25	-	μ s
SCP_CLK high time	t_{iicckh}	1.25	-	μ s
SCP_SCK rising to SCP_SDA rising or falling for START or STOP condition	$t_{iicckcmd}$	1.25		μ s
START condition to SCP_CLK falling	$t_{iicstscf}$	1.25	-	μ s
SCP_CLK falling to STOP condition	t_{iicstp}	2.5	-	μ s
Bus free time between STOP and START conditions	t_{iicbft}	3	-	μ s
Setup time SCP_SDA input valid to SCP_CLK rising	t_{iicsu}	100		ns
Hold time SCP_SDA input after SCP_CLK falling	t_{iich}	20	-	ns
SCP_CLK low to SCP_SDA out valid	t_{iicdov}	-	18	ns

1. The specification f_{iicck} indicates the maximum speed of the hardware. The system designer should be aware that the actual maximum speed of the communication port may be limited by the firmware application.

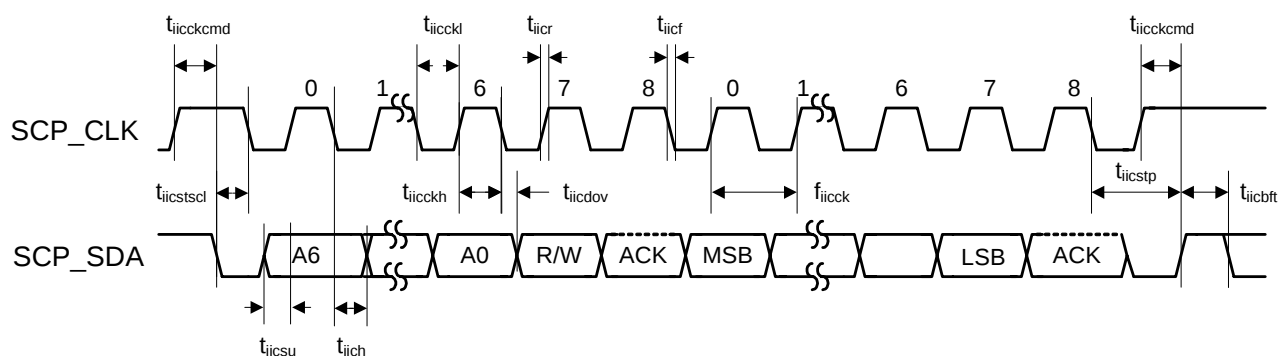


Figure 6. Serial Control Port - I²C Master Mode Timing

5.13 Switching Characteristics — Digital Audio Slave Input Port

Parameter	Symbol	Min	Max	Unit
DAI_SCLK period	$T_{daiclkp}$	40	-	ns
DAI_SCLK duty cycle	-	45	55	%
Setup time DAI_DATAn	t_{daidsu}	10	-	ns
Hold time DAI_DATAn	t_{daidh}	5	-	ns

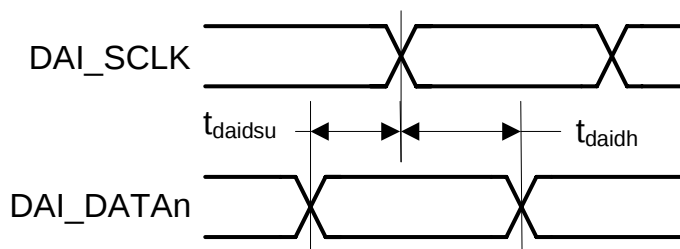


Figure 7. Digital Audio Input (DAI) Port Timing Diagram

5.14 Switching Characteristics — DSD Slave Input Port

Parameter	Symbol	Min	Typ	Max	Unit
DSD_SCLK Pulse Width Low	t_{sckl}	78	-	-	ns
DSD_SCLK Pulse Width High	t_{sckh}	78	-	-	ns
DSD_SCLK Frequency (64x Oversampled)	-	1.024	-	3.2	MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	-	-	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	20	-	-	ns

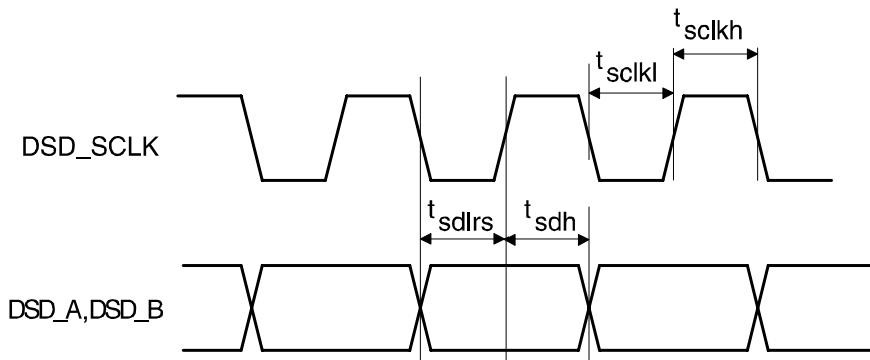
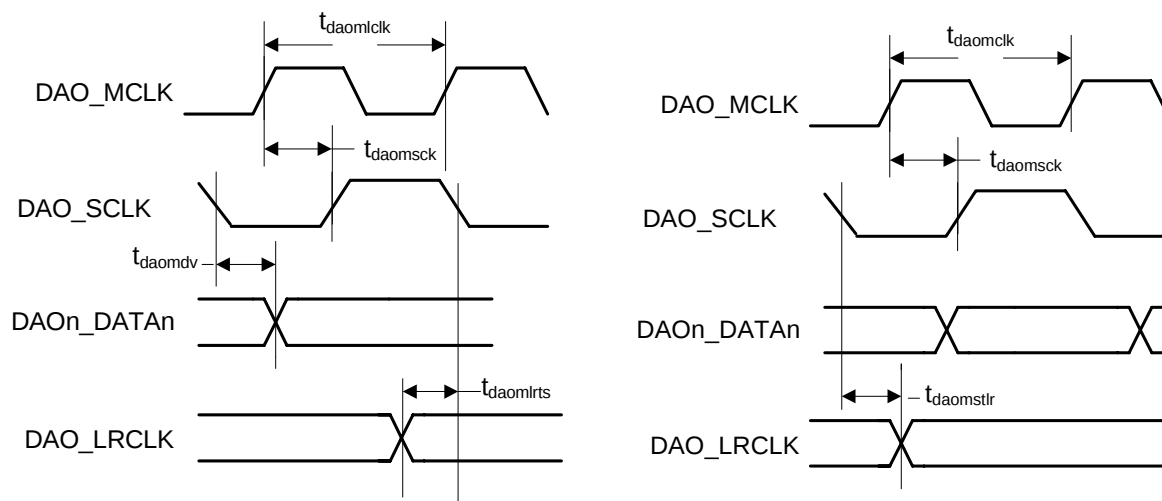


Figure 8. Direct Stream Digital - Serial Audio Input Timing

5.15 Switching Characteristics — Digital Audio Output Port

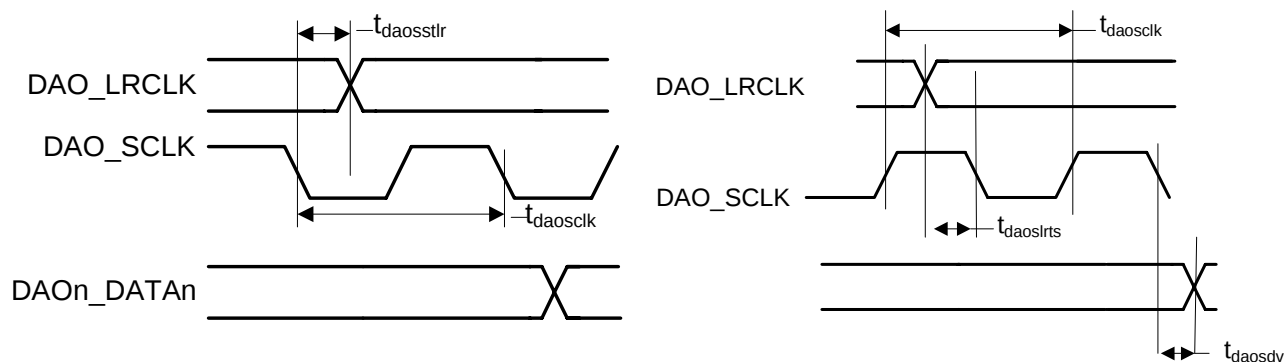
Parameter	Symbol	Min	Max	Unit
DAO_MCLK period	$T_{daomclk}$	40	-	ns
DAO_MCLK duty cycle	-	45	55	%
DAO_SCLK period for Master or Slave mode ¹	$T_{daosclk}$	40	-	ns
DAO_SCLK duty cycle for Master or Slave mode ¹	-	40	60	%
Master Mode (Output A1 Mode)^{1,2}				
DAO_SCLK delay from DAO_MCLK rising edge, DAO_MCLK as an input	$t_{daomsck}$	-	19	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively ³	$t_{daomstlr}$	-	8	ns
DAO_SCLK delay from DAO_LRCLK transition, respectively ³	$t_{daomlrts}$	-	8	ns
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition ³	t_{daomdv}	-	10	ns
Slave Mode (Output A0 Mode)⁴				
DAO1_DATA[3..0], DAO2_DATA[1..0] delay from DAO_SCLK transition ³	t_{daosdv}	-	15	ns
DAO_LRCLK delay from DAO_SCLK transition, respectively ³	$t_{daosstlr}$	-	30	ns
DAO_SCLK delay from DAO_LRCLK transition, respectively ³	$t_{daoslrts}$	-	15	ns

1. Master mode timing specifications are characterized, not production tested.
2. Master mode is defined as the CS48DVxx driving both DAO_SCLK, DAO_LRCLK. When MCLK is an input, it is divided to produce DAO_SCLK, DAO_LRCLK.
3. This timing parameter is defined from the non-active edge of DAO_SCLK. The active edge of DAO_SCLK is the point at which the data is valid.
4. Slave mode is defined as DAO_SCLK, DAO_LRCLK driven by an external source.



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 9. Digital Audio Output Port Timing, Master Mode



Note: In these diagrams, Falling edge is the inactive edge of DAO_SCLK

Figure 10. Digital Audio Output Timing, Slave Mode (Relationship LRCLK to SCLK)

6. Ordering Information

The CS48AU2B part number is described as follows:

CS48AU2I-XYZR

where

I - ROM ID Number

X - Product Grade

Y - Package Type

Z - Lead (Pb) Free

R - Tape and Reel Packaging

Table 3. Ordering Information

Part No.	Grade	Temp. Range	Package
CS48AU2B-CQZ	Commercial	0 to +70 °C	48-pin LQFP

NOTE: Please contact the factory for availability of the -D (automotive grade) package.

7. Environmental, Manufacturing, & Handling Information

Table 4. Environmental, Manufacturing, & Handling Information

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS48AU2B-CQZ	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8. Device Pinout Diagram

8.1 CS48AU2B, 48-pin LQFP Pinout Diagram

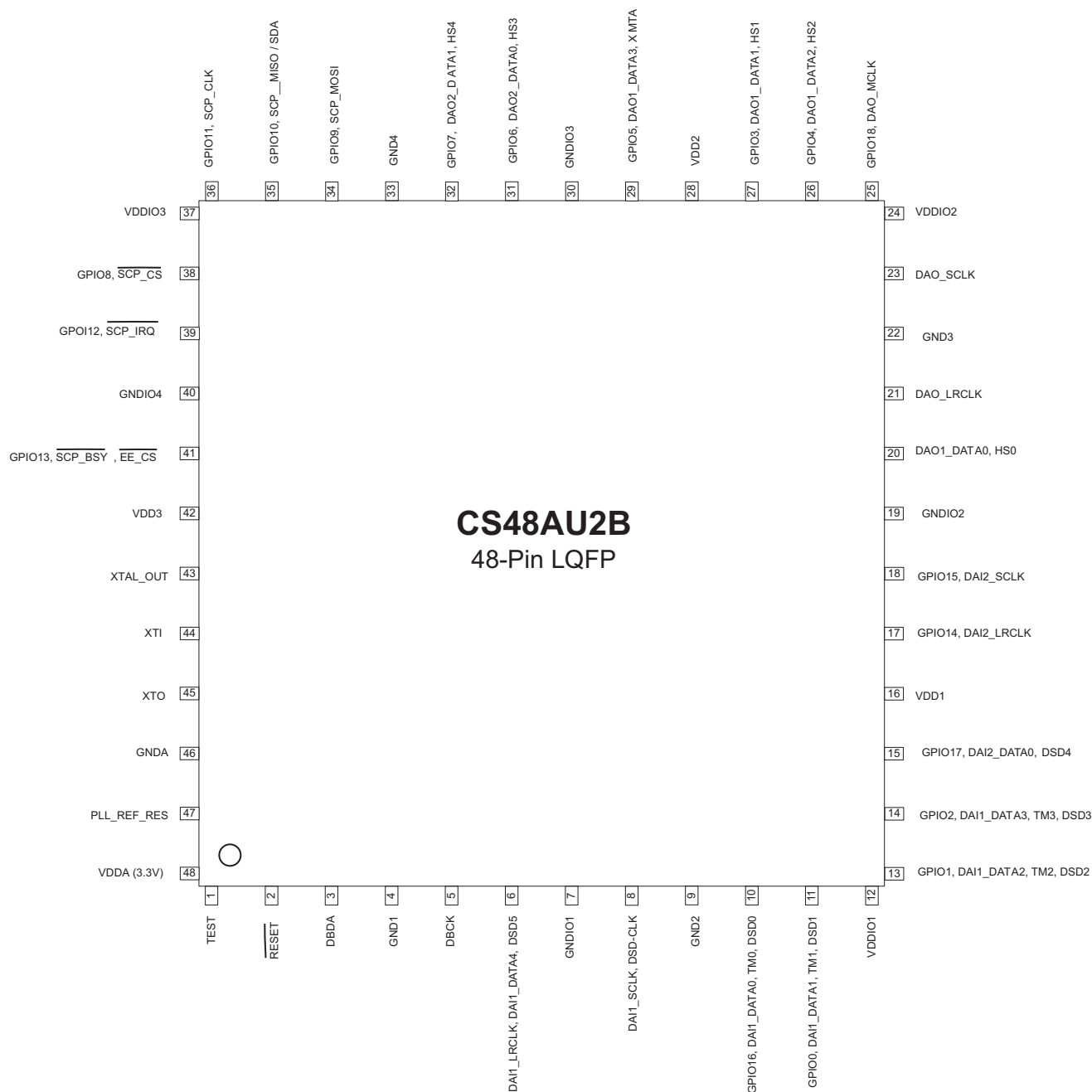
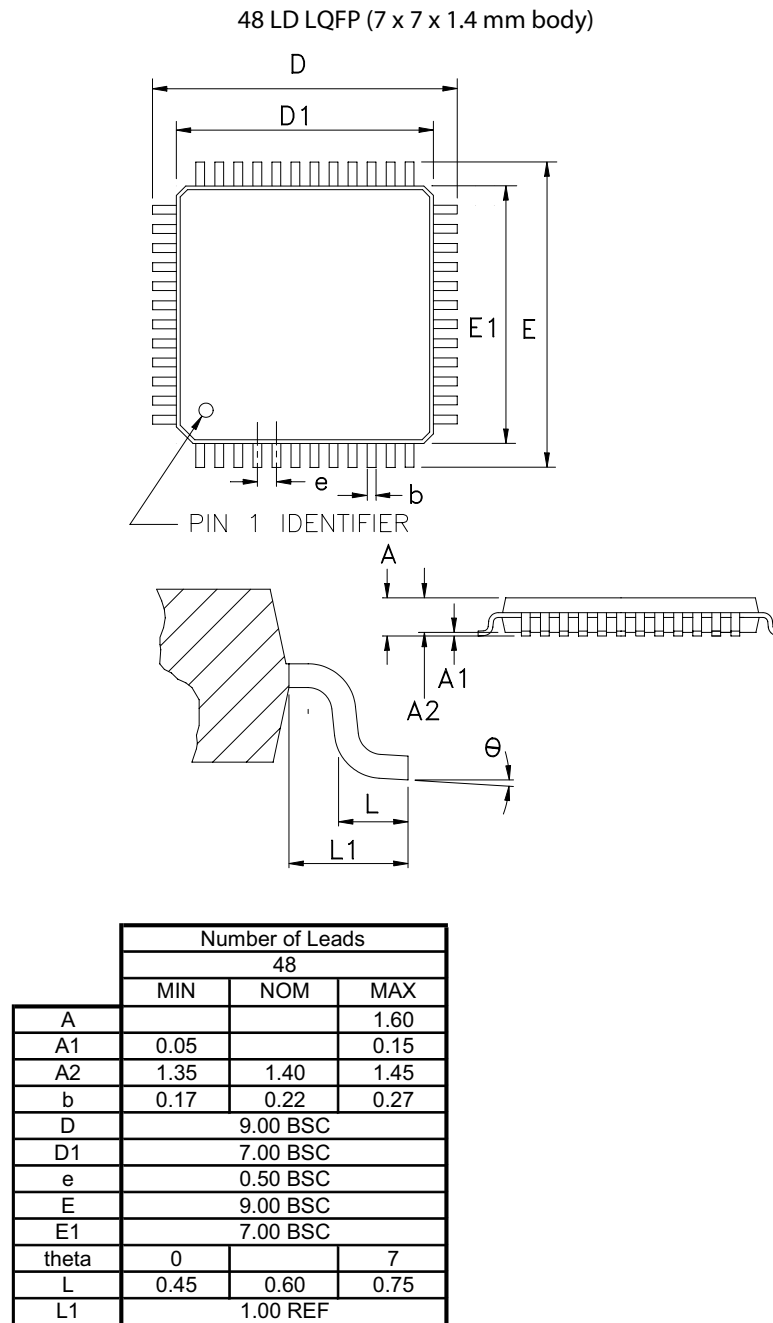


Figure 11. CS48AU2B, 48-Pin LQFP Pinout

9. Package Mechanical Drawings

9.1 48-pin LQFP Package Drawing



NOTES:

- 1) Reference document: JEDEC MS-026
- 2) All dimensions are in millimeters and controlling dimension is in millimeters.
- 3) D1 and E1 do not include mold flash which is 0.25 mm max. per side. A1
- 4) Dimension b does not include a total allowable dambar protrusion of 0.08 mm max.

Figure 12. 48-Pin LQFP Package Drawing

10. Revision History

Revision	Date	Changes
F1	December 2, 2008	Initial Release
F2	February 16, 2009	Updated Section 5.5 , adding Junction Temperature specification.
F3	May 27, 2009	Updated Note 1 in Section 5.7 .

