

N-Channel Trench Power MOSFET

General Description

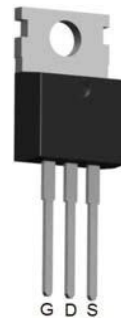
The CS40N27 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged E_{AS} capability and ultra low $R_{DS(ON)}$ is suitable for PWM, load switching .

Features

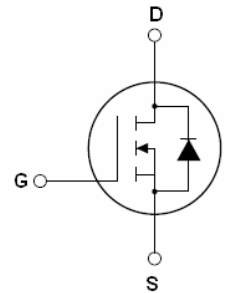
- $V_{DS}=40V$; $I_D=170A@ V_{GS}=10V$;
 $R_{DS(ON)}<3.6m\Omega @ V_{GS}=10V$
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

Application

- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



To-220 Top View



Schematic Diagram

$$V_{DSS} = 40V$$

$$I_{DSS} = 170A$$

$$R_{DS(ON)} = 3.0m\Omega$$

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
CS40N27	CS40N27	TO-220	-	-	-

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{GS}=0V$)	40	V
V_{GS}	Gate-Source Voltage ($V_{DS}=0V$)	± 20	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	170	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	119	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	680	A
dv/dt	Peak Diode Recovery Voltage	1.83	V/ns
P_D	Maximum Power Dissipation($T_c=25^\circ C$)	231	W
	Derating Factor	1.54	W/°C
E_{AS}	Single Pulse Avalanche Energy (Note 2)	1800	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, I_{AS}=85A, V_{GS}=10V, R_G=25\Omega$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	---	0.65	°C/W

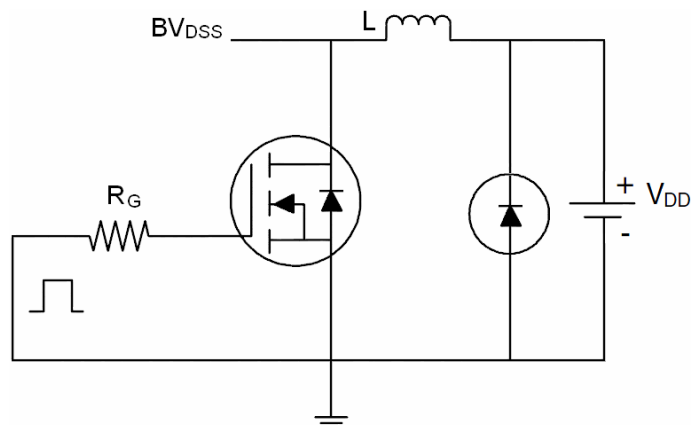
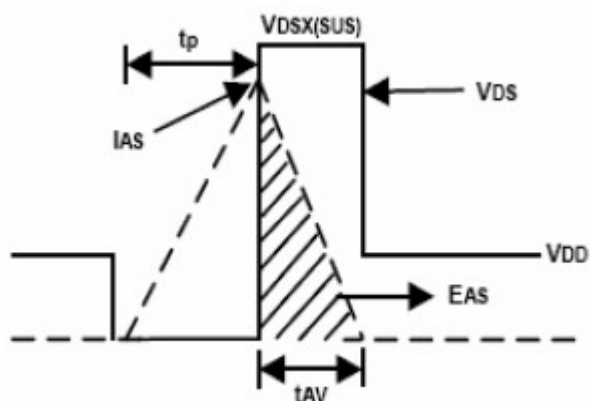
Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V I _D =250μA	40			V
I _{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V _{DS} =40V,V _{GS} =0V			1	μA
I _{DSS}	Zero Gate Voltage Drain Current(Tc=125℃)	V _{DS} =40V,V _{GS} =0V			1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V,V _{DS} =0V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	2		4	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =40A		3.0	3.6	mΩ
Dynamic Characteristics						
g _{FS}	Forward Transconductance	V _{DS} =10V,I _D =40A	40			S
C _{iss}	Input Capacitance	V _{DS} =25V,V _{GS} =0V f=1.0MHz		7585		PF
C _{oss}	Output Capacitance			967		PF
C _{rss}	Reverse Transfer Capacitance			625		PF
Q _g	Total Gate Charge	V _{DS} =32V,I _D =75A V _{GS} =10V		144		nC
Q _{gs}	Gate-Source Charge			36		nC
Q _{gd}	Gate-Drain Charge			53		nC
Switching Times						
t _{d(on)}	Turn-on Delay Time	V _{DD} =20V,I _D =75A V _{GS} =10V,R _G =3.0Ω		38		nS
t _r	Turn-on Rise Time			47		nS
t _{d(off)}	Turn-Off Delay Time			64		nS
t _f	Turn-Off Fall Time			26		nS
Source-Drain Diode Characteristics						
I _{SD}	Source-Drain Current(Body Diode)			170		A
I _{SDM}	Pulsed Source-Drain Current(Body Diode)			680		A
V _{SD}	Forward On Voltage ^(Note 1)	T _J =25℃,I _{SD} =40A,V _{GS} =0V		0.82	0.99	V
t _{rr}	Reverse Recovery Time ^(Note 1)	T _J =25℃,I _F =40A di/dt=100A/μs		28		nS
Q _{rr}	Reverse Recovery Charge ^(Note 1)			22		nC
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by L _S +L _D)				

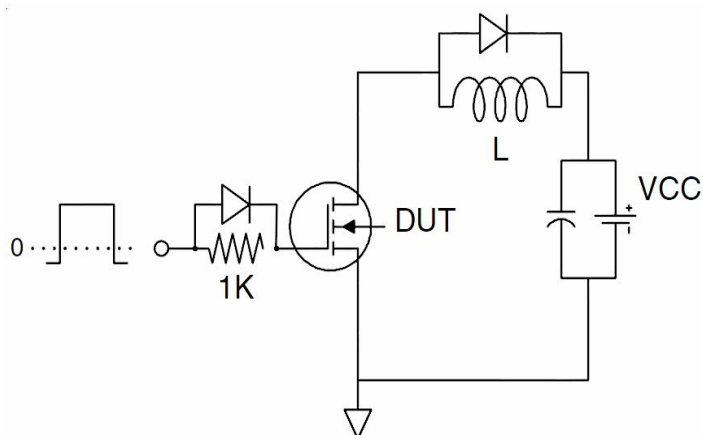
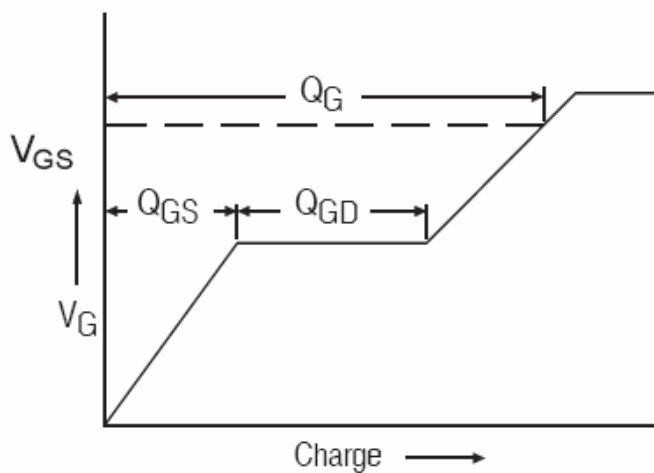
Notes 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 1.5\%$, $R_G=25\Omega$, Starting $T_J=25^\circ C$

Test Circuit

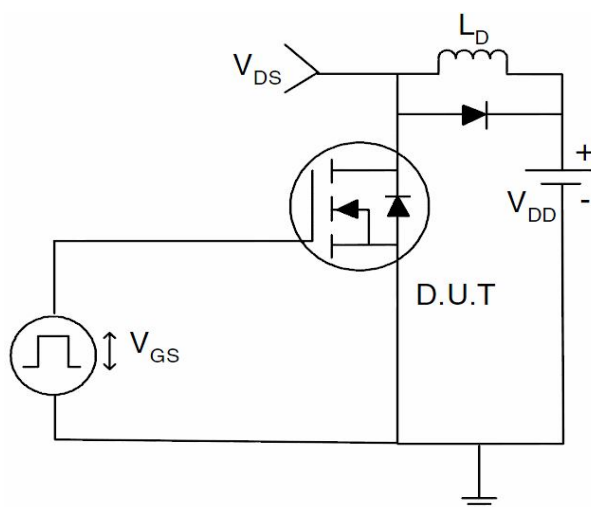
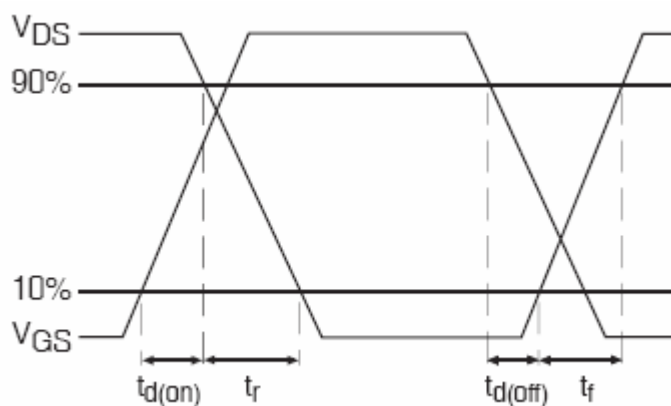
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Output Characteristics

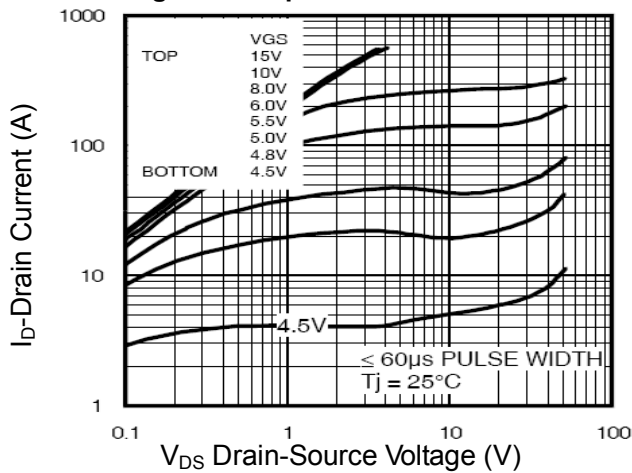


Figure2. Transfer Characteristics

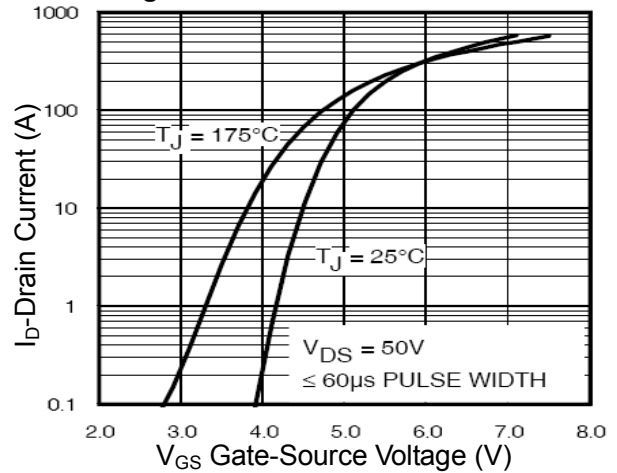


Figure3. VGS(th) vs Junction Temperature

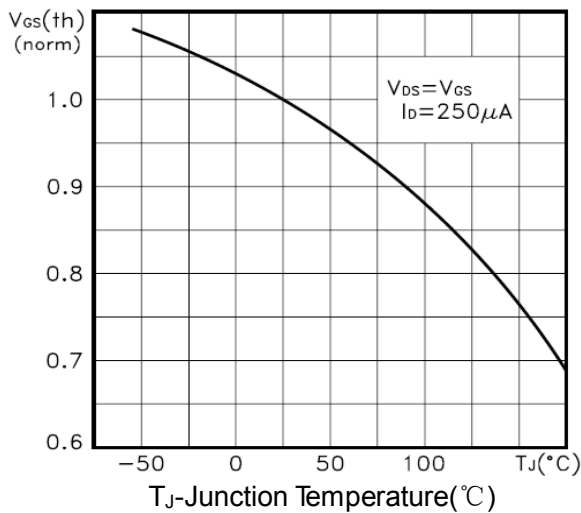


Figure4. BVDS vs Junction Temperature

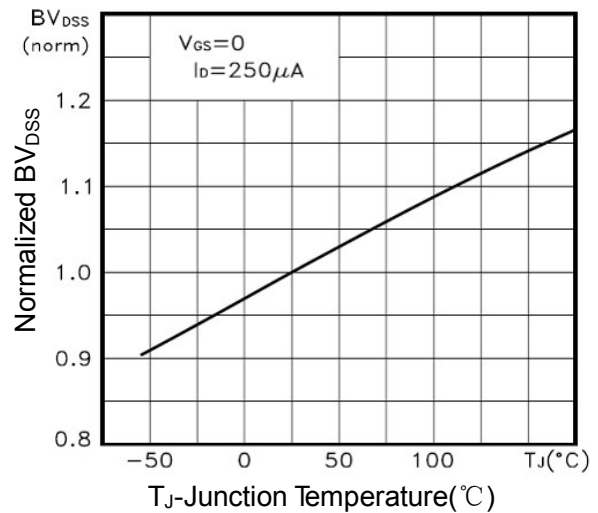


Figure5. ID vs Junction Temperature

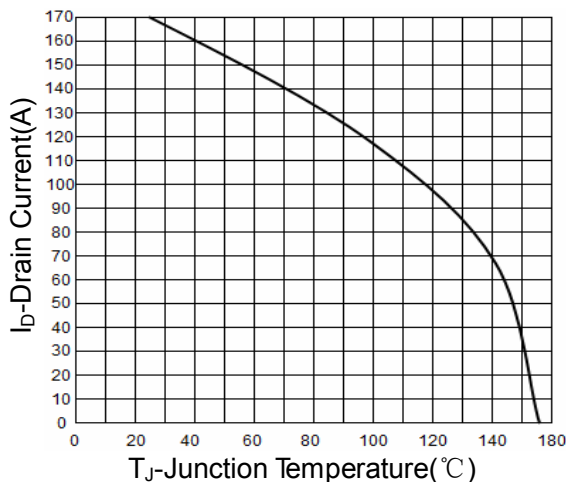


Figure6. RDS(ON)- Junction Temperature

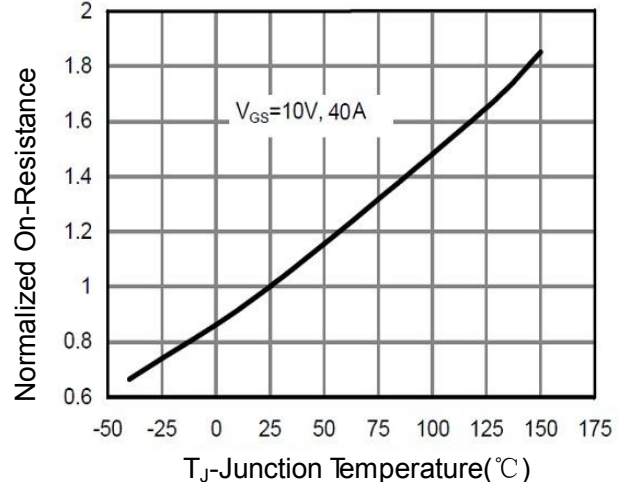


Figure7. Gate Charge

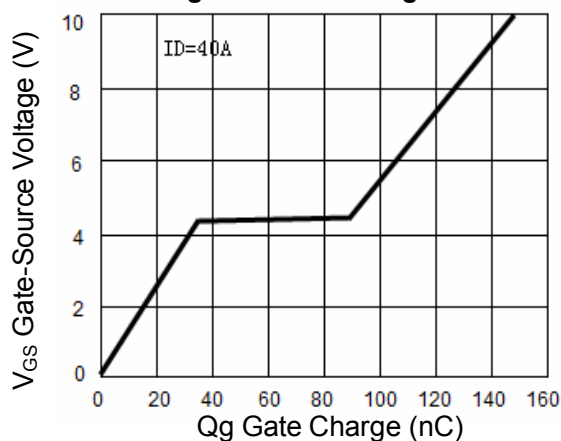


Figure8. Capacitance vs V_{DS}

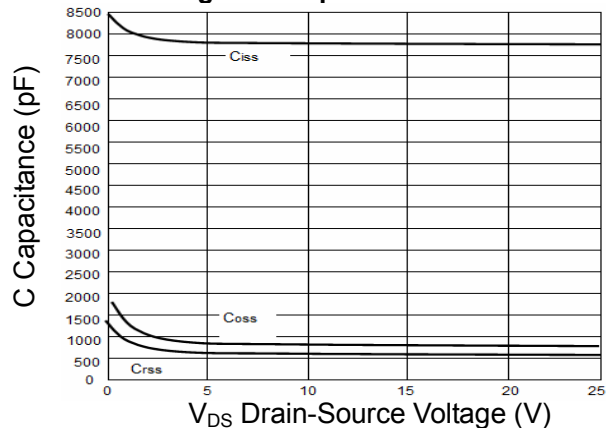


Figure9. Source- Drain Diode Forward

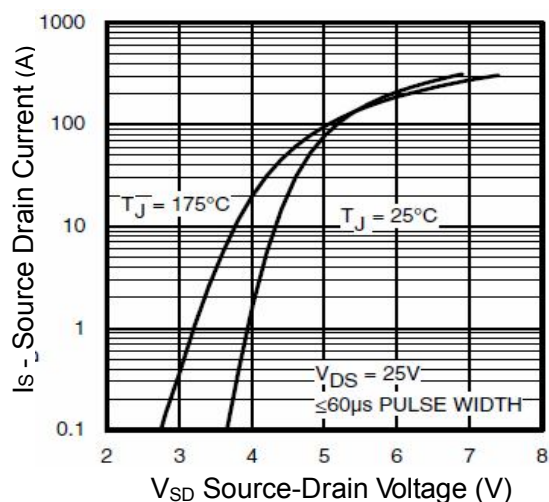


Figure10. Safe Operation Area

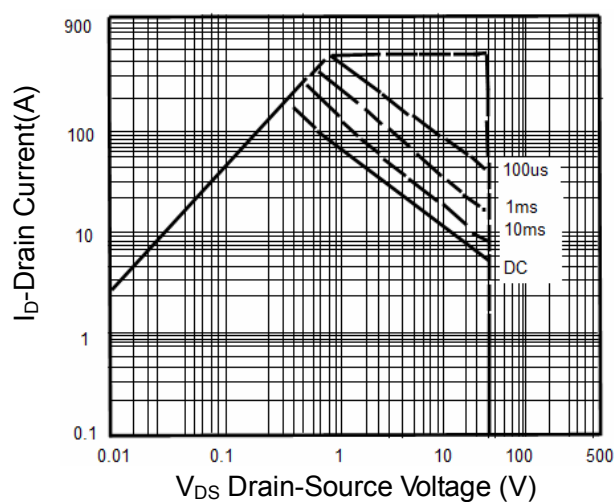
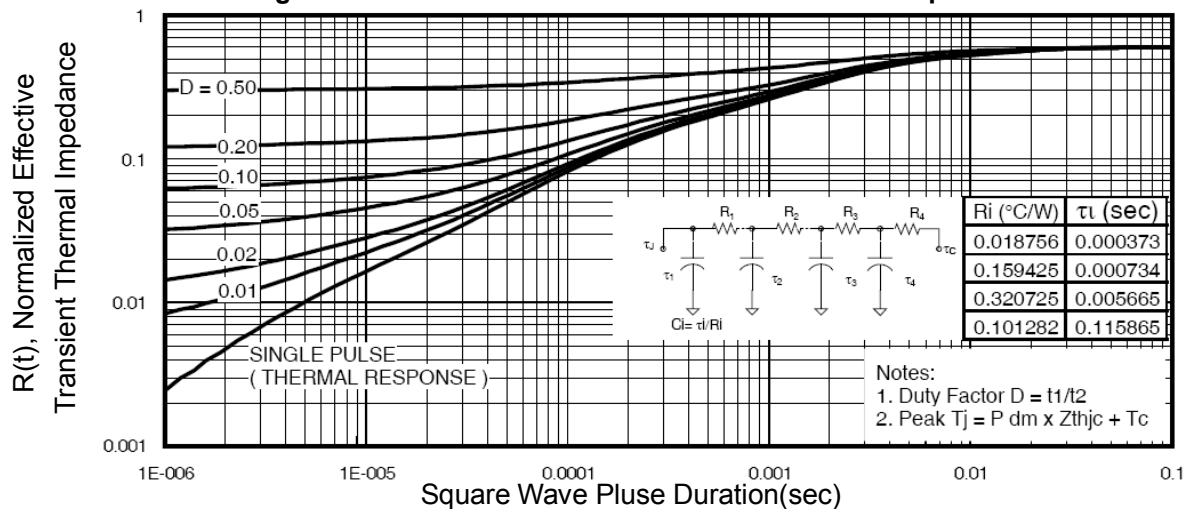
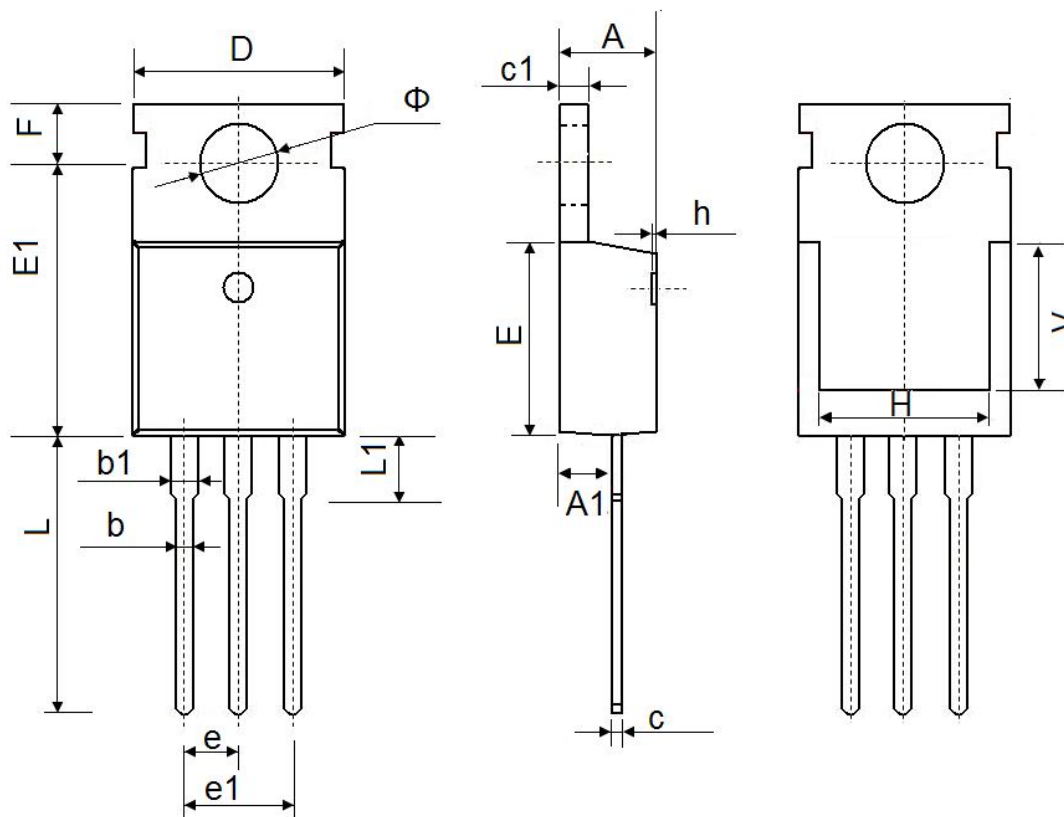


Figure11. Normalized Maximum Transient Thermal Impedance



TO-220 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max
A	4.300	4.700	0.169	0.185
A1	2.200	2.600	0.087	0.102
b	0.700	0.950	0.028	0.037
b1	1.170	1.410	0.046	0.056
c	0.450	0.650	0.018	0.026
c1	1.200	1.400	0.047	0.055
D	9.600	10.400	0.378	0.409
E	8.8500	9.750	0.348	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.750	14.300	0.502	0.563
L1	2.850	3.950	0.112	0.156
V	7.500 REF.		0.295 REF.	
Φ	3.400	4.000	0.134	0.157