1. Product overview

1.1. Functional features

- Core
  - 32-bit ARM® Cortex® -M0 CPU
  - Max operating frequency 24 MHz
- Memorizer
  - 64 K Bytes Flash memory
  - 4K Bytes SRAM
- Clock module
  - Internal 4/24MHz RC oscillator (HRC), with the accuracy of ± 1% in a typical case
  - Internal 38.4KHz/32.768KHz RC oscillator (LRC), with the accuracy of ± 10% in a typical case
  - 4~24MHz crystal oscillator (HXT)
  - 32.768KHz low-speed crystal oscillator (LXT)
- Operating environment
  - VDD voltage: 2.5 to 5.5V
  - Temperature range: -40 to 85℃
- Power management
  - Low-power mode: Sleep, deep sleep
  - Support POR (power-on reset)/ PDR (power-down reset)
  - Support LVD (low voltage detection)
- General-purpose I/O (input/ output)
  - 16 inputs and outputs (I/O)
  - All I/O mapped external interrupt vectors
- Analog-to-digital convertor (ADC)
  - One 12-bit ADC
  - Max 1μs conversion time
  - Support 7 external input channels
  - Operating voltage range: 2.5 to 5.5V
  - Input voltage conversion range: 0~5.5V
- Analog comparator
  - Built-in filter
  - With built-in 2.5V comparison reference (V_{REF}), and support taking V_{REF}, $3/4V_{REF}$, $1/2V_{REF}$, $1/4V_{REF}$ as comparison reference
- Timer
  - 1 × 16bit advanced control timer (TIM1), support 6 PWM output channels with dead zone control.
  - 1 × 16-bit general-purpose timer, support 4-channel compare output/input capture, PWM output
  - 1 × 16-bit PWM controller, support 5-channel input capture/compare output and PWM output
  - 2 × 16-bit/32-bit basic timer/counter
  - 1 × 16-bit low-power timer
  - 1 × Automatic wake-up timer (AWT)
  - 1 × independent watchdog timer (FWDT)
  - 1 × window watchdog timer (WWDT)
  - 1 system timer: 24-bit self-decrement counter
- Interrupt and event
  - Up to 32 interrupt channels that can be shielded separately
  - 4 priorities optionally
  - 16 external interrupt lines
- RTC and standby register
  - Calendar function
  - Alarm and periodically wake up from the sleep mode
  - RTC clock source: LXT, LRC, HXT
- Serial peripheral interface (SPI)
  - Configured as master or slave by programming
  - Full-duplex communication capability
  - 7 optional baud rates
  - 4 transmission modes
  - Maximum baud rate in master mode: 1/2 system clock
  - Maximum baud rate in slave mode: 1/4 system clock
  - Configurable serial clock polarity and phase
  - Support interrupt mode
  - 8-bit data transmission (high bit first, low bit then)
- Universal synchronous/ asynchronous receiver/ transmitter(USART)
  - 2 USART
  - Support half duplex and full duplex transmission;
  - Support 8bit and 9bit data format;
  - Support multi-machine communication mode; support automatic address recognition; support given address and broadcast address.
- Low power asynchronous receiver/transmitter (LPUART)
  - 1 LPUART
  - Support half duplex and full duplex transmission;
  - Support 8BITand 9BIT data format;
  - Support multi-machine communication mode; support automatic address recognition; support given address and broadcast address
  - Support low-power mode
- I^2C
  - 1 I^2C, support master/ slave mode
  - Support standard (100Kbps)/fast (400Kbps)
  - Support 7-bit addressing function
  - Support noise filtering function
  - Support broadcast address
  - Support interrupt status query function
- CRC generator/ checker
- 96bit unique ID for chip (UNID)
- Serial wire debugging (SWD)

1.2. Product description

The CS32L010 microcontroller incorporates the 32-bit ARM® Cortex®-M0 core with ultra-low power consumption. It can operate at a frequency up to 24 MHz. An embedded Flash of 64K bytes and a SRAM of 4K bytes are built in, and a great number of peripheral interfaces such as 12-bit 1 Msps high-precision SAR-type ADC, RTC, comparator, multi-channel UART, SPI, I^2C and PWM are integrated, making it a highly-integrated product with strong anti-interference and high reliability.

Series CS32L010 MCU has the operating temperature range of -40℃~85℃ and the operating voltage range of 2.5V~5.5V. The chip provides a series of operating modes of power supply to meet the requirements for different applications of low power consumption.

Series CS32L010 MCU is applicable to various application scenarios, i.e. electronic cigarette, wearable devices, personal care products, and other consumer applications.

1.3. Component list

Package types for series CS32L010 include: QFN20, SSOP20

Table 1 Series CS32L010

Components		CS32L010
Flash memory (K Bytes)		64
SRAM (K Bytes)		4
Timer	16-bit advanced control	1
	16-bit general purpose	1
	Low power	1
	Basic	2
	Independent watchdog	1
	Window watch dog timer	1
	Tick timer	1
Communication interfaces	SPI	1
	I^2C	1
	USART	2
	LPUART	1
ADC	Number	1
	Number of external channels	7
	Number of internal channels	3
I/O		16
Clocks: HXT/LXT/HRC/LRC		1/1/1/1
Operating voltage		2.5~5.5V
Operating temperature		Ambient temperature: -40~85°C
Package type		QFN20, SSOP20

1.4. System block diagram

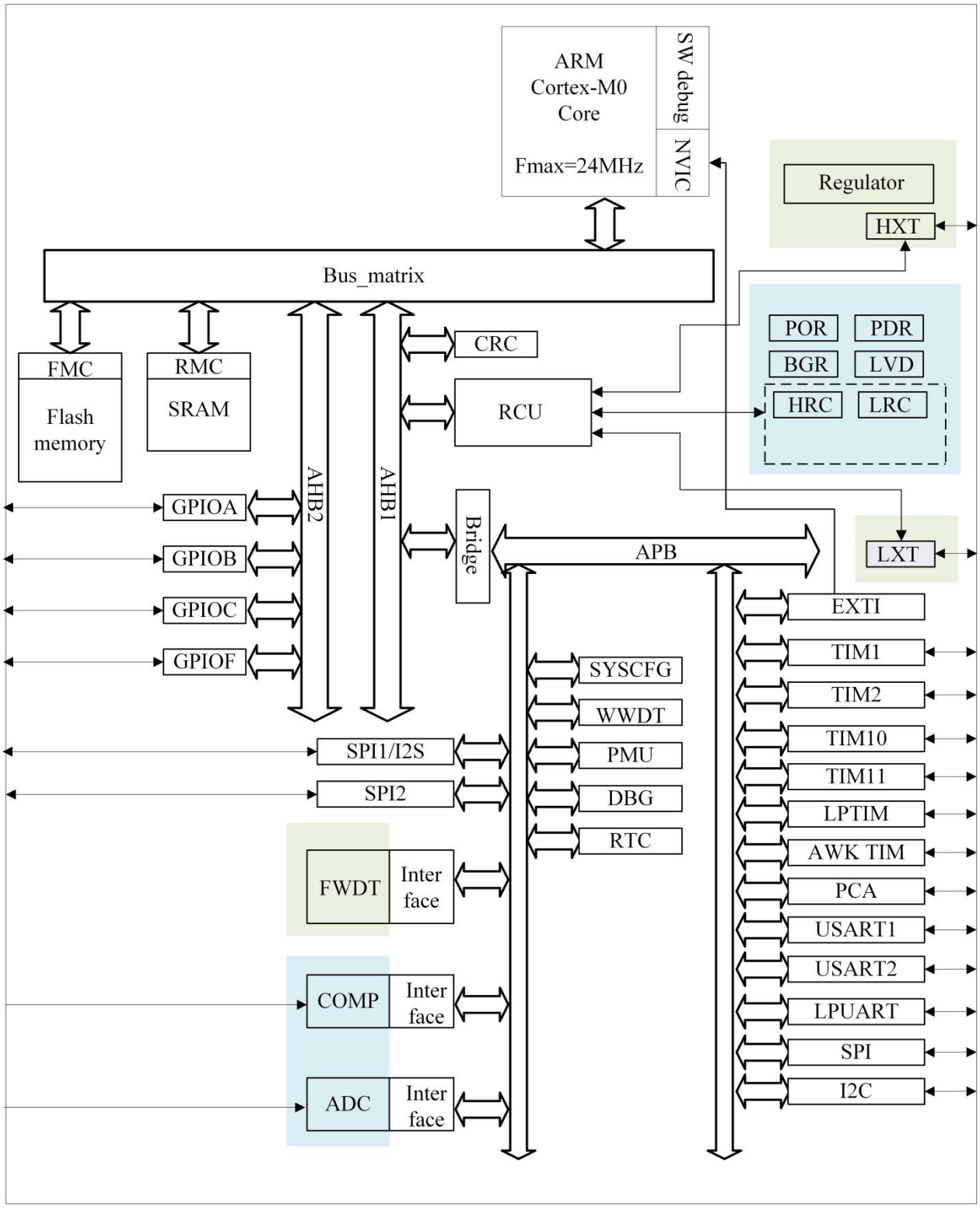


Figure 1 Block diagram of system module

Table of Contents

Revision History

Version	Change Recrod	Date
V1.0	Officially released	October 21, 2021
V1.1	Change the cover; and add a screen print on order information	December 27, 2021
V1.2	Update PD3 port output low level $\|I_{sunk\text{-}pin}\|$ data	December 28, 2021
V1.4	Add Reflow curve, package description and HSF statement	August 11, 2022

2. Pin description

2.1. QFN20

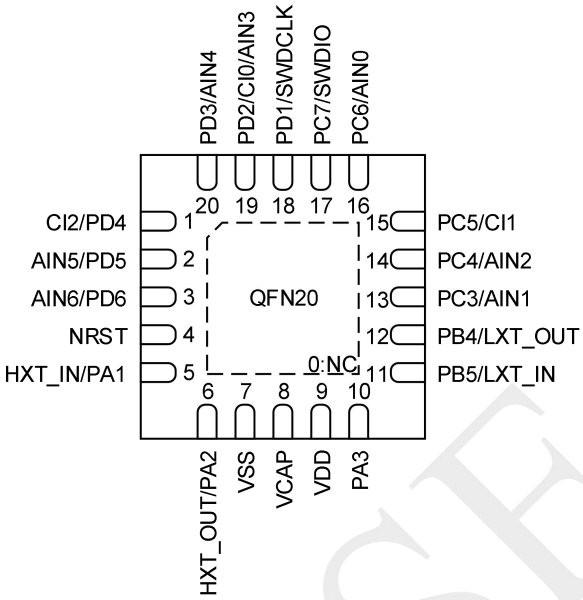


Figure 2 Pin diagram of QFN20 package

2.2. SSOP20

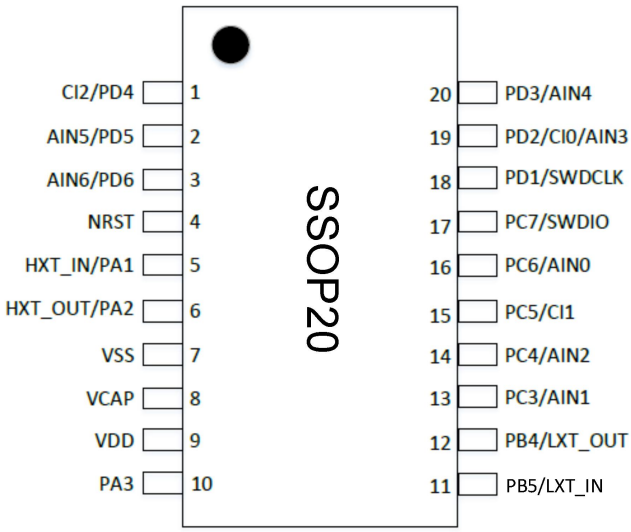


Figure 3 Pin diagram of SSOP20 package

2.3. Pin description

Table 2 Pin descriptions

Pin No.		Name of pin	Type	Alternate function	Description
QFN20	SSOP20				
4	4	NRST	I	Reset input/ internal reset output (active low)	
5	5	HXT_IN/PA1	I/O	OSC_IN	External crystal oscillator input
				PA1	PA1 general digital input/output pin
				TIM1_CH2N	TIM1 PWM2 reverse output
				SPI_CLK	SPI module clock signal
				I2C_SDA	I^2C data
				UART0_RX	UART0 RX
				TIM10_TOG	TIM10 toggle output
				UART1_RX	UART1 RX
6	6	HXT_OUT/PA2	I/O	OSC_OUT	External crystal oscillator output
				PA2	PA2 general digital input/output pin
				TIM1_CH3	TIM1 PWM output 3
				SPI_NSS	SPI module slave mode selection signal
				I2C_SCL	I^2C clock
				UART0_TX	UART0 TX
				TIM10_TOGN	TIM10 flip reverse output
				UART1_TX	UART1 TX
				TIM2_CH2	TIM2 capture input/compare output 2
7	7	VSS	S	Chip ground	
8	8	VCAP	S	LDO core power supply (only for internal circuits, and external circuit is connected to capacitance)	
9	9	VDD	S	Chip power supply	
10	10	PA3	I/O	PA3	PA3 general digital input/output pin
				TIM1_CH3N	TIM1 PWM3 reverse output
				PWMC_CH2	PWMC capture input/compare output 2
				SPI_NSS	SPI module slave mode selection signal
				RTC_1HZ	RTC 1Hz output
				LPUART_RX	LPUART RX
				PWMC_ECI	PWMC external clock input
				CO	Analog comparator output
				TIM2_CH3	TIM2 capture input/compare output 3
11	11	LXT_IN/PB5	I/O	X32K_IN	External 32K crystal oscillator input
				PB5	PB5 general digital input/output pin
				TIM1_BKIN	TIM1 break signal input
				PWMC_CH4	PWMC capture input/compare output 4
				SPI_CLK	SPI module clock signal
				I2C_SDA	I^2C data
				UART0_RX	UART0 RX
				TIM11_TOG	TIM11 toggle output

Pin No.		Name of pin	Type	Alternate function	Description
QFN20	SSOP20				
				LVD_OUT	Low-voltage detection comparator output
				TIM2_CH1	TIM2 capture input/compare output 1
12	12	LXT_OUT/PB4	I/O	X32K_OUT	External 32K crystal oscillator output
				PB4	PB4 general digital input/output pin
				LPTIM_GATE	LPTIM gate control
				PWMC_ECI	PWMC external clock input
				SPI_NSS	SPI module slave mode selection signal
				I2C_SCL	I^2C clock
				UART0_TX	UART0 TX
				TIM1_TOGN	TIM11 flip reverse output
13	13	AIN1/PC3	I/O	PC3	PC3 general digital input/output pin
				TIM1_CH3	TIM1 PWM output 3
				TIM1_CH1N	TIM1 PWM1 reverse output
				I2C_SDA	I^2C data
				UART1_TX	UART1 TX
				PWMC_CH1	PWMC capture input/compare output 1
				TIM2_CH3	TIM2 capture input/compare output 3
				AIN1	ADC analog input channel 1
14	14	PC4/AIN2	I/O	PC4	PC4 general digital input/output pin
				TIM1_CH4	TIM1 PWM output 4
				TIM1_CH2N	TIM1 PWM2 reverse output
				I2C_SCL	I^2C clock
				UART1_RX	UART1 RX
				PWMC_CH0	PWMC capture input/compare output 0
				CLK_MCO	CPU clock output
				TIM2_CH4	TIM2 capture input/compare output 4
				AIN2	ADC analog input channel 2
				-	-
15	15	PC5/CI1	I/O	PC5	PC5 general digital input/output pin
				TIM1_BKIN	TIM1 break signal input
				PWMC_CH0	PWMC capture input/compare output 0
				SPI_CLK	SPI module clock signal
				LPUART_TX	LPUART TX
				TIM1_GATE	TIM11 gate control
				LVD_OUT	Low-voltage detection comparator output
				TIM2_CH1	TIM2 capture input/compare output 1
				CI1	Analog comparator input
16	16	PC6/AIN0	I/O	PC6	PC6 general digital input/output pin
				TIM1_CH1	TIM1 PWM output 1
				PWMC_CH3	PWMC capture input/compare output 3
				SPI_MOSI	SPI module MOSI (master output slave input) signal

Pin No.		Name of pin	Type	Alternate function	Description
QFN20	SSOP20				
				LPUART_RX	LPUART RX
				TIM11_EXT	TIM11 external pulse input
				CLK_MCO	CPU clock output
				TIM2_CH4	TIM2 capture input/compare output 4
				AIN0	ADC analog input channel 0
17	17	PC7/SWDIO	I/O	SWDIO	SWD IO
				PC7	PC7 general digital input/output pin
				TIM1_CH2	TIM1 PWM output 2
				PWMC_CH4	PWMC capture input/compare output 4
				SPI_MISO	SPI module MISO (master input slave output) signal
				UART1_RX	UART1 RX
				LRC_OUT	38.4 KHz output of internal low-frequency RC clock
				X32K_OUT	External low-frequency crystal oscillator output
18	18	PD1/SWDCLK	I/O	SWDCLK	SWD clock
				PD1	PD1 general digital input/output pin
				PWMC_ECI	PWMC external clock input
				UART1_TX	UART1 TX
				HRC_OUT	24 MHz output of internal high-frequency RC clock
				CO	Analog comparator output
19	19	PD2/CI0/AIN3	I/O	PD2	PD2 general digital input/output pin
				TIM1_CH2	TIM1 PWM output 2
				PWMC_CH2	PWMC capture input/compare output 2
				SPI_MISO	SPI module MISO (master input slave output) signal
				RTC_1HZ	RTC 1Hz output
				LPUART_TX	LPUART TX
				LPTIM_TOG	LPTIM toggle output
				CI0	Analog comparator input channel 0
				AIN3	ADC analog input channel 3
20	20	PD3/AIN4	I/O	PD3	PD3 general digital input/output pin
				TIM1_CH3N	TIM1 PWM3 reverse output
				PWMC_CH1	PWMC capture input/compare output 1
				SPI_MOSI	SPI module MOSI (master output slave input) signal
				HXT_OUT	External-connected high-frequency crystal oscillator output
				UART0_RX	UART0 RX
				LPTIM_TOGN	LPTIM flip reverse output
				TIM2_CH2	TIM2 capture input/compare output 2
				AIN4	ADC analog input channel 4
0	-	NC			

Pin No.		Name of pin	Type	Alternate function	Description
QFN20	SSOP20				
1	1	PD4/CI2	I/O	PD4	PD4 general digital input/output pin
				TIM1_CH1	TIM1 PWM output 1
				PWMC_CH0	PWMC capture input/compare output 0
				RTC_1HZ	RTC 1Hz output
				TIM10_TOG	TIM10 toggle output
				UART0_TX	UART0 TX
				TIM10_EXT	TIM10 external pulse input
				TIM2_CH1	TIM2 capture input/compare output 1
				CI2	Analog comparator input channel 2
2	2	PD5/AIN5	I/O	PD5	PD5 general digital input/output pin
				TIM1_CH1N	TIM1 PWM1 reverse output
				PWMC_CH4	PWMC capture input/compare output 4
				SPI_MISO	SPI module MISO (master input slave output) signal
				I2C_SCL	I^2C clock
				UART1_TX	UART1_TX
				TIM10_GATE	TIM10 gate control
				UART0_TX	UART0 TX
				TIM2_CH4	TIM2 capture input/compare output 4
				AIN5	ADC analog input channel 5
3	3	PD6/AIN6	I/O	PD6	PD6 general digital input/output pin
				TIM1_CH2	TIM1 PWM output 2
				PWMC_CH3	PWMC capture input/compare output 3
				SPI_MOSI	SPI module MOSI (master output slave input) signal
				I2C_SDA	I^2C data
				UART1_RX	UART1 RX
				LPTIM_EXT	LPTIM external pulse input
				UART0_RX	UART0 RX
				TIM2_CH2	TIM2 capture input/compare output 2
				AIN6	ADC analog input channel 6

3. Function description

3.1. ARM® Cortex®-M0 core

ARM® Cortex®-M0 is a kind of ARM 32-bit RISC processor. ARM® Cortex®-M0 supports low power consumption and high-efficiency operations, and high-performance interrupt response. Compared with other 8-bit and 16-bit MCU, it has higher code density and can be used in wider embedded system. It has excellent performance and can be compatible with other Cortex-M processors.

3.2. Memory

CS32L010 supports the following features

- Flash is comprised of three parts:
  - 64K Bytes Flash program store
  - NVR, including option byte and system store
- 4K Bytes embedded SRAM

Table 3 Memory mapping

Bus	Module	Starting Address	Size (Bytes)
Memory	Flash memory	0x0000 0000	64K
	Option byte	0x0800 0000	512
	System store	0x1800 0000	256
	SRAM	0x2000 0000	4K
APB	UART0	0x4000 0000	1K
	UART1	0x4000 0400	1K
	SPI	0x4000 0800	1K
	I^2C	0x4000_0C00	1K
	TIM1	0x4000 1000	1K
	PWMC	0x4000 1400	1K
	TIM10/11	0x4000 1800	1K
	SYSCON	0x4000 1C00	1K
	WWDT	0x4000 2000	1K
	IWDT	0x4000 2400	1K
	AWK	0x4000 2800	1K
	ADC	0x4000 2C00	1K
	RTC	0x4000 3000	1K
	CLKTRIM	0x4000 4000	1K
	OWIER	0x4000 3C00	1K
	TIM2	0x4000 3C00	1K
	LVD/COMP	0x4000 4000	1K
	LPTIM	0x4000 4400	1K
	BEEP	0x4000 4800	1K
	DEBUG	0x4000 4C00	1K
	LPUART	0x4000 5000	1K
AHB	RCC	0x4002_0000	1K
	FMC	0x4002_0400	1K
	CRC16	0x4002 0800	1K
	GPIOA	0x4002 1000	1K
	GPIOB	0x4002 1400	1K
	GPIOC	0x4002 1800	1K
	GPIOD	0x4002 1C00	1K
Cortex-M0 internal peripherals		0xE000 0000	1M

3.3. Clock

Clock system includes the following clocks:

- 4-24MHz internal high-speed RC oscillator (HRC)
- 32.768KHz/38.4KHz internal high-speed RC oscillator (LRC)
- 4~24MHz crystal oscillator (HXT)
- 32.768KHz crystal oscillator (LXT)

3.4. Power management

3.4.1. Low-power mode

The chip has 2 low-power modes:

- Sleep Mode

In sleep mode, only CPU stops and all peripherals continue to run and CPU will be awakened in case of interrupt/ event.

- Deep Sleep mode

In the deep sleep mode, CPU stop running, the master clock of the system is disabled, and most modules stop running. The system is working in built-in 38.4 KHz/32.768 KHz low-speed clock. RTC interrupt, AWK interrupt or external interrupt can be used to wake up the chip. In normal operating mode, the frequency division mode can be used or some unnecessary module clocks can be disabled for flexible switching between power consumption and performance.

3.4.2. POR/ PDR

The chip has POR and PDR circuits. POR module will monitor VDD voltage while PDR module will monitor VDD and VDDA voltage.

The circuit is always in service and it can assure that the component can work normally when the voltage is no less than the minimum operating voltage. When the monitoring power supply voltage is lower than the specified threshold value VPOR/PDR, the component is in reset mode.

3.4.3. LVD (Low-voltage reset module)

LVD is used to monitor VDD power supply or chip pin voltage, and compare it with threshold value V_{LVD}. When VDD is lower than V_{LVD} or higher than V_{LVD} threshold value, interrupt will happen. LVD threshold value is under programmable control, and support 8-grade voltage monitoring values (2.5-4.4V).

3.5. General-purpose input/output port (I/O)

Every GPIO pin can be configured as input (with or without pull-up or pull-down), output (push-pull or open-drain) or alternate peripheral function port. A majority of GPIO pins are shared with digital or analog alternate peripherals.

3.5.1. IO port alternate function

Table 4 Description about PA port alternate function

Name of pin	Alternate function 0	Alternate function 1	Alternate function 2	Alternate function 3	Alternate function 4	Alternate function 5	Alternate function 6	Alternate function 7	Alternate function 8
PA1	PA1	TIM1_CH2N		SPI_CLK	I2C_SDA	UART0_RXD	TIM10_TOG	UART1_RXD	
PA2	PA2	TIM1_CH3		SPI_NSS	I2C_SCL	UART0_TXD	TIM10_TOGN	UART1_TXD	TIM2_CH2
PA3	PA3	TIM1_CH3N	PWMC_CH2	SPI_NSS	RTC_1HZ	LPUART_RXD	PWMC_ECI	CO	TIM2_CH3
PB4	PB4	LPTIM_GATE	PWMC_ECI	SPI_NSS	I2C_SCL	UART0_TXD	TIM11_TOGN		
PB5	PB5	TIM1_BKIN	PWMC_CH4	SPI_CLK	I2C_SDA	UART0_RXD	TIM11_TOG	LVD_OUT	TIM2_CH1
PC3	PC3	TIM1_CH3	TIM1_CH1N		I2C_SDA	UART1_TXD	PWMC_CH1	1-WIRE	TIM2_CH3
PC4	PC4	TIM1_CH4	TIM1_CH2N		I2C_SCL	UART1_RXD	PWMC_CH0	CLK_MCO	TIM2_CH4
PC5	PC5	TIM1_BKIN	PWMC_CH0	SPI_CLK		LPUART_TXD	TIM11_GATE	LVD_OUT	TIM2_CH1

Name of pin	Alternate function 0	Alternate function 1	Alternate function 2	Alternate function 3	Alternate function 4	Alternate function 5	Alternate function 6	Alternate function 7	Alternate function 8
PC6	PC6	TIM1_CH1	PWMC_CH3	SPI_MOSI		LPUART_RXD	TIM11_EXT	CLK_MCO	TIM2_CH4
PC7	PC7	TIM1_CH2	PWMC_CH4	SPI_MISO		UART1_RXD	LIRC_OUT	LXT_OUT	
PD1	PD1		PWMC_ECI			UART1_TXD	HIRC_OUT	CO	
PD2	PD2	TIM1_CH2	PWMC_CH2	SPI_MISO	RTC_1HZ	LPUART_TXD	LPTIM_TOG		
PD3	PD3	TIM1_CH3N	PWMC_CH1	SPI_MOSI	HXT_OUT	UART0_RXD	LPTIM_TOGN		TIM2_CH2
PD4	PD4	TIM1_CH1	PWMC_CH0	RTC_1HZ	TIM10_TOG	UART0_TXD	TIM10_EXT		TIM2_CH1
PD5	PD5	TIM1_CH1N	PWMC_CH4	SPI_MISO	I2C_SCL	UART1_TXD	TIM10_GATE	UART0_TXD	TIM2_CH4
PD6	PD6	TIM1_CH2	PWMC_CH3	SPI_MOSI	I2C_SDA	UART1_RXD	LPTIM_EXT	UART0_RXD	TIM2_CH2

3.6. Analog-to-digital convertor (ADC)

CS32L010 includes one 12-bit successive-approximation ADC (analog-to-digital converter). It supports 7 channels at most. Conversion modes for different channels include one-shot, scanning and cycle. In scanning mode, the selected analog input channel group will be converted automatically. It supports different conversion settings, include sampling time, converter resolution, data format alignment and channel scanning direction selection.

ADC conversion can be triggered by software/ hardware events generated by different timers, and ADC sampling can be triggered by external pins, and internal modules such as TIM1, TIM2, TIM10/TIM11 and COMP.

3.7. Analog comparator (COMP)

Chip pin voltage monitoring/comparison circuit. 3 configurable positive/negative external input channels; 1 internal BGR 2.5V reference voltage. COMP output can be used for timers TIM1, TIM10/TIM11, LPTimer and programmable counter array PWMC capture, gate control, and external counting. Asynchronous interrupt is generated based on rising/falling edge. Wake up MCU in low-power mode. The software anti-shake function is configurable.

3.8. Timer

The chip has one advanced timer, five general-purpose timers and one basic timer

Table 5 Comparison of characteristics between various timers

Type	Timer	Counter bit width	Direction	Pre-scale factor	Generate DMA requirement	Channel count	Number of complementary channels
Advanced control	TIM1	16 digit	Up, down, up/down	1/2/4/8/16/64/256/1024	-	4	3
General	TIM2	16 digit	Up, down, up/down	1/2/4/8/16/64/256/1024	-	4	0
Basic	TIM10	16/32-bit	Up	1/2/4/8/16/32/64/128	-	0	0
	TIM11	16/32-bit	Up	1/2/4/8/16/32/64/128	-	0	0
Low power	LPTIM	16 digit	Up	-	-	0	0
PWM	PWMC	16 digit	Up	2/4/8/16/32	-	5	0
Others	AWT	8 digits	Up	1/2 to 1/65536	-	0	0

3.8.1. Advanced timer (TIM1)

TIM1 is a 16-bit counter with 16-bit prescale and enables up, down, and up/ down counting. It has 4 channels and all those channels support input capture and output compare. Outgoing PWM signal can be used for motor control or power consumption management. Complementary output of each channel will share the same embedded dead-time configuration.

TIM1 can be internally connected to other timers by means of synchronization or event triggering.

In debug mode, counter can be stopped.

3.8.2. General-purpose timer (TIM2)

TIM2 is a 16-bit counter with 16-bit prescale and enables up, down, and up/ down counting. They have four channels and all those channels support independent input capture, output compare and PWM.

TIM2 can be internally connected to other timers by means of synchronization or event triggering.

In debug mode, counter can be stopped.

3.8.3. Basic timer (TIM10/11)

There are two basic timers including 16/32-bit optional timers TIM10/TIM11, which have identical functions and can be used as the timing reference for the system. It supports the reload mode and the non-reload mode

3.8.4. Low-power timer (LPTIM)

The timing/counting is also available through internal low-speed LRC or external low-speed crystal oscillator after the system clock is turned off. Wake up the system in low-power mode by interrupt.

3.8.5. FWDT (independent watchdog timer)

FWDT uses the internal LRC as the clock source and is independent of the master clock. FWDT is comprised of a 20bit down counter, and it enables standalone operation in the deep sleep mode and the power down mode. When the counter reaches 0, FWDT will generate a reset.

In debug mode, counter can be stopped.

3.8.6. WWDT (window watchdog timer)

WWDT uses PCLK as the master clock and is comprised of one prescaler and 8-bit free-running down-counter. It can be seen as a watchdog to reset devices when a system problem occurs. It has an early-warning interrupt capability.

In debug mode, counter can be stopped.

3.8.7. SysTick (tick timer)

SysTick can be used for RTOS (real-time operating system) and meanwhile a standard down counter.

It uses HCLK or HCLK/8 as the clock source and has 24-bit down counter with automatic reloading function. When the counter reaches 0, SysTick will generate a maskable system interrupt.

3.8.8. Automatic wake-up timer (AWT)

AWT provides an internal wake-up time reference when MCU enters the low-power mode. The time reference clock is provided by internal low-speed RC oscillator clock (LRC) or prescale HXT crystal oscillator clock.

3.8.9. PWM controller (PWMC)

PWM controller (PWMC) supports up to five 16-bit capture/compare modules, and it can be used for the capture/compare function of a general clock counter/event counter. Each channel can be independently programmed to provide input capture/output compare, or pulse width modulation.

3.9. Interrupt and event

Cortex-M0 integrated NVIC (nested vectored interrupt controller) can handle with exceptions and interrupts efficiently. For more details, please refer to Cortex-M0 Technical Reference Manual.

EXTI is consisted of 32 independent edge detectors, which will generate interrupt request & event and give them to CPU or interrupt controller. For EXTI, there are three trigger modes, i. e. rising edge, falling edge and dual-edge trigger. Every edge detector can be configured and enabled independently.

3.10. Real time clock (RTC)

RTC has the following features:

— Support RTC counting (second/minute/hour) and calendar function (dd/mm/yy)
— Support alarm register (second/minute/hour/dd/mm/yy)
— Support wake up sleep mode

3.11. Serial peripheral interface (SPI)

SPI module can communicate with external devices by SPI protocol.

SPI supports transmission and receiving of master/ slave. It supports full-duplex and simple modes, with the max traffic rate up to 12 Mbit/s. This module also achieves hardware CRC function.

3.12. Universal asynchronous receiver/transmitter (UART1/UART2/LPUART)

USART provides a general-purpose interface for continuous communication of MCU and external devices. UART supports asynchronous full-duplex and single-wire half-duplex communication. One programmable baud rate generator or TIM10/11 can provide different communication baud rates.

Low-power universal synchronous/asynchronous transceiver (LPUART) support low-power applications, and different communication baud rates are provided by programmable baud rate generator or LPTIM.

Besides, UART/LPUART also supports multi-processor communication; support automatic address recognition; support given address and broadcast address.

Table 6 UARTx Functions

USART characteristics/ mode	UART1	UART2	LPUART
Asynchronous full-duplex communication	√	√	√
Single-wire half-duplex	√	√	√
Multi-processor communication	√	√	√
IrDA mode	√	√	
Clock frequency division	Baud rate generator TIM10	Baud rate generator TIM11	Baud rate generator LPTIM
Low-power mode			√

3.13. Built-in integrated circuit interface（I²C）

I²C module provides an industrial-grade standard I²C interface and can run in master and slave modes. The interface realizes standard, fast and ultrafast modes.

It mainly includes the following characteristics:

— Support master/ slave modes
— Support broadcast address
— Configurable filter
— Support 7-bit address mode
— Support standard mode (up to 100 KHz), fast speed (up to 400 KHz)

Table 7 Table 7 I²Cx functions

I²C characteristics/ mode	I²C
7-bit address mode	√
10-bit address mode	×
Standard mode	√
Fast mode	√
Ultrafast mode	√

3.14. Cyclic Redundancy Check

In the fields of data storage and communication, CRC (cyclic redundancy check) is widely used to assure the data correctness.

CRC calculation unit can figure out 16-bit CRC code according to the fixed CRC polynomial.

3.15. Serial debug port (SWD-DP)

ARM Cortex-M0 internal integration debug component; SWD debug port is used to connect those debug components.

Warning: After the SWD interface is disabled, the MCU will not be able to program, update or erase the Flash through the SWD interface. If the SWD interface needs to be disabled and the program needs to be updated later, the program needs to support the IAP function.

4. Electrical characteristics

4.1. Description

Figure 4 shows the typical application circuit of CS32L010.
Unless otherwise specified, all typical values are based on T_{range}=25℃ and VDD = 3.3V.
Unless otherwise specified, all voltages use VSS as reference.
Unless otherwise specified, all data are for design reference only.
Test conditions such as pin input voltage and load etc. are shown in Figure 5.

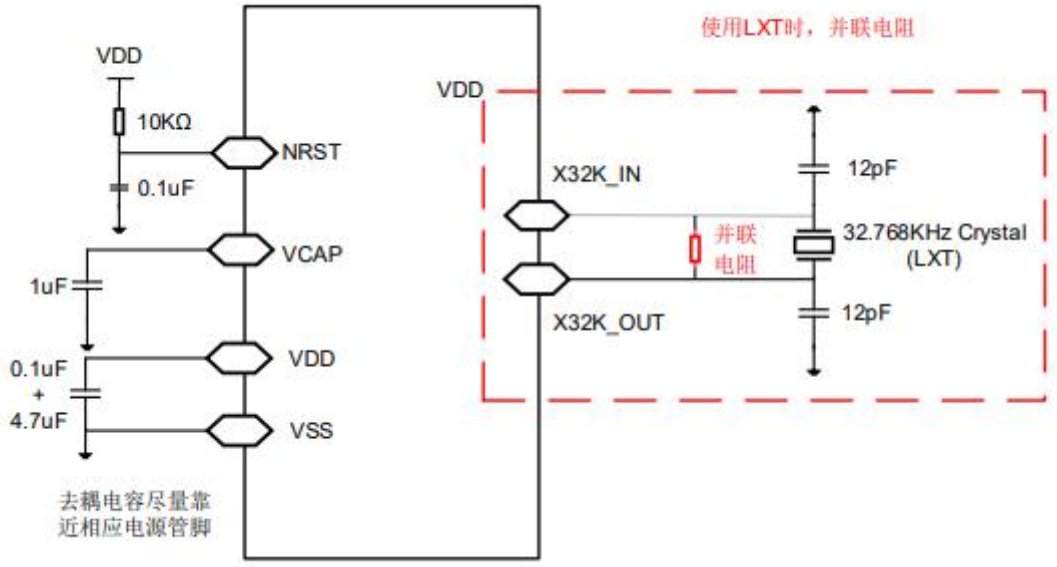
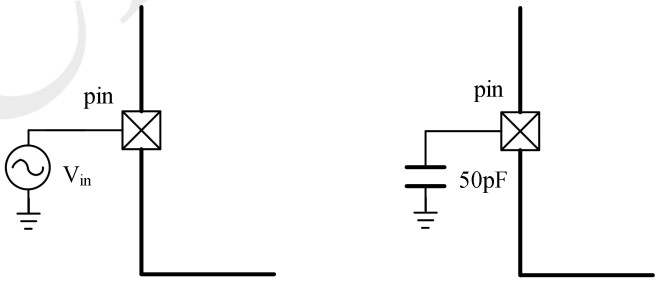


Figure 4 Typical application circuit

Notice:

① It is recommended to use the filter ceramic decoupling capacitors as above for VDD and VSS; and these capacitors must be as close as possible to the pins to ensure that the capacitors have the desired effect.

② The above filter ceramic decoupling capacitors must be used between VCAP and VSS, otherwise the system will not work properly; and these capacitors must be as close as possible to the pins to ensure that the capacitors have the desired effect.



(a) Input voltage (b) Loading

Figure 5 Pin input voltage and load conditions

4.2. Absolute maximum rating

Table 8 Absolute maximum rating

Symbol	Description	Minimum	Typical value	Maximum	Unit
VDD	Voltage between VDD and VSS	-0.3	-	5.5	V
$V_{i/o}$	I/O pin voltage	VSS-0.3	-	VDD+0.3	V
$T_{storage}$	Storage temperature	-40	-	150	℃
$T_{junction}$	Junction temperature	-40	-	150	℃

4.3. Operating conditions

Table 9 Operating conditions

Symbol	Description	Minimum	Typical value	Maximum	Unit
$V_{VDD-range}$	VDD operating voltage range	2.5	-	5.5	V
T_{range}	Chip environment temperature	-40	-	85	℃
C_s	VCAP capacitance	0.47	1.0	2.2	μF
$T_{VDD-POR}$	VDD POR threshold value	2.2	2.25	2.3	V
$T_{VDD-fall}$	VDD PDR threshold value	2.2	2.25	2.3	V
$T_{reset-tempo}$	Reset duration when $V_{VDD-range}$≤ 5.5V	-	4.2	10	mS
	Reset duration when $V_{VDD-range}$≤ 3.6V	-	4.2	7.5	mS
V_{LVD}	LVD rise threshold voltage 0	2.36	2.46	2.54	V
	LVD rise threshold voltage 1	2.52	2.63	2.72	V
	LVD rise threshold voltage 2	2.70	2.82	2.92	V
	LVD rise threshold voltage 3	2.90	3.04	3.16	V
	LVD rise threshold voltage 4	3.14	3.29	3.40	V
	LVD rise threshold voltage 5	3.44	3.59	3.72	V
	LVD rise threshold voltage 6	3.78	3.95	4.08	V
	LVD rise threshold voltage 7	4.20	4.39	4.54	V

4.4. I/O port characteristics

Table 10 I/O port characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
V_{IH}	Input high level (VDD=2.5)	1.4	-	-	V
	Input high level (VDD=3.3)	1.8			V
	Input high level (VDD=5.5)	3			V
V_{IL}	Input low level (VDD=2.5)	-	-	0.9	V
	Input low level (VDD=3.3)			1.3	V
	Input low level (VDD=5.5)			2.4	V
V_{OH}	Output high level, $\|I_{source-pin}\|$=6mA	VDD-0.3	-	-	V
V_{OL}	Output low level $\|I_{sink-pin}\|$=6mA (except for PD3 port)	-	-	VSS+0.3	V
V_{OL}	PD3 port output low level $\|I_{sink-pin}\|$=3.6mA	-	-	VSS+0.3	V
$R_{pull-up}$	I/O pull-up resistor		50		kΩ

4.5. Wake-up time from low power mode

Table 11 Wake-up time from low power mode

Symbol	Description	Minimum	Typical value	Maximum	Unit
$T_{wk-deepsleep}$	Wake-up time from deep sleep mode	-			
	4MHz		11.5		μs
	24MHz		4.2		μs

4.6. RC oscillation characteristics

Table 12 HRC characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
f_{HRC}	HRC frequency		4.0 24		MHz
$TRIM_{HRC}$	HRC adjusting accuracy	-	-	1	%
$Duty_{HRC}$	HRC duty cycle	45	-	55	%
$f_{accuracy-HRC}$	Frequency deviation of HRC under relatively typical conditions VDD = 2.5V ~ 5.5V, Ta = -40°C ~ 85°C	-2.5	-	2.5	%
T_{setup_HRC}	HRC set-up time, f_{HRC}=4MHz	4.04	4.71	5.60	µS
	HRC set-up time, f_{HRC}=24MHz	1.64	1.78	1.99	µS
I_{pd-HRC}	HRC module power consumption, f_{HRC}=4MHz	30 100	60 200	120 400	µA

Table 13 LRC characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
f_{LRC}	LRC frequency	37.83 32.28	38.4 32.768	38.97 33.26	KHz
T_{setup_LRC}	LRC set-up time	-	-	80	µS
I_{pd-LRC}	LRC module power consumption	-	0.25	0.35	µA

4.7. Crystal oscillator characteristics

Figure 6 indicates the external conditions of crystal oscillator such as crystals, load and parasitic capacitance.

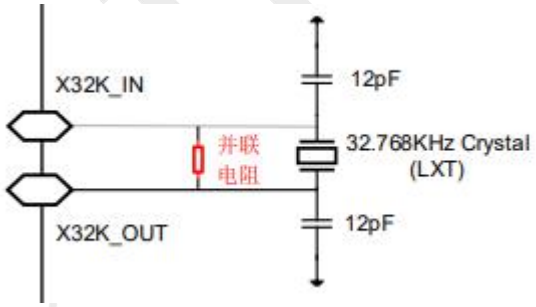


Figure 6 crystal oscillator such as crystals, load and parasitic capacitance.

CL (CL_{LXT} or CL_{HXT}) is load capacitance of crystal oscillator, including the on-board capacitance and the parasitic capacitance of the PCB board and package. Specific crystal needs to be connected with load capacitance within a specified range.

Table 14 LXT characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
I_{pd-LXT}	LXT module power consumption		250	350	nA
CL_{LXT}	LXT load capacitance		12		pF
ESR_{LXT}	Parallel resistor for LXT	40	65	85	kΩ
T_{setup}	LXT set-up time	-	2	-	S

Table 15 HXT characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
f_{HXT-IN}	HXT frequency	4	16	24	MHz
I_{pd-HXT}	VDD=3.3V, Rm=30Ω, CL=12pF@16MHz	-	300	-	µA

Symbol	Description	Minimum	Typical value	Maximum	Unit
CL_{HXT}	HXT load capacitance	-	12	-	pF
ESR_{HXT}	Parallel resistor for LXT	30	60	1500	Ω
T_{setup}	HXT set-up time	-	234.5	-	μS

4.8. Power consumption

Table 16 Power consumption characteristics in operation and sleep modes

Operating mode	Code execution position	Condition	f_{HCLK} (Hz)	IVDD (Peripheral open) (μA)		IVDD (Peripheral close) (μA)	
				Typ(1)	Max(2)	Typ(1)	Max(2)
Normal mode	RAM	HRC	4M			157.20	171.00
Normal mode	RAM	HRC	24M			605.00	626.00
Normal mode	Flash	HRC	4M	491.40	520.00	432.80	460.00
Normal mode	Flash	HRC	24M	2566.60	2691.00	2217.80	2334.00
Normal mode	Flash	LXT	32.768K	28.00	30.00	27.20	30.00
Sleep Mode	-	HRC	4M	148.60	162.00	90.40	102.00
Sleep Mode	-	HRC	24M	588.00	616.00	239.20	255.00
Sleep Mode	-	LXT	32.768K	26.00	28.00	25.60	28.00

Table 17 Power consumption characteristics in deep sleep and standby modes

Operating mode	Condition	f_{HCLK} (Hz)	IVDD (Peripheral open) (μA)		IVDD (Peripheral close) (μA)	
			Typ	Max	Typ	Max
Deep sleep mode	All Peripherals clock OFF, except RTC	32768			1.03	
Deep sleep mode	All Peripherals clock OFF, except IWDG	32768			1.02	
Deep sleep mode	All Peripherals clock OFF, except LPTIM	32768			1.03	
Deep sleep mode	All Peripherals clock OFF, except AWK	32768			0.99	
Deep sleep mode	All Peripherals clock OFF	32768			1.02	

4.9. ADC characteristics

Table 18 ADC characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
$I_{VDDA-ADC}$	ADC power consumption (VDDA), Autoff=0, VDDA=3.3V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	0.5	4	16	MHz
$T_{convert-time}$	Conversion duration of ADC	16	16	20	1/ f_{ADC}
$T_{swtich-on}$	ADC switch on-time	-	-	4	uS
$V_{range-input}$	ADC input voltage range	0	-	VDD	V
$C_{input-ADC}$	ADC input capacitance	-	-	4.5	pF
Resolution	ADC resolution	-	-	12	Bit
INL	ADC integral nonlinearity	-	±1	±3	LSB
DNL	ADC differential nonlinearity	-	±1	±2	LSB
ERR_{Gain}	ADC gain error	-	±1	±2	LSB
ERR_{Offset}	ADC Offset error	-	±1	±2	LSB
ENOB		9.5	10	10.4	Bit

4.10. Characteristics of comparator

Table 19 ADC characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
I_{comp}	COMP operating current	-	12	-	μA
$T_{response}$	COMP response time	-	5	-	μS
$V_{range-input}$	COMP input voltage range	0	-	VDD	V
$V_{range-com-input}$	COMP common-mode input voltage range	0	-	VDD	V
V_{Offset}	COMP Offset error	-	±5	±10	mV

4.11. Characteristics of Flash

Table 20 Flash characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
T_{prog}	32-bit programming time	30	45	60	μS
T_{erase}	Page erase time	3.5	3.7	4.5	mS
$T_{mass-erase}$	Mass erase time	29.1	30.3	31.6	mS
$Cyc_{endurance}$	Write/ erase cycles	20,000	-	-	Cycles
$T_{retention}$	Data retention	20	-	-	Year

4.12. Timer characteristics

Table 21 TIMx characteristics

Symbol	Description	Minimum	Typical value	Maximum	Unit
$T_{resolution}$	Temporal Resolution	-	$T_{TIMx\ CLK}$	-	nS
$f_{ext-clk}$	CHx external clock frequency	-	$T_{TIMx\ CLK}/4$	-	MHz
$T_{max-count}$	Max time of 16-bit timer	-	$2^{16} * T_{TIMx\ CLK}$	-	nS

Table 22 FWDT characteristics

Prescale	PDIV[2:0]	Min overflow value UVAL[11:0]=0x000	Max overflow value UVAL[11:0]=0x000	Unit
/4	0	4 * T_{LRC}	16384 * T_{LRC}	mS
/8	1	8 * T_{LRC}	32768 * T_{LRC}	mS
/16	2	16 * T_{LRC}	65536 * T_{LRC}	mS
/32	3	32 * T_{LRC}	131072 * T_{LRC}	mS
/64	4	64 * T_{LRC}	262144 * T_{LRC}	mS
/128	5	128 * T_{LRC}	524288 * T_{LRC}	mS
/256	6 or 7	256 * T_{LRC}	1048576 * T_{LRC}	mS

Table 23 WWDT characteristics

Prescale	PDIV[1:0]	Min overflow value	Max overflow value	Unit
/1	0	4096 * T_{PLCK}	262144 * T_{PLCK}	mS
/2	1	8192 * T_{PLCK}	524288 * T_{PLCK}	mS
/4	2	16384 * T_{PLCK}	1048576 * T_{PLCK}	mS
/8	3	32768 * T_{PLCK}	2097152 * T_{PLCK}	mS

4.13. ESD property

Table 24 ESD characteristics

Symbol	Description	Level	Value	Unit
$V_{ESD-HBM}$	ESD discharge human body model, based on MIL-STD-883E, Temperature = 23 ± 5℃ Relative humidity: 55% ± 10% (RH)	3A	≥4000	V
V_{ESD-MM}	ESD discharge machine model, Based on JEDEC EIA/JESD22-A115, Temperature = 23 ± 5℃ Relative humidity: 55% ± 10% (RH)	C	≥400	V
$V_{ESD-CDM}$	EDS discharge device model, Based on JEDEC EIA/JESD22-C101F, Temperature = 23 ± 5℃ Relative humidity: 55% ± 10% (RH)	C2	≥500	V
$I_{latchup}$	ESD discharge machine model, Based on JEDEC STANDARD NO.78C SEPTMBER 2010, Temperature =105±5℃ Relative humidity: 55% ± 10% (RH)	II	≥200	mA

5. Encapsulation information

5.1. QFN20 (3mm*3mm)

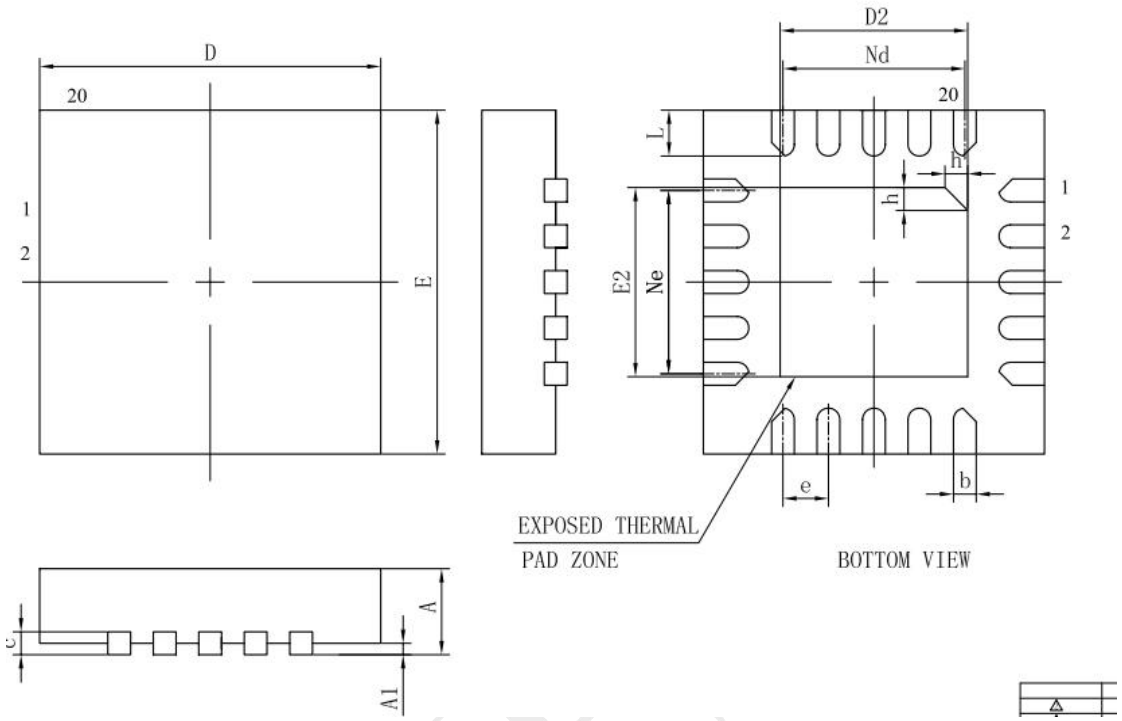
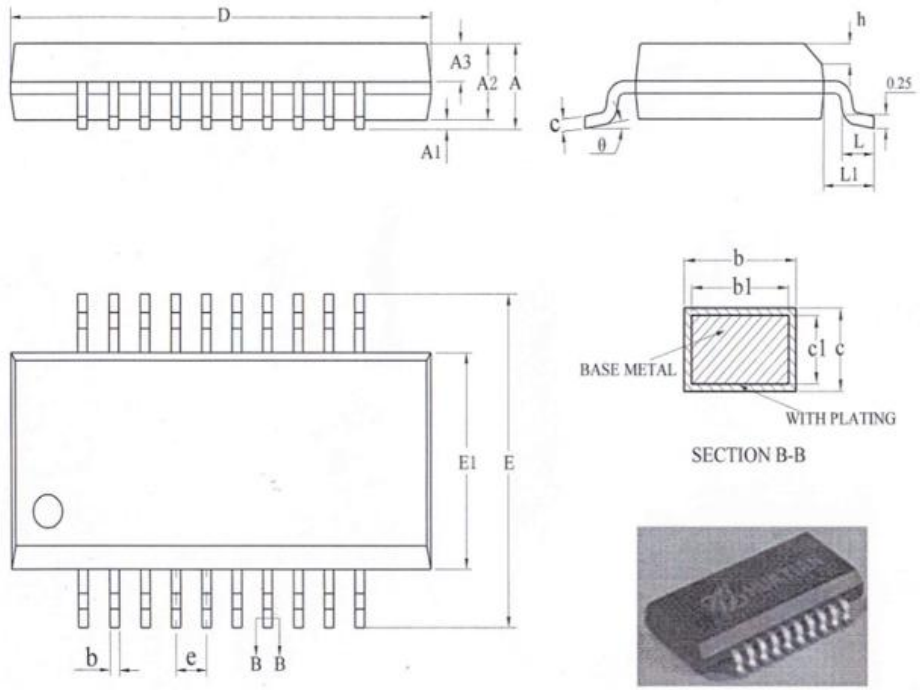


Figure 7 Block diagram of QFN20 package

Table 25 Dimensions of QFN20 package

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (Mil)	75*75		

5.2. SSOP20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 8 Block diagram and dimensions of QFN20 package

5.3. Thermal characteristics

The maximum chip junction temperature, Tjunction, must not exceed the junction temperature given in Section 4.2 Absolute Maximum Rating.

The maximum junction temperature Tjunction of the chip can be calculated by the following formula

$$T_{junction} = T_{A\ max} + (P_{D\ max} \times \Theta_{JA})$$

In the formula

- $T_{A\ max}$ is the maximum ambient temperature, unit is ℃
- Θ_{JA} is the thermal resistance from the package junction to ambient, unit is ℃/W
- $P_{D\ max}$ is the sum of $P_{INT\ max}$ and $P_{I/O\ max}$（$P_{D\ max} = P_{INT\ max} + P_{I/O\ max}$）
- $P_{INT\ max}$ is the product of I_{VDD} and V_{VDD}, unit is W. It is the maximum internal power consumption of this chip.
- $P_{I/O\ max}$ is the maximum power consumption of the output pin,
  $P_{I/O\ max} = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{VDD} - V_{OH}) \times I_{OH})$

The exact values of V_{OL}/I_{OL} and V_{OH}/I_O when IO is at low or high level in the application need to be considered.

Symbol	Parameters	Value	Unit
Θ_{JA}	Junction to ambient thermal resistance QFN20 (to ePad)	57.9312	℃/W
	Junction to ambient thermal resistance QFN20 (to air)	87.05	
	Junction to ambient thermal resistance SSOP20	TBD	

6. Naming conventions of products

6.1. Description of product model

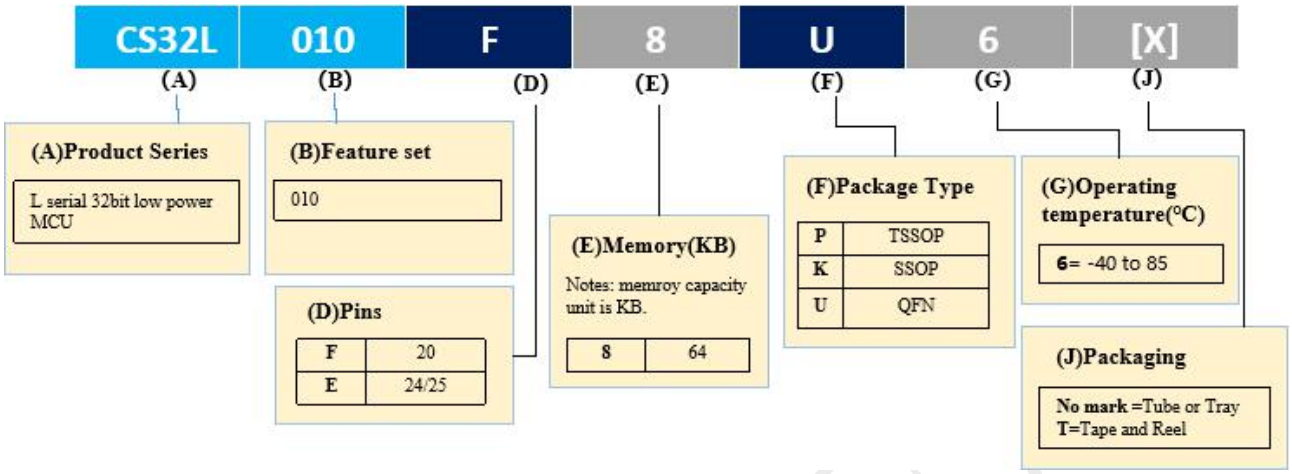


Figure 9 Naming conventions of CS32L010 products

6.2. Product silk-screen marks instructions

Silk screen marking instructions:	
1	Front page Pin 1 mark;
2	Front page 1st line (CHIPSEA);
3	Front page 2nd line (product model), see Table 26 Order information for details;
4	Front page 3rd line (YYWWXXX) shows the main batch number: The two bits on the left YY indicate the last two digits of the solar calendar year; The two bits in the middle WW indicate the number of calendar weeks of the year, and "0" shall be used as place holder in case of an one-digit number; The two bits on the right XXX is a variable number specified in the order;
5	Font: “Arial”;
6	Print mode: laser front printing

7. Order Information

Table 26 Order information

Product model	Pin	Storage space	Package type	Packaging	Packaging Quantity	Ambient operating environment(^{0}C)	MSL	Silk screen
CS32L010F8K6	20	64KB	SSOP20	Tube	5000	-40 ~85	3	L010F8K6
CS32L010F8U6	20	64KB	QFN20 (3*3*0.75-e=0.40)	Tray	4900	-40~85	3	L010F8

8. Reflow curve for reference, peak temperature

Table 27 Lead-free process Package classification Reflow temperature

Package thickness	Volume mm3 <350	Volume mm3 350-2000	Volume mm3 >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *
*Tolerances: Equipment manufacturers/suppliers should ensure process compatibility up to and including the stated rating temperature (this means peak Reflow temperature +0°C. For example, 260°C+0°C) at the rated MSL level.			

Table 28 Hierarchical Reflow Curve

Features of curve	Lead-free components
Average ramp rate（Ts_{max} to Tp）	3° C/second max
Preheating – Lowest temperature（Ts_{min}） – Highest temperature（Ts_{max}） – Time（ts_{min} to ts_{max}）	 150 °C 200 °C 60-180 seconds
Lasting time: – Temperature（T_L） – Time（t_L）	 217 °C 60-150 seconds
Peak/Hierarchical temperature（Tp）	Please refer to**Table 27 for details**
Time within 5°C of actual peak temperature (tp)	20-40 seconds
Ramp-down rate	6 °C/second max
Time from 25°C to peak temperature	8 minutes max

Note: All temperatures refer to the top temperature of the package, measured on the surface of the package.

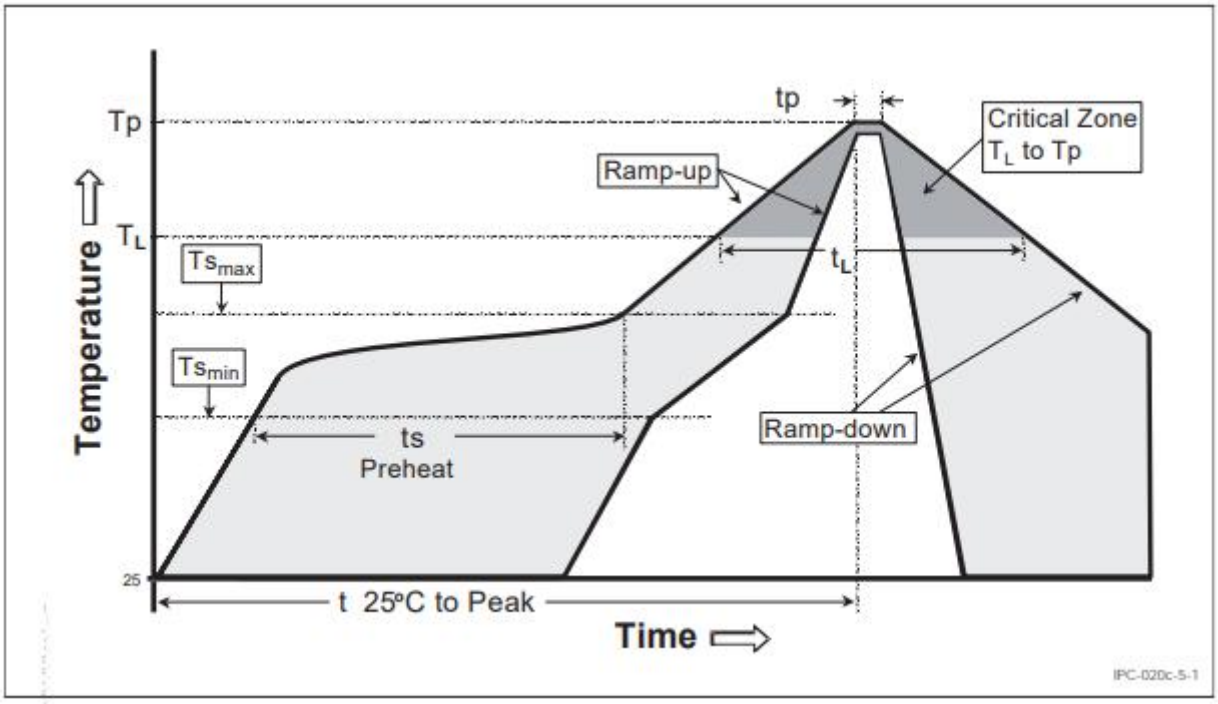


Figure 10 Reflow curve

9. Package information

Package type and quantity:

Product model	Package size	Package type	Quantity/Package
CS32L010F8K6	SSOP20 e=0.635mm, D1.4	Tube	50EA/tube, 100 tubes（5000EA）/box, 10 boxes/carton（5000EA）
CS32L010F8U6	QFN20 3mm*3mm*0.75mm-e=0.40mm	Tray	490EA/tray, 10 trays（4900EA）+1（empty tray）/box, 6 boxes/carton（29400EA）

Packaging specifications list:

Inner packaging material	Tray, cable ties, desiccant, humidity indicator card, aluminum foil bag, bubble bag, inner box label, inner box (with our logo).
External packaging material	Carton (with our logo), tape, outer carton label.
Requirements for carton	Outer carton (with our logo): double-layer corrugated cardboard (thickness ≤6mm), bursting strength ≥14kg/cm2, the gap between the inner box and the carton ≥1cm must be filled with bubble pads or sponge pads.
Partial carton	Only one partial carton is allowed per batch for the same order.

Inner box	Cable ties	Desiccant	Humidity indicator card	Aluminum foil bag	Bubble bag	Carton	Cable ties
370*150*88 mm	>6mm	Abouve 10g	6 dots	495*240 mm	440*240mm	385*320*275mm or 395*320*285mm	>6mm

Label description:

Label type

Outer carton label（100*70mm）

Inner box label（100*50mm）

Name	Description
P/N	Label model
M/C	Product model
Lot	Lot number of products
Q'ty	Quantity of products, unit is PCS
Carton ID	Serial number on outer carton defined by the test factory The test factory defines the inner traceability identifier: BIN file: (x) means untested, (0) means defective product, (1) means good product BIN1, (2) means good product BIN2, greater than 1 means inferior product. SN code, i.e. the test factory assembly lot number, LY04+ (BIN file) + date (6 digits) + packaging method (2 digits) + serial number (4 digits) Packing: F0 TRAY vacuum bag, F1 TRAY inner box, G0 TRAY outer carton

Box ID	Serial number on inner box defined by the test factory The test factory defines the inner traceability identifier: BIN file: (x) means untested, (0) means defective product, (1) means good product BIN1, (2) means good product BIN2, greater than 1 means inferior product. SN code, i.e. the test factory assembly lot number, LY04+ (BIN file) + date (6 digits) + packaging method (2 digits) + serial number (4 digits) Packing: F0 TRAY vacuum bag, F1 TRAY inner box, G0 TRAY outer carton
MMCU	PO NO
MFG Lot	Sub-process card number
D/C	YYWW
DATE	YYYY-MM-DD（packing date）
QR Code	It is comprised of “P/N”, “M/C”, “Lot&MFG Lot”, “Qty”, “PO NO”, “D/C”, “DATE”, “Carton ID(outer carton label)” or “Box ID(inner box label)”, using “)” to separate each item. No Qty unit will be printed and “Date” shall be a blank space.
Font	SimSun, 10 pt, bold

10. HSF Statement

10.1. RoHS

It complies with *The Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment* developed by the EU (EU RoHS2.0) (2011/65/EU & Amendment(EU) 2015/863).

10.2. REACH

REACH SVHC 223 and Annex XVII comply with REACH-EU Regulation "Regulation(EC) No. 1907/2006 of the European Parliament and of the Council of 18 December 2006 concerning the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH)".

10.3. Material composition

10.3.1. Material composition of CS32L010F8U6

Figure 11 Material composition of CS32L010F8U6

Material	Supplier	Type	Weight(mg)	Composition	CAS No.	% of weight	Composition Weight(mg)
Die	/	/	0.979	Silicon	7440-21-3	100.00%	0.979
Lead frame	AAMI	A194FH	6.435	Cu	7440-50-8	92.240%	5.936
				Fe	7439-89-6	2.400%	0.154
				Pb	7439-92-1	0.010%	0.001
				p	7723-14-0	0.150%	0.010
				Zn	7440-66-6	0.200%	0.013
				Ag	7440-22-4	5.000%	0.322
Epoxy	YONGOO	S502	0.958	Arcylate resin	Proprietary	20.00%	0.192
				Curing agent & hardener	Proprietary	5.00%	0.048
				Silver	7440-22-4	75.00%	0.719
Wire	Nippon	EX1p	0.966	Cu	7440-50-8	96.55%	0.933
				Pd	7440-05-3	3.10%	0.030
				Au	7440-57-5	0.35%	0.003
Mold Compound	SDMSZ	CEL-9240HF	10.300	Epoxy Resin 1	Trade Secret	4.100%	0.422
				Epoxy Resin 2	Trade Secret	3.000%	0.309
				Hardener	Trade Secret	4.000%	0.412
				Organic Phosphorus compounds(additives)	Trade Secret	0.110%	0.011
				Carbon Black	1333-86-4	0.290%	0.030
				Amorphous silica 1	60676-86-0	81.000%	8.343
				Amorphous silica 2	7631-86-9	7.500%	0.773
Plating	JIANGSUAISEN	Tin	0.962	Tin	7440-31-5	99.9918%	0.962
				Lead	7439-92-1	0.0035%	0.000
				Arsenic	7440-38-2	0.0005%	0.000
				Iron	7439-89-6	0.0008%	0.000
				Copper	7440-50-8	0.0003%	0.000
				Bismuth	7440-69-9	0.0017%	0.000
				Antimony	7440-36-0	0.0009%	0.000
				zinc	7440-66-6	0.0001%	0.000
				Aluminum	7429-90-5	0.0001%	0.000
				Cadmium	7440-43-9	0.0003%	0.000

10.3.2. Material composition of CS32L010F8K6

Figure 12 Material composition of CS32L010F8K6

Material	Supplier	Type	Weight(mg)	Composition	CAS No.	% of weight	Composition Weight(mg)
Die	/	/	3.00	Silicon	7440-21-3	100.000%	3.0000
Lead Frame	HTBJ	A194	12.50	Copper	7440-50-8	96.630%	12.0788
				Iron	7439-89-6	2.200%	0.2750
				Phosphorus	7723-14-0	0.065%	0.0081
				Zinc	7440-66-6	0.100%	0.0125
				Lead	7439-92-1	0.005%	0.0006
				Silver	7440-22-4	1.000%	0.1250
Epoxy	Yongoo	S502D1	1.00	Acrylate	proprietary	22.000%	0.2200
				Curing agent & hardener	proprietary	7.000%	0.0700
				Silver powder	7440-22-4	71.000%	0.7100
Wire	Matfron	Au PdCu	3.50	Copper	7440-50-8	98.80%	3.4580
				Palladium	7440-05-3	1.000%	0.0350
				Gold	7440-57-5	0.200%	0.0070
Mold Compound	Sumitomo	EME-G630AY	81.00	Epoxy Resin A	Trade secret	2.500%	2.0250
				Epoxy Resin B	29690-82-2	2.500%	2.0250
				Phenol Resin	Trade secret	2.500%	2.0250
				Silica(Amorphous)A	60676-86-0	89.500%	72.4950
				Silica(Amorphous)B	7631-86-9	2.500%	2.0250
				Carbon black	1333-86-4	0.500%	0.4050
Plating	Aisen	Tin	1.00	Sn	7440-31-5	99.990%	0.9999
				Others	/	0.010%	0.0001

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