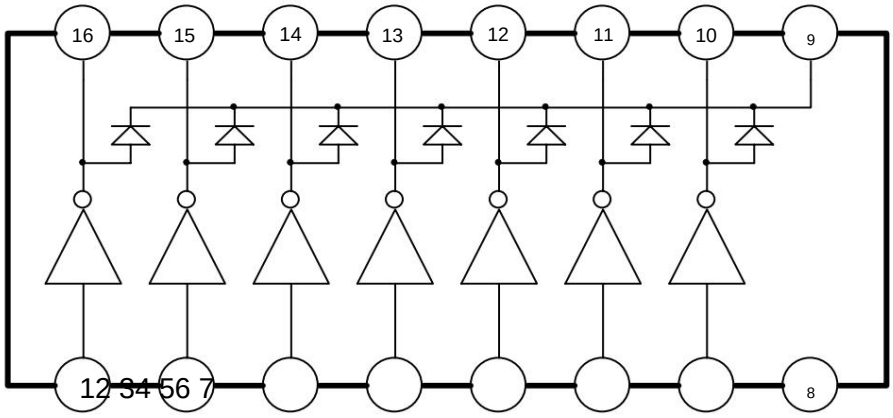
1. Overview

CS2003CP is a high voltage, high current Darlington transistor array driver circuit, which contains seven groups of NPN Darlington transistors. The emitters of each group of Darlington tubes are connected together, and the collectors are open circuit output. Mainly used to drive relays, electric bell hammers, Lighting equipment and LED display systems. Its features are as follows:

- The maximum current sink of a single channel can reach 500mA
- Continuous output high voltage can reach minimum 50V
- Under 5V working condition, the output terminal can be directly connected to TTL and CMOS
- Integrated clamping diode at output
- Package type: DIP16 / SOP16

2. Functional block diagram and pin description

2.1 Functional block diagram



2. 2. Pin Description

Pin Symbols		Function pin symbol		Function
1	IN1	Input 1	9 WITH	Common
2	IN2	Input 2	10 OUT7	output 7
3	IN3	Input 3	11 OUT6	Output 6
4	IN4	Input 4	12 OUT5	Output 5
5	IN5	Input 5	13 OUT4	Output 4
6	IN6	Input 6	14 OUT3	Output 3
7	IN7	Input 7	15 OUT2	Output 2
8	GND	Ground	16 OUT1	Output 1

3. Electrical characteristics

3.1 ÿ Limit parameters

Unless otherwise specified, Tamb = 25°C

Parameter Symbol Continuous output			scope	unit
voltage VCE (SUS) Output current			-0.5ÿ50	V
		IOUT	500	mA/ch
Input voltage VIN Clamp diode reverse			-0.5ÿ30	V
voltage VR Clamp diode forward current IF			50	V
			500	mA
Power loss	DIP16	PD	1.47	IN
	SOP16		0.54/0.625 (Note)	
Operating temperature range		Topr	-40ÿ85	ÿ
Storage temperature		Tstg	-55ÿ150	ÿ

Note: Mounted on 30mm x 30mm x 1.6mm 50% copper epoxy board.

3.2 Recommended conditions of use

Tamb=-40ÿ85ÿ

Parameter name symbol		Conditions of Use		Specifications			unit
				Min.	Typ.	Max.	
Output holding voltage VCE (SUS)				0		50	V
Output current IOUT		Tpw=25ms 7 channels Tamb=85ÿ Tj=120ÿ	The duty cycle is 10ÿ	0		ÿ 370	mA
			The duty cycle is 50ÿ	0		ÿ 130	
Input voltage VIN Input				0		24	V
voltage (Output on)	VIN (ON)	IOUT =400mA hFE =800		2.8		24	V
Input voltage (output off)	WIN (OFF)			0		0.7 V	
Clamp diode reverse	VR					50	V
voltage Clamp diode	IF	Tamb=85ÿ				ÿ 350 mA	
forward current Power loss PD		Tamb=85ÿÿNoteÿ				ÿ 0.76 W	

Note: Mounted on 30mm x 30mm x 1.6mm 50% copper epoxy board.

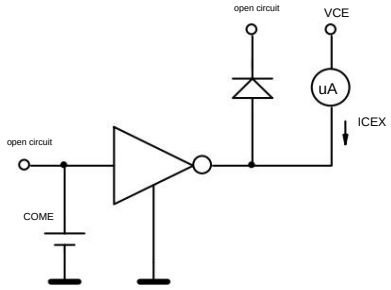
3.3 Electrical characteristics

Unless otherwise specified, Tamb = 25°C

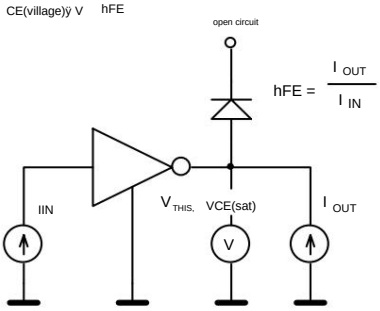
Parameter name symbol		Test conditions	Specifications			unit	picture Number
			Min.	Typ.	Max.		
Output sink current ICEX		VCE=50VÿTaMB=25ÿ -		·	50	ÿA 1	
		VCE=50VÿTaMB=85ÿ -		·	100		
Collector, Emitter Saturation voltage drop	VCE (sat)	IOUT=350mA IIN=500ÿA	·	1.3	1.6	In 2	
		IOUT=200mA IIN=350ÿA	·	1.1	1.3		
		IOUT=100mA IIN=250ÿA	·	0.9	1.1		
DC Current Transfer	hFE	VCE=2V IOUT=350mA	1000	·	·		2
Ratio Input Current	IN(ON)	VIN=2.4V IOUT=350mA	·	0.4	0.7 mA	3	
(Output On) Input Current	IIN(OFF)	IOUT=500ÿA Tamb=85ÿ	50	65	- ÿA	4	
(Output Off) Input Voltage	VIN(ON)	VCE=2V IOUT=350mA - hFE=800		·	2.6	In the 5th	
		IOUT=200mA -		·	2.0		
(Output On) Clamping	AND	VR=50VÿTamb=25ÿ	·	·	50	ÿA 6	
		VR=50VÿTamb=85ÿ	·	·	100		
Diode Reverse Current	VF	IF=350mA	·	·	2.0 V	7	
Clamping Diode Forward Voltage Input Capacitance CIN			·	15	·	pF ÿ	
Turn on delay time tON		VOUT=50V RL=125ÿÿCL=15pF	·	0.1	·	ÿs	8
Turn off delay time tOFF		VOUT=50V RL=125ÿÿCL=15pF	·	0.2	·		

4. Test circuit

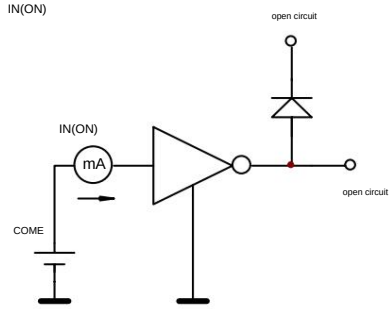
1. ICEX



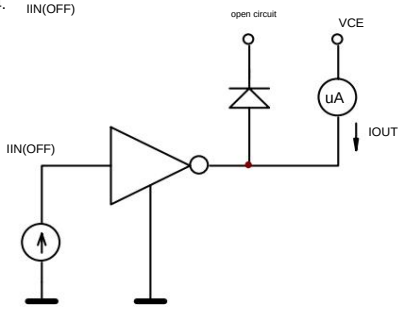
2. CE(village)ÿ V hFE



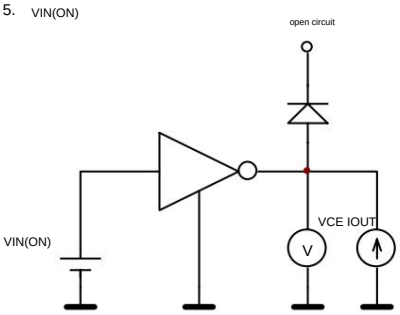
3. IN(ON)



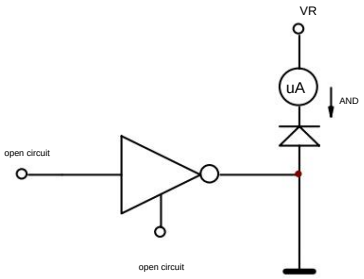
4. IIN(OFF)



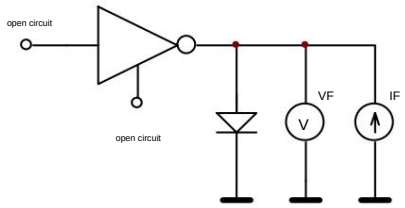
5. VIN(ON)



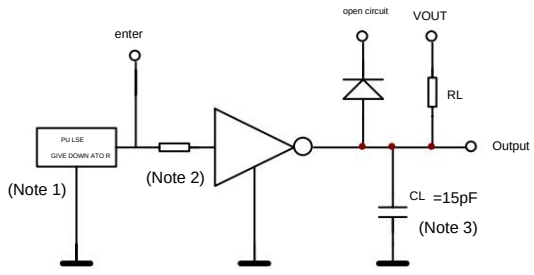
6. AND

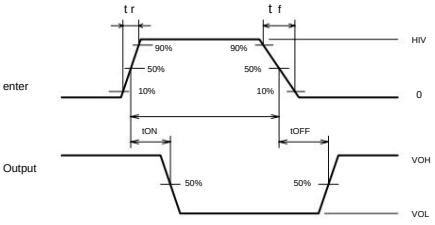


7. VF



8. tON, tOFF

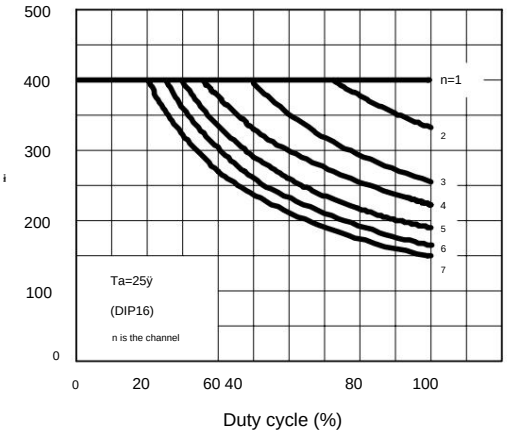




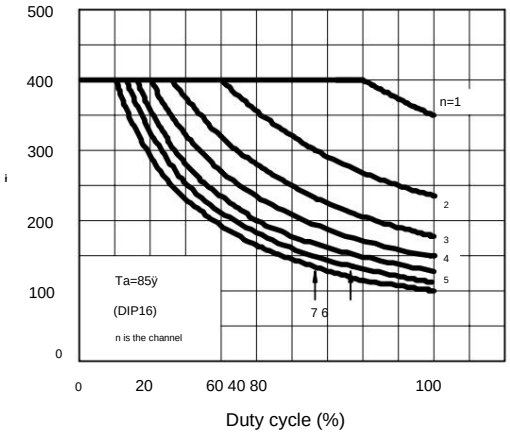
Note 1: Pulse width is 50us, duty cycle is 10%, output impedance is 50ÿ, trÿ5ns, tfÿ10ns. Note 2:
Resistance is 0, input voltage is 3V. Note 3:
CL includes the capacitance on the probe and fixture

5. Characteristic curve

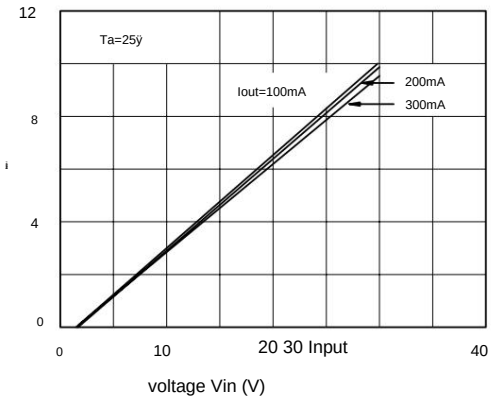
Iout-duty cycle



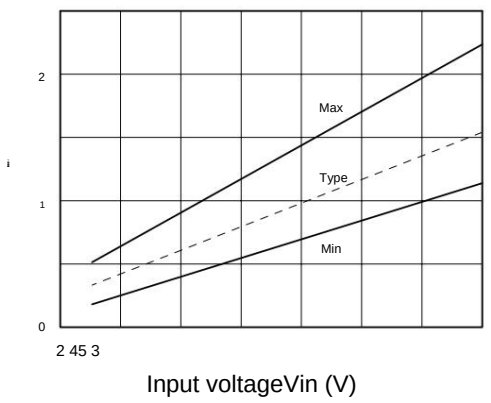
Iout-duty cycle



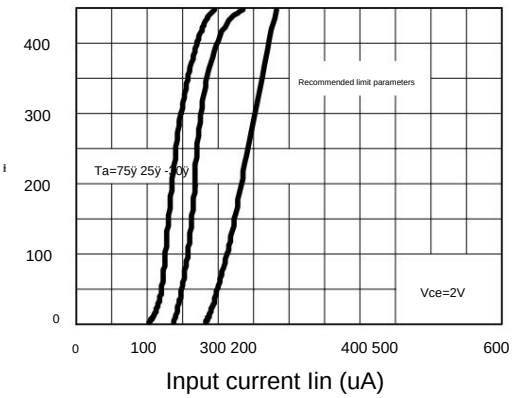
Wine



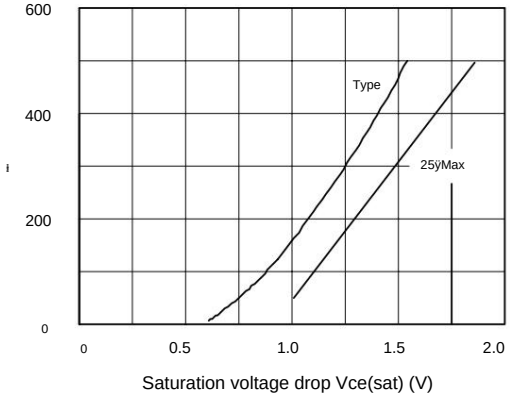
Wine



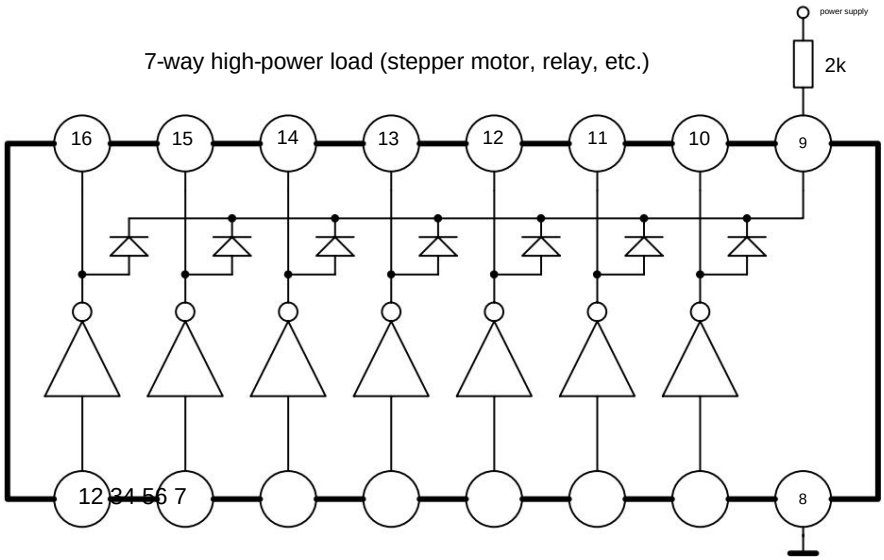
Iout-Iin



Iout-Vce(sat)



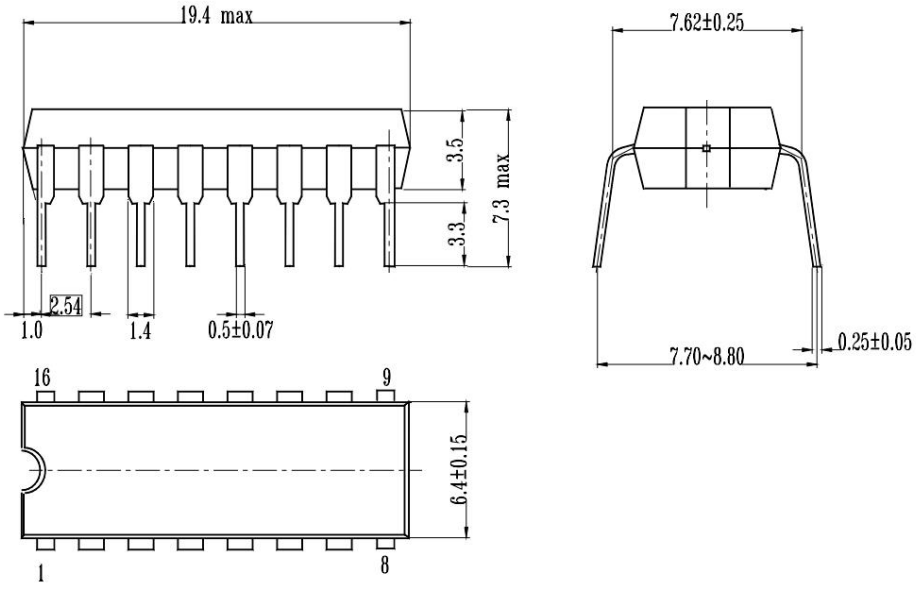
6. Typical application circuit



7-way TTL level control signal input

7. Dimensions and appearance

7.1 DIP16 package



7.2 SOP16 Package