



CS10N65F A9HD

General Description:

CS10N65F A9HD, the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

Features:

- ! Fast Switching
- ! ESD Improved Capability
- ! Low Gate Charge (Typical Data:39nC)
- ! Low Reverse transfer capacitances(Typical:16pF)
- ! 100% Single Pulse avalanche energy Test

Applications:

Power switch circuit of adaptor and charger.

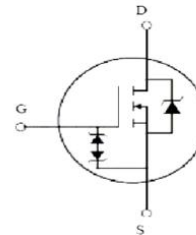
Absolute (Tc= 25℃ unless otherwise specified):

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	10	A
	Continuous Drain Current $T_C = 100^\circ\text{C}$	8.2	A
I_{DM}^{a1}	Pulsed Drain Current	40	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}^{a2}	Single Pulse Avalanche Energy	700	mJ
E_{AR}^{a1}	Avalanche Energy ,Repetitive	70	mJ
I_{AR}^{a1}	Avalanche Current	3.7	A
dv/dt^{a3}	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	50	W
	Derating Factor above 25℃	0.4	W/℃
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	4000	V
T_J, T_{stg}	Operating Junction and Storage Temperature Range	150, -55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

V_{DSS}	650	V
I_D	10	A
$P_D (T_C=25^\circ\text{C})$	50	W
$R_{DS(ON)Typ}$	0.65	Ω

TO-220F**1. Gate 2. Drain 3. Source**

Inner Equivalent Principium Chart





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Electrical Characteristics (Tc= 25℃ unless otherwise specified):

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V _{DSS}	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	650	--	--	V
ΔBV _{DSS} /ΔT _J	Bvdss Temperature Coefficient	ID=250uA, Reference 25℃	--	0.74	--	V/℃
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 650V, V _{GS} = 0V, T _a = 25℃	--	--	1	μA
		V _{DS} =520V, V _{GS} = 0V, T _a = 125℃	--	--	100	
I _{GSS(F)}	Gate to Source Forward Leakage	V _{GS} =+20V	--	--	10	μA
I _{GSS(R)}	Gate to Source Reverse Leakage	V _{GS} =-20V	--	--	-10	μA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
R _{DS(ON)}	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =5A	--	0.65	0.85	Ω
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.0		4.0	V
Pulse width tp≤300μs, δ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g _{fs}	Forward Trans conductance	V _{DS} =15V, I _D =5.0A	--	9	--	S
C _{iss}	Input Capacitance	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz	--	1553	--	pF
C _{oss}	Output Capacitance		--	155	--	
C _{rss}	Reverse Transfer Capacitance		--	16	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
t _{d(ON)}	Turn-on Delay Time	I _D =10.0A V _{DD} = 325V V _{GS} = 10V R _G =9.1Ω	--	15	--	ns
t _r	Rise Time		--	25	--	
t _{d(OFF)}	Turn-Off Delay Time		--	51	--	
t _f	Fall Time		--	31	--	
Q _g	Total Gate Charge	I _D =10.0A V _{DD} =325V V _{GS} = 10V	--	39		nC
Q _{gs}	Gate to Source Charge		--	7	--	
Q _{gd}	Gate to Drain (“Miller”)Charge		--	16	--	



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Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	10	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	40	A
V_{SD}	Diode Forward Voltage	$I_S=10.0A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=10.0A, T_J = 25^{\circ}C$	--	275	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt=100A/us, V_{GS}=0V$	--	1766	--	nC
Pulse width $t_p \leq 300\mu s, \delta \leq 2\%$						

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case	2.5	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-Ambient	100	$^{\circ}C/W$

Gate-source Zener diode

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	$I_{GS} = \pm 1mA$ (Open Drain)	30			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

^{a1}: Repetitive rating; pulse width limited by maximum junction temperature

^{a2}: $L=10.0mH, I_D=12.6A$, Start $T_J=25^{\circ}C$

^{a3}: $I_{SD}=10A, di/dt \leq 100A/us, V_{DD} \leq BV_{DS}$, Start $T_J=25^{\circ}C$

Characteristics Curve:

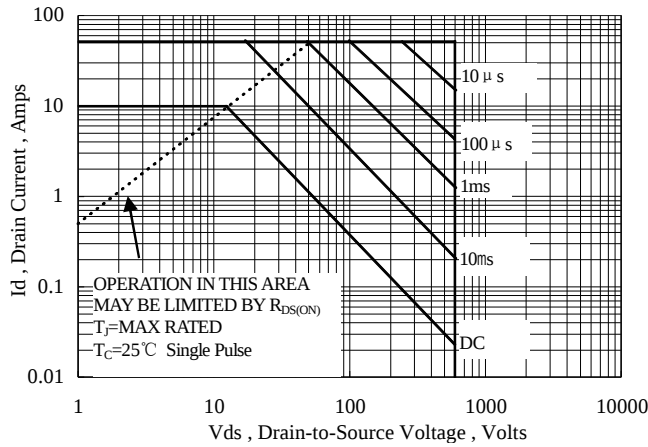


Figure 1 Maximum Forward Bias Safe Operating Area

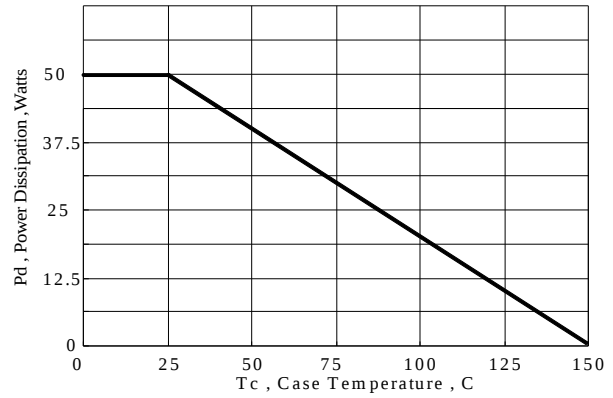


Figure 2 Maximum Power Dissipation vs Case Temperature

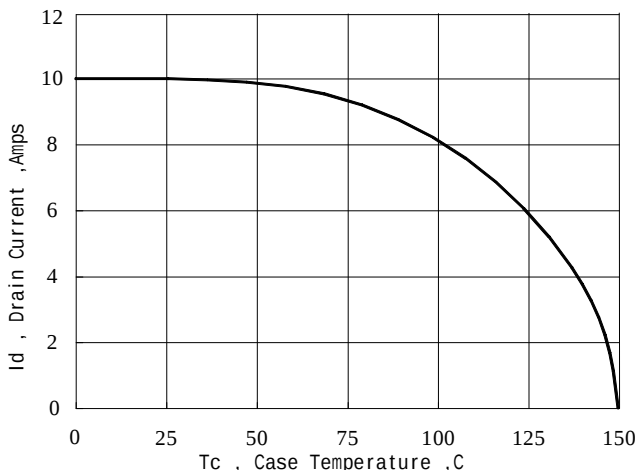


Figure 3 Maximum Continuous Drain Current vs Case Temperature

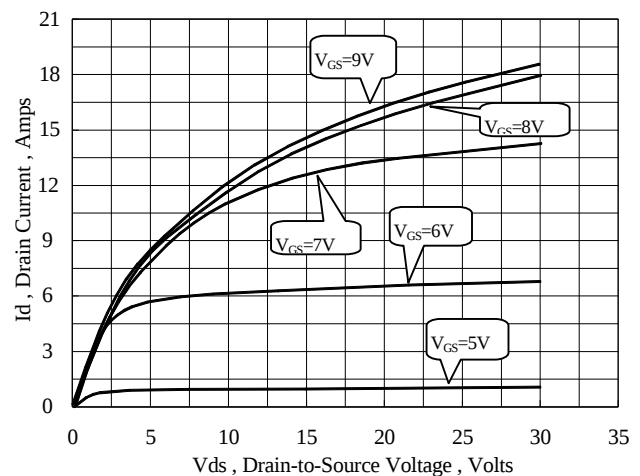


Figure 4 Typical Output Characteristics

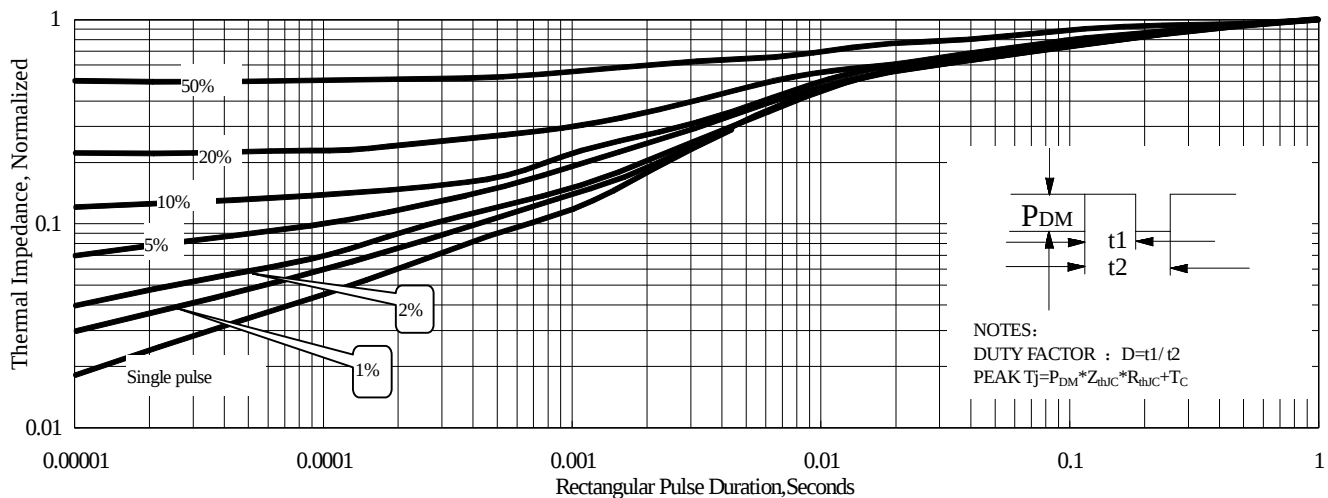


Figure 5 Maximum Effective Thermal Impedance, Junction to Case



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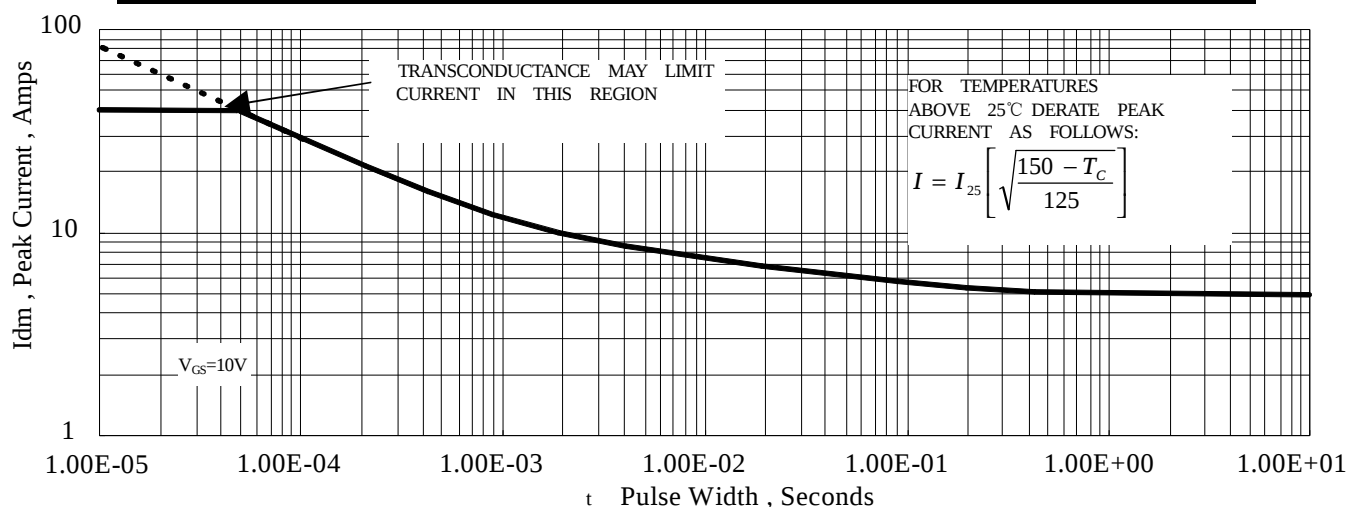


Figure 6 Maximum Peak Current Capability

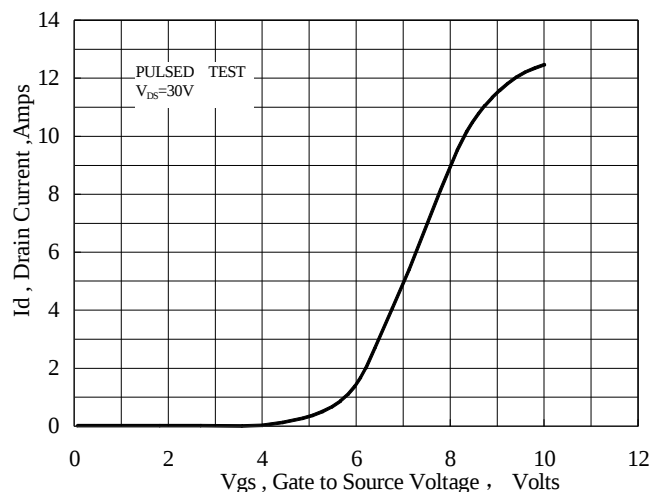


Figure 7 Typical Transfer Characteristics

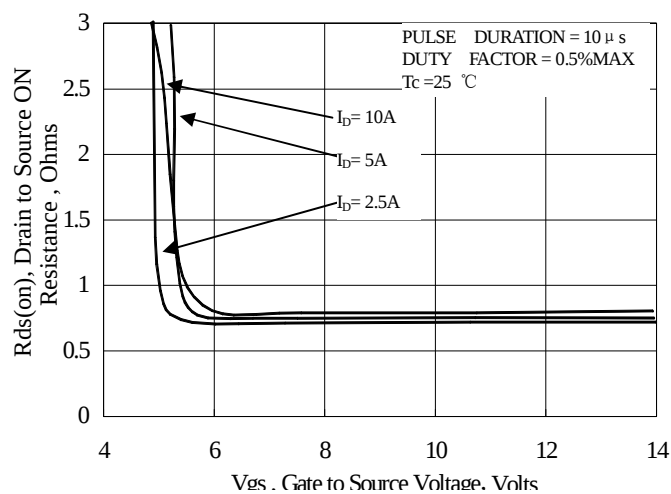


Figure 8 Typical Drain to Source ON Resistance vs Gate Voltage and Drain Current

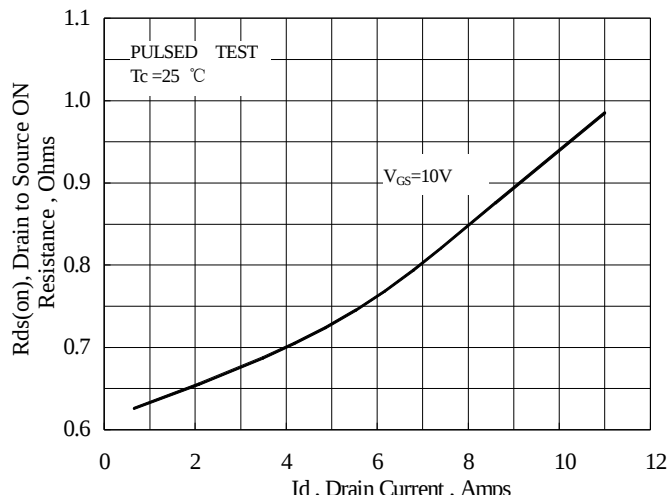


Figure 9 Typical Drain to Source ON Resistance vs Drain Current

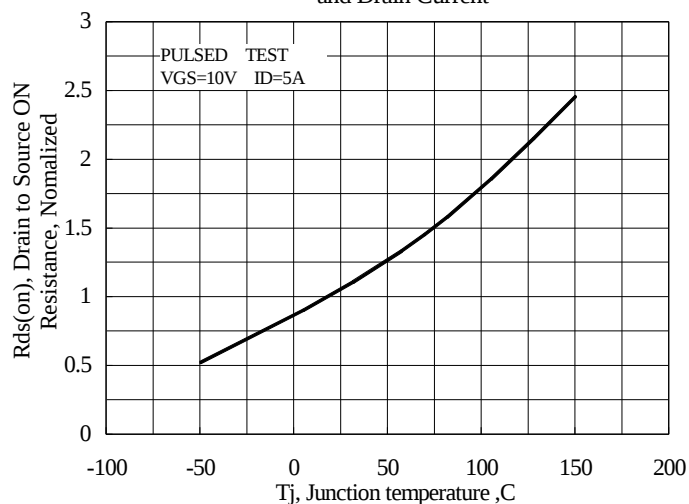


Figure 10 Typical Drain to Source on Resistance vs Junction Temperature



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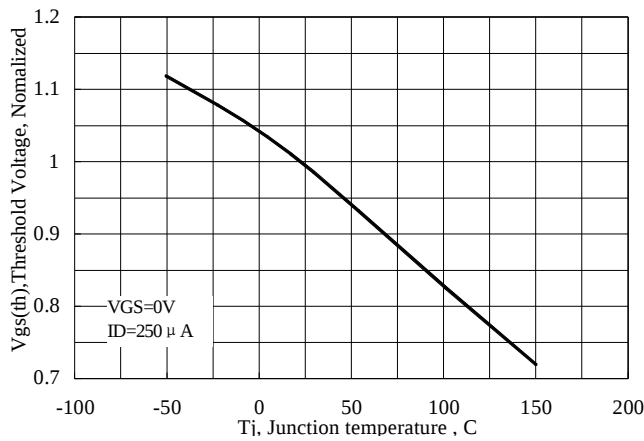


Figure 11 Typical Threshold Voltage vs Junction Temperature

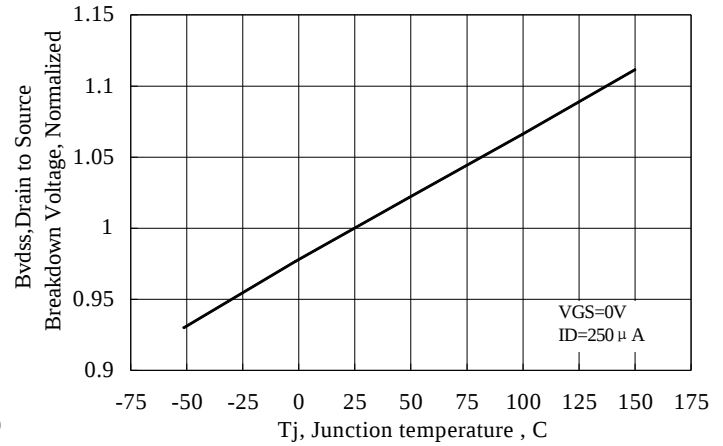


Figure 12 Typical Breakdown Voltage vs Junction Temperature

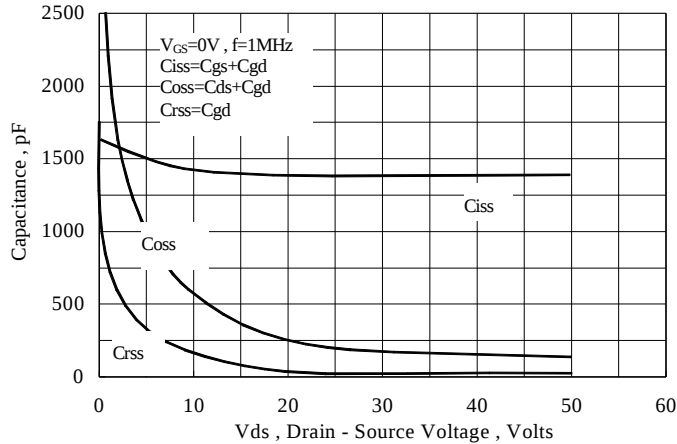


Figure 13 Typical Capacitance vs Drain to Source Voltage

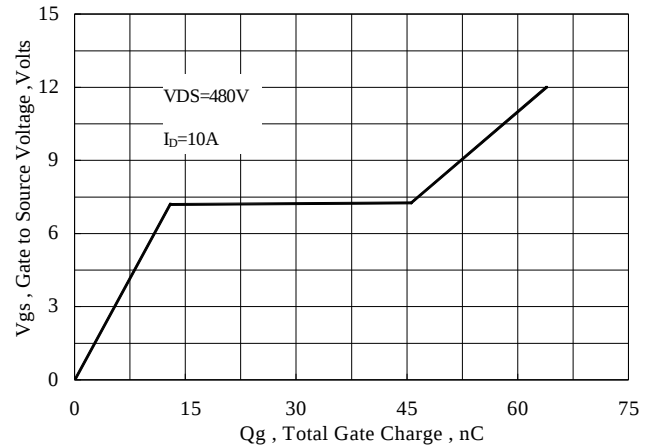


Figure 14 Typical Gate Charge vs Gate to Source Voltage

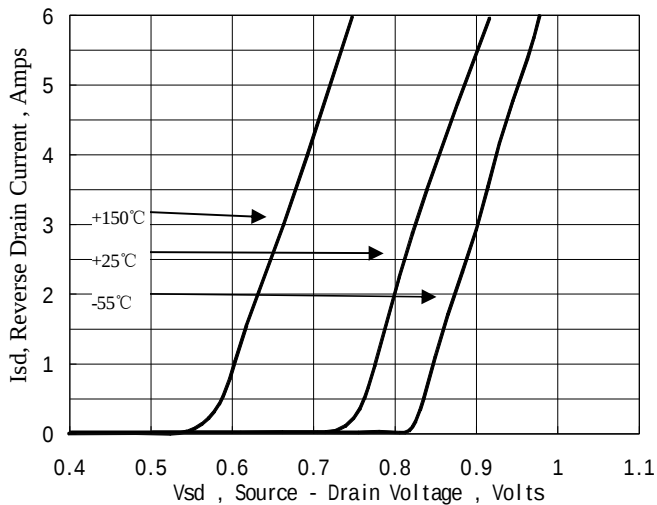


Figure 15 Typical Body Diode Transfer Characteristics

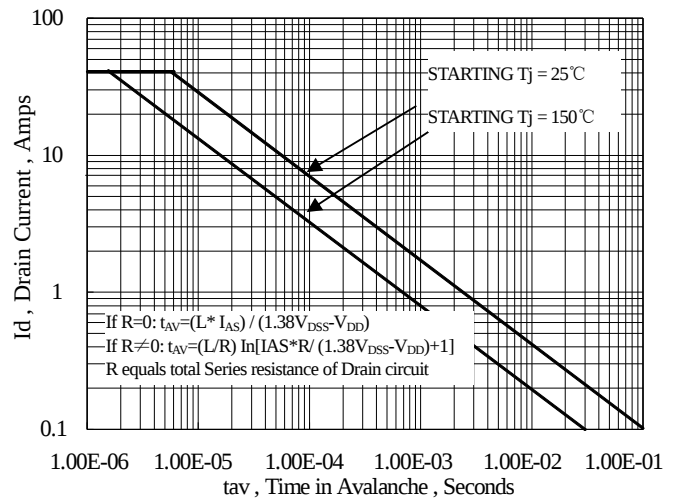


Figure 16 Unclamped Inductive Switching Capability

Test Circuit and Waveform

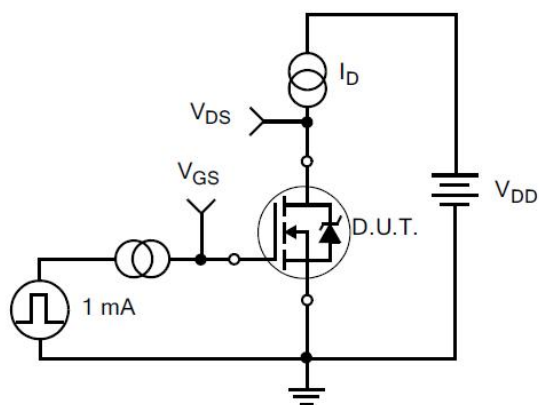


Figure 17. Gate Charge Test Circuit

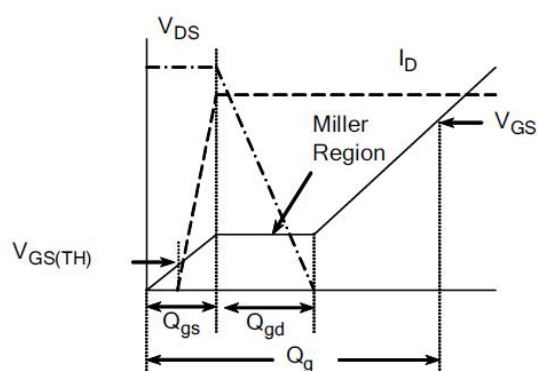


Figure 18. Gate Charge Waveform

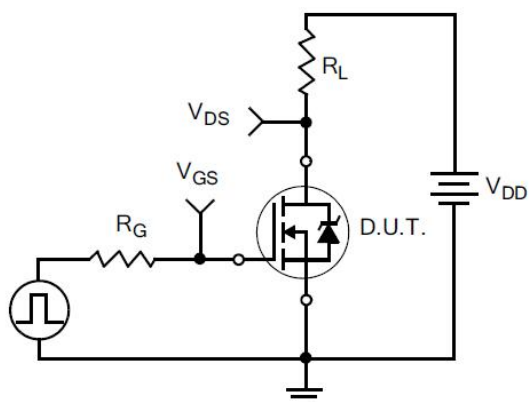


Figure 19. Resistive Switching Test Circuit



Figure 20. Resistive Switching Waveforms

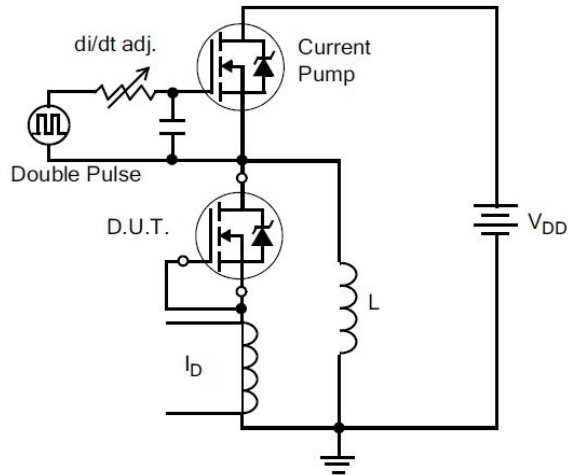


Figure 21. Diode Reverse Recovery Test Circuit

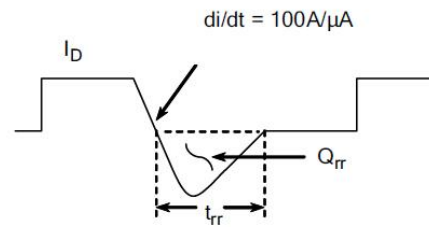


Figure 22. Diode Reverse Recovery Waveform

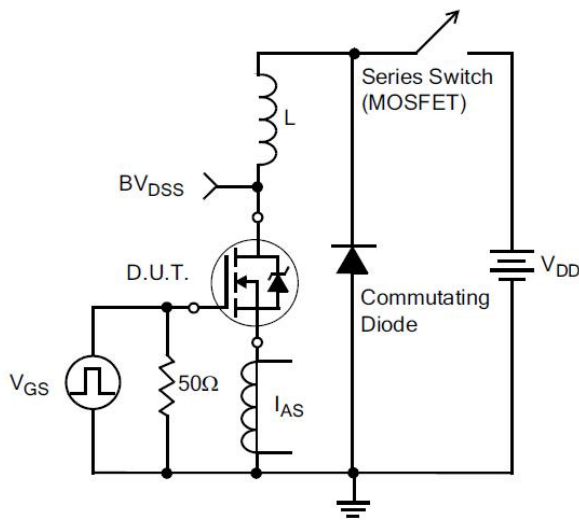


Figure 23. Unclamped Inductive Switching Test Circuit

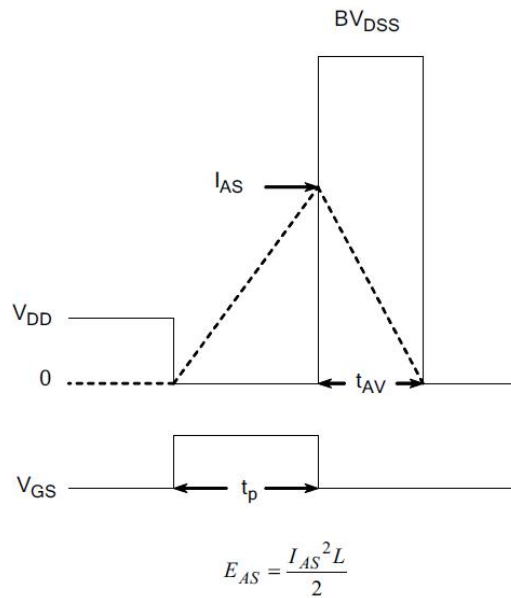
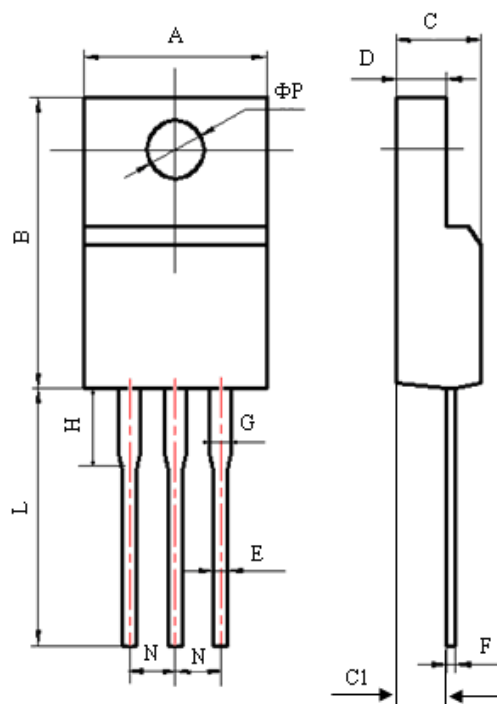


Figure 24. Unclamped Inductive Switching Waveforms

Package Information:



Items	Values(mm)	
	MIN	MAX
A	9.60	10.40
B	15.40	16.20
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	2.00	2.40
L	12.00	14.00
	6.30	7.70
N	2.34	2.74
Φ P	3.00	3.30

TO-220F Package

**The name and content of poisonous and harmful material in products**

Part's Name	Hazardous Substance					
	Pb	Hg	Cd	Cr(VI)	PBB	PBDE
Limit	≤0.1%	≤0.1%	≤0.01%	≤0.1%	≤0.1%	≤0.1%
Lead Frame	○	○	○	○	○	○
Molding Compound	○	○	○	○	○	○
Chip	○	○	○	○	○	○
Wire Bonding	○	○	○	○	○	○
Solder	×	○	○	○	○	○
Note	○: means the hazardous material is under the criterion of SJ/T11363-2006. ×: means the hazardous material exceeds the criterion of SJ/T11363-2006. The plumbum element of solder exist in products presently, but within the allowed range of Eurogroup's RoHS.					

Warnings

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. It is suggested to be used under 80 percent of the maximum ratings of the device.
2. When installing the heatsink, please pay attention to the torsional moment and the smoothness of the heatsink.
3. VDMOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. This publication is made by Huajing Microelectronics and subject to regular change without notice.

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