

Features

- Uses CRM(CQ) advanced SkyMOS4 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

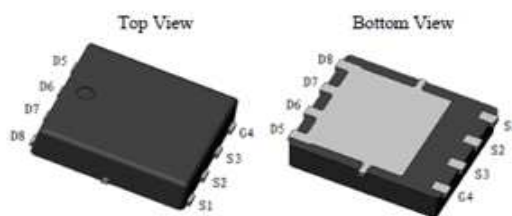
Product Summary

V_{DS}	100V
$R_{DS(on).typ}$	5.8mΩ
I_D	60A

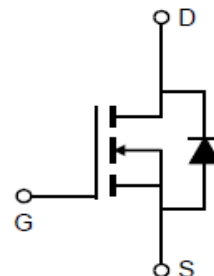
Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management System
- UPS (Uninterruptible Power Supplies)

100% DVDS Tested
100% Avalanche Tested



CRSM069N10L4Z



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRSM069N10L4Z	069N10L4Z	DFN5X6	Tape&Reel	N/A	N/A	4k/5k

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 25^\circ\text{C}$ (Package limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	80 60 48	A
Pulsed drain current ($T_C = 25^\circ\text{C}$, t_p limited by T_{jmax})	$I_{D \text{ pulse}}$	240	A
Avalanche energy, single pulse ($I_D = 26\text{A}$, $R_g = 25\Omega$) ^[1]	E_{AS}	174	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation ($T_C = 25^\circ\text{C}$)	P_{tot}	75	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	T_{sold}	260	$^\circ\text{C}$

※. Notes:

1.EAS is tested at starting $T_j = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $I_{AS} = 26\text{A}$, $V_{GS} = 10\text{V}$.

2.Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX}) = 150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^\circ\text{C}$.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	1.66	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	53	

Electrical Characteristic (at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	105	-	-	V	$V_{GS}=0V, I_D=250\mu A$
		105	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{GS(th)}$	1.5	2.0	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=100V, V_{GS}=0V$ $T_j=25^{\circ}\text{C}$
		-	-	100		$T_j=125^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	0	-	± 100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	5.8	6.9	mΩ	$V_{GS}=10V, I_D=30A$
		-	7.6	9.2		$V_{GS}=4.5V, I_D=30A$
Transconductance	g_{fs}	-	96.7	193.4	S	$V_{DS}=5V, I_D=30A$

Dynamic Characteristic

Input Capacitance	C_{iss}	1731	2596	3894	pF	$V_{GS}=0V, V_{DS}=50V,$ $f=1MHz$
Output Capacitance	C_{oss}	253	380	570		
Reverse Transfer Capacitance	C_{rss}	7	14	28		
Gate Total Charge	Q_G	31	47.0	70.5	nC	$V_{GS}=10V, V_{DS}=50V,$ $I_D=30A$
Gate-Source charge	Q_{gs}	8	11.4	17.1		
Gate-Drain charge	Q_{gd}	4	8.8	17.6		
Turn-on delay time	$t_{d(on)}$	6	12.0	24	ns	$V_{GS}=10V, V_{DD}=50V,$ $R_{G_ext}=2.7\Omega$
Rise time	t_r	24	36.0	54		
Turn-off delay time	$t_{d(off)}$	24	36.0	54		
Fall time	t_f	7	11.0	16.5		
Gate resistance	R_G	0	1.0	5	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.85	1.4	V	$V_{GS}=0V, I_{SD}=30A$
Body Diode Reverse Recovery Time	t_{rr}	24	47.8	95.5	ns	$I_F=30A, dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	27	53.8	107.6	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

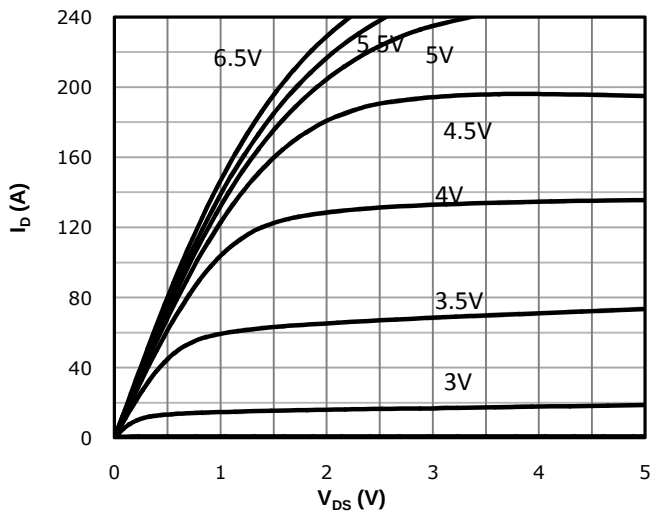


Fig 2: Transfer Characteristics

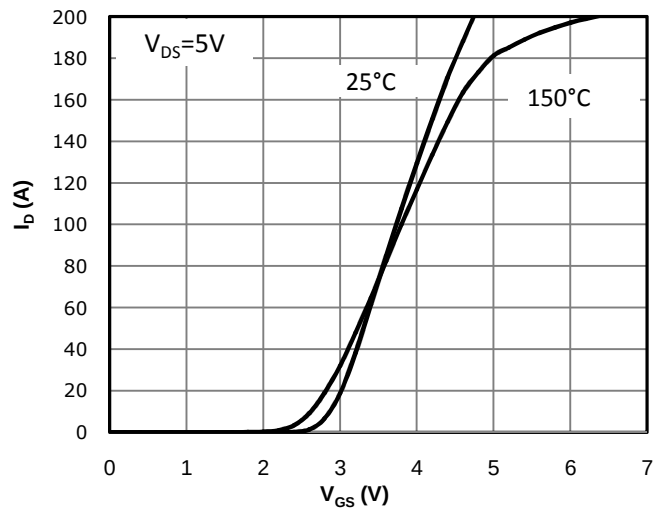


Fig 3: Rds(on) vs Drain Current and Gate Voltage

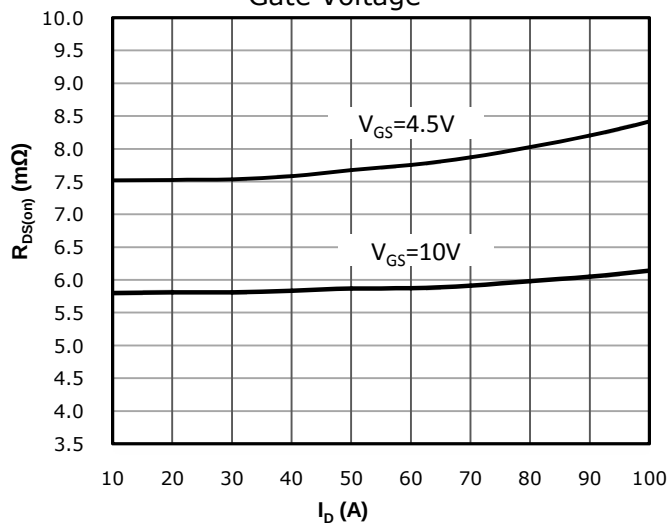


Fig 4: Rds(on) vs Gate Voltage

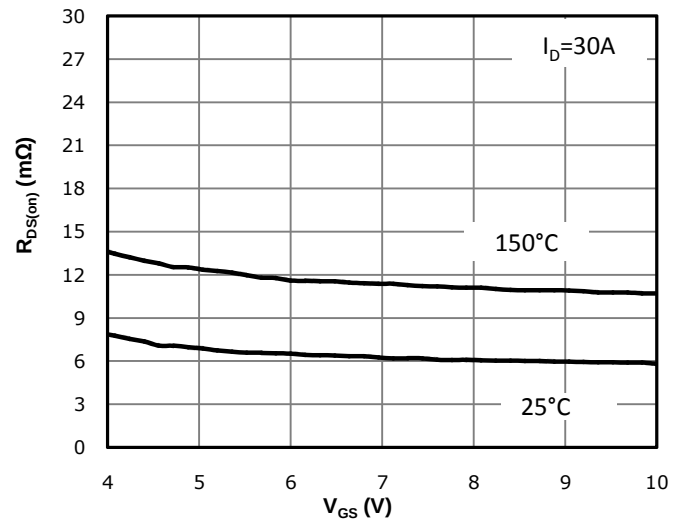


Fig 5: Rds(on) vs. Temperature

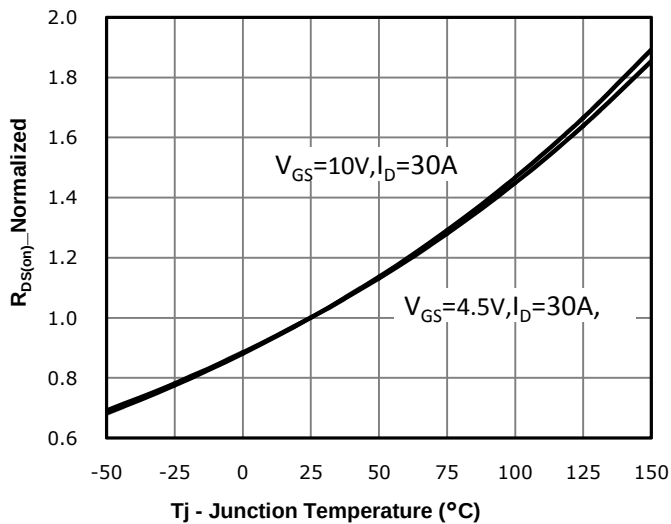


Fig 6: Vgs(th) vs. Temperature

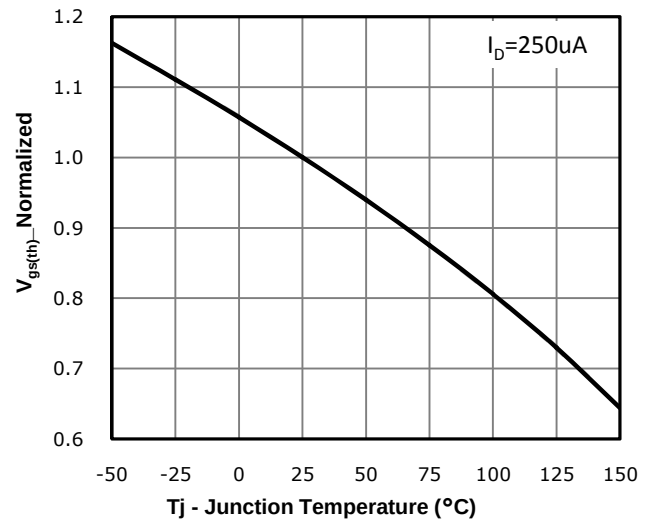


Fig 7: BVdss vs. Temperature

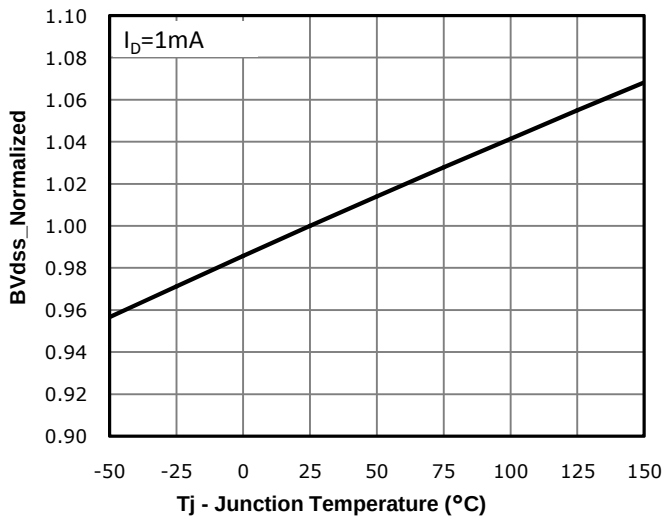


Fig 8: Capacitance Characteristics

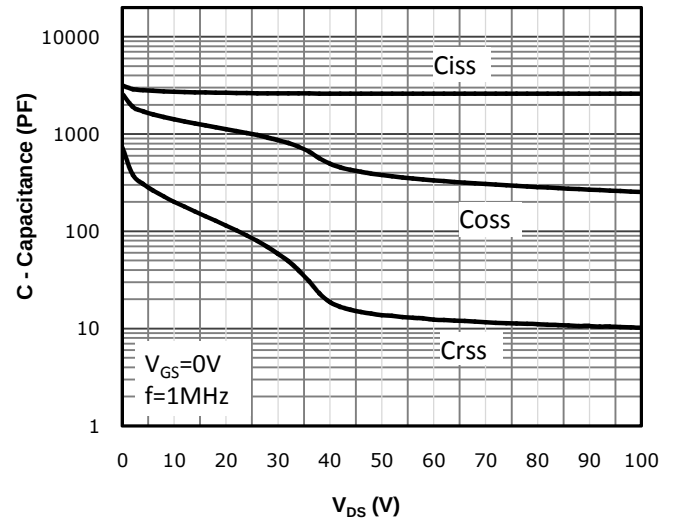


Fig 9: Gate Charge Characteristics

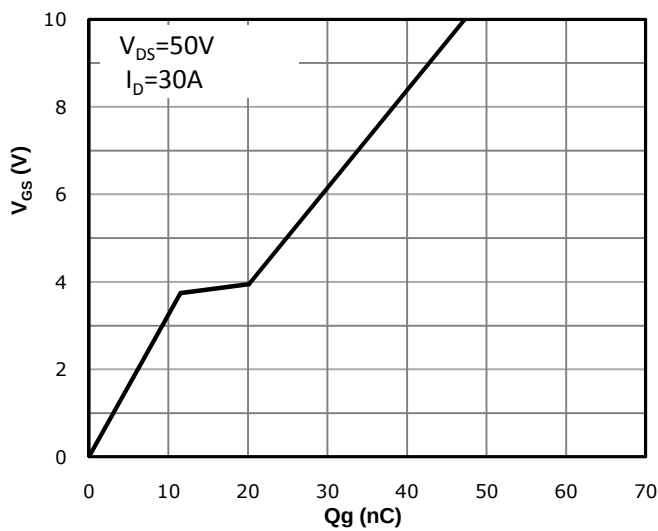


Fig 10: Body-diode Forward Characteristics

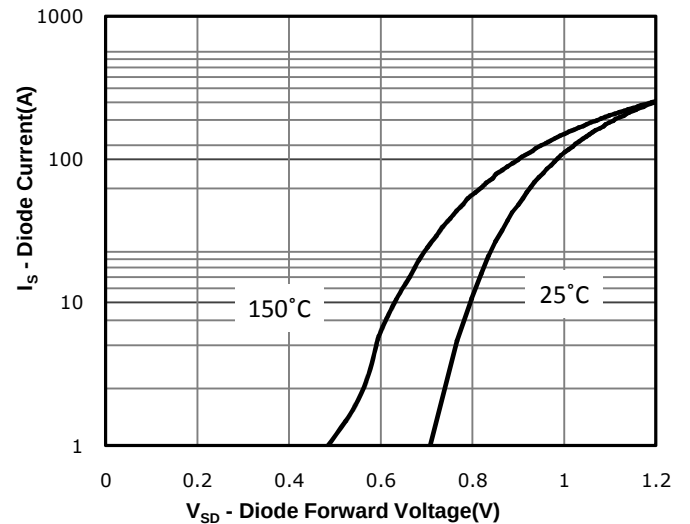


Fig 11: Power Dissipation

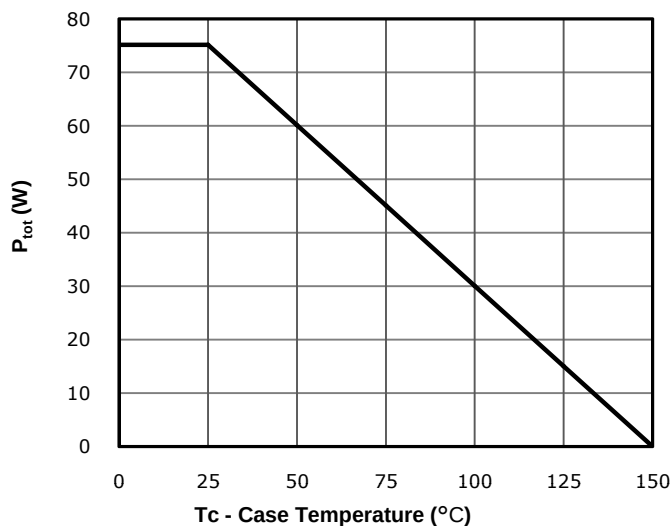


Fig 12: Drain Current Derating

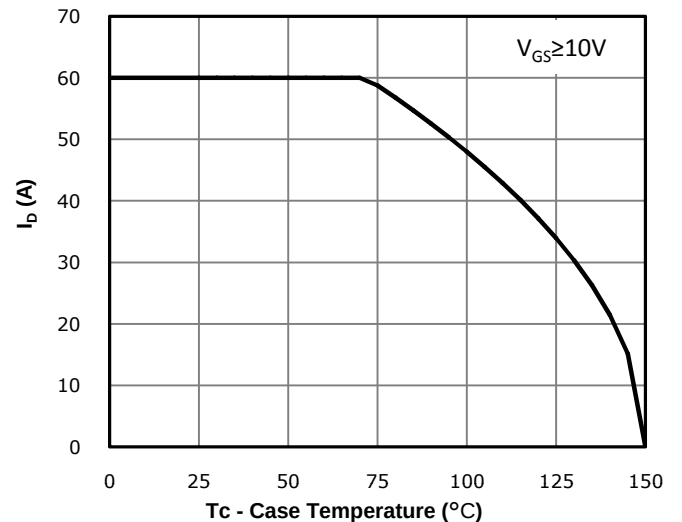


Fig 13: Safe Operating Area

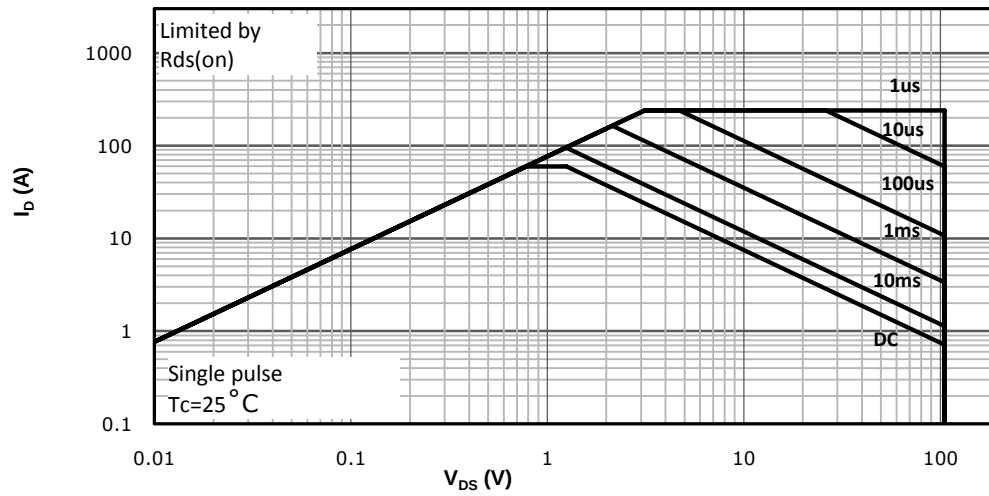
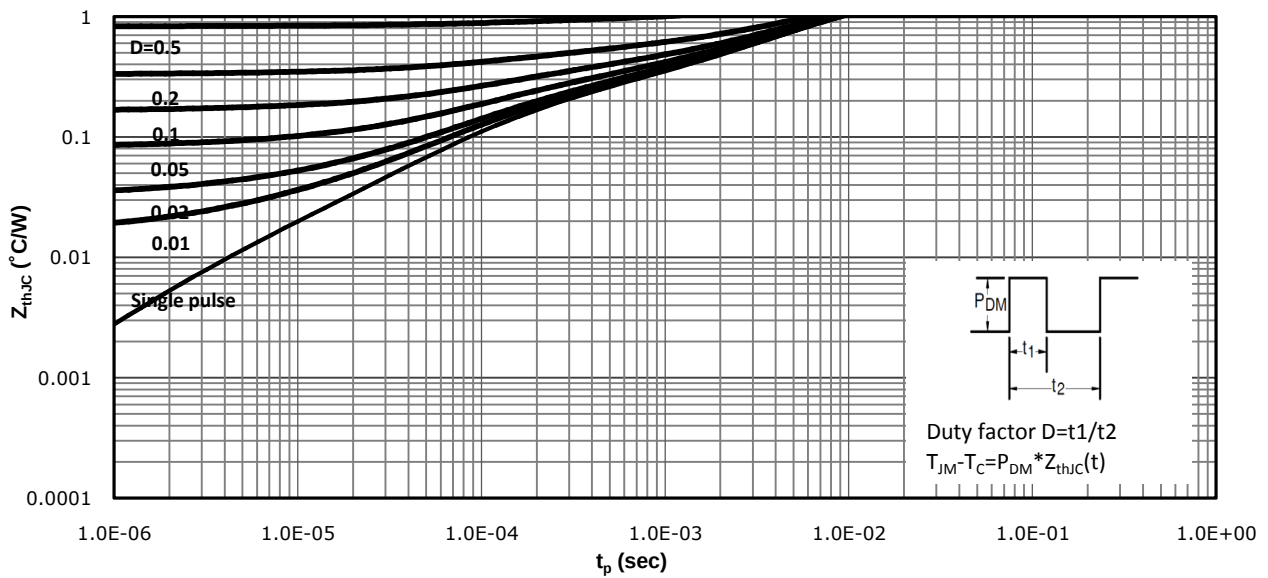
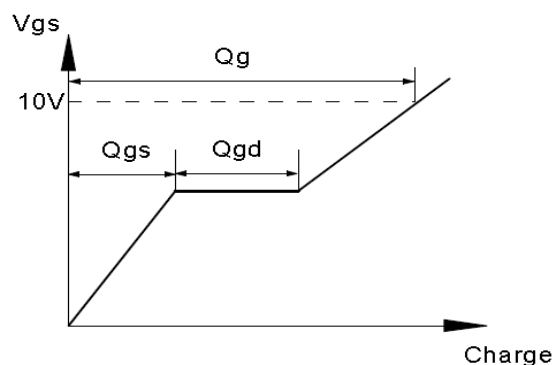
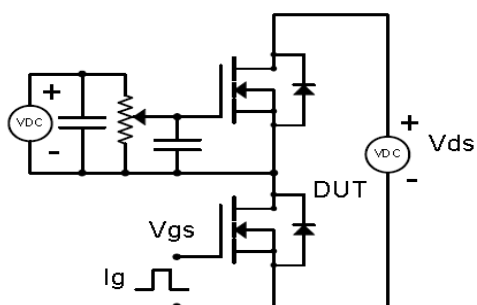


Fig 14: Max. Transient Thermal Impedance

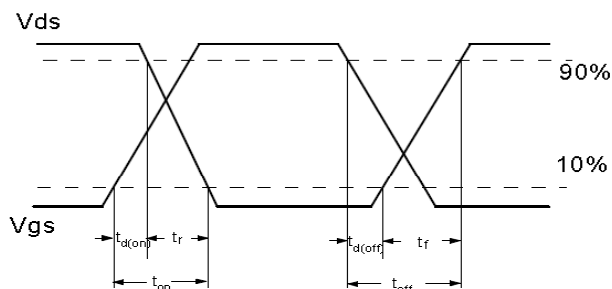
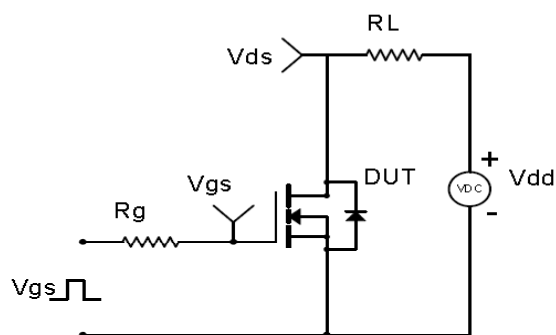


Test Circuit & Waveform

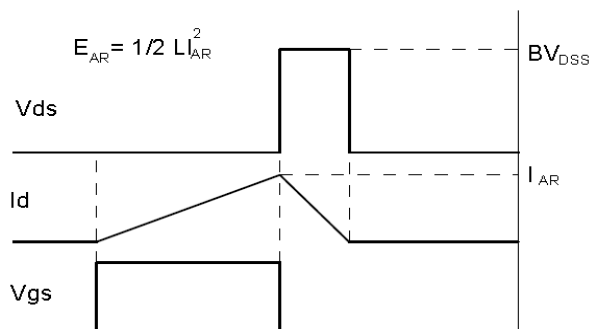
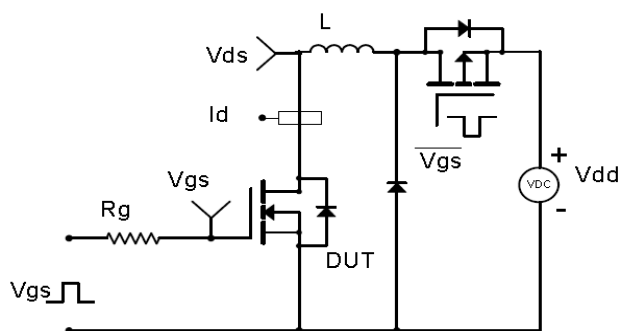
Gate Charge Test Circuit & Waveform



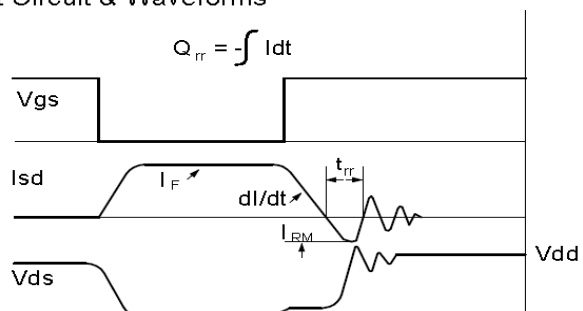
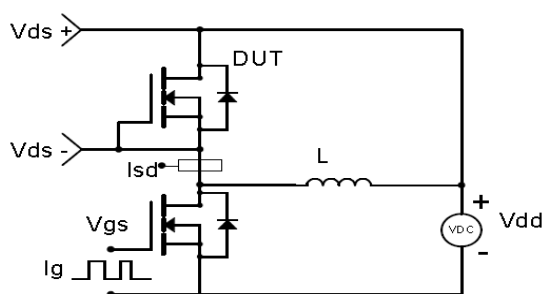
Resistive Switching Test Circuit & Waveforms



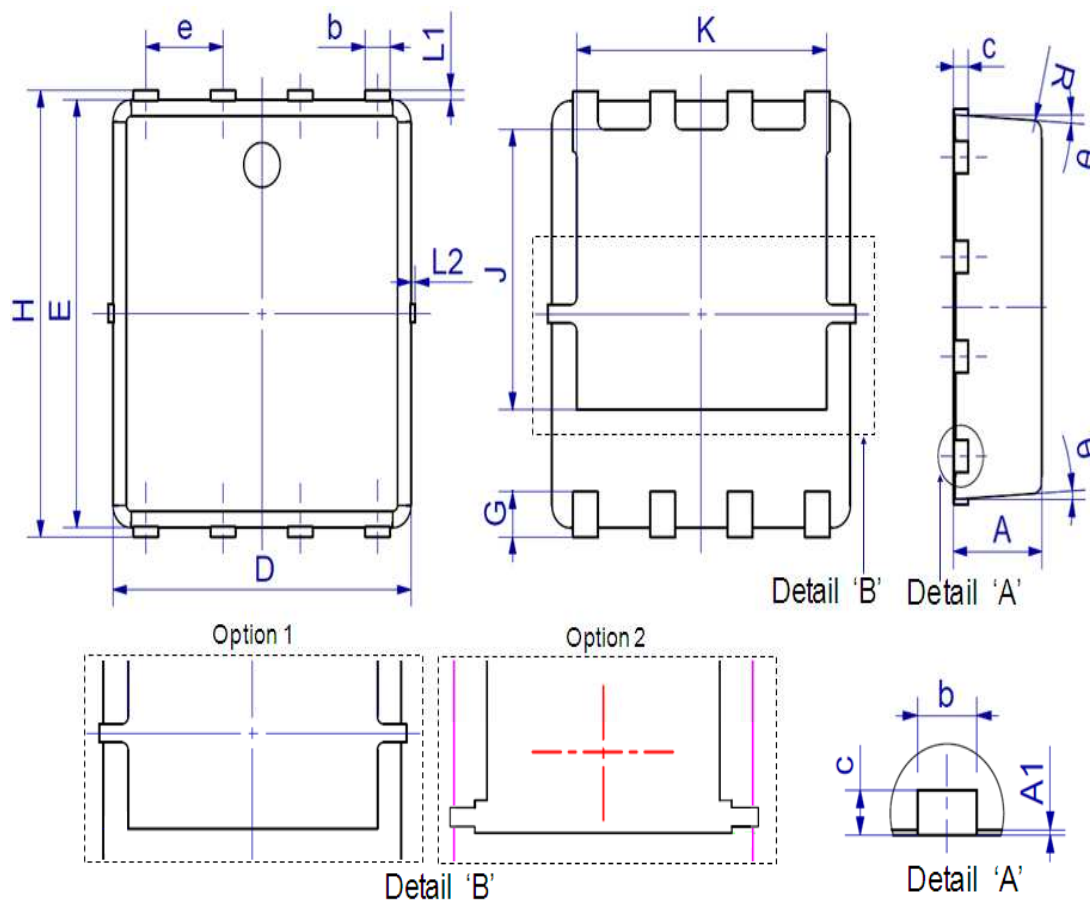
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: DFN5*6



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.20	0.031	0.047
A1	0.00	0.05	0.000	0.002
b	0.30	0.51	0.012	0.020
c	0.15	0.35	0.006	0.014
D	4.80	5.40	0.189	0.213
e	1.27 BSC		0.050 BSC	
E	5.66	6.06	0.223	0.239
G	0.30	0.71	0.012	0.028
H	5.90	6.35	0.232	0.250
J	3.32	3.92	0.131	0.154
K	3.61	4.25	0.142	0.167
L1	0.05	0.25	0.002	0.010
L2	0.00	0.15	0.000	0.006
R	0.25 REF		0.010 REF	
θ	0°	12°	0°	12°

Marking**NOTE:**

NXBBAAAAY

N —Wire Bond code

X —Assembly location code

BB —Fab code

AAAA —Lot code

Y —Bin code

Revision History

Revision	Date	Major changes
1.0	2024-03-08	Release of Preliminary version.

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qualified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

CRM(CQ) reserves the right to improve product design, function and reliability without notice.