

Features

- Uses CRM(CQ) advanced SkyMOS2 technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- Qualified according to JEDEC criteria

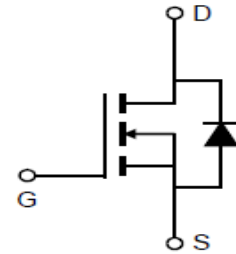
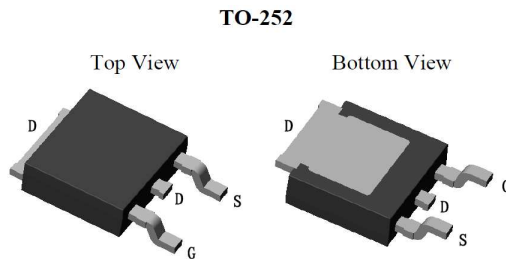
Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management
- UPS (Uninterruptible Power Supplies)

Product Summary

V_{DS}	100V
$R_{DS(on)}@10V$ typ	11.0mΩ
$R_{DS(on)}@4.5V$ typ	14.3mΩ
I_D	65A

100% Avalanche Tested



Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
CRSD130N10L2	CRSD130N10L2	TO-252	Tape\Reel	N/A	N/A	2500pcs

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	100	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	65 41	A
Pulsed drain current ($T_A = 25^\circ\text{C}$, t_p limited by T_{jmax})	$I_{D \text{ pulse}}$	261	A
Avalanche Current ($L=0.5\text{mH}$)	I_{AS}	16	A
Avalanche energy, single pulse ($L=0.5\text{mH}$, $R_g=25\Omega$)	E_{AS}	64	mJ
Repeative avalanche Current ($L=0.5\text{mH}$)*	I_{AR}	12	A
Repeative avalanche ($L=0.5\text{mH}$)*	E_{AR}	33	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation ($T_C = 25^\circ\text{C}$, $R_{thJA}=94 \text{ K/W}$)	P_{tot}	101.2	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	$^\circ\text{C}$

*Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J = 25^\circ\text{C}$.

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	1.24	°C/W
Thermal resistance, junction – ambient(min. footprint)*	R_{thJA}	94	
Soldering temperature, wave and reflow soldering are allowed (reflow MSL1)	T_{solder}	260	°C

* Surface mounted FR-4 board by JEDEC (jesd51-7). Continuous current at TC=25°C is silicon limited

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	100	115	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	1.4	1.8	2.2	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	0.05	1	μA	$V_{DS}=100V, V_{GS}=0V$ $T_j=25^\circ C$
		-	-	10		$T_j=125^\circ C$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=\pm 20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	11.0	13.2	mΩ	$V_{GS}=10V, I_D=50A$ $T_j=100^\circ C$
		-	16.7	20.0		$V_{GS}=4.5V, I_D=50A$ $T_j=100^\circ C$
		-	14.3	17.2		
		-	20.1	24.1		
Transconductance	g_{fs}	-	70.8	-	S	$V_{DS}=5V, I_D=50A$

Dynamic Characteristic

Input Capacitance	C_{iss}	809	1618	2427	pF	$V_{GS}=0V, V_{DS}=50V,$ $f=1MHz$
Output Capacitance	C_{oss}	139	277	416		
Reverse Transfer Capacitance	C_{rss}	11	22	44		
Gate Total Charge	Q_G	-	28	42	nC	$V_{GS}=10V, V_{DS}=50V,$ $I_D=50A, f=1MHz$
Gate-Source charge	Q_{gs}	-	7	10		
Gate-Drain charge	Q_{gd}	-	5	7		
Turn-on delay time	$t_{d(on)}$	-	30	45	ns	$V_{GS}=10V, V_{DD}=50V,$ $R_{G_ext}=2.7\Omega$
Rise time	t_r	-	81	122		
Turn-off delay time	$t_{d(off)}$	-	24	36		
Fall time	t_f	-	7	11		
Gate resistance	R_G	0.8	1.6	2.4	Ω	$V_{GS}=V_{DS}=0V, f=1MHz$

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	0.87	1	V	$V_{GS}=0V, I_{SD}=20A$
Body Diode Reverse Recovery Time	t_{rr}	-	80	-	ns	$I_F=50A,$ $dI/dt=100A/\mu s$
Body Diode Reverse Recovery Charge	Q_{rr}	-	198	-	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

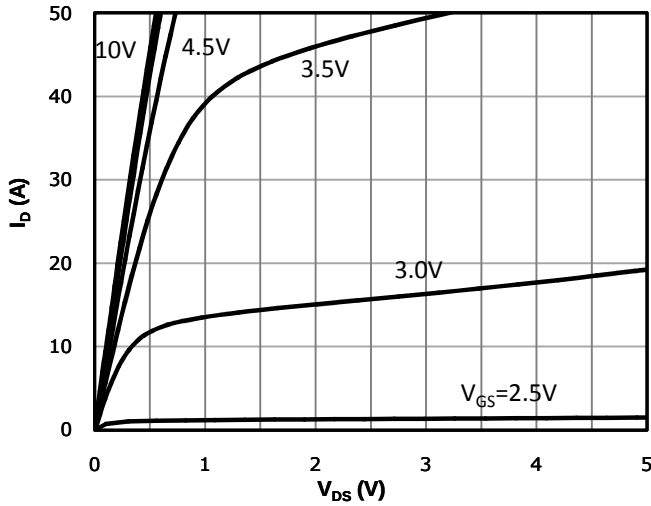


Fig 2: Transfer Characteristics

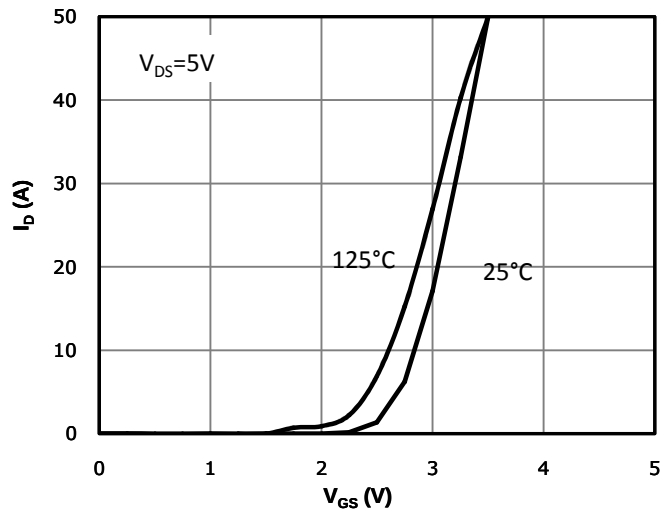


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

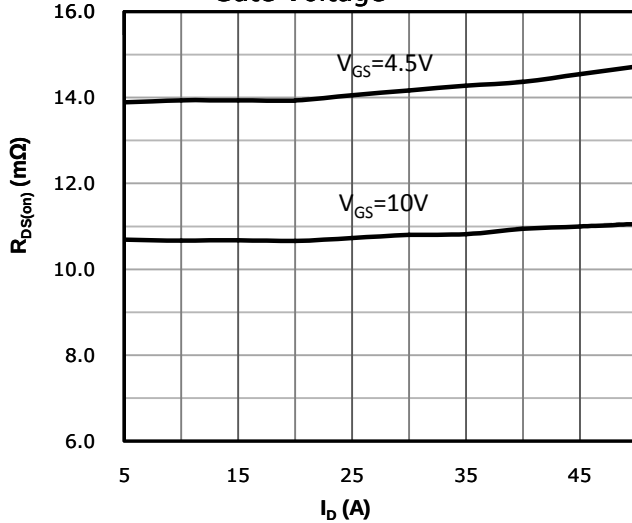


Fig 4: $R_{DS(on)}$ vs Gate Voltage

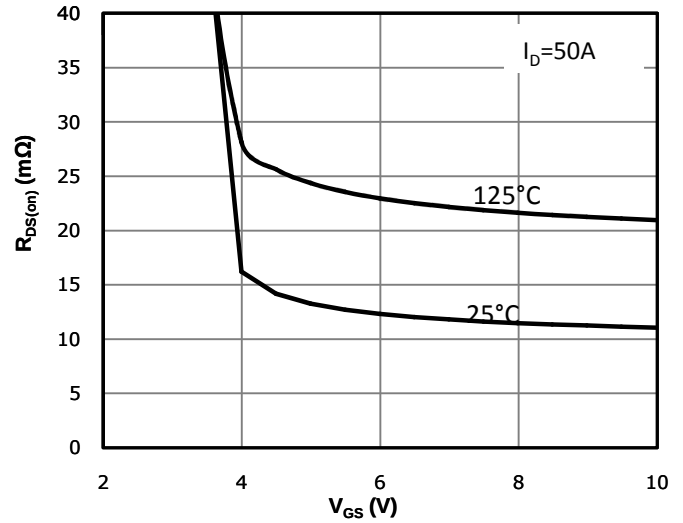


Fig 5: $R_{DS(on)}$ vs. Temperature

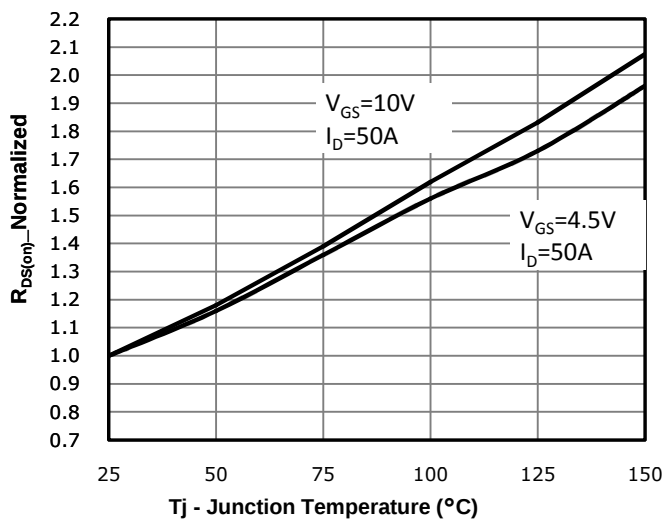


Fig 6: Capacitance Characteristics

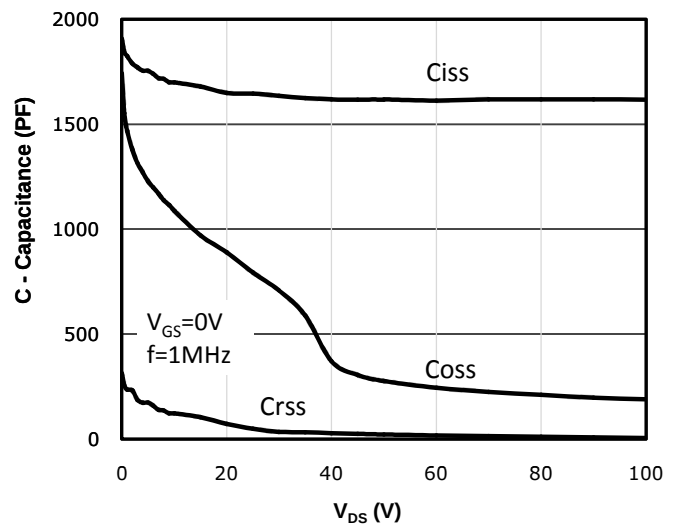


Fig 7: Gate Charge Characteristics

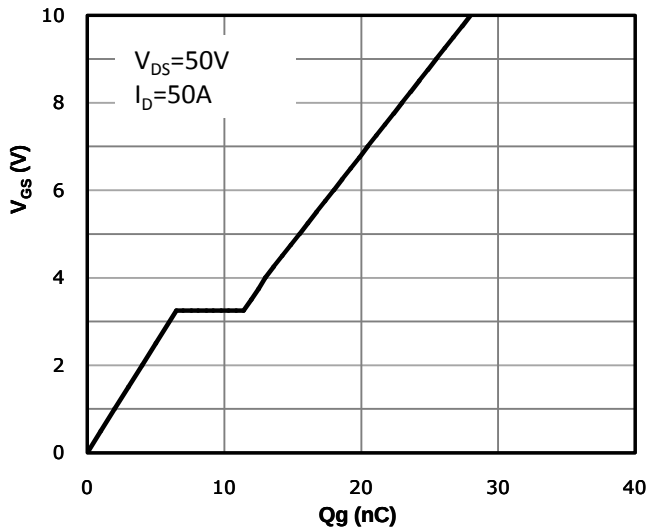


Fig 8: Body-diode Forward Characteristics

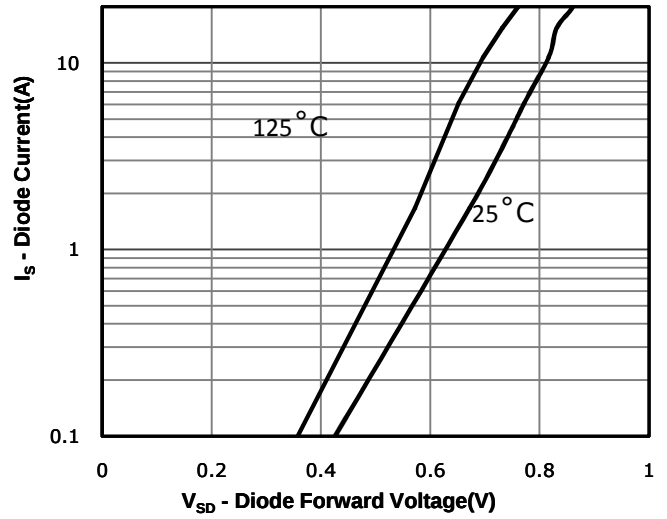


Fig 9: Power Dissipation

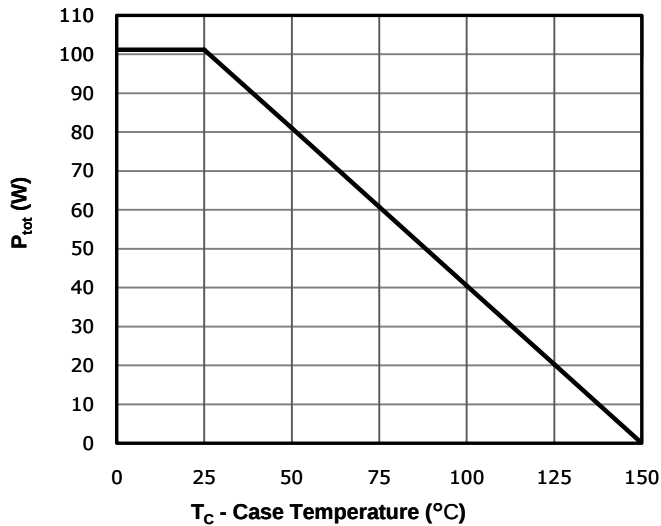


Fig 10: Drain Current Derating

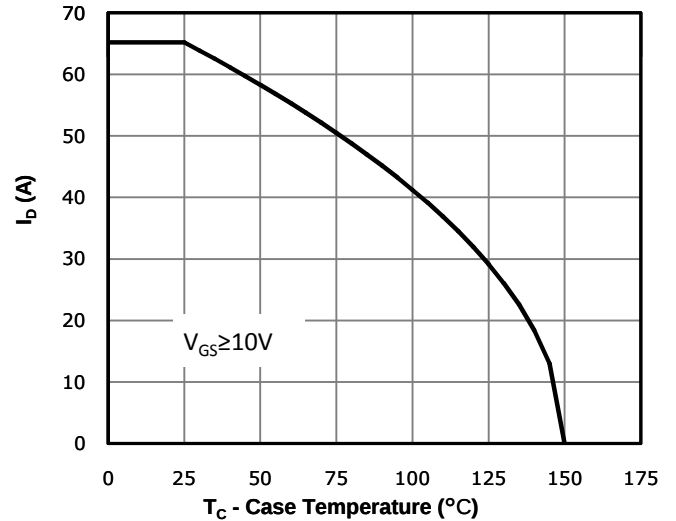


Fig 11: Safe Operating Area

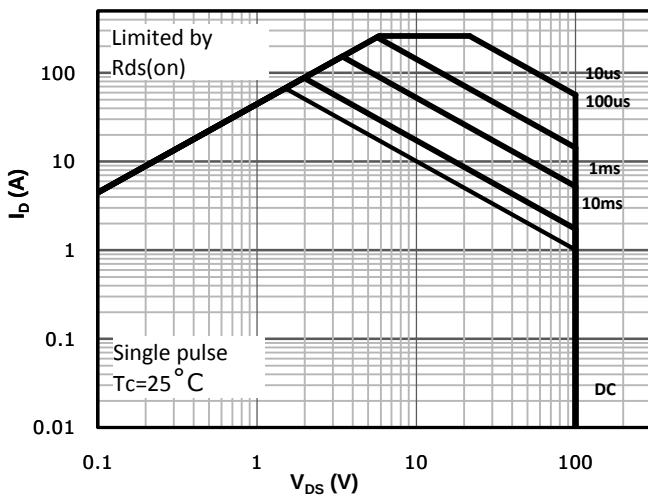
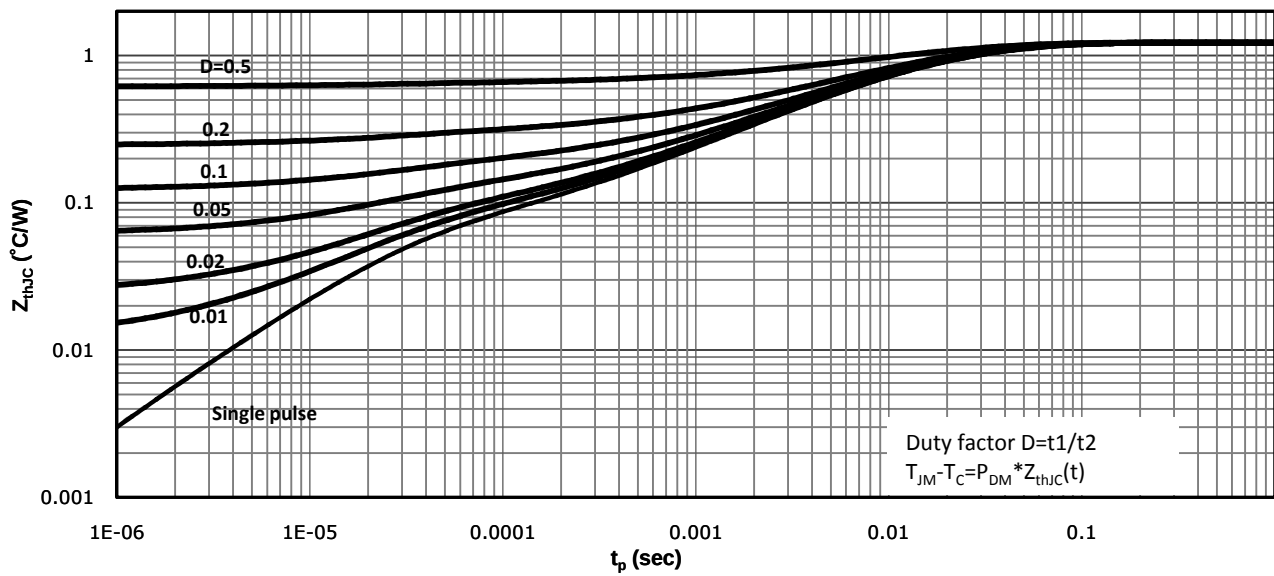
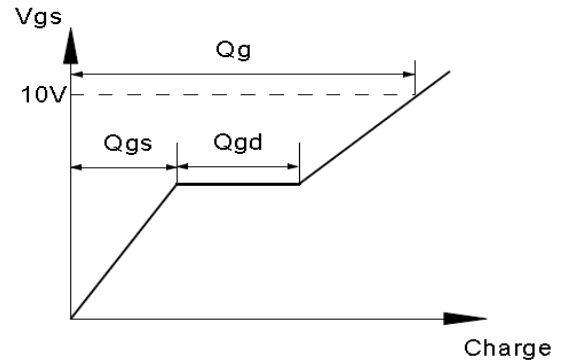
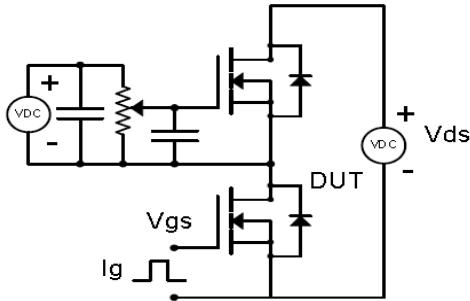


Fig 12: Max. Transient Thermal Impedance

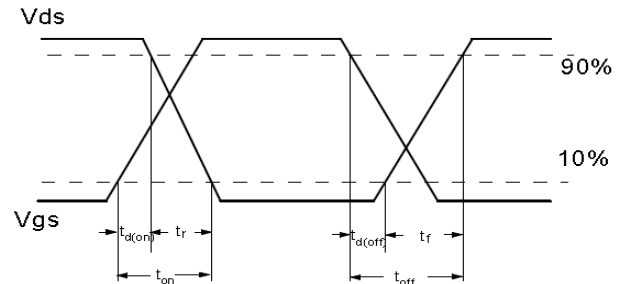
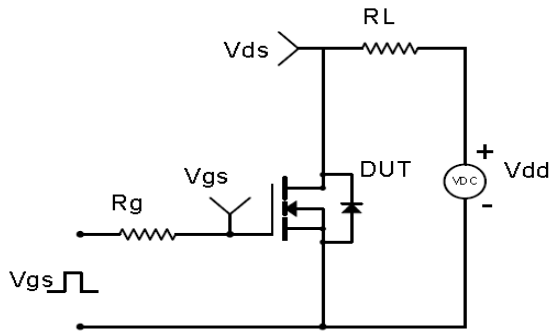


Test Circuit & Waveform

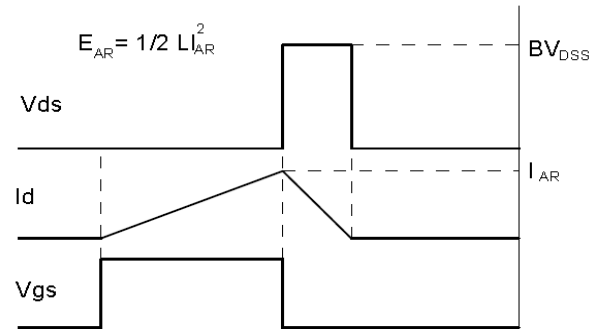
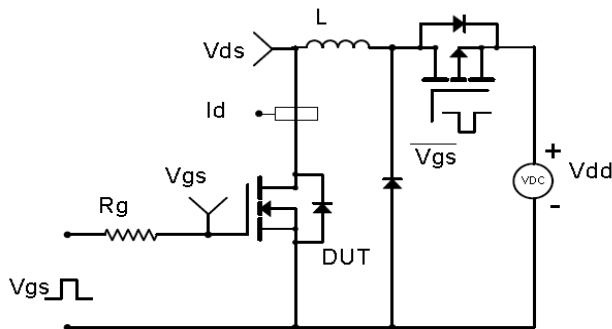
Gate Charge Test Circuit & Waveform



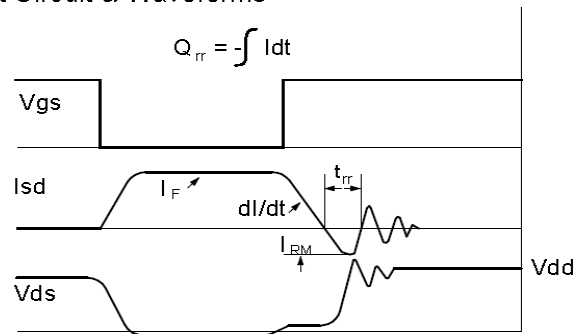
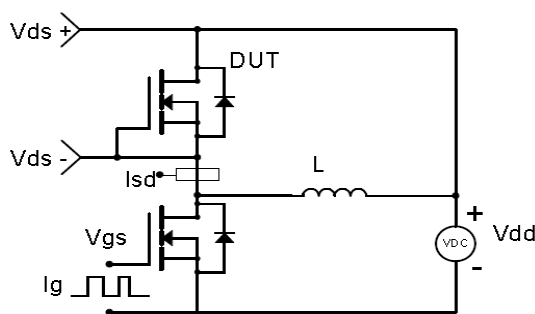
Resistive Switching Test Circuit & Waveforms

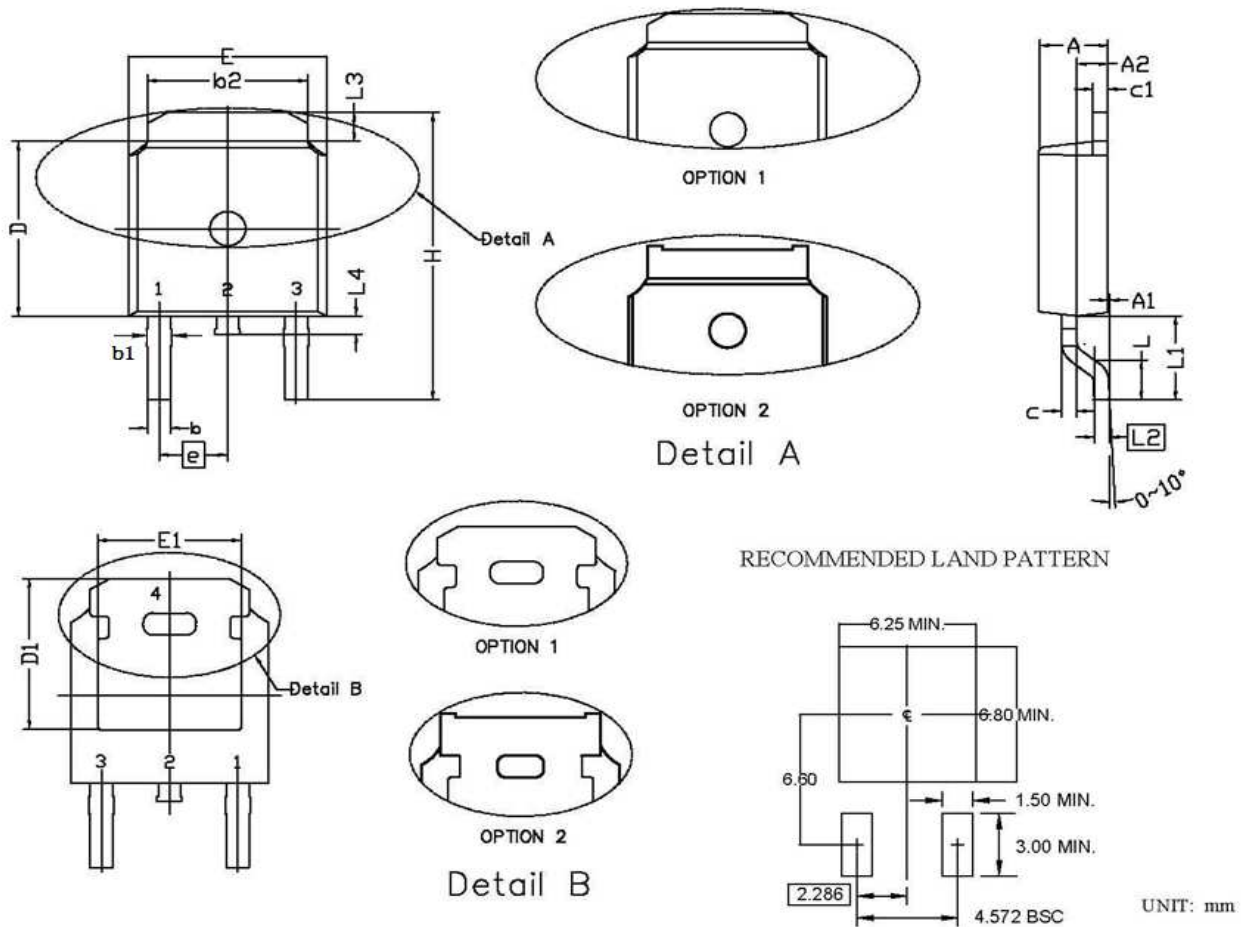


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: TO-252-3L


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.15	2.45	0.085	0.096
A1	0.00	0.15	0.000	0.006
A2	0.76	1.36	0.030	0.054
b	0.60	0.91	0.024	0.036
b1	0.65	1.15	0.026	0.045
b2	5.00	5.64	0.197	0.222
c	0.45	0.61	0.018	0.024
c1	0.36	0.66	0.014	0.026
D	5.80	6.30	0.228	0.248
D1	5.00	6.00	0.197	0.236
e	2.29 BSC.		0.090 BSC.	
E	6.30	6.90	0.248	0.272
E1	4.55	5.30	0.179	0.209
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L1	2.92 REF		0.115 REF	
L2	0.36	0.66	0.014	0.026
L3	0.72	1.35	0.028	0.053
L4	0.60	1.20	0.024	0.047

Revision History

Revision	Date	Major changes
1.0	2018-06-12	priliminary version.
2.0	2019-05-28	Supplement package outline info.

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qualified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

CRM(CQ) reserves the right to improve product design, function and reliability without notice.