

Description

N-channel Advanced Mode Power MOSFET

Features

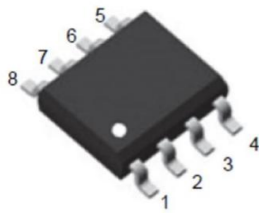
- 100V, 3.5A
 $R_{DS(ON)}$ Typ = 95m Ω @ V_{GS} = 10V
 $R_{DS(ON)}$ Typ = 135m Ω @ V_{GS} = 4.5V
- Advanced Split Gate Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free

Applications

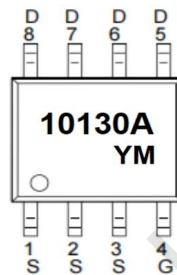
- DC/DC Converter
- LED Backlighting
- Motor Control



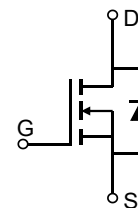
100% UIS TESTED!



SOP-8



Marking and Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

| Device Marking | Device | Outline | Package | Reel Size | Reel(pcs) | Per Carton (pcs) |
|----------------|--------------|---------|---------|-----------|-----------|------------------|
| 10130A | CRMPGL10130A | TAPING | SOP-8 | 13" | 4000 | 40000 |

Absolute Maximum Ratings (@ T_J = 25°C unless otherwise specified)

| Symbol | Parameter | Value | Units |
|-----------------|--|---------------------------|-------|
| V_{DS} | Drain-to-Source Voltage | 100 | V |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| I_D | Continuous Drain Current | $T_A = 25^\circ\text{C}$ | A |
| | | $T_A = 100^\circ\text{C}$ | |
| I_{DM} | Pulsed Drain Current ⁽¹⁾ | 14 | A |
| E_{AS} | Single Pulsed Avalanche Energy ⁽²⁾ | 7.2 | mJ |
| P_D | Power Dissipation | $T_A = 25^\circ\text{C}$ | W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient ⁽³⁾ | 40.3 | °C/W |
| T_J, T_{STG} | Junction & Storage Temperature Range | -55 to 150 | °C |



Electrical Characteristics (T_J = 25°C unless otherwise specified)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--|--|--|------|------|------|------|
| Off Characteristics | | | | | | |
| V _{(BR)DSS} | Drain-Source Breakdown Voltage | I _D = 250μA, V _{GS} = 0V | 100 | - | - | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 100V, V _{GS} = 0V | - | - | 1.0 | μA |
| I _{GSS} | Gate-Body Leakage Current | V _{DS} = 0V, V _{GS} = ±20V | - | - | ±100 | nA |
| On Characteristics | | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} = V _{GS} , I _D = 250μA | 1.0 | 1.65 | 2.5 | V |
| R _{DS(ON)} | Static Drain-Source ON-Resistance ⁽⁴⁾ | V _{GS} = 10V, I _D = 3A | - | 95 | 130 | mΩ |
| | | V _{GS} = 4.5V, I _D = 1A | - | 135 | 190 | mΩ |
| Dynamic Characteristics | | | | | | |
| C _{ISS} | Input Capacitance | V _{GS} = 0V, V _{DS} = 50V, f = 1MHz | - | 200 | - | pF |
| C _{OSS} | Output Capacitance | | - | 30 | - | pF |
| C _{RSS} | Reverse Transfer Capacitance | | - | 3 | - | pF |
| Q _g | Total Gate Charge | V _{GS} = 0 to 10V V _{DS} = 50V, I _D = 3A | - | 4 | - | nC |
| Q _{gs} | Gate Source Charge | | - | 0.9 | - | nC |
| Q _{gd} | Gate Drain("Miller") Charge | | - | 1.1 | - | nC |
| Switching Characteristics | | | | | | |
| t _{d(on)} | Turn-On DelayTime | V _{GS} = 10V, V _{DD} = 50V I _D = 3A, R _{GEN} = 3Ω | - | 13 | - | ns |
| t _r | Turn-On Rise Time | | - | 19 | - | ns |
| t _{d(off)} | Turn-Off DelayTime | | - | 20 | - | ns |
| t _f | Turn-Off Fall Time | | - | 28 | - | ns |
| Drain-Source Diode Characteristics and Max Ratings | | | | | | |
| I _S | Maximum Continuous Drain to Source Diode Forward Current | | - | - | 3.5 | A |
| I _{SM} | Maximum Pulsed Drain to Source Diode Forward Current | | - | - | 14 | A |
| V _{SD} | Drain to Source Diode Forward Voltage | V _{GS} = 0V, I _S = 3A | - | - | 1.2 | V |

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting T_J=25°C, V_{DD}=25V, V_G=10V, R_G=25ohm, L=0.4mH, I_{AS}=6A
 3. R_{θJA} is measured with the device mounted on a 1inch² pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%.

Typical Performance Characteristics

Figure 1: Output Characteristics

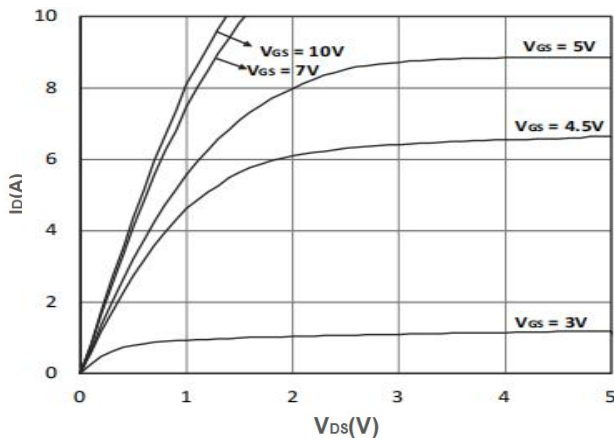


Figure 2: Typical Transfer Characteristics

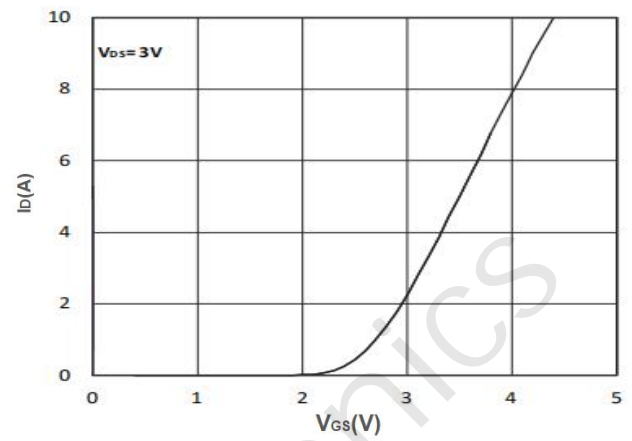


Figure 3: On-resistance vs. Drain Current

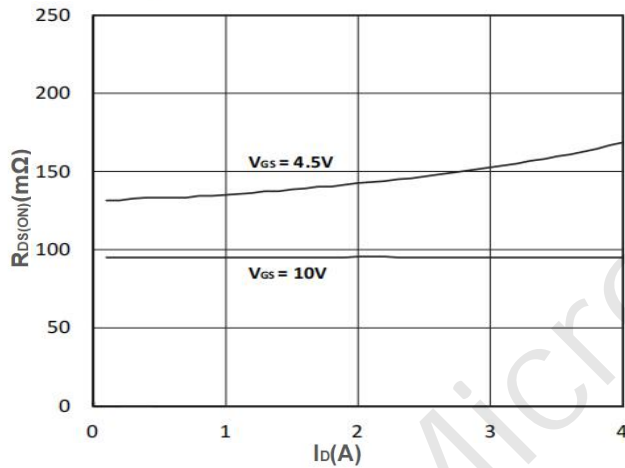


Figure 4: Body Diode Characteristics

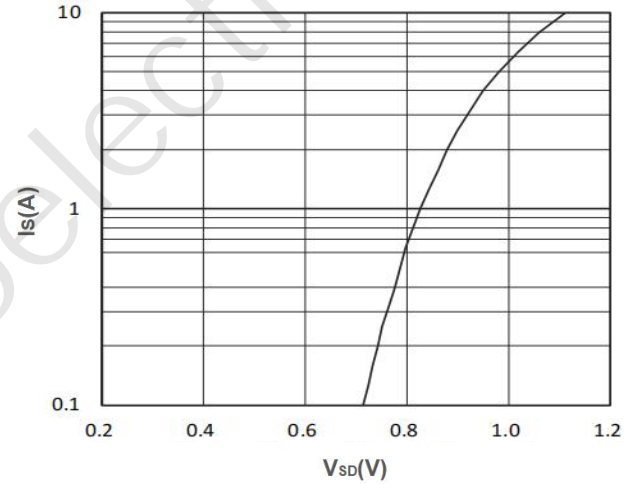


Figure 5: Gate Charge Characteristics

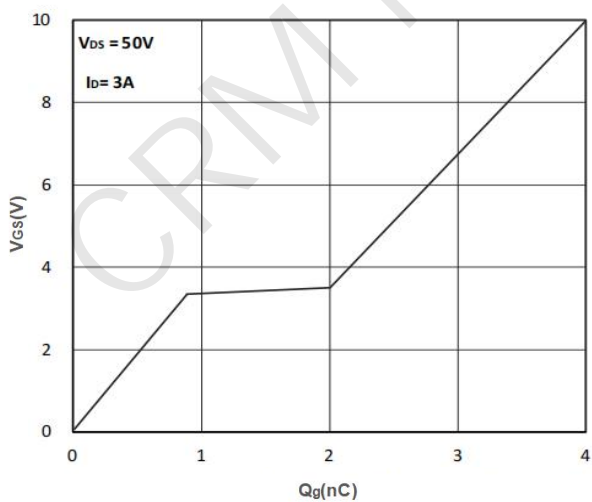
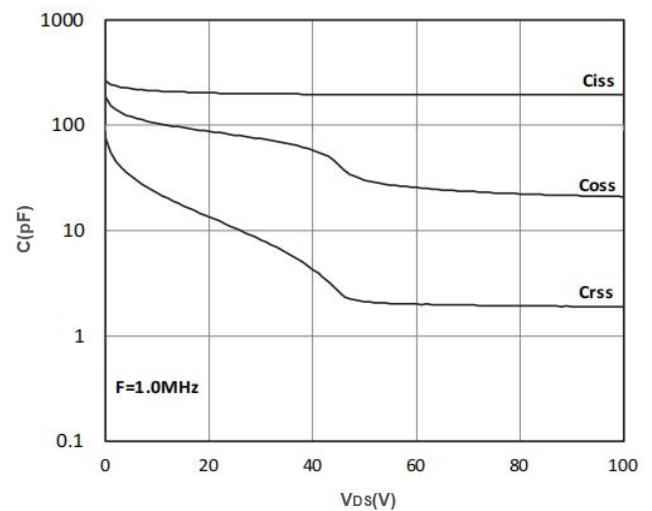


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

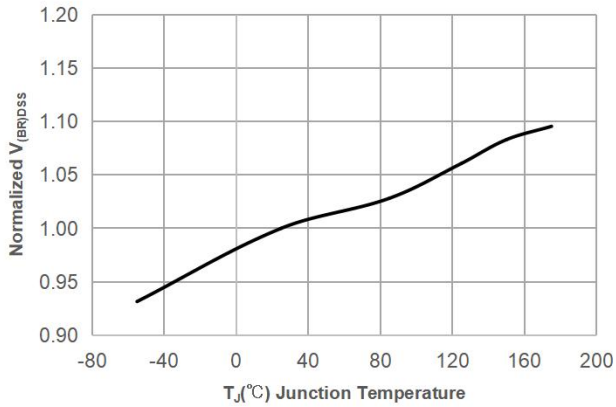


Figure 8: Normalized on Resistance vs. Junction Temperature

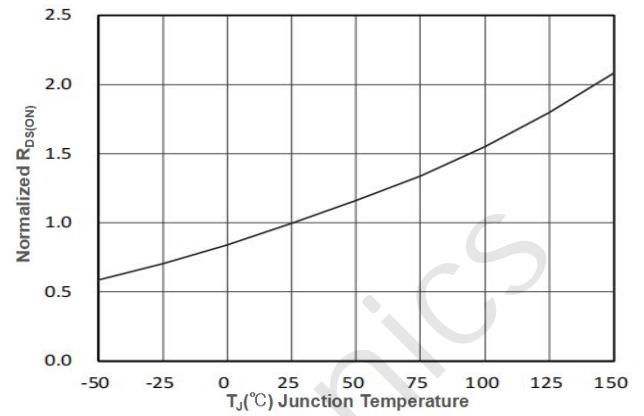


Figure 9: Maximum Safe Operating Area

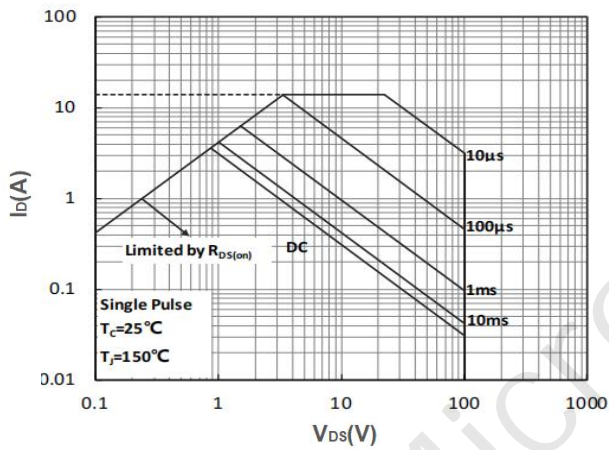


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

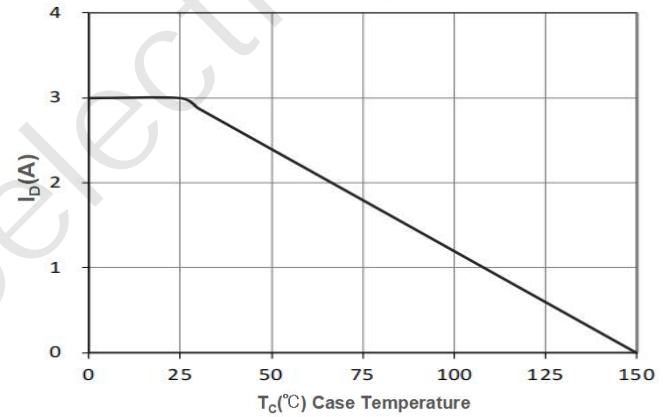


Figure 11: Normalized Maximum Transient Thermal Impedance

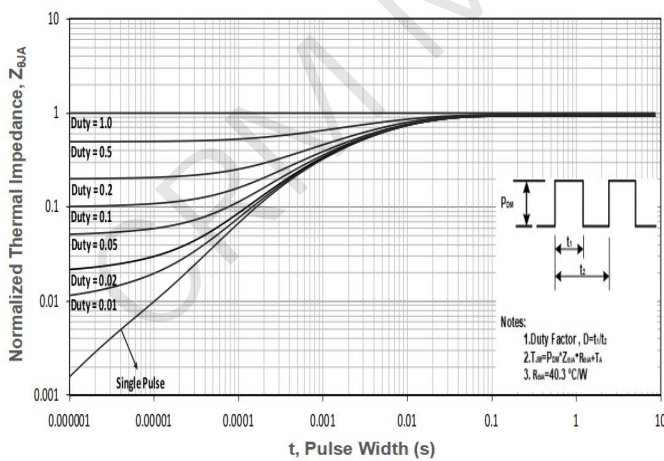
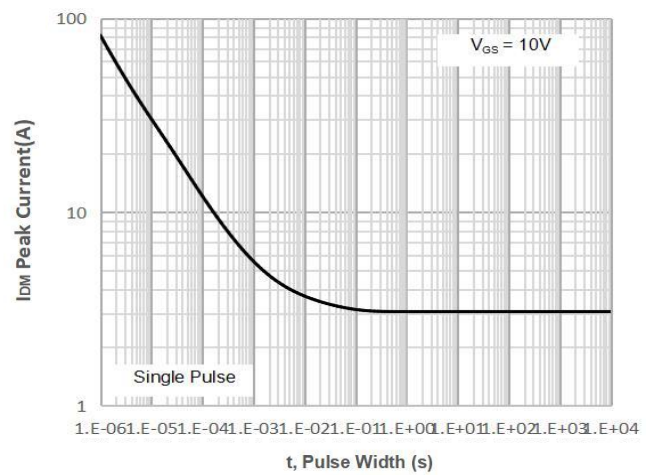


Figure 12: Peak Current Capacity



Test Circuit

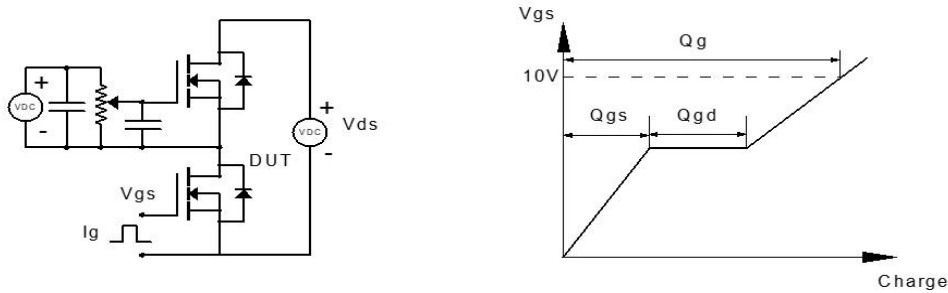


Figure 1: Gate Charge Test Circuit & Waveform

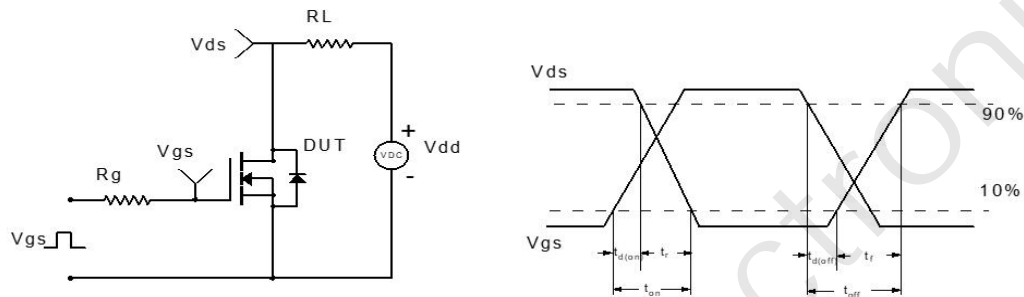


Figure 2: Resistive Switching Test Circuit & Waveform

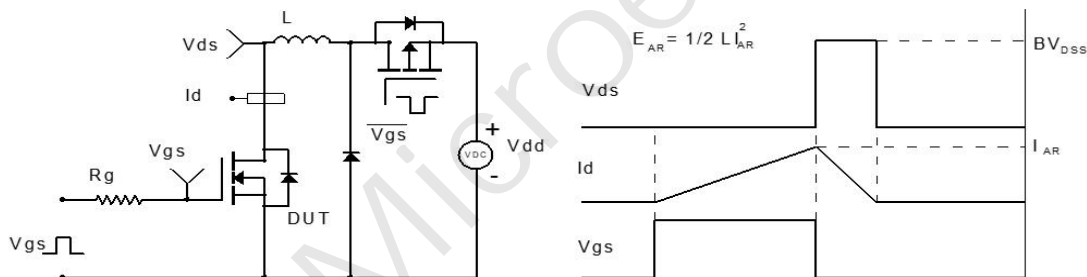


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

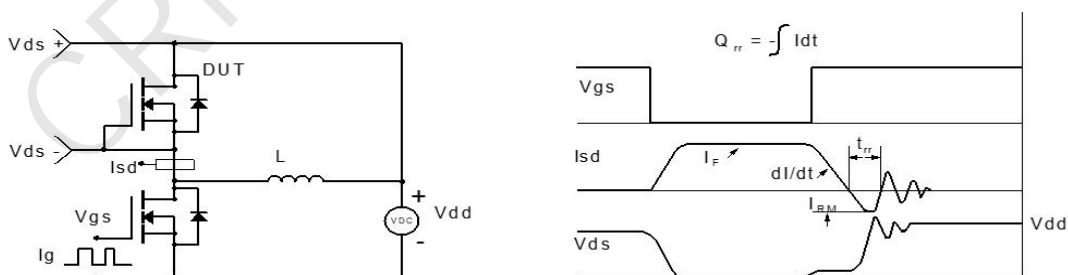
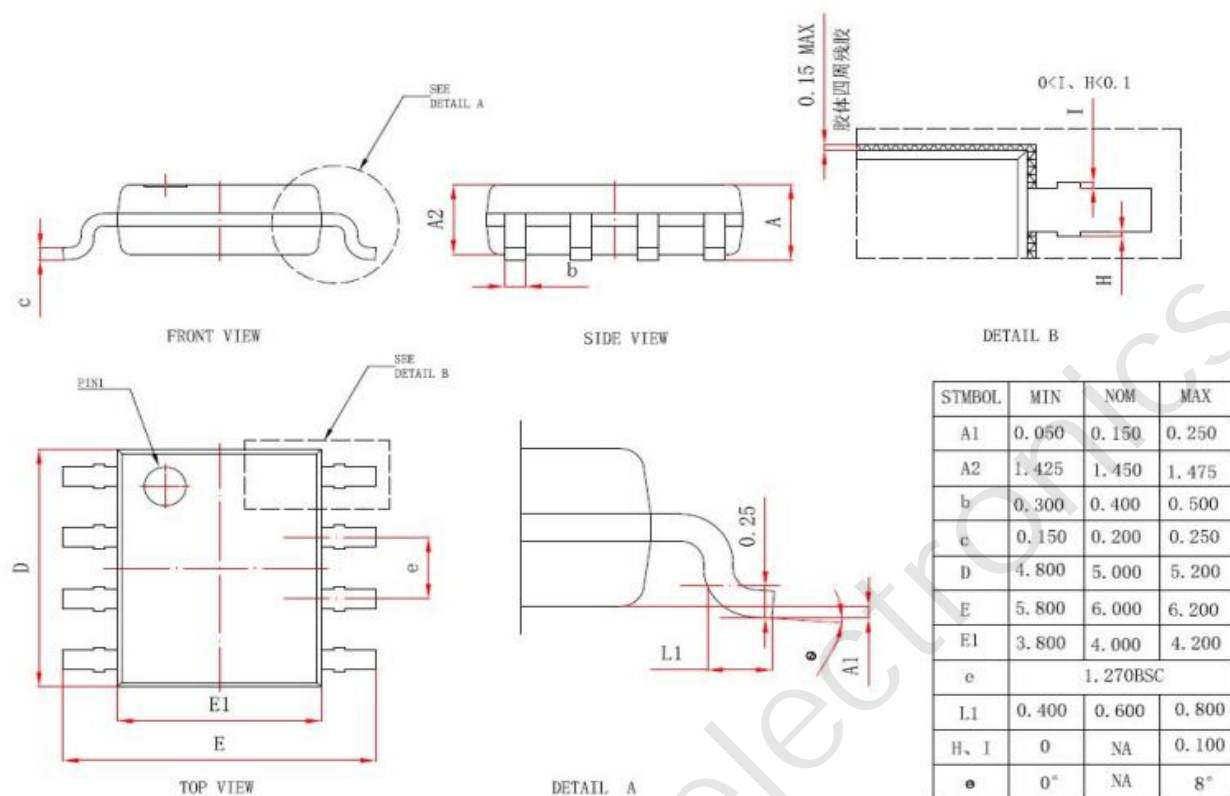


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(SOP-8)



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