CRD4525

2 x 15 W CS4525 Digital Amplifier Reference Design

Features

- Output Filters Optimized for 8 Ω Loads
- Delivers 15 W/Ch into 8 Ω at 10 % THD+N
- Single-Ended 2 V_{RMS} Stereo Analog Inputs
- Optical and Coaxial S/PDIF Inputs
- Flexible I/O Headers Provided
  - PCM Input Signal Interface
  - Auxiliary Serial Port Signal Interface
  - Delay Port Signal Interface
  - PWM Logic Level Signal Interface
- Optional CRD4412 Daughter-Card for Subwoofer Channel
  - Implements a 2.1 Configuration
- Demonstrates Recommended Layout and Grounding Arrangements
- +18 V Switching Mode Power Supply Included
- Windows® Compatible Software Interface
  - Easy and Intuitive Graphical Interface
  - Supports USB PC Connectivity

Description

The CRD4525 demonstrates the CS4525 digital PWM controller with integrated power stages. This reference design implements a two-channel amplifier which delivers 15 W per full-bridge channel into 8 Ω loads using a single +18 V supply. The CRD4525 is powered by an included 80 W switching mode power supply.

Standard RCA phono jacks are provided to easily interface analog input signals with the evaluation board. Optical and coaxial inputs are provided to interface with S/PDIF digital audio input signals.

The PWM audio power outputs are routed through an inductor/capacitor 2nd order low-pass filter (LPF) to remove high frequency components from the output signal, effectively converting it from digital to analog.

The Windows software provides a GUI to make configuration of the CRD4525 easy. The software communicates through the PC's USB port to configure the control port registers so that all features of the CS4525 can be evaluated.

ORDERING INFORMATION

CRD4525	CS4525 Reference Design

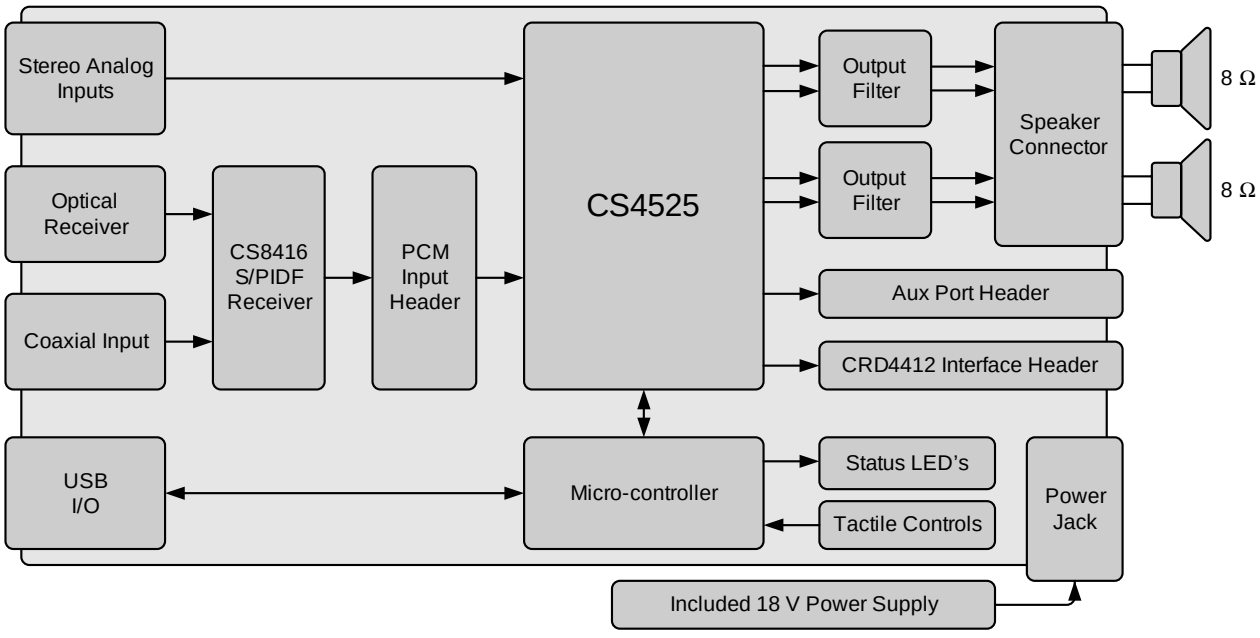

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. SYSTEM OVERVIEW

The CRD4525 reference design is an excellent means for evaluating the CS4525 30 W digital TV amplifier with integrated ADC. Analog and digital audio input signal interfaces are provided, an on-board microcontroller and USB PC interface is used for easily configuring the CS4525's internal registers, and a USB cable is included for use with the FlexGUI Windows configuration software.

The CRD4525 schematic set is shown in Figure 6 through Figure 9.

1.1 Power

A 80 W OEM switching-mode power supply is included to power the CRD4525. The power supply provides +18 V to the CS4525 power stages, and an on-board buck-converter and regulator provide power to the logic-level digital circuitry.

Power must be supplied from the included power supply to the CRD4525 via the power connector J3 (see the System Connections table on page 13).

1.2 CS4525 Digital TV Amplifier

A complete description of the CS4525 is included in the CS4525 product data sheet.

The required configuration settings of the CS4525 are achieved via its control port registers, accessible through the CS4525 tab of the Cirrus Logic FlexGUI software. A register-level configuration interface is provided on the Register Maps tab. See the "PC Software Control" section on page 6 for more information.

1.3 CS8416 Digital Audio Receiver

A complete description of the CS8416 receiver (Figure 8 on page 16) and a discussion of the digital audio interface are included in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream into PCM data and clocks for the CS4525. The CS8416 operates in master mode and can provide PCM data in Left-Justified, I²S, Right-Justified 16-bit, and Right-Justified 24-bit interface formats.

The most common operations of the CS8416 may be controlled via the S/PDIF Input Controls tab in the GUI software application. Advanced options are accessible through the CS8416 sub-tab on the Register Maps tab of the Cirrus Logic FlexGUI software.

1.4 System Clocking

A 24.576 MHz parallel resonant crystal, Y1, is available to provide a clock source to the CS4525. The crystal is mounted in pin sockets, allowing easy removal or replacement. Alternatively, an input SYS_CLK signal can be provided on pin 3 of the serial audio input header (J2).

1.5 External Data Headers

The evaluation board has been designed to allow interfacing with external systems via the headers J2, J4, and J11. Figure 6 shows the headers' electrical connections.

The 12-pin, 3 column header, J2, provides access to the CS4525's serial audio input and SYS_CLK input signals. Place shunts across the SCLK, LRCK, and SDIN pins located in the columns labeled "S/PDIF" to connect to the on-board S/PDIF digital interface receiver circuitry. To use an external digital audio source, simply remove the shunts and connect a ribbon across the SCLK, LRCK, and SDIN pins located in the columns labeled "EXT SAI". A single ground column for the ribbon cable's ground connection is provided to maintain signal integrity.

The 8-pin, 2 column header, J11, provides access to the CS4525's auxiliary serial audio port output signals, as well as the SYS_CLK output signal. A single ground column is provided to maintain signal integrity.

The 20-pin, 2 column header, J4, is included to interface with a CRD4412 card. Various signals, power, and ground are presented on this header. Notably, this header includes the DLY_SDOUT and DLY_SDIN signals which can be used to interface with an external delay device or DSP. See Figure 6 for complete connectivity information.

1.6 Analog Inputs

RCA connectors supply the CS4525 analog inputs through single-ended passive circuits with one pole of input filtering. A resistive attenuation network is implemented to allow 2 V_{RMS} input levels to be supplied to the CRD4525. Refer to the CS4525 data sheet for the maximum input signal level at the analog input pins.

1.7 Speaker Outputs

The CS4525 power outputs are configured for stereo parallel full-bridge operation. The outputs are routed through a 2nd order low-pass filter to remove high-frequency content from the output signals and then presented at the speaker wire crimp terminals (J5). The output filters are optimized for 8 Ω speaker loads. The speaker terminal connections are shown below.

Figure 1. Speaker Terminal Configuration

1.8 PC Interface

A USB connection is provided to facilitate software control of the CS4525's internal registers.

A graphical user interface is available for the CRD4525 to allow easy manipulation of the CS4525's internal registers. See the CS4525 datasheet for complete internal register descriptions.

To enable the CRD4525, simply connect the supplied USB cable from an available USB port on a PC to the USB connector (J37) and launch the Cirrus Logic FlexGUI software.

Refer to "PC Software Control" on page 6 for a description of the Graphical User Interface (GUI).

1.9 Tactile Controls

A volume control knob (S1), reset button (S2), and mute button (S3) are included for stand-alone operation of the CRD4525. These controls are currently unsupported by the firmware running on the CRD4525, and the PC interface must be used in order to operate the board.

The CRD4525 firmware is field-upgradable through the Cirrus Logic FlexGUI application. When available, a new version of the FlexGUI (downloadable at www.cirrus.com/msasoftware) will automatically upgrade the firmware upon its first launch.

1.10 CRD4412 Interface

A keyed connector (J4) is included to interface with the CRD4412. The CRD4525 can be used with or without a CRD4412 attached.

Without the CRD4412 attached, the CRD4525 configures itself for 2-channel stereo full-bridge operation. When the CRD4412 is attached, the CS4525 enables its bass manager and routes the LFE channel to the CRD4412 which amplifies the signal in mono parallel full-bridge mode. Together, the CRD4525 and CRD4412 implement a 2.1 configuration.

The CRD4412 must be inserted and removed while power is not applied to the CRD4525.

2. PC SOFTWARE CONTROL

The CRD4525 is designed for use with the Microsoft Windows based FlexGUI graphical user interface. This interface provides comprehensive control over the CS4525's internal registers via a PC's USB port.

The FlexGUI software may be downloaded and installed from www.cirrus.com/msasoftware.

Step-by-step instructions for using the FlexGUI are provided as follows:

1. Download and install the FlexGUI software from www.cirrus.com/msasoftware.
2. Connect the CRD4525 to a host PC using the supplied USB cable.
3. Connect load speakers to the speaker output terminals.
4. Connect an input source to the S/PDIF or analog input connectors.
5. Plug the input to the included +18 V power supply into an available power outlet.
6. Plug the output of the included +18 V power supply into the power input connector on the CRD4525.
7. Launch the FlexGUI software. *The GUI will load and be displayed.*
8. Un-check the "Power Down CS4525" check box to power-up the device. *In this state, the CRD4525 will convert and amplify the content present on the optical S/PDIF input.*

2.1 CS4525 Main Controls Tab

The CS4525 Main Controls tab provides a high-level intuitive interface to many of the basic configuration options of the CS4525. Use this tab to access functions such as power-down, input source, and volume control.

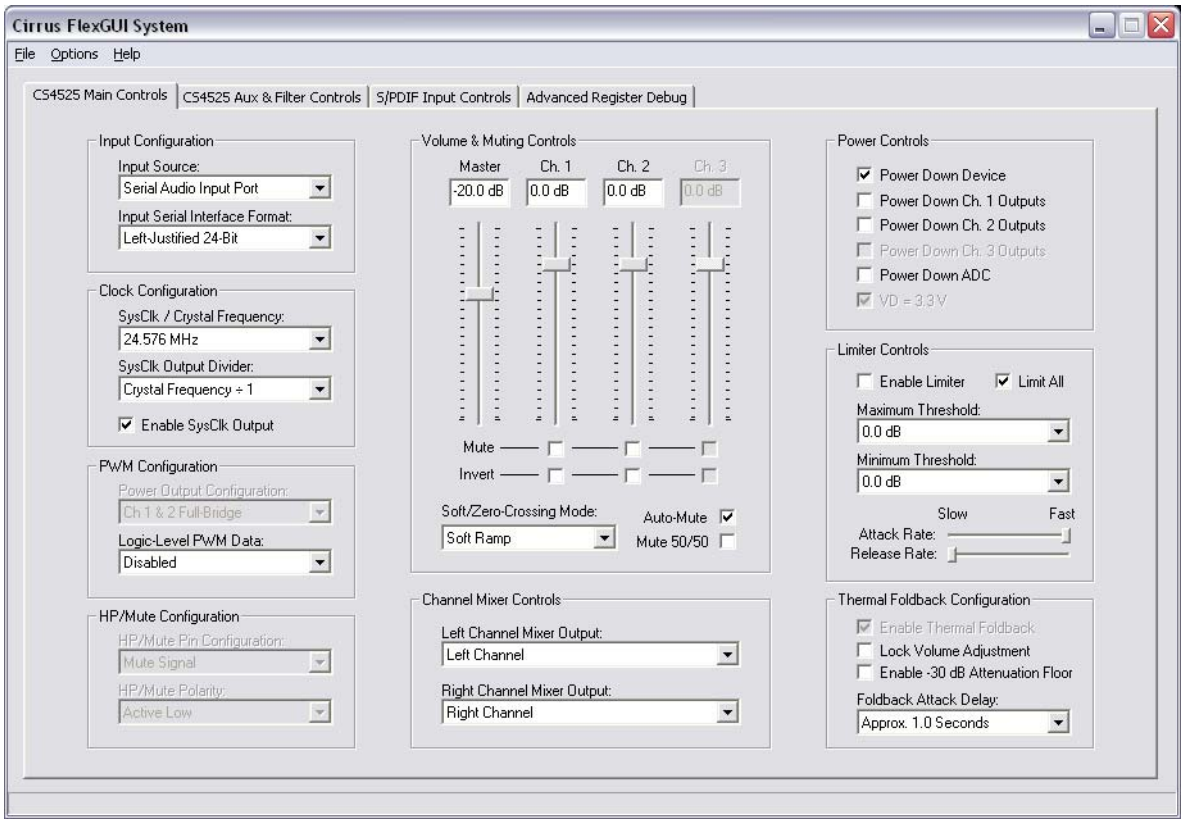

Figure 2. CS4525 Main Controls Tab

2.2 CS4525 Aux & Filter Controls Tab

The CS4525 Aux & Filter Controls tab provides a high-level intuitive interface to many of the advanced configuration options of the CS4525. Use this tab to configure the auxiliary port, the internal filters, and advanced PWM adjustments. Control over device and board resets is also provided.

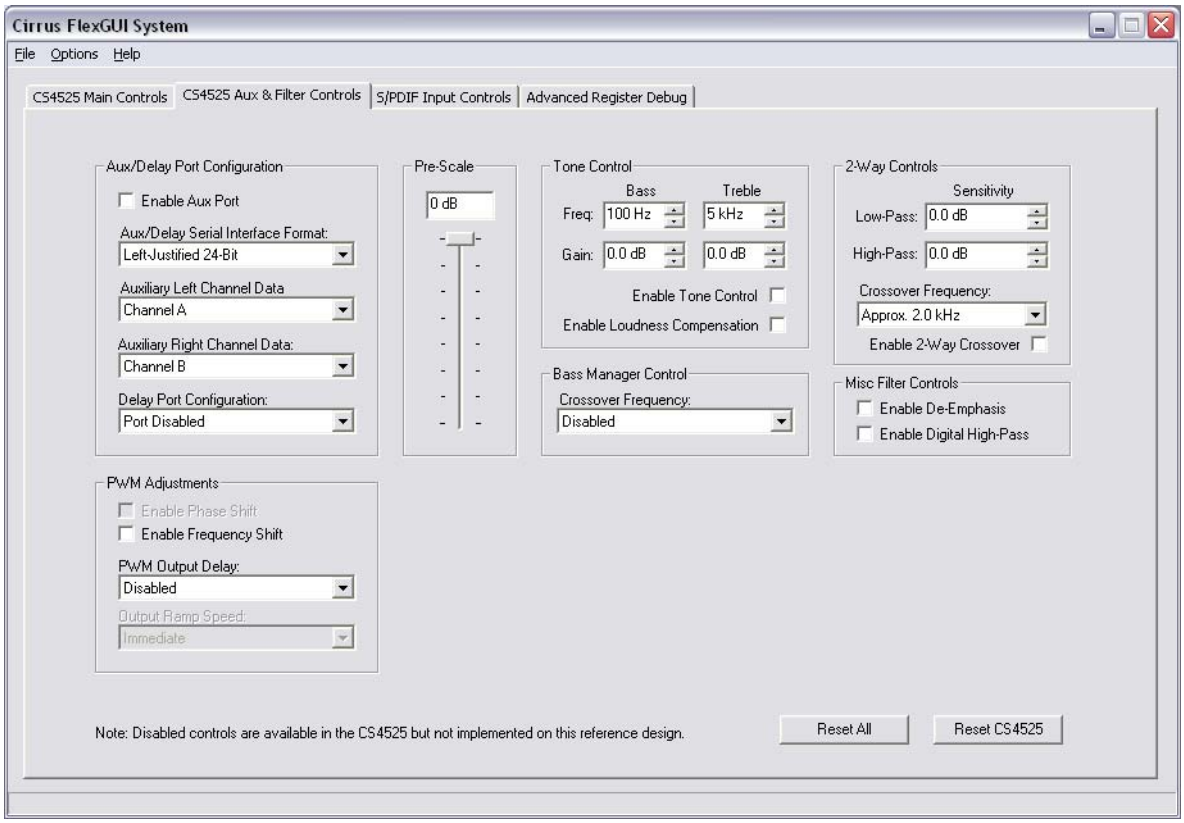

Figure 3. CS4525 Aux & Filter Controls Tab

2.3 S/PDIF Input Controls Tab

When the CRD4525 is configured to make use of the CS8416 S/PDIF receiver, the devices must be configured for proper operation. The S/PDIF Input Controls tab provides a high-level intuitive interface to the most common configuration options of the CS8416.

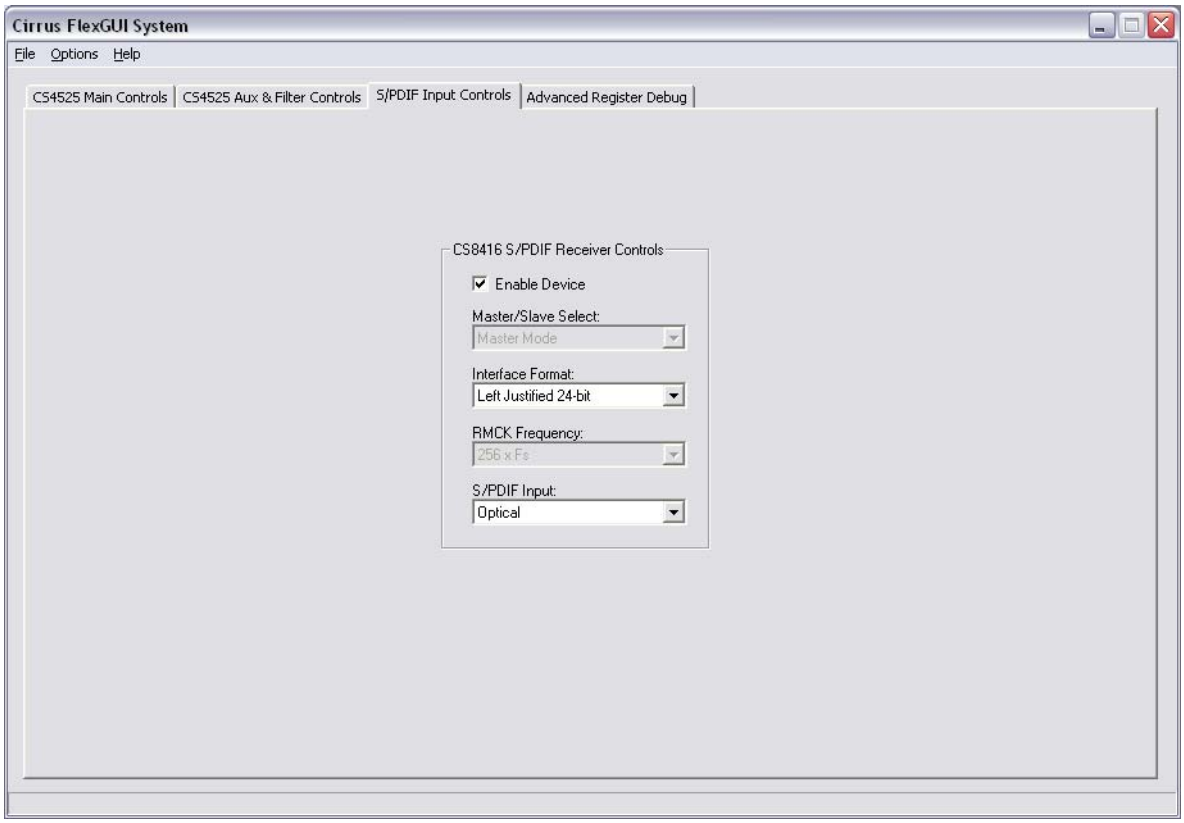

Figure 4. S/PDIF Input Controls Tab

2.4 Register Maps Tab

The Register Maps tab provides an easy register-level interface to the on-board devices. Register values can be modified on a bit-wise or byte-wise basis. To modify a single bit, first select the register by clicking its position in the register matrix, then click the appropriate push-button for the desired bit. To modify an entire register, simply enter the register's new value directly into the register matrix.

Within the Register Maps tab, the CS4525 tab is used to access the CS4525's internal registers, and the CS8416 tab is used to access the CS8416's internal registers.

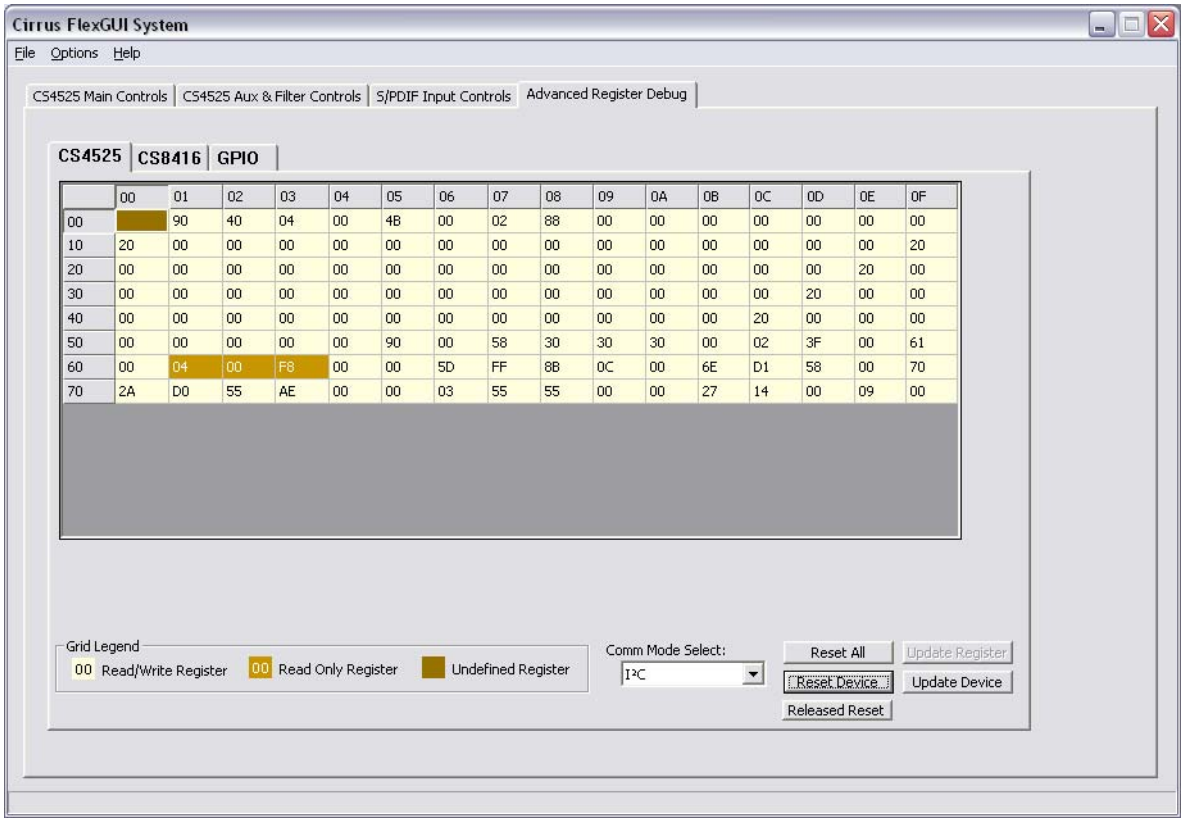

Figure 5. Register Maps Tab

2.5 Pre-Configured Script Files

Pre-configured script files are provided with the CRD4525 to allow easy initial board bring-up. The board configurations stored within these files are described in sections 2.5.1 - 2.5.3.

2.5.1 Analog In

Using the pre-configured script file named “Analog In.fgs”, an analog input signal applied to the analog inputs of the CRD4525 will be used as the CS4525’s input source. The device will be powered up with no internal processing active and the master volume control set to -20 dB.

2.5.2 Optical SPDIF In

Using the pre-configured script file named “Optical SPDIF In.fgs”, the optical S/PDIF input signal will be received by the CS8416 S/PDIF receiver. The CS8416 PCM output signals will be used as the CS4525’s input source. The device will be powered up with no internal processing active and the master volume control set to -20 dB.

2.5.3 Coaxial SPDIF In

Using the pre-configured script file named “Coaxial SPDIF In.fgs”, the coaxial S/PDIF input signal will be received by the CS8416 S/PDIF receiver. The CS8416 PCM output signals will be used as the CS4525’s input source. The device will be powered up with no internal processing active and the master volume control set to -20 dB.

3. GROUNDING AND POWER SUPPLY DECOUPLING

The CS4525 requires careful attention to power supply and grounding arrangements to optimize performance and heat dissipation and minimize radiated emissions. Figure 10 on page 18 shows the component placement. Figure 11 on page 19 shows the top layout. Figure 14 on page 22 shows the bottom layout. The decoupling capacitors are located as close to the CS4525 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

3.1 Power Supply Decoupling

Proper power supply decoupling is one key to maximizing the performance of a Class-D amplifier. Because the design uses an open loop output stage, noise on the power supply rail will be coupled to the output. Careful decoupling of the power stage supply rails is essential. Figure 10 on page 18 demonstrates good decoupling capacitor placement. Notice that the small value decoupling capacitors are placed as close as physically possible to the power pins of the CS4525. The ground side of the capacitors is connected directly to top side ground plane, which is also used by the power supply return pins. This keeps the high frequency current loop small to minimize power supply variations and EMI. 470 µF electrolytic capacitors are also located in close proximity to the power supply pins to supply the current locally for each channel. These are not required to be expensive low ESR capacitors. General purpose electrolytic capacitors that are specified to handle the ripple current can be used.

3.2 Electromagnetic Interference (EMI)

The EMI challenges that face a maker of Class-D amplifiers are largely the same challenges that have been faced by the switch mode power supply industry for many years. The numerous EMI consulting firms that have arisen and the many books that have been written on the subject indicate the scope of potential problems and available solutions. They should be considered a resource - most makers of switch mode equipment would benefit from developing a working relationship with a qualified EMI lab and from bringing their experience to bear on design issues, preferably early in the design process.

This reference design is a board level solution which is meant to control emissions by minimizing and suppressing them at the source in contrast to containing them in an enclosure.

The EMI requirements for an amplifier have added dimensions beyond those imposed on power supplies. Audio amplifiers are usually located in close proximity to radio receivers, particularly AM receivers which are notoriously sensitive to interference. Amplifiers also need to operate with speaker leads of unpredictable length and construction which make it possible for any high frequency currents that appear on the outputs to generate nuisance emissions. The criteria for judging successful EMI control is not as well defined for amplifier design as it is for power supplies. While the techniques of measuring conducted and radiated emissions are similar for both types of products, power supplies have a number of clearly defined (and legally imposed) thresholds that are useful mainly as guidelines when testing amplifiers.

3.2.1 Suppression of EMI at the Source

Several techniques are used in the circuit design and board layout to minimize high frequency fields in the immediate vicinity of the high power components. Specific techniques include the following:

- As mentioned in Section 3.1, effective power supply decoupling of high frequency currents, and minimizing the loop area of the decoupling loop is one aspect of minimizing EMI.
- Each output of the CS4525 includes “snubbing” components. For example, OUT1 and OUT2 include snubber components R24 (20 Ω) and C23 (330 pF). These components serve to damp ringing on the switching outputs in the 30-50 MHz range. The snubbing components should be as close as practical to the output pins to maximize their effectiveness.

- A separate ground plane with a solid electrical connection to the chassis and which surrounds the speaker output connector should be implemented. This allows the speaker outputs to be RF decoupled to the chassis just before they exit the chassis from the speaker connector.
- Make use of source termination resistors on all digital signals whose traces are longer than about 25 mm.

It is extremely critical that the layout of the power amplifier section of the CRD4525 be copied as exactly as possible to assure best RF/EMI performance.

4. SYSTEM CONNECTIONS & JUMPERS

Connector Name	Reference Designator	Signal Direction	Connector Function
Power In	J3	Input	Power connector. +18V.
Left In Right In	J1 J10	Input	Analog input to CS4525.
S/PIDF Input	J6	Input	Coaxial digital input to CS8416
S/PIDF Input	J7	Input	Optical digital input to CS8416
Speaker Connector	J5	Output	Analog output from CS4525.
USB	J8	Input/Output	USB connection to PC for software control.
C2	J9	Input/Output	Connection for programming the on-board microcontroller (U3).

Table 1. System Connections

Control Name	Reference Designator	Tactile Control Function
Master Volume	S1	Tactile controls not currently supported. See “Tactile Controls” on page 4.
Board Reset	S2	
Mute	S3	

Table 2. On-Board Tactile Controls

Connector Name	Reference Designator	Header Function
DSP IN	J2	When shunts are placed across column 1 and 2, the CS4525 serial audio input data is sourced by the CS8416. To use external serial audio input data, connect the PCM source cable across column 2 and 3.
DSP OUT	J11	Auxiliary serial audio data from the CS4525.
CRD4412 I/F	J4	Connection to CRD4412 daughter card.

Table 3. System Headers

5. CRD SCHEMATICS

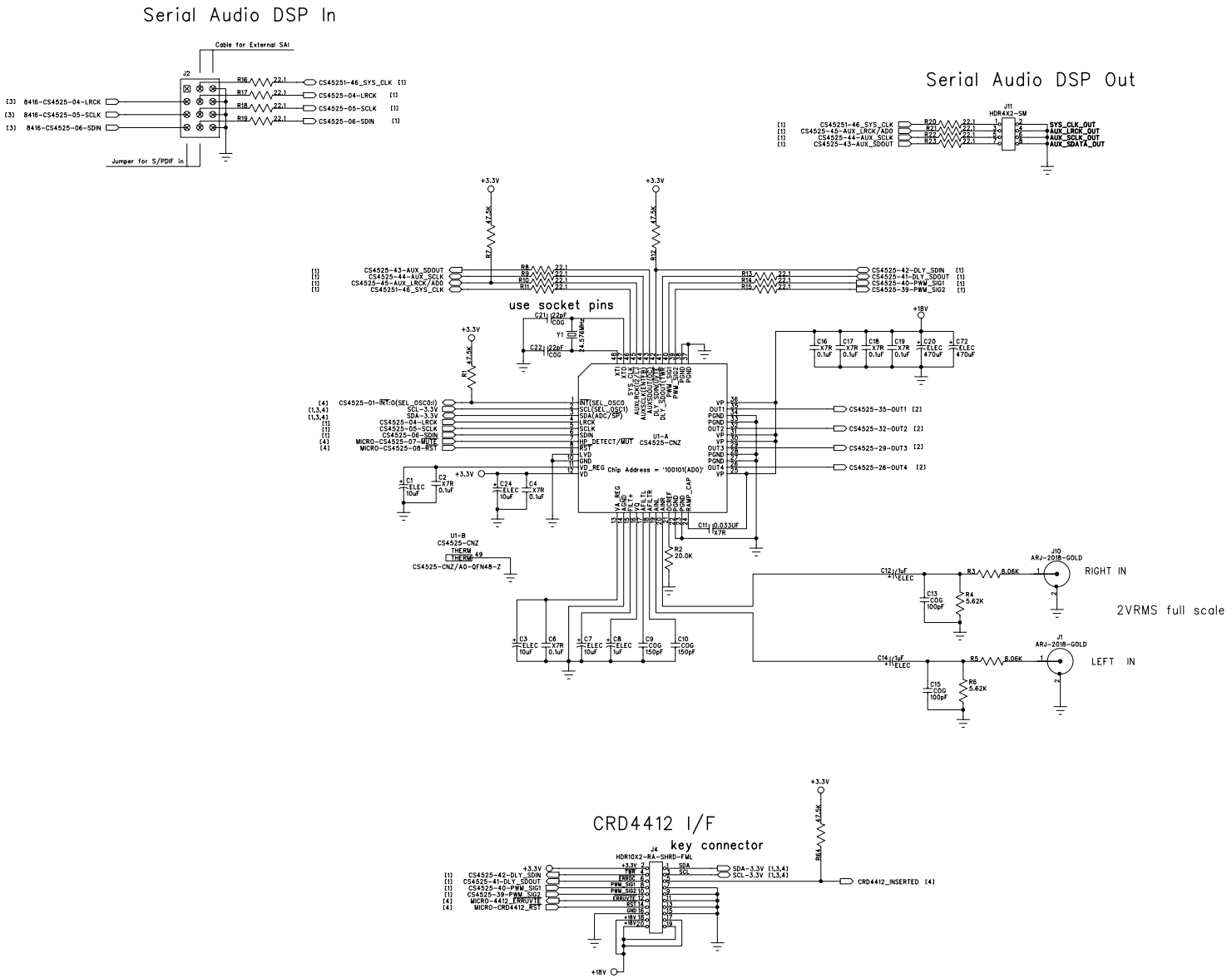

Figure 6. CS4525 - Schematic Page 1

Output filters optimized for 8-ohm loads.

FULL BRIDGE OUTPUT 1

FULL BRIDGE OUTPUT 2

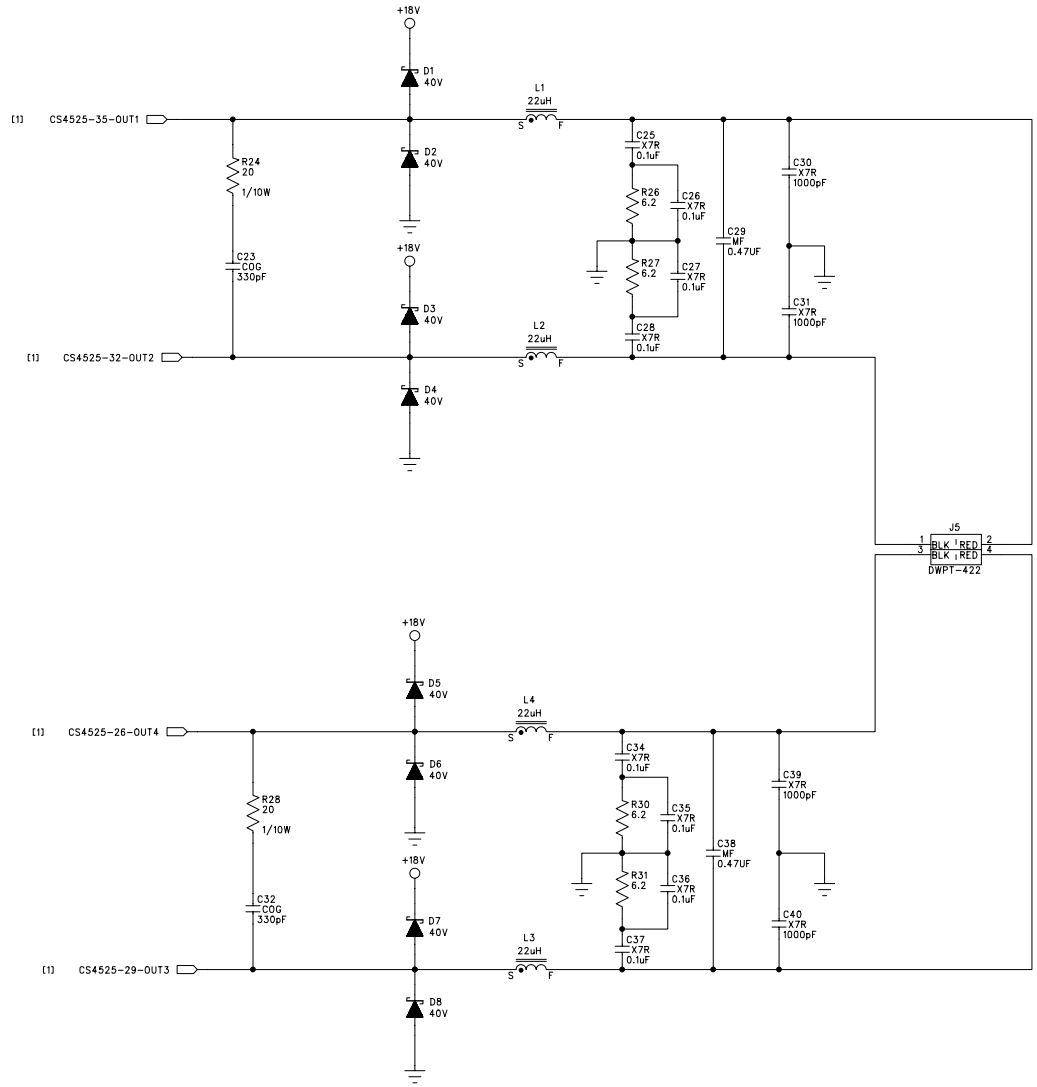

Figure 7. Power Outputs - Schematic Page 2

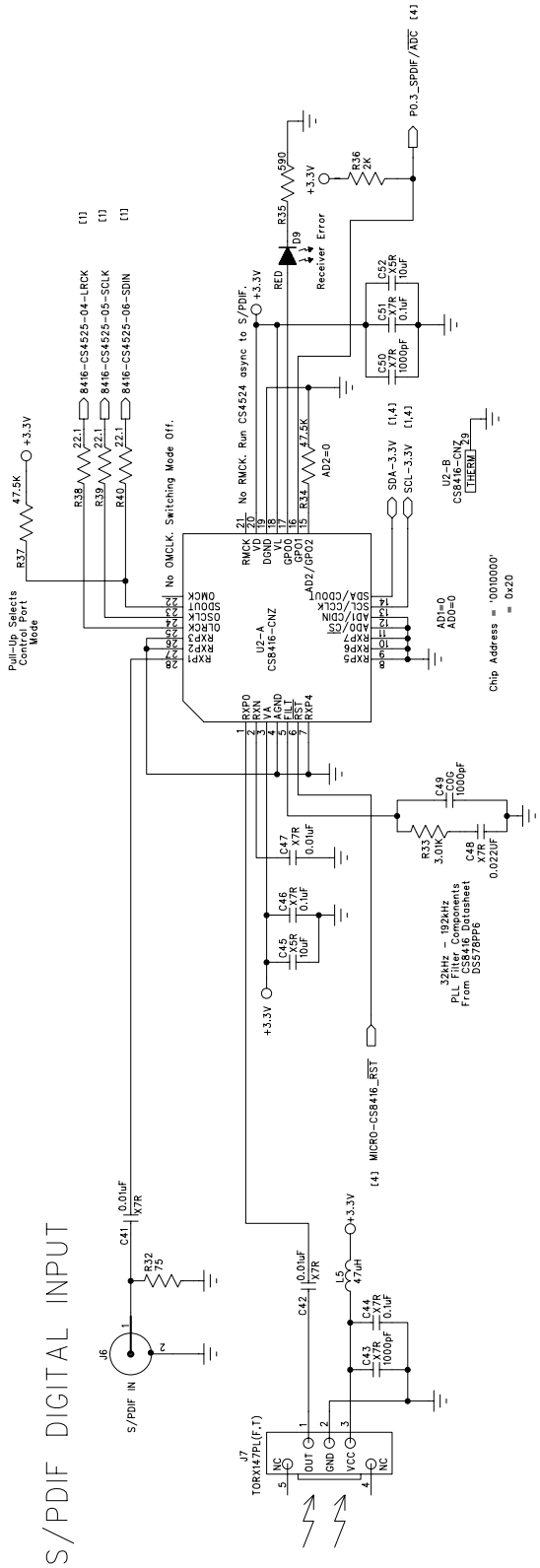

Figure 8. S/PDIF Digital Audio Input - Schematic Page 3

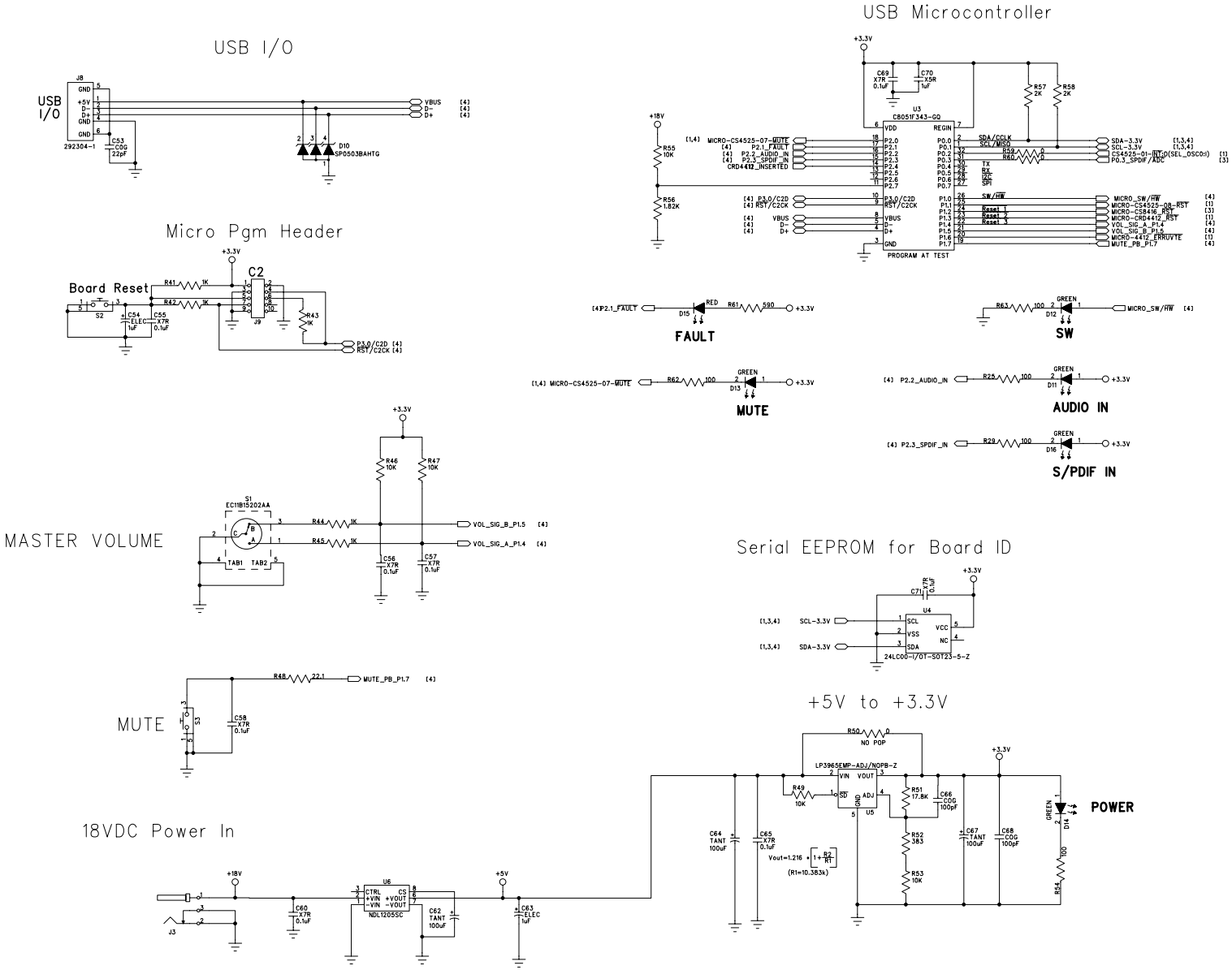

Figure 9. Serial Control / Power - Schematic Page 4

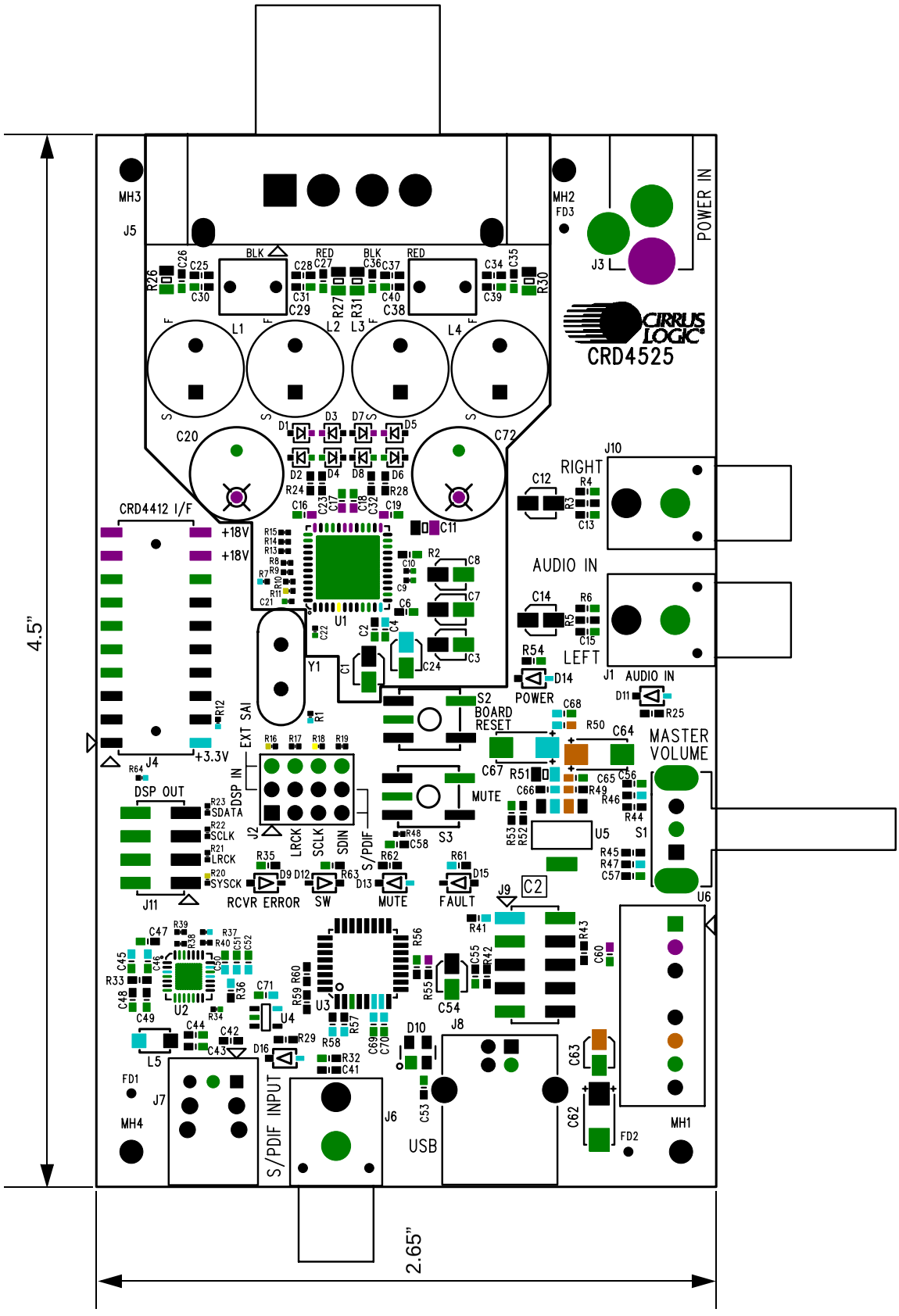

Figure 10. Silkscreen Top

6. CRD LAYOUT

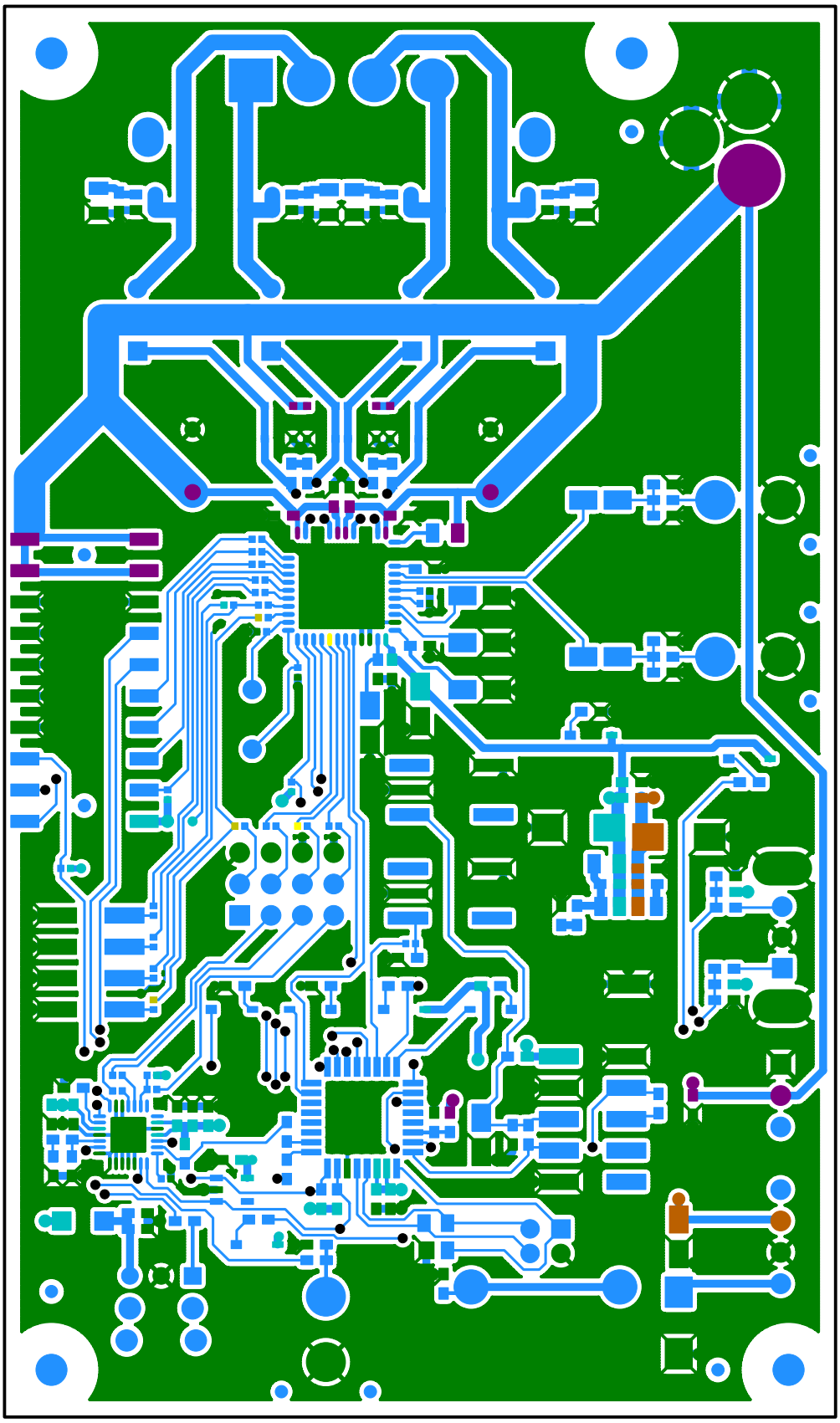

Figure 11. Topside Copper Layer

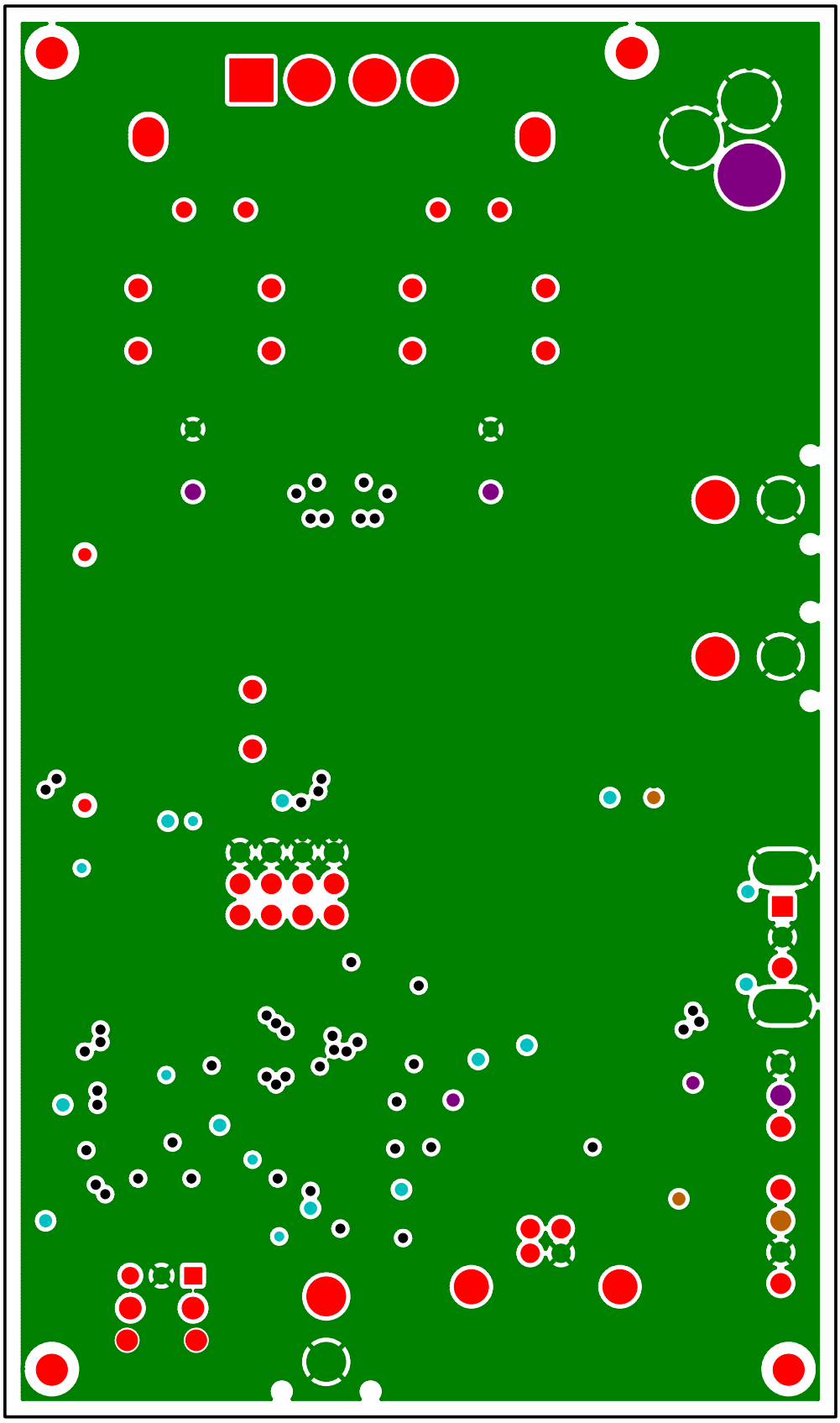

Figure 12. Inner Copper Layer 1

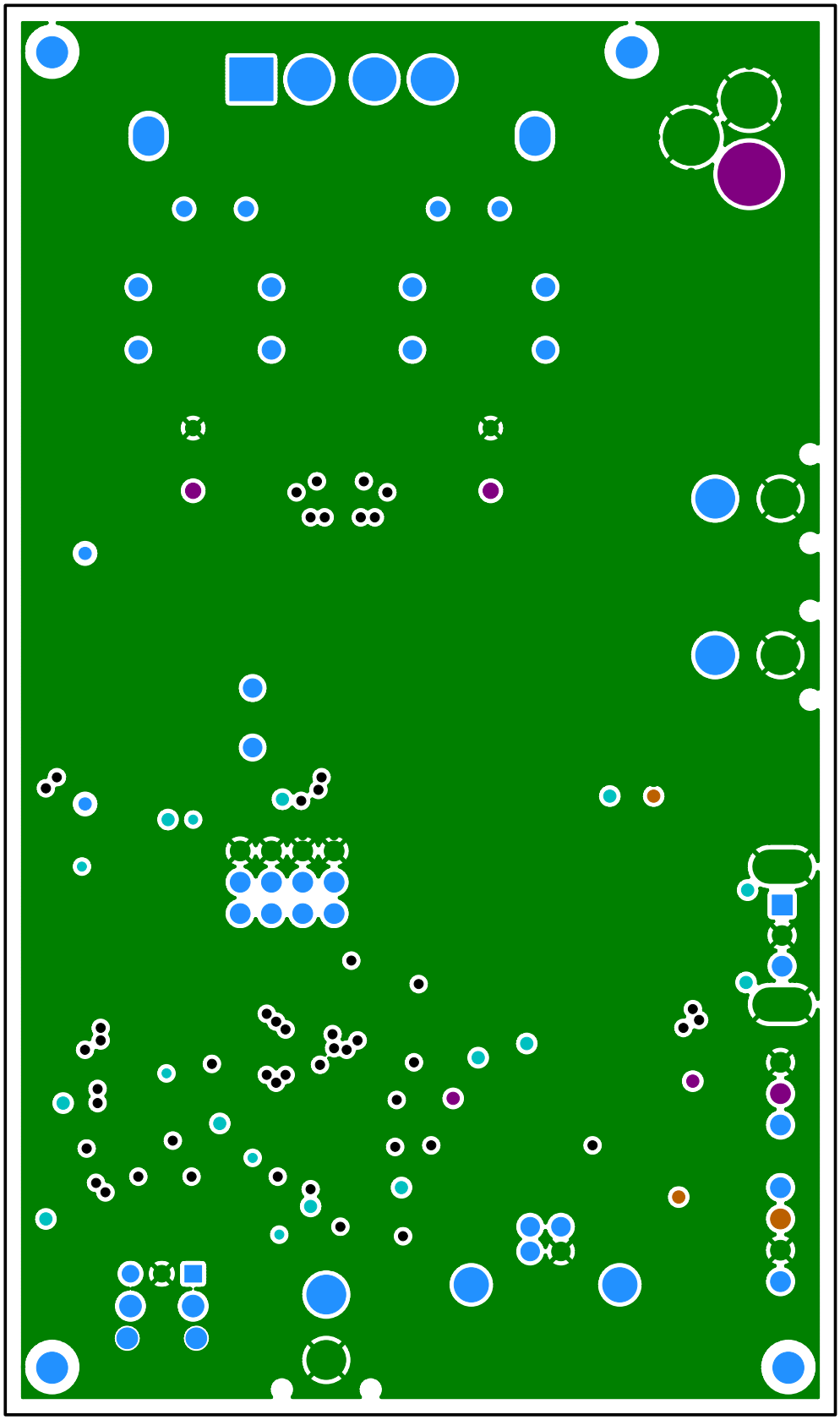

Figure 13. Inner Copper Layer 2

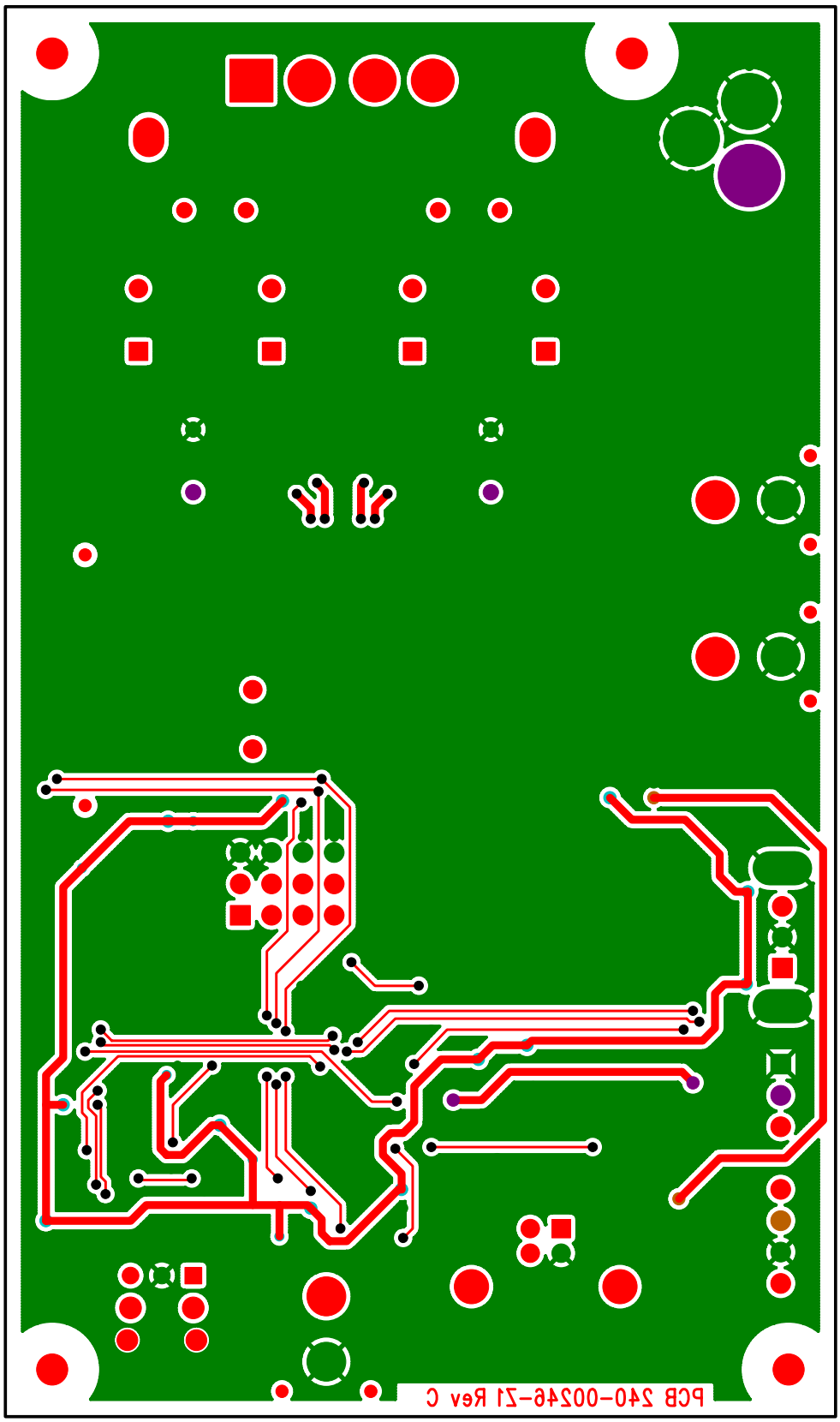

Figure 14. Bottomside Copper Layer

7. REVISION HISTORY

Release	Changes
RD1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest to you, go to www.cirrus.com.