CRD4202-1

CrystalClear™ AC '97 Six Channel CNR Audio Reference Design

Features

- Six Channel Analog Audio Outputs
- Headphone Sense using GPIO
- CS4202 codec and two CS4334 DACs
- 20-bit D to A conversion (DAC)
- 18-bit A to D conversion (ADC)
- S/PDIF (IEC-958) optical digital output
- Complete suite of Analog I/O connections:
  - Line, Mic, CD, Video, Modem, and Aux Inputs
  - Modem, Headphone, Line Front, Line Rear and Line Center/Sub-Woofer Outputs
- 2-layer low cost PC board
- Meets Intel ® AC '97 revision 2.2
- Exceeds Microsoft's® PC 2001 audio performance requirements.

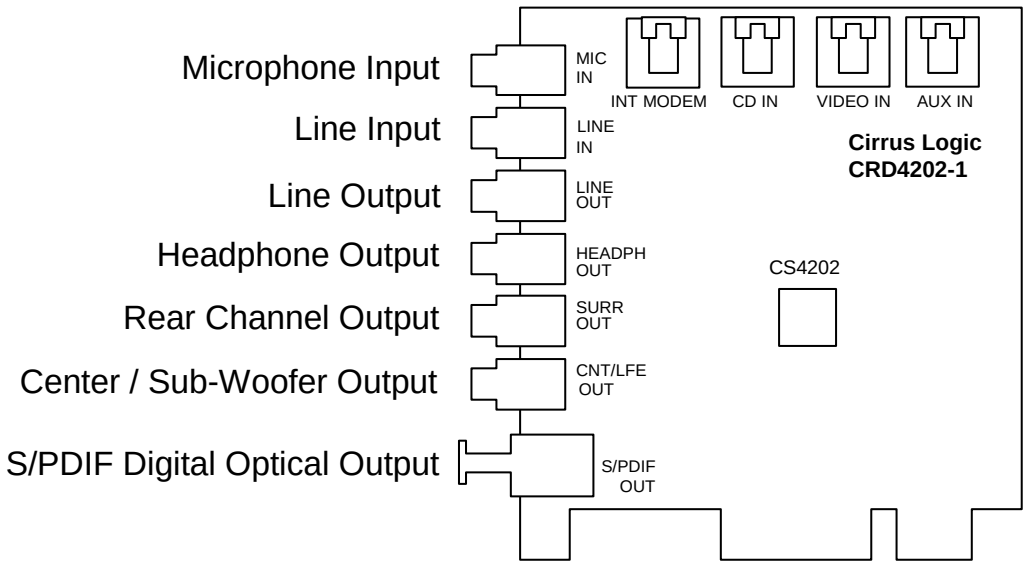
Description

The CRD4202-1 reference design features six channel analog audio outputs, an optical S/PDIF digital output, and Communication and Networking Riser (CNR) interface. This design uses the CS4202 audio codec which has several advanced features including a built-in headphone amplifier, simultaneous six channel analog and S/PDIF optical digital output, GPIO for headphone detection, and up to 30 dB of internal microphone boost.

The CRD4202-1 reference design is available by ordering the *CMK4202-1* manufacturing kit. This kit includes the CRD4202-1 board, a full set of schematic design files (OrCAD® format), PCB job files (PADS® ASCII), PCB artwork files, and bill of materials. This reference design offers significant cost savings over competing solutions and can be easily modified to meet your specific design goals.

ORDERING INFO

CMK4202-1 (Manufacturing Kit)



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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JAN '02
DS549RD1A1

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1. GENERAL INFORMATION

The CRD4202-1 reference design is a CNR card that features six channel CD quality analog and S/PDIF digital audio outputs. The card includes a CS4202 AC '97 audio codec and two CS4334 24-bit serial stereo DACs. This combination gives the CRD4202-1 a rich feature set and industry leading audio performance.

The CS4202 audio codec includes a stereo 20-bit DAC, a stereo 18-bit ADC, and a very flexible analog audio mixer. The serial data outputs are paired with two CS4334 DACs to provide four additional channels of analog audio. The CS4202 also features three stereo pairs of line level analog inputs, a microphone input, and a stereo pseudo-differential CD input. The input signals can be routed to the ADC for recording or mixed together for recording and direct playback. The CS4202 has internal registers that are used to control its various features such as volume levels, audio muting, and signal routing. The CS4202 maintains high audio quality and exceeds the Microsoft® PC 2001 audio performance specifications.

The CS4202 audio codec communicates to the audio controller across the CNR interface through the AC-Link. The AC-Link is a 5-wire serial digital interface that transfers digital audio between the two devices and also sends commands from the audio controller to the CS4202 registers. For more information on the AC-Link, see the Intel® AC '97 revision 2.2 specification.

2. SCHEMATIC DESCRIPTION

The block diagram in Figure 1 illustrates the interconnections between the schematic pages found at the end of this document. Sections 2.1 through 2.8 describe the circuitry contained in these schematics.

2.1 CS4202 Audio Codec

The CS4202 audio codec is shown in Figure 2. The analog input signals to the CS4202 originate from the inputs in Figure 3, while the analog outputs are shown in Figure 4 and Figure 5. AFLT1 and AFLT2 (pins 29, 30) require 1000 pF NPO/COG capacitors connected to analog ground. These capacitors provide a single pole lowpass filter to the inputs of the CS4202 ADC. No other input filtering is required.

The AC-Link may require series termination resistors to prevent reflections. These are normally placed as close as possible to the transmitting end of the AC-Link signal. The CS4202 SDATA_IN (pin 8) and BIT_CLK (pin 6) outputs have 47 Ω series termination resistors.

The CS4202 is powered by separate analog and digital power supplies, each with their own respective grounds. The AGND symbols refer to analog ground and DGND symbols refer to digital ground. For best results, connect the grounds together at a single point with a 0.050 inch trace underneath the CS4202. Each power pin requires an individual decoupling capacitor. These decoupling capacitors are placed as close as possible to their respective pins. The CS4202 audio codec uses a 0.1 µF ceramic capacitor for each of the 3.3 V digital and 5 V analog supply pins.

2.2 Analog Inputs

The LINE_IN, VIDEO_IN, and AUX_IN stereo inputs in Figure 3 are connected to 6 dB voltage dividers and AC-coupled to the CS4202 with 1 µF capacitors to minimize low frequency roll-off. The voltage divider allows input signal levels of up to 2 Vrms. The 6 dB dividers are for PC 99 compatibility and not required for PC 2001 compliance.

The microphone input is AC-coupled using a 1 µF capacitor to minimize low frequency roll-off. The microphone circuit provides low voltage phantom power for electret microphones. Phantom power is derived from the +5 V analog supply and provides a maximum of 4.2 V under no load and a minimum of 2.0 V under a 0.8 mA load, as required by PC 2001 specifications.

The CS4202 features a pseudo-differential CD input that minimizes common mode noise and interference. Each CD signal acts as one side of the differential input and CD_COM acts as the other side. CD_COM is used as the common return path for both the left and right channels.

2.3 Center, LFE, and Surround Outputs

The audio outputs in Figure 4 drive the rear speakers (surround), center speaker (CNT), and subwoofer (LFE) in six channel applications. These four outputs are driven digitally from the CS4202 through two serial output ports and converted to analog audio through two high-performance CS4334 24-bit stereo DACs.

2.4 Front Channel and Headphone Outputs

Figure 5 details the Headphone and Line Output circuits. The Line Outputs are the main analog outputs in a two channel system, and become the Front Outputs in a six channel audio system.

The CS4202 has a built in headphone amplifier on pins 39 and 41. These outputs are capable of driving headphones with impedances as low as 32 Ω. The headphone outputs are AC-coupled through 220 µF capacitors. These large capacitor values create excellent low frequency response even under 32 Ω loads.

2.5 S/PDIF Optical Output

The S/PDIF (IEC-958) digital output shown in Figure 6 is compatible with digital inputs on consumer devices such as Mini Disk recorders and consumer stereo receivers. The S/PDIF output operates at a fixed sampling frequency of 48 kHz. It uses an industry standard Toshiba TOTX-173 digital optical TOSLINK transmitter.

2.6 CNR Connector and EEPROM

The CNR connector is shown in Figure 7. CNR is a motherboard interface that supports audio, modem, and LAN subsystems. CNR applications are targeted at OEMs, system manufacturers, and system integrators who wish take advantage of physically separating their audio, modem, or LAN circuitry from the PC motherboard. CNR accomplishes this without the additional cost associated with the interface circuitry required for a PCI bus add-in card.

The CRD4202-1 uses the AC-Link, SMBus, and power supply pins. The SMBus signals are connected to an AT24C02 EEPROM to provide Plug-and-Play functionality for the CNR card. The EEPROM holds the Subsystem Vendor ID and Subsystem ID. It also contains other information for implementing a Plug-and-Play CNR card. For additional information on the CNR design specifications, programming utilities, and information on programming the EEPROM, visit the Intel® Communications and Network Riser (CNR) homepage at http://developer.intel.com/technology/cnr/.

2.7 Auto Demotion Circuit

The configuration of the codec on the CRD4202-1 will always be set as the primary audio codec. However, it can automatically demote to secondary in the presence of a motherboard codec when R54 is changed to 100 kΩ (Figure 9). This feature is in accordance with the *AC '97 Codec Disable and Demotion Rules.*

2.8 Phase Locked Loop (Optional)

The internal ADCs, DACs, and AC-Link operate at a fixed 48k Hz rate. The CS4202 is clocked by a 24.576 MHz (±50 PPM) crystal. Footprint Y2 is for an optional surface mounted clock oscillator for use with the Phase Locked Loop (PLL) feature of the CS4202. Figure 8 shows the population options for implementing the PLL that will convert various clock rates to the required 24.576 MHz operating speed.

2.9 Component Selection

Great attention was given to the particular components used on the CRD4202-1 board with cost, per-

formance, and package selection as the most important factors. Listed are some of the guidelines used in the selection of components:

- No components smaller than 0805 SMT package.
- Only single package passive components. No resistor packs. This reduces the risk of crosstalk between analog audio signals.
- All components except connectors are in surface mount packages.

2.10 EMI Components

Optional capacitors or inductors may be included to help the board meet EMI compliance tests, such as FCC Part 15. Choose these component values according to individual requirements.

3. GROUNDING AND LAYOUT

The component layout and signal routing of the CRD4202-1 provide a good model for developing new CNR add-in card designs.

3.1 Partitioned Voltage and Ground Planes

It is critical for good audio performance to separate digital and analog sections to prevent digital noise from affecting the performance of the analog circuits. The analog section of the CRD4202-1 is physically isolated from the digital section with a 0.10 inch partition. Partitioning is defined as the absence of copper on all PCB signal layers. The analog and digital sections have their own separate ground planes. All analog components, power traces, and signal traces are routed over the analog ground plane. Digital components, power traces, and signal traces are not allowed to crossover into the analog section.

The CS4202 audio codec is placed at the transition point between the analog and digital ground planes. The codec pins are grouped into analog and digital sections to help facilitate printed circuit board layout. *The analog and digital ground planes must be tied together externally for the CS4202 to maintain proper voltage references.* For best results, the two ground planes are tied together with a single 0.050 inch trace under the CS4202 near its digital ground pins.

Data converters are generally susceptible to noise on the crystal pins. In order to reduce noise from coupling onto these pins, the area around the 24.576 MHz crystal and its signal traces are filled with copper on the top and bottom of the PCB and attached to digital ground.

A separate chassis ground provides a noise-free reference point for all of the EMI suppression components. The chassis ground plane is connected to the analog ground plane at the external jacks.

3.2 AC-Link

According to the AC '97 revision 2.2 specification, the AC-Link signals can have a maximum capacitance (including traces, connectors, and circuitry) of 47.5 pF on BIT CLK and SDATA_IN (assuming a single codec). If this capacitance is exceeded, timing violations may occur and cause the system to malfunction. In order to avoid adding excessive capacitance, do not add any EMI capacitors to ground on any of the AC-Link lines. In addition, keep the trace length of the AC-Link as short as possible. *Keeping the AC-Link trace length under 8 inches is strongly recommend.*

3.3 CS4202 Layout Notes

Refer to the *CS4202 Data Sheet* for analog and digital partitioning guidelines and bypass capacitor placement. Pay special attention to the location of bypass capacitors on REFFLT, AFLT1, AFLT2, and the placement of the power supply capacitors.

4. REFERENCES

1) Intel®, Audio Codec '97 Component Specification, Revision 2.2, September, 2000.
http://developer.intel.com/ial/scalableplatforms/audio/index.htm/

2) Intel®, CNR Specification, Revision 1.1, October 18, 2000.
http://developer.intel.com/technology/cnr/

3) Cirrus Logic, CS4202 Audio Codec '97 Data Sheet
http://www.cirrus.com/products

4) Steve Harris, Clif Sanchez, Personal Computer Audio Quality Measurements, Version 1.0
http://www.cirrus.com/pubs/meas100.pdf

5) Microsoft, PC Design Guidelines,
http://www.microsoft.com/hwdev/desguid.htm

6) M. Montrose, Printed Circuit Board Design Techniques for EMC Compliance (2nd edition), IEEE Press, New York: 2000.

4.1 ADDENDUM

- Schematic drawings
- Layout drawings
- Bill of materials

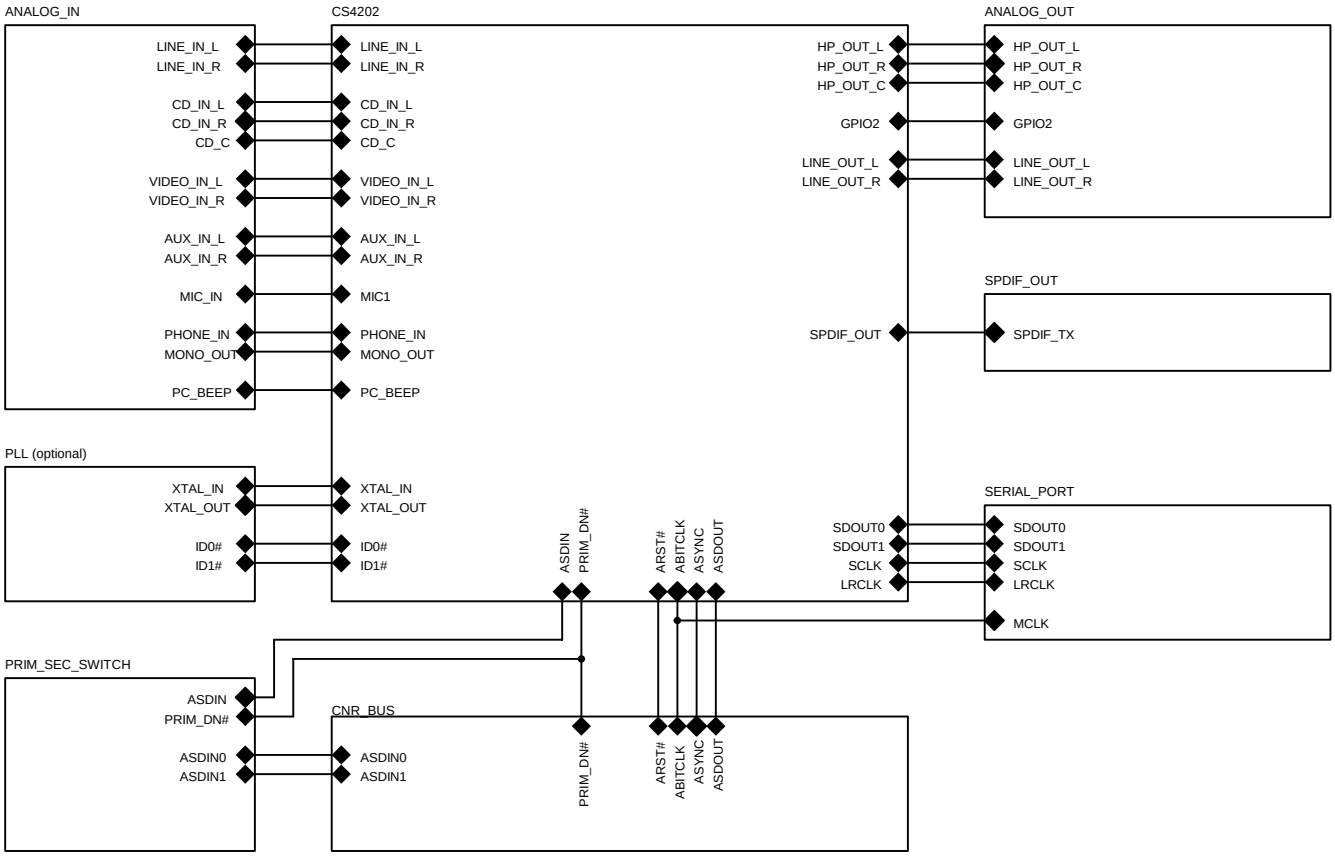


Figure 1. Block Diagram

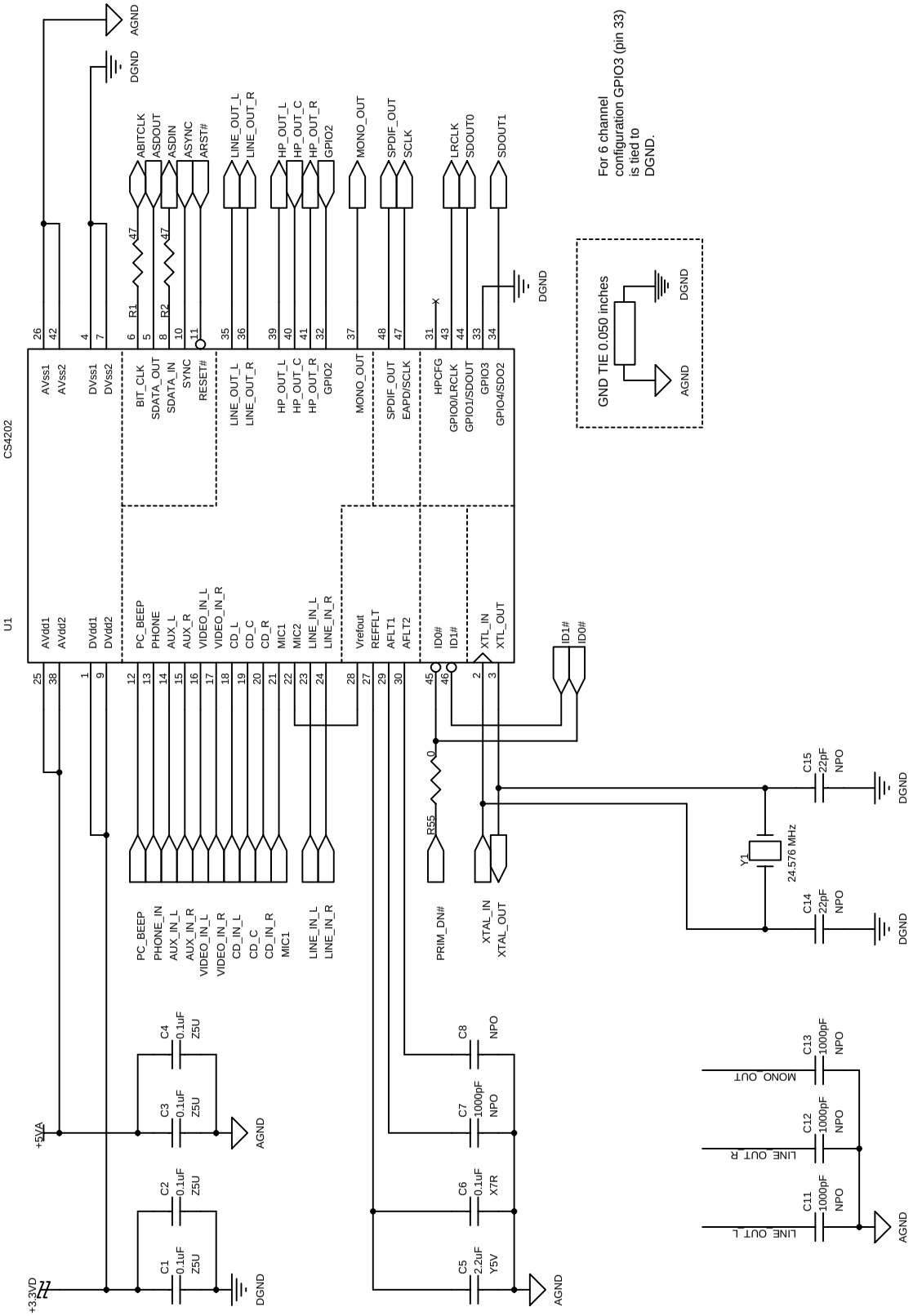
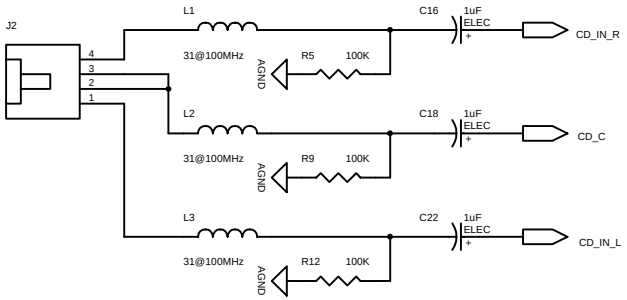
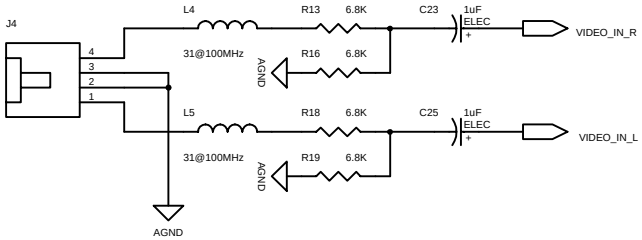


Figure 2. CS4202 Audio Codec

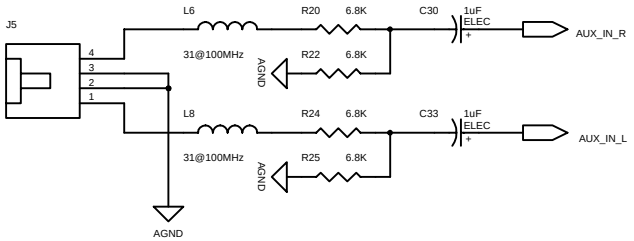
CD IN



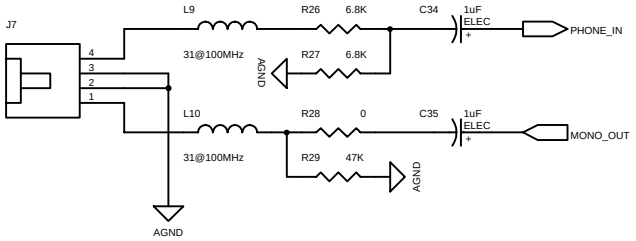
VIDEO IN



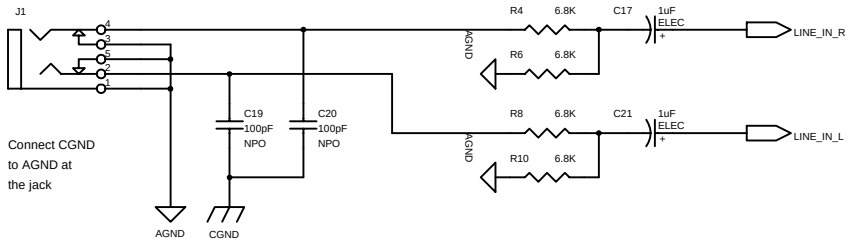
AUX IN



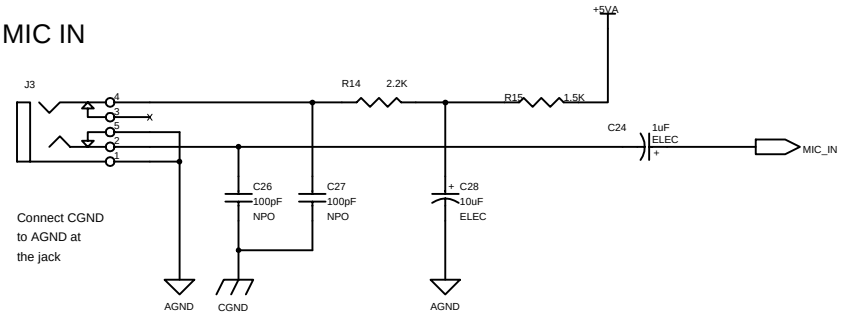
INTERNAL MODEM CONNECTION



LINE IN



MIC IN



BEEP IN

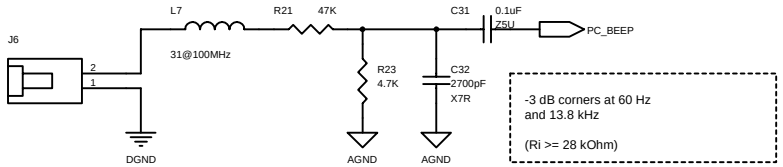


Figure 3. Analog Inputs

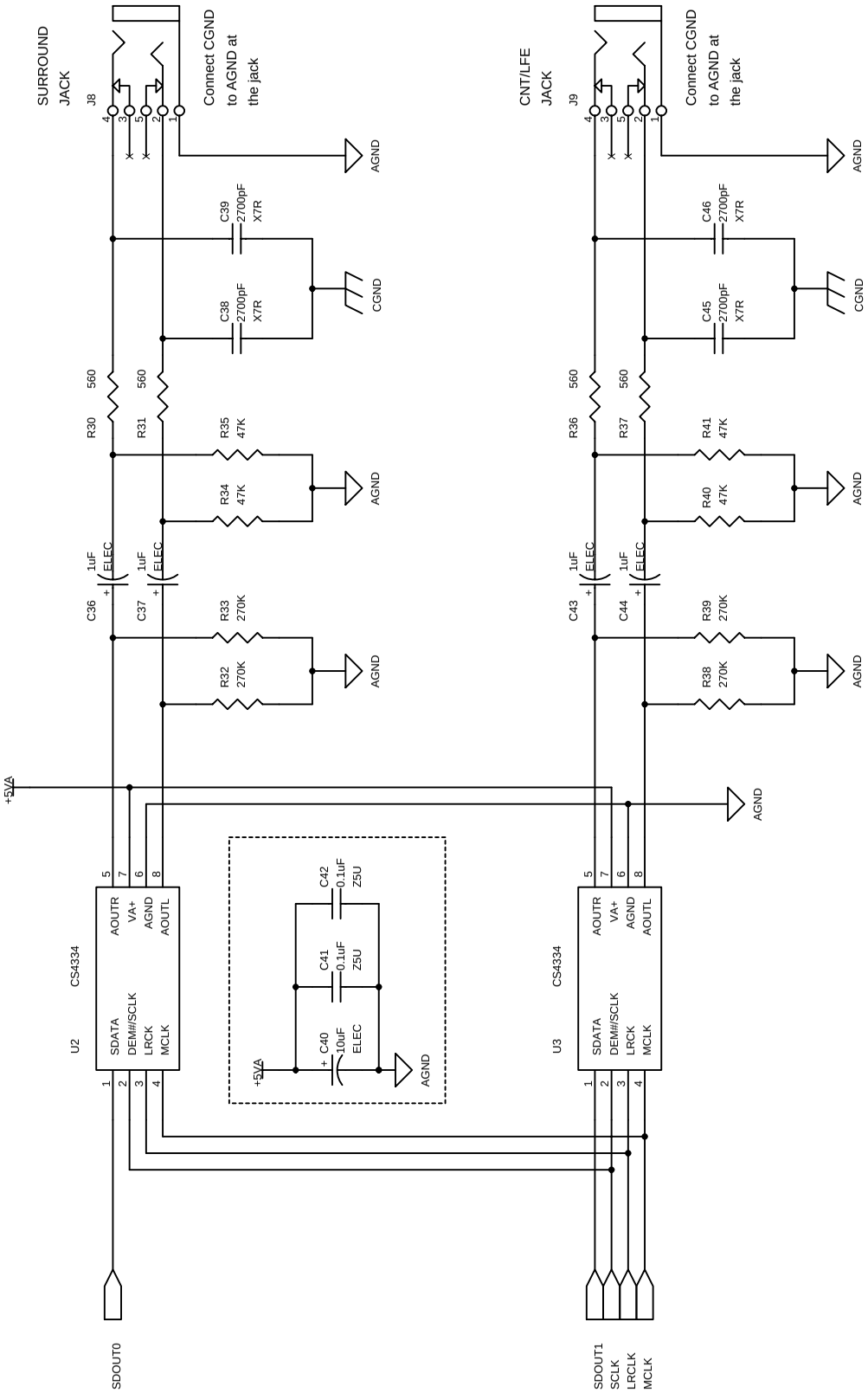


Figure 4. Center Channel, Surround, and Sub-Woofer Outputs

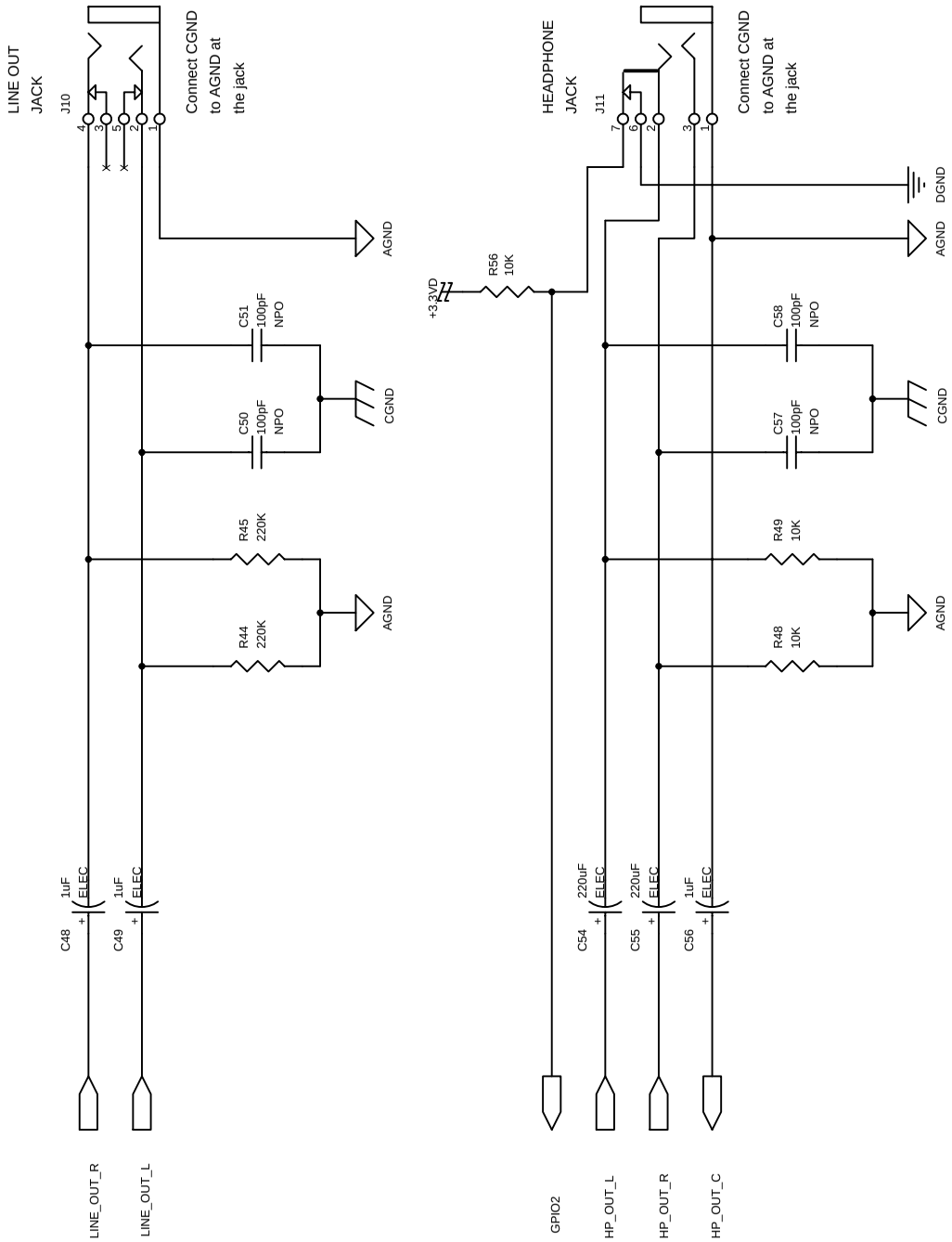


Figure 5. Front Channel and Headphone Sense Output

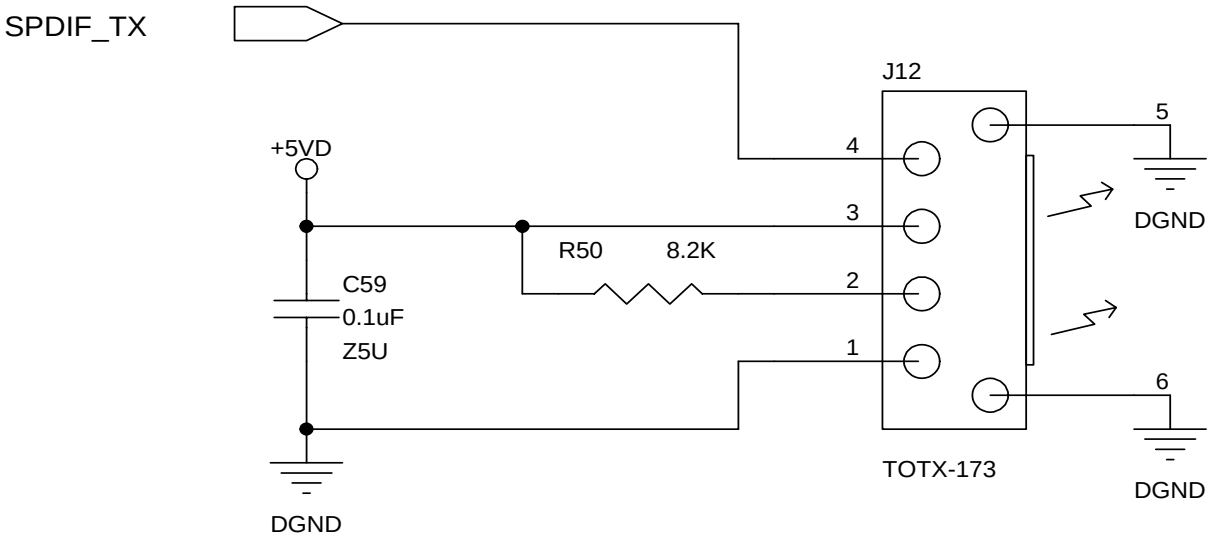
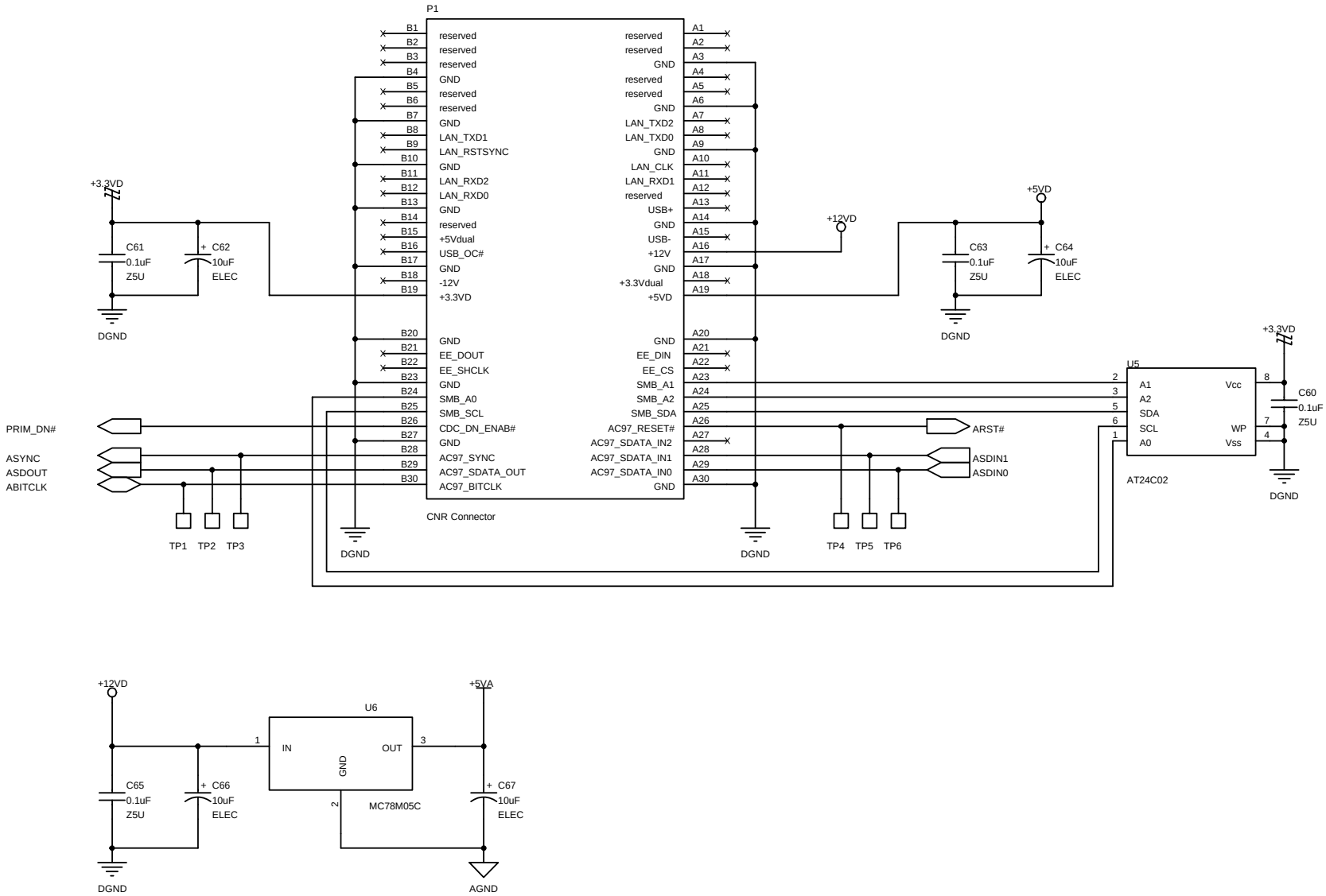


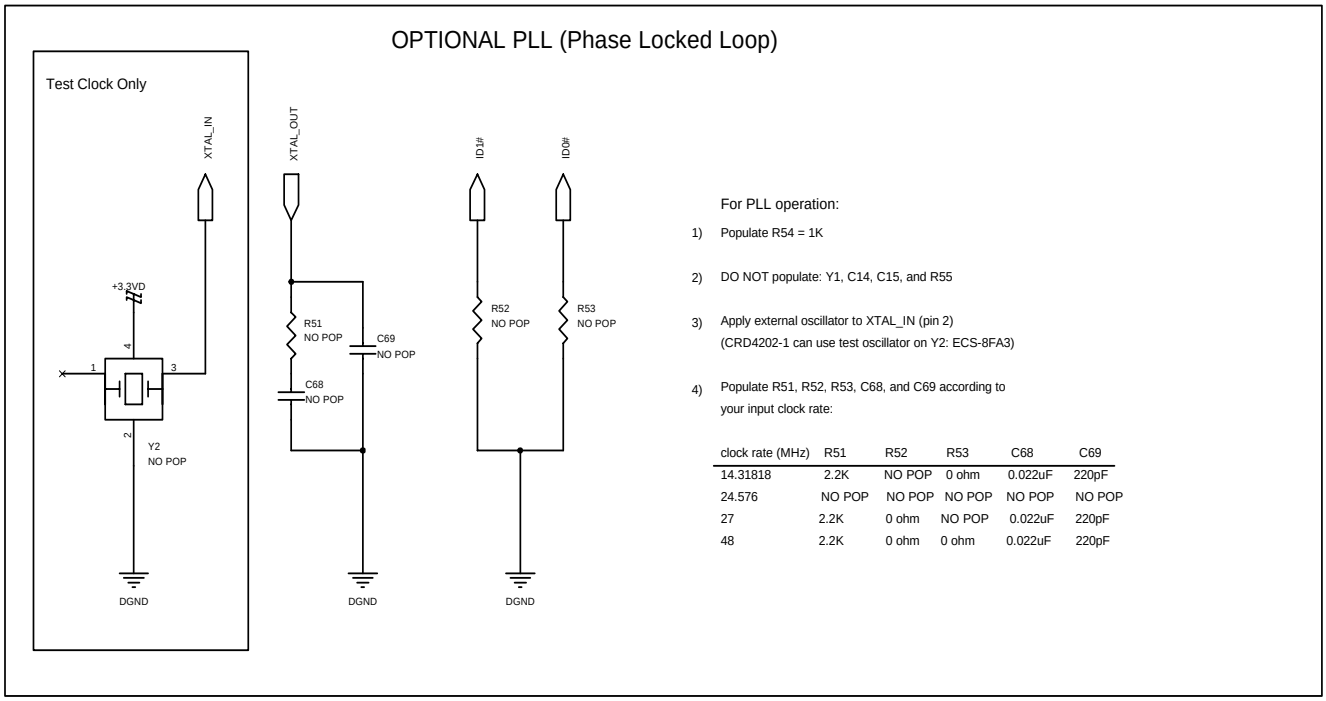
Figure 6. S/PDIF Optical Output



Connect AGND to DGND with a 50 mil trace near the codec.

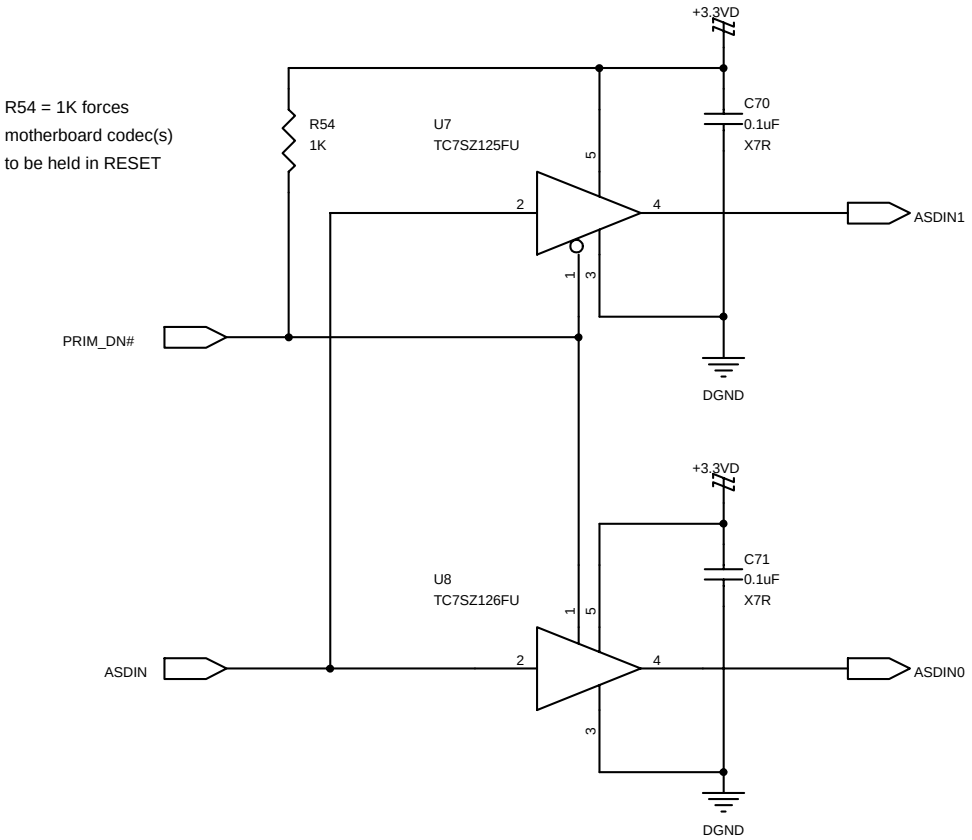
Connect CGND to DGND with a 50 mil trace near the finger edge of the board.

Figure 7. CNR Connector



clock rate (MHz)	R51	R52	R53	C68	C69
14.31818	2.2K	NO POP	0 ohm	0.022uF	220pF
24.576	NO POP	NO POP	NO POP	NO POP	NO POP
27	2.2K	0 ohm	NO POP	0.022uF	220pF
48	2.2K	0 ohm	0 ohm	0.022uF	220pF

Figure 8. Phase Locked Loop



DO NOT use this circuit for motherboard designs. This circuit is strictly for CNR cards.

For motherboard designs:
connect ASDIN to ASDIN0 if primary codec,

connect ASDIN to ASDIN1 if secondary codec.

Replace R54 with 100K for automatic demotion
when used with primary motherboard codec(s).

Figure 9. Auto Demotion and Serial Buffers

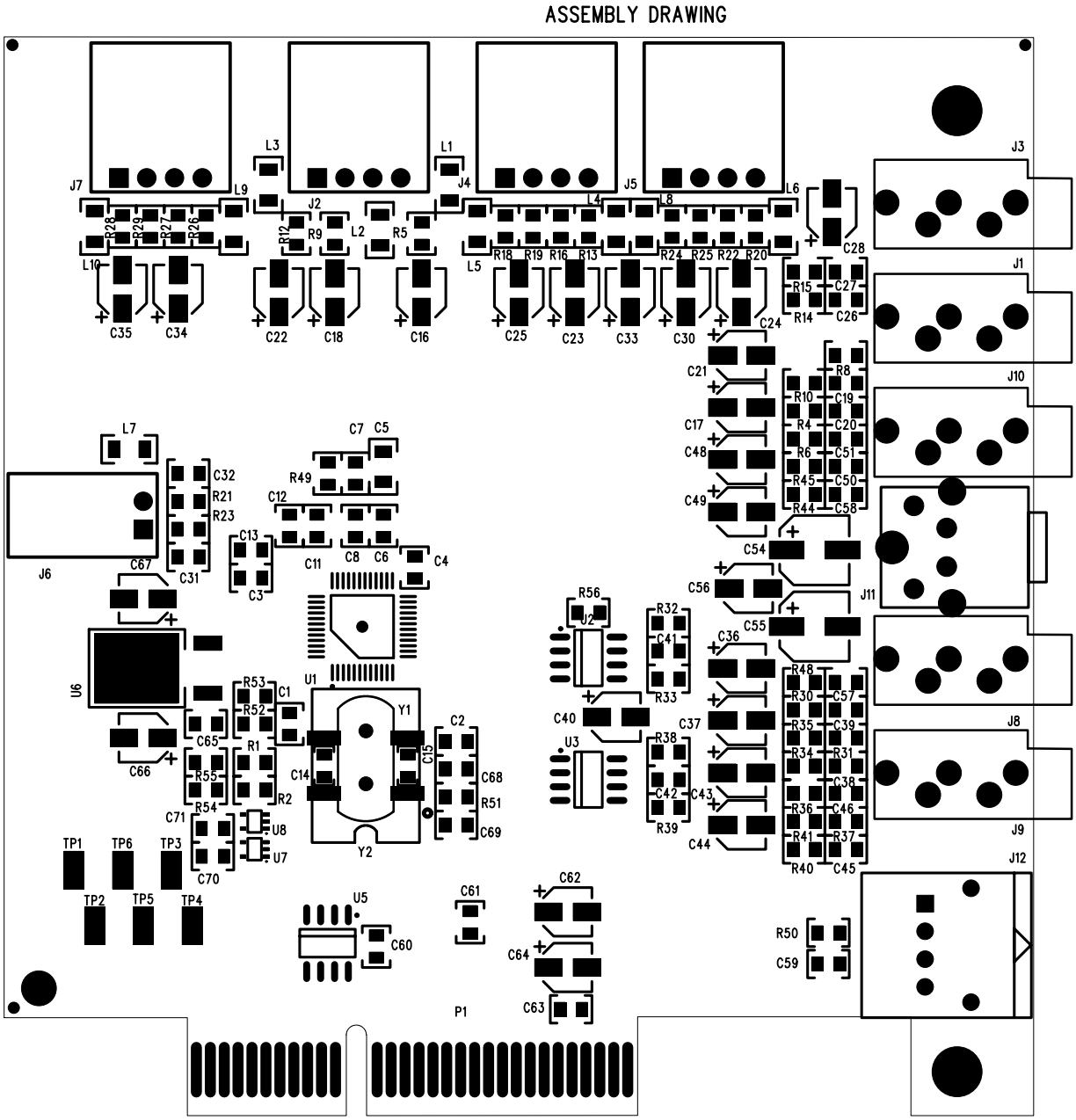


Figure 10. PCB Layout: Top Assembly Drawing

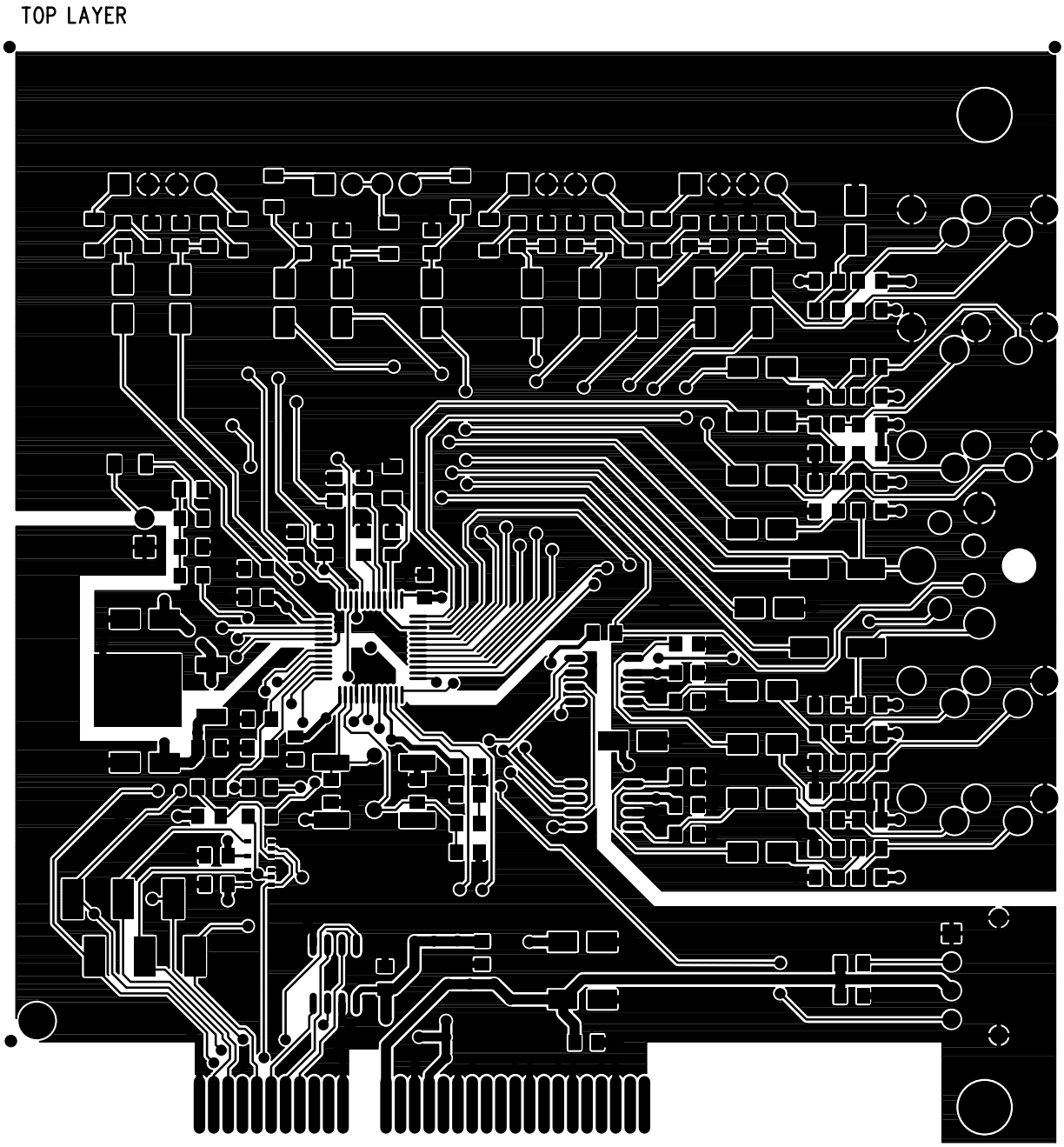


Figure 11. PCB Layout: Top Layer

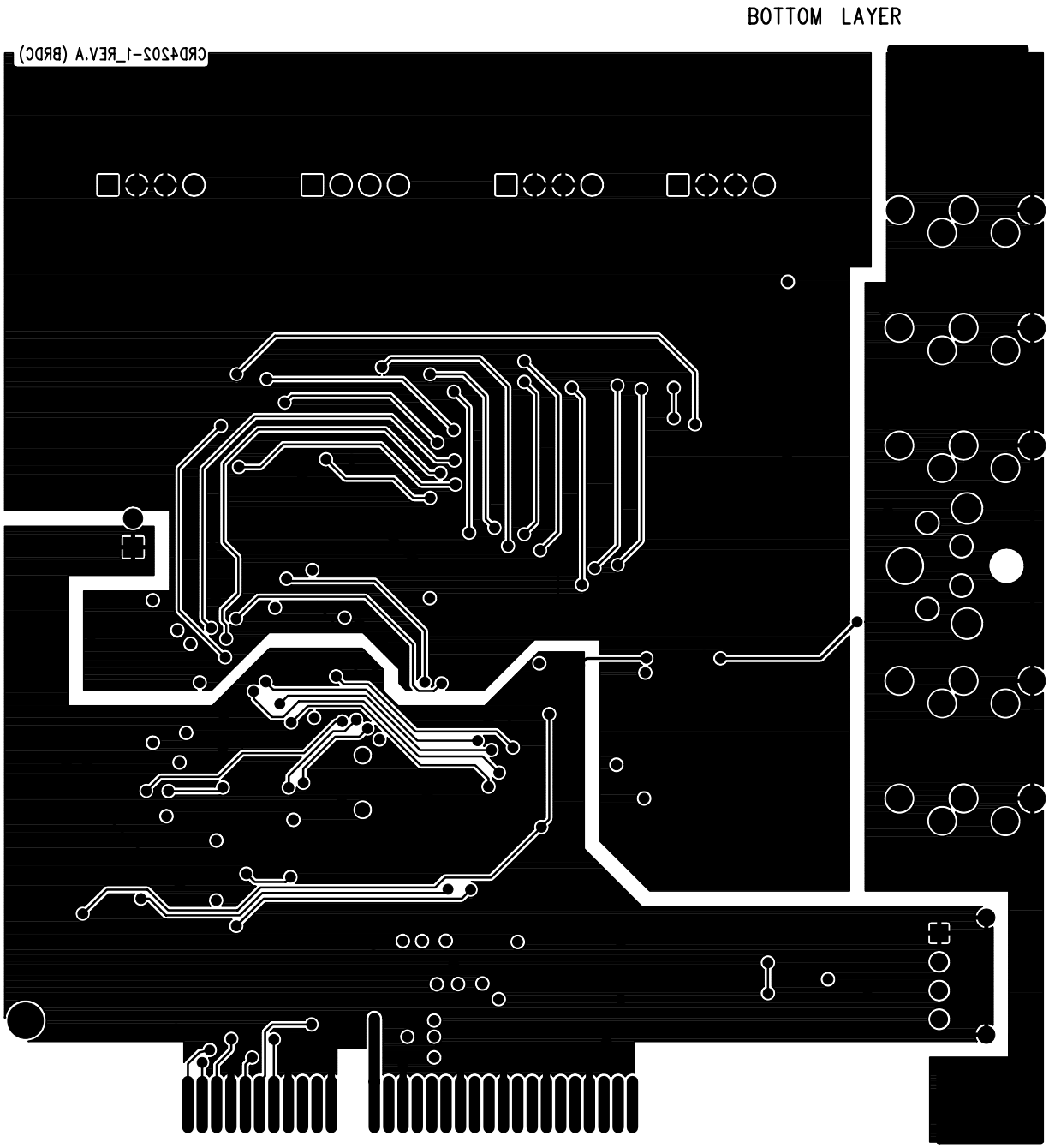
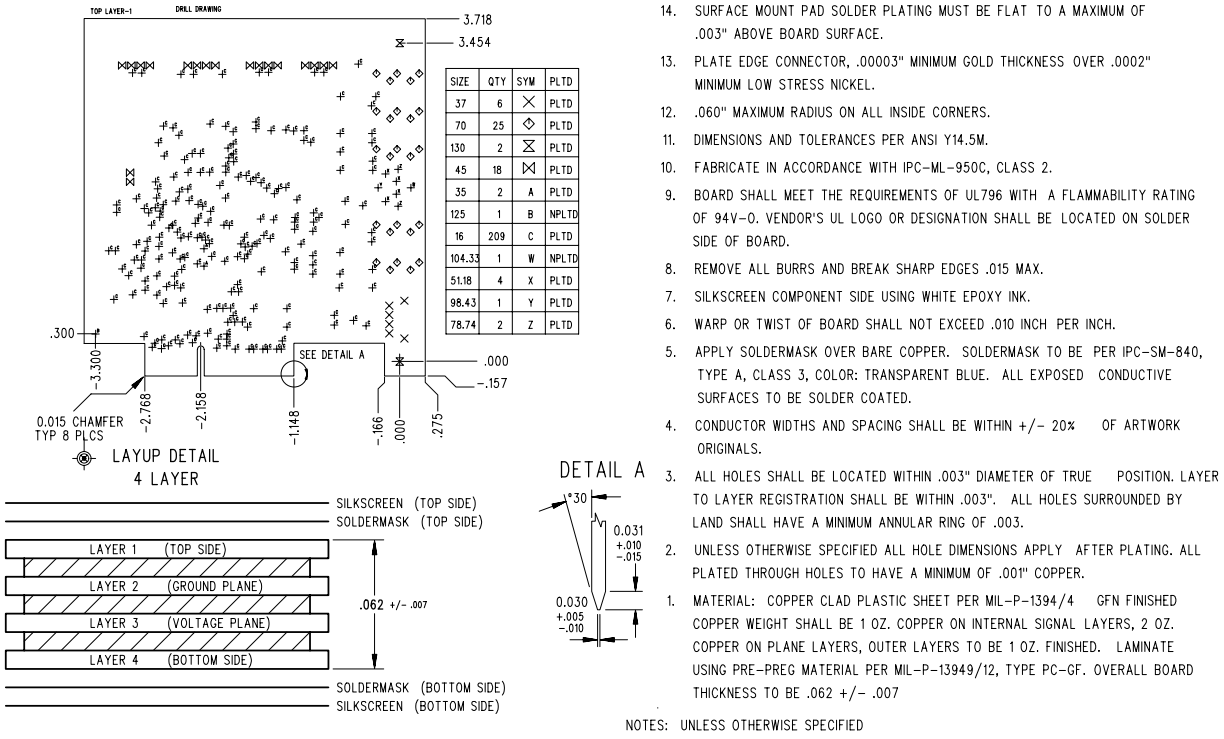


Figure 12. PCB Layout: Bottom Layer



14. SURFACE MOUNT PAD SOLDER PLATING MUST BE FLAT TO A MAXIMUM OF .003" ABOVE BOARD SURFACE.
13. PLATE EDGE CONNECTOR, .00003" MINIMUM GOLD THICKNESS OVER .0002" MINIMUM LOW STRESS NICKEL.
12. .060" MAXIMUM RADIUS ON ALL INSIDE CORNERS.
11. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M.
10. FABRICATE IN ACCORDANCE WITH IPC-ML-950C, CLASS 2.
9. BOARD SHALL MEET THE REQUIREMENTS OF UL796 WITH A FLAMMABILITY RATING OF 94V-O. VENDOR'S UL LOGO OR DESIGNATION SHALL BE LOCATED ON SOLDER SIDE OF BOARD.
8. REMOVE ALL BURRS AND BREAK SHARP EDGES .015 MAX.
7. SILKSCREEN COMPONENT SIDE USING WHITE EPOXY INK.
6. WARP OR TWIST OF BOARD SHALL NOT EXCEED .010 INCH PER INCH.
5. APPLY SOLDERMASK OVER BARE COPPER. SOLDERMASK TO BE PER IPC-SM-840, TYPE A, CLASS 3, COLOR: TRANSPARENT BLUE. ALL EXPOSED CONDUCTIVE SURFACES TO BE SOLDER COATED.
4. CONDUCTOR WIDTHS AND SPACING SHALL BE WITHIN +/- 20% OF ARTWORK ORIGINALS.
3. ALL HOLES SHALL BE LOCATED WITHIN .003" DIAMETER OF TRUE POSITION. LAYER TO LAYER REGISTRATION SHALL BE WITHIN .003". ALL HOLES SURROUNDED BY LAND SHALL HAVE A MINIMUM ANNULAR RING OF .003.
2. UNLESS OTHERWISE SPECIFIED ALL HOLE DIMENSIONS APPLY AFTER PLATING. ALL PLATED THROUGH HOLES TO HAVE A MINIMUM OF .001" COPPER.
1. MATERIAL: COPPER CLAD PLASTIC SHEET PER MIL-P-1394/4 GFN FINISHED COPPER WEIGHT SHALL BE 1 OZ. COPPER ON INTERNAL SIGNAL LAYERS, 2 OZ. COPPER ON PLANE LAYERS, OUTER LAYERS TO BE 1 OZ. FINISHED. LAMINATE USING PRE-PREG MATERIAL PER MIL-P-13949/12, TYPE PC-GF. OVERALL BOARD THICKNESS TO BE .062 +/- .007

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 13. PCB Layout: Drill Drawing

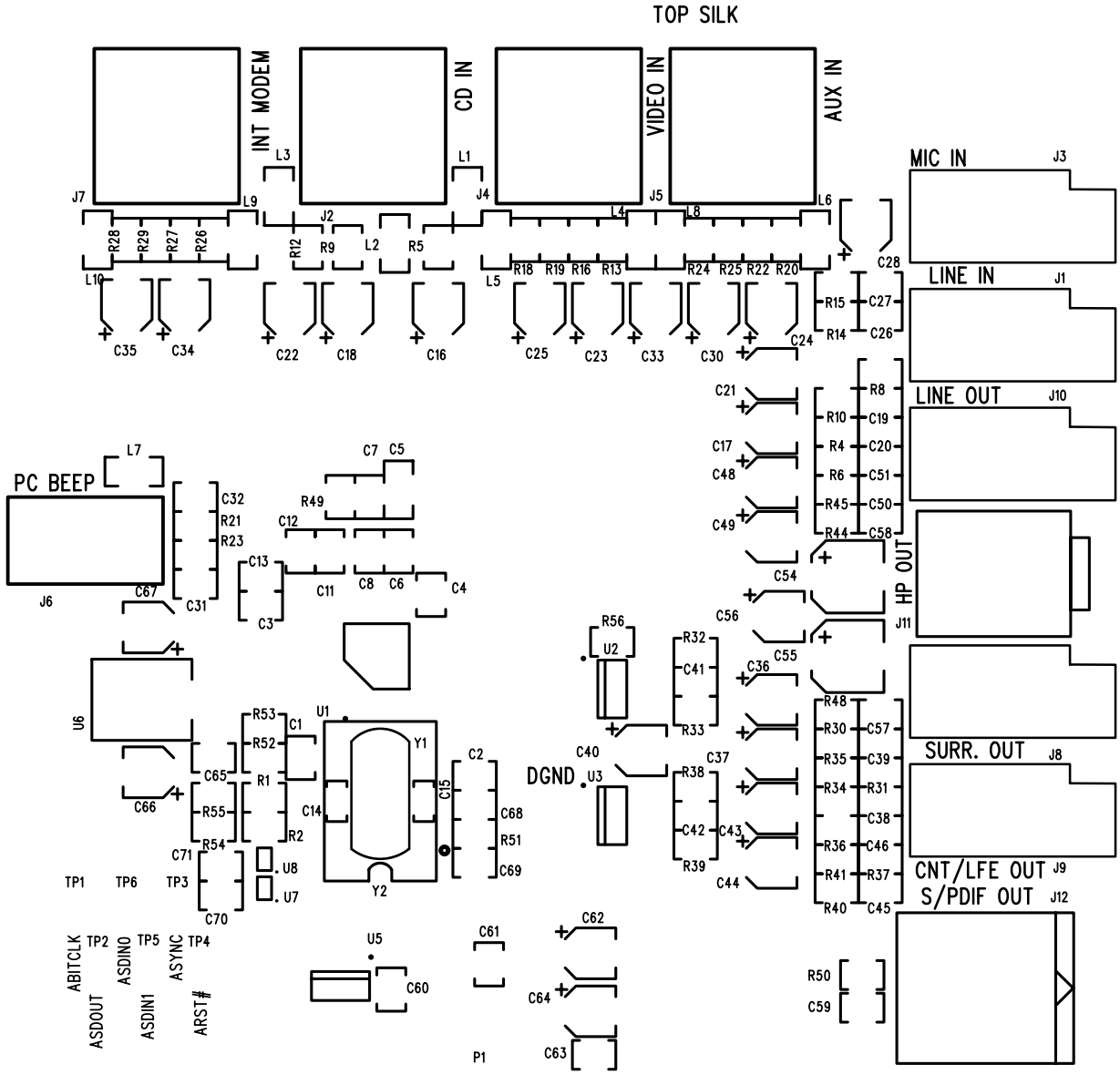


Figure 14. PCB Layout: Top Silkscreen

5. BILL OF MATERIALS

Item	Quantity	Reference	Manufacturer	Part Number	Description
1	12	C1,C2,C3,C4,C31,C41, C42,C59,C60,C61,C63,C65	KEMET	C0805C104M5UAC	CAP, 0805, Z5U, 0.1 µF, 20%, 50V
2	1	C5	KEMET	C1206C225M8VAC	CAP, 1206, Y5V, 2.2 µF, 20%, 10V
3	3	C6,C70,C71	KEMET	C0805C104K5RAC	CAP, 0805, X7R, 0.1 µF, 10%, 50V
4	5	C7,C8,C11,C12,C13	KEMET	C0805C102K5GAC	CAP, 0805, C0G, 1000 pF, 10%, 50V
5	2	C14,C15	KEMET	C0805C220K5GAC	CAP, 0805, C0G, 22 pF, 10%, 50V
6	19	C16,C17,C18,C21,C22, C23,C24,C25,C30,C33, C34,C35,C36,C37,C43, C44,C48,C49,C56	PANASONIC	ECE-V1HA010R	CAP, SMT B, ELEC, 1 µF, 20%, 50V
7	4	C19,C20,C26,C27	KEMET	C0805C101J5GAC	CAP, 0805, COG, 100 pF, 5%, 50V
8	6	C28,C40,C62,C64,C66,C67	PANASONIC	ECE-V1CA100R	CAP, SMT B, ELEC, 10 µF, 20%, 16V
9	5	C32,C38,C39,C45,C46	KEMET	C0805C272K5RAC	CAP, 0805, X7R, 2700 pF, 10%, 50V
10	4	C50,C51,C57,C58	KEMET	C0805C101J5GAC	CAP, 0805, C0G, 100 pF, 5%, 50V
11	2	C54,C55	PANASONIC	ECE-V0GA221P	CAP, SMT D, ELEC, 220 µF, 20%, 4V
12	2	C68,C69	NO POP	NO POP	NO POP
13	5	J1,J3,J8,J9,J10	A/D ELEC-TRONICS	3570-50	CONN, 1/8" DOUBLE SW. STEREO PHONE JACK
14	4	J2,J4,J5,J7	MOLEX	70553-0003	HDR, 4X1, 0.025" PIN, 0.1" CTR, 15u" AU
15	1	J6	MOLEX	70553-0036	HDR, 2X1, 0.025" PIN, 0.1" CTR, 150u" SN/PB
16	1	J11	SINGATRON	2SJ-09075N53	CONN, 1/8" SINGLE SW. STEREO PHONE JACK W/INSULATOR
17	1	J12	TOSHIBA	TOTX173	CONN, OPTICAL TOSLINK TRANSMITTER

18	10	L1,L2,L3,L4,L5,L6,L7,L8, L9,L10	TDK	HF50ACB321611-T	IND, FBEAD, 1206, 31@100MHz, 25%
19	1	P1	NONE	NONE	CNR BUS CONNECTOR
20	2	R2,R1	PHILIPS	9C08052A47R0J	RES, SO, 0805, 47, 5%, 1/10W, METAL FILM
21	14	R4,R6,R8,R10,R13,R16, R18,R19,R20,R22,R24, R25,R26,R27	PHILIPS	9C08052A6801F	RES, SO, 0805, 6.8K, 1%, 1/10W, METAL FILM
22	3	R5,R9,R12	PHILIPS	9C08052A1003J	RES, SO, 0805, 100K, 5%, 1/10W, METAL FILM
23	1	R14	PHILIPS	9C08052A2201J	RES, SO, 0805, 2.2K, 5%, 1/10W, METAL FILM
24	1	R15	PHILIPS	9C08052A1501J	RES, SO, 0805, 1.5K, 5%, 1/10W, METAL FILM
25	6	R21,R29,R34,R35,R40,R41	PHILIPS	9C08052A4702J	RES, SO, 0805, 47K, 5%, 1/10W, METAL FILM
26	1	R23	PHILIPS	9C08052A4701J	RES, SO, 0805, 4.7K, 5%, 1/10W, METAL FILM
27	2	R28,R55	PHILIPS	9C08052A0R00J	RES, SO, 0805, 0, 5%, 1/10W, METAL FILM
28	4	R30,R31,R36,R37	PHILIPS	9C08052A5600J	RES, SO, 0805, 560, 5%, 1/10W, METAL FILM
29	4	R32,R33,R38,R39	PHILIPS	9C08052A2703J	RES, SO, 0805, 270K, 5%, 1/10W, METAL FILM
30	2	R45,R44	PHILIPS	9C08052A2203J	RES, SO, 0805, 220K, 5%, 1/10W, METAL FILM
31	3	R48,R49,R56	PHILIPS	9C08052A1002J	RES, SO, 0805, 10K, 5%, 1/10W, METAL FILM
32	1	R50	PHILIPS	9C08052A8201J	RES, SO, 0805, 8.2K, 5%, 1/10W, METAL FILM
33	3	R51,R52,R53	NO POP	NO POP	NO POP
34	1	R54	PHILIPS	9C08052A1001J	RES, SO, 0805, 1K, 5%, 1/10W, METAL FILM
35	6	TP1,TP2,TP3,TP4,TP5,TP6	KEYSTONE	5015	mini SMT test point
36	1	U1	Cirrus Logic	CS4202-JQ	IC, TQFP, AC '97 2.2 SERIAL CODEC W/ HP AMP + SRC
37	2	U2,U3	Cirrus Logic	CS4334-KS	IC, SO, SOIC8, STEREO DAC, 24 BITS

38	1	U5	ATMEL	AT24C02N-10SC-2.7	IC, SO, SOIC8, SERIAL EEPROM, 256 x 8, 2.7V
39	1	U6	MOTOROLA	MC78M05CDT	IC, SO, +5V REGULATOR, DPAK, 4%, 500mA
40	1	U7	TOSHIBA	TC7SZ125FU	IC, SSOP5-P-0.65A, single 3 state buffer, 2.6ns
41	1	U8	TOSHIBA	TC7SZ126FU	IC, SSOP5-P-0.65A, single 3 state buffer, 2.6ns
42	1	Y1	FOX	FS24.576	XTAL, 24.576MHz, HC49S, Fund Mode, Par Res
43	1	Y2	NO POP	NO POP	NO POP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