

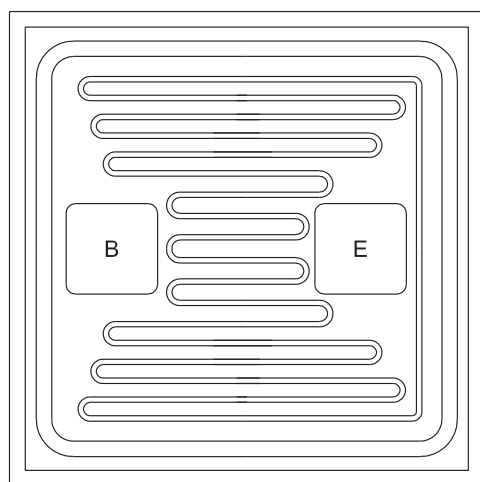
PROCESS CP782X
Small Signal Transistor
PNP - Low $V_{CE(SAT)}$ Transistor Chip



PROCESS DETAILS

Die Size	26 x 26 MILS
Die Thickness	5.9 MILS
Base Bonding Pad Area	5.5 x 5.5 MILS
Emitter Bonding Pad Area	5.5 x 5.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE COLLECTOR

R0

GROSS DIE PER 5 INCH WAFER

25,536

PRINCIPAL DEVICE TYPES

CMLT7820G

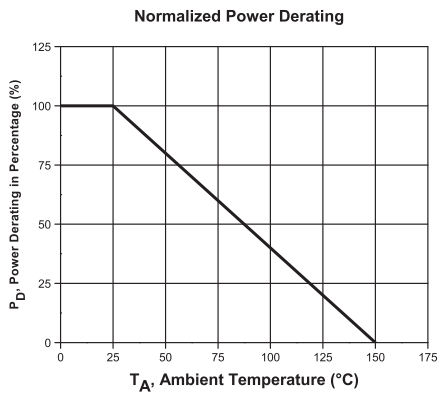
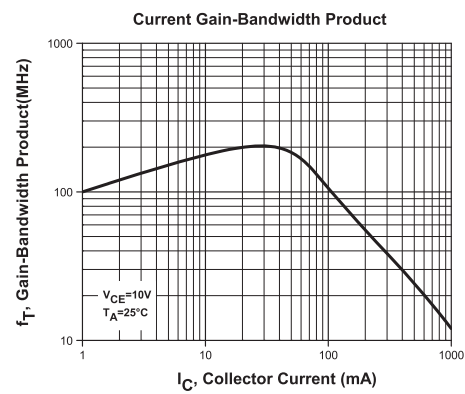
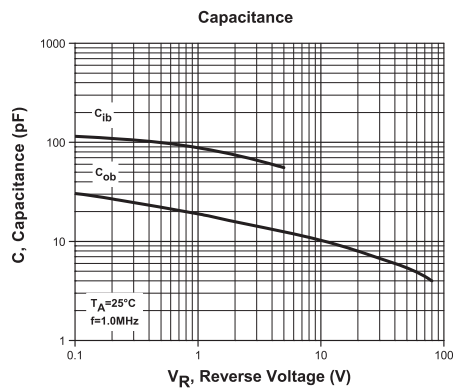
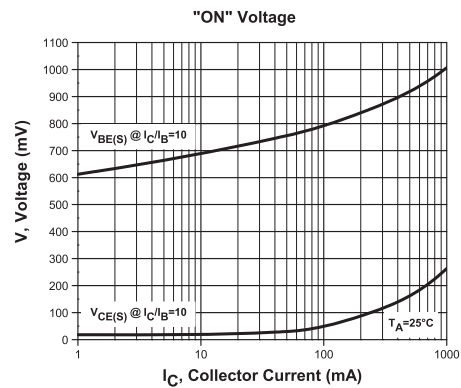
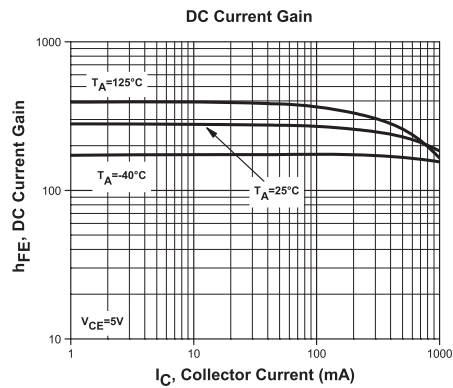
CMPT7820

CXT7820

R0 (9-September 2010)

PROCESS CP782X

Typical Electrical Characteristics



R0 (9-September 2010)