CP7208
Datasheet

D1 CMOS IMAGE SENSOR

Version 0.1

Document No. : CP-M-7208

ClairPixel Co., Ltd.

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Revision History

Issue	Rev No.	Originator	Details of Change	Date
1	0.1	limks	Initial Version	2015-03-11

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1/4-Inch, CMOS D1 WDR Image Sensor

1. Specification

DESCRIPSION

CP7208 is single-chip video/image camera sensor that is designed to fit on automotive rear view system, which allow video capture in extremely diverse lighting conditions. CP7208 is set up with a 720x480 image array, outputs up to 60 frames (720x480) per second, and supports various forms of digital output format and NTSC/PAL composite output. CP8104 has various camera control functions, and can be programmed through a two-wire serial interface.

PARAMETER		TYPICAL VALUE
Optical Dimension	Optical Format	1/4 inch
	Pixel Size	5 um X 5.6 um
	Effective Resolution	720(H) X 480(V)
	Active Pixel Area	3.600 mm(H) X 2.688 mm(V)
Digital Output		10bit, 8bit RGB Bayer, YCbCr422, RGB565/555, CCIR656
Analog Output		CVBS(NTSC/PAL) @ 27MHz
Input Clock Frequency		27MHz
Maximum Frame Rate		720x480, 60fps @ (YCbCr) 720x480, 60fps @ (Bayer)
Shutter Type		Electronic Rolling Shutter
Sensitivity		7 V / lux-sec
Dynamic Range		75 dB
SNR		46 dB
Max. Programmable Gain		analog (x72), digital (x31.5)
Supply Voltage	Pixel	3.3V ± 10%
	Analog	3.3V ± 10%
	Digital	1.5V ± 10%
	I/O	3.3V ± 10%
Power Consumption	Active	320 mW
	Standby	[T.B.D] uW
Operating Temperature		-40°C ~ 85°C
Package Type		PLCC, CLCC

FEATURES

- System-on-a-chip(SOC)-completely integrated camera system
- Integrated microcontroller for flexibility
- ±2.5% additional columns and rows for lens alignment
- CVBS, 8-,10-bit parallel digital output
- Lens Shading Compensation, Dead Pixel Compensation, Edge Enhancement
- Color Correction, Gamma Correction
- Hue/Saturation, Contrast/Brightness Control
- Integrated lens distortion correction
- Parking Guide, overlay up to 2 plane
- Automatic features :
  Auto Exposure, Auto White Balance,
  Anti-Flicker, Black Level Calibration
- NTSC/PAL encoder with 10bit DAC
- 2 channel(Master, Slave) Two-wire serial interface
- Integrated temperature sensor

APPLICATIONS

. Automotive

. Machine Visions

. Security surveillance cameras

2. System Block Diagram

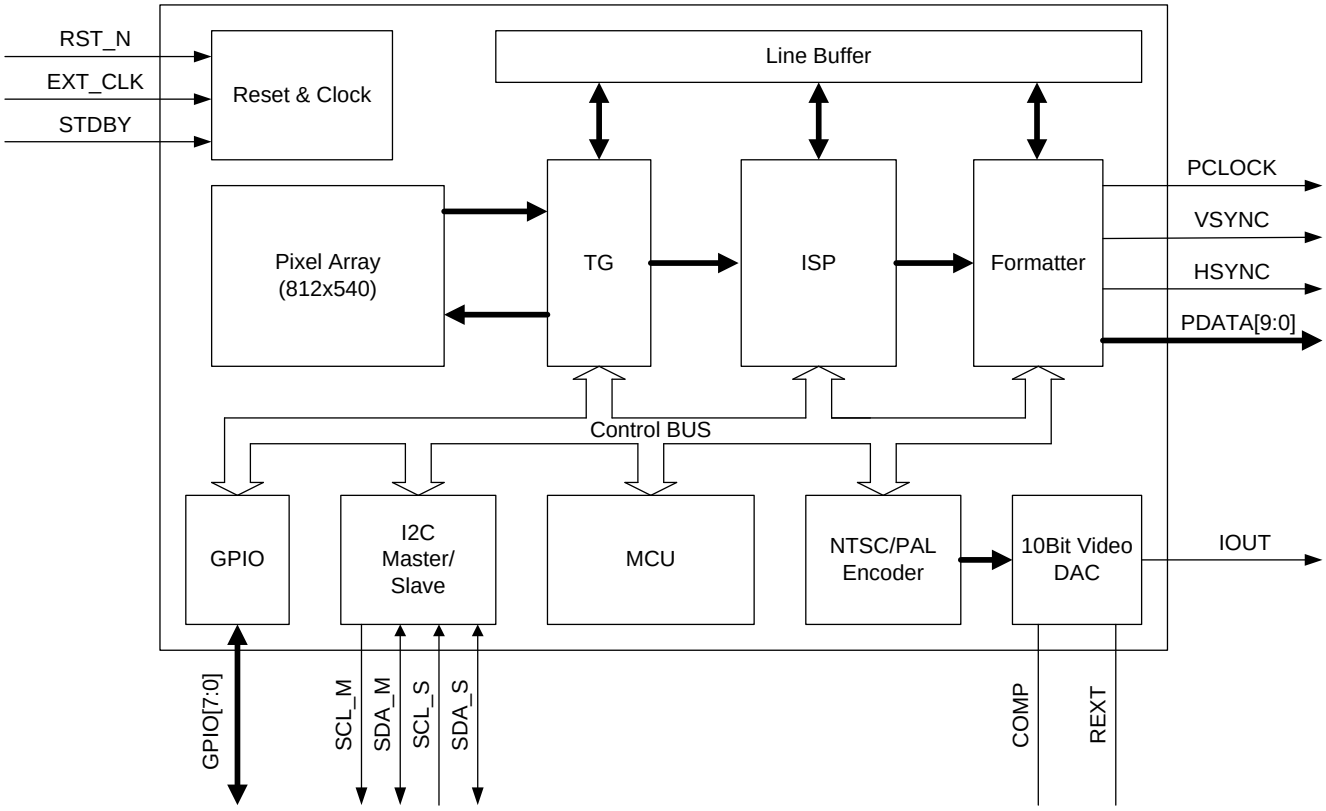


Figure 2-1 Block Diagram

CP7208 is a CMOS D1 Image Sensor in 1/4-inch optical format with 340,000 pixels.

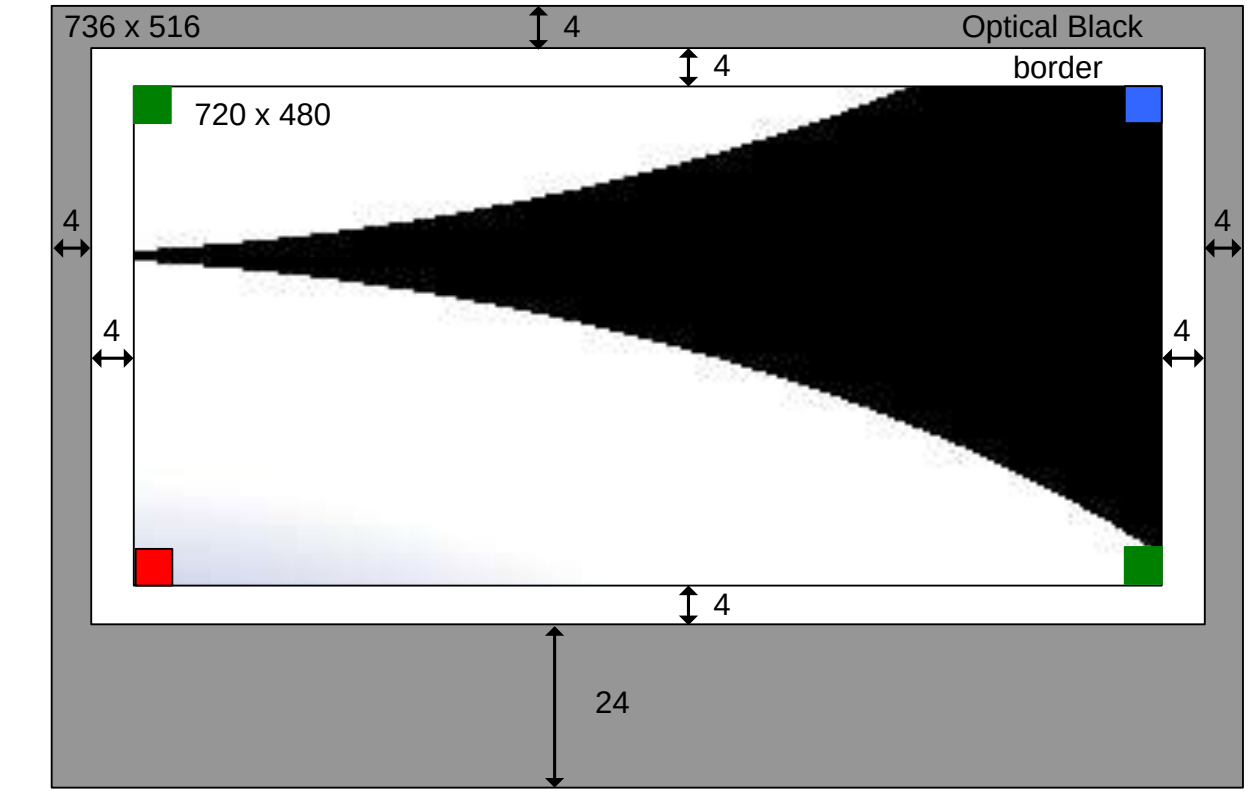
Figure 2-1 is a broad view of the block diagram of CP8104 and the 736x516 pixel array is output through TG, WDR, ISP, Formatter to the 10-bit digital parallel port, or through NTSC/PAL Encoder, 10-bit Video DAC to analog composite port.

2 channel (master, slave) two-wire serial interface and 8 channel GPIO are provided for external interface.

8 bit MCU is built in to provide an overall chip control and flexibility.

3. Pixel Array Structure

Figure 3-1 shows the pixel array structure of CP7208.



Total number of pixels : 736 x 516
Total active pixels : 720 x 480
boarder : left 4, right 4, top 4, bottom 4

Figure 3-1 Pixel Array Structure

4. Pixel Data Output Timing

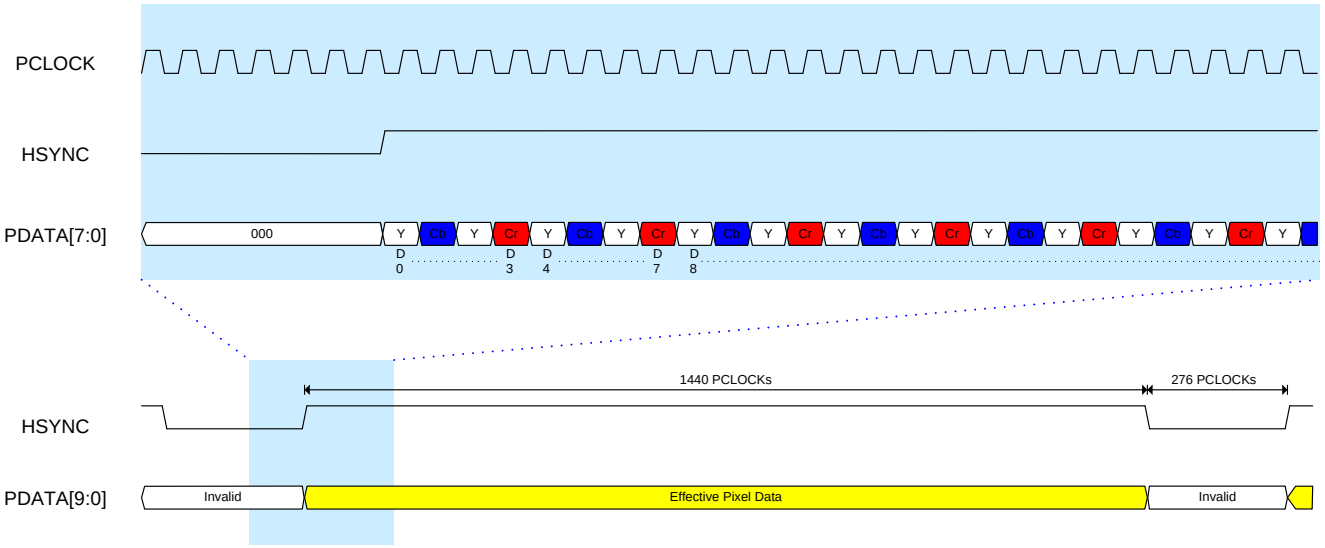


Figure 4-1 Horizontal Timing

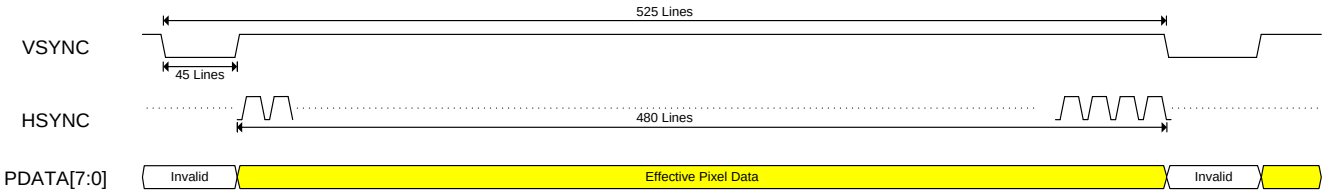


Figure 4-2 Vertical Timing

5. System Interface

5.1. System Initialization

Figure 5-1 is an outline of the reset scheme which initializes CP7208. When external reset is approved, Internal Reset Generation is initialized, and the entire system is uninitialized together.

(Note. Reset signal needs to be maintained to 200us or more LOW after Ext Clock has been stabilized.)

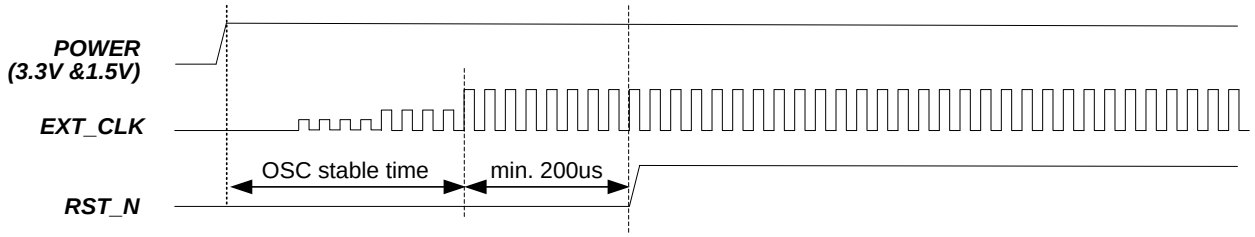


Figure 5-1 System Reset Scheme

5.2. Power-Down Mode

Power-down mode is controlled by the STDBY pin, operates as active high and enters power-down mode upon HIGH approval. Relevant pin needs to be maintained at low for Normal Operation Mode. For accurate power down operation, at least 4 clocks of external clock needs to be approved after STDBY signal input and after 4 clock approval, external clock can be maintained at LOW for reducing power consumption.

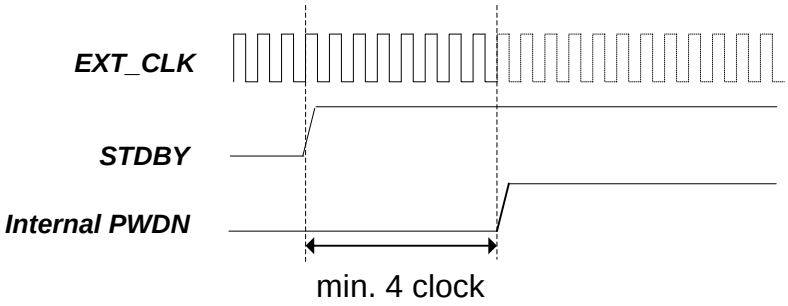


Figure 5-2 System Power Down Scheme

5.3. I2C interface

I2C Master and Slave interface each are built-in CP7208 internally. I2C device address can be modified through the MCU (system register 0x4006).

*** I2C Slave Device Address**

Write Device Address	0x76
Read Device Address	0x77

5.3.1. I2C Condition

- **Start / Stop Condition**

Data Line and Clock Line are maintained at High when Bus is not in use. Start condition is defined as the time during which Data Line transits from high to low while Clock Line maintains its high position. The time during when the data line transits from low to high is defined as the stop condition.

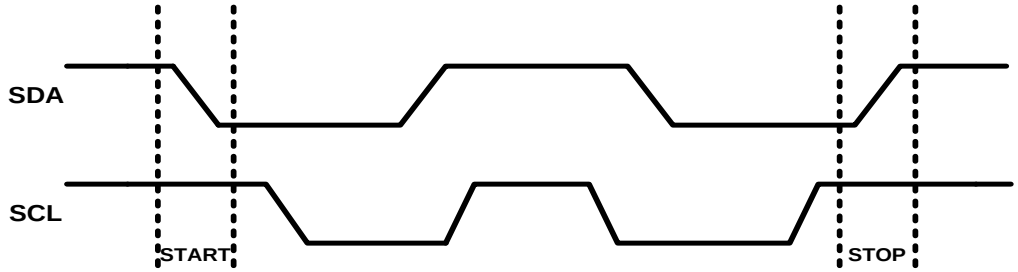


Figure 5-3 Start / Stop

- **Acknowledge**

All addresses and data are continuously transferred or received in 8-bit words to I2C slave. I2C slave sends 0 as an acknowledgement signal after each word sent. This happens in 9 clock intervals.

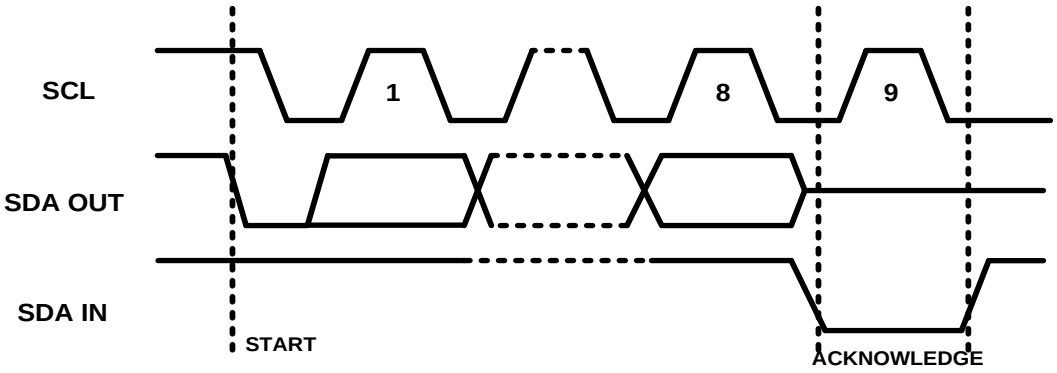


Figure 5-4 Acknowledge

5.3.2. I2C Master Operation

CP7208 operates as master through I2C interface SCL_M, SDA_M pins. It can be used as an interface to control various external devices such as AF module control.

- **Write Operation**

Write operation is composed of three parts including Device Address, Index Address and Write Data and the success of the communication of each part can be verified through the Acknowledge Bit after the transmission. I2C master can select the Target Device through the Address of the Device through which data is to be sent, and a maximum of 5byte data can be sent at once

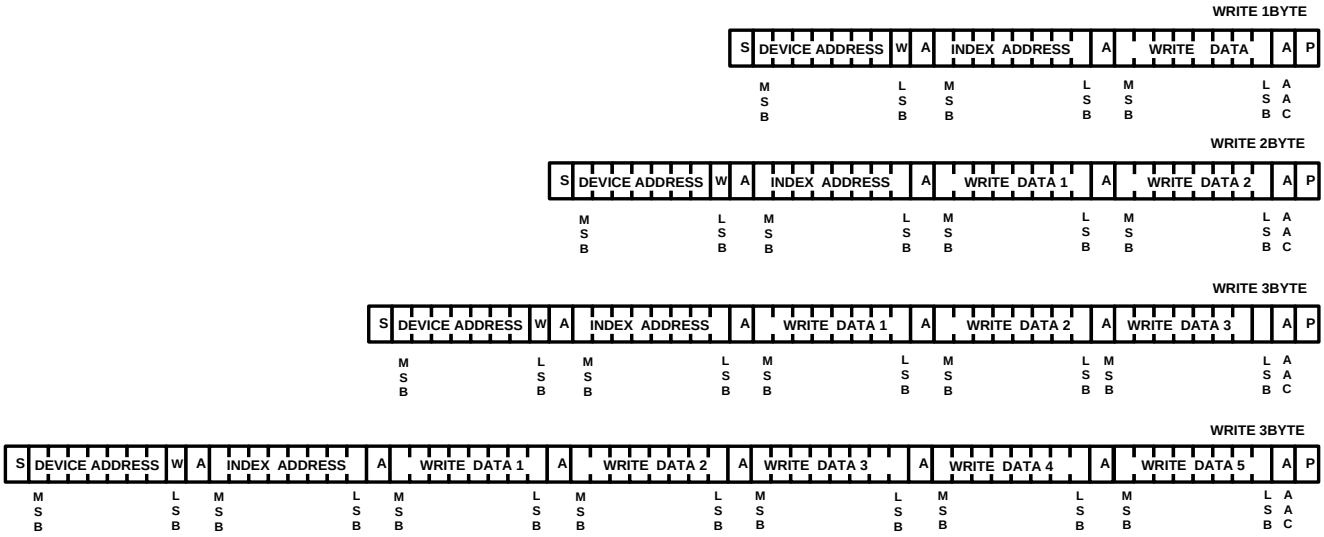


Figure 5-5 I2C Master Write Operation

- **Read Operation**

In order to access a random register to read the register value, " Dummy Write" needs to be performed. This is because internal address register automatically increases after the transmission is complete. In order to read data from a certain address register, write index address first to read the data at the relevant register. The blue dotted line in the figure below shows that in dummy write, STOP condition may be output after the index address has been sent, or the START condition may be output without the STOP condition. The function mentioned above is carried out by internal register settings. I2C master built in CP7208 can read a maximum of 2 Bytes in series.

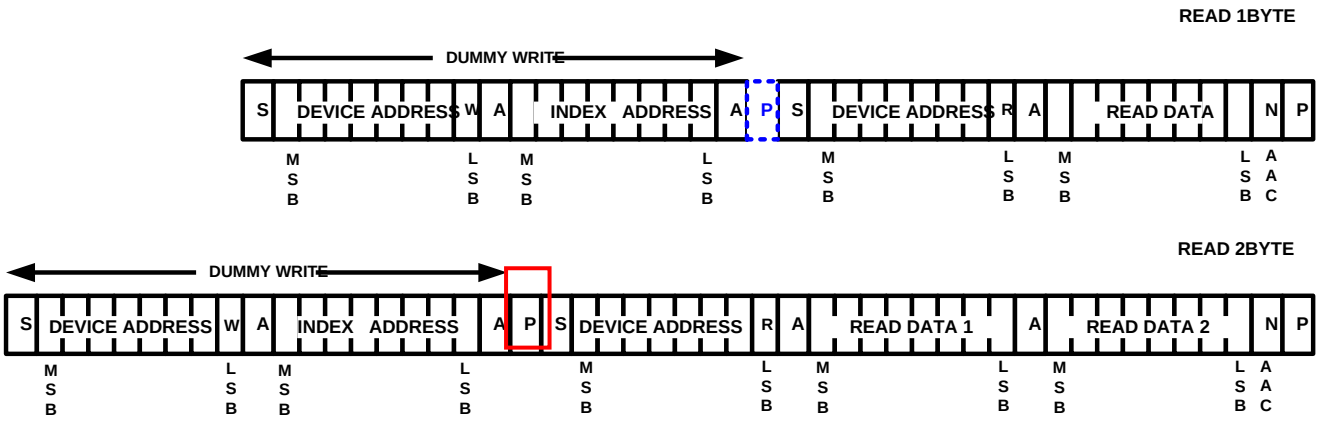


Figure 5-6 I2C Master Read Operation

5.3.3. I2C Slave Operation

CP7208 operates as slave through I2C interface SCL_S, SDA_S pin. Certain registers of CP7208 can be controlled through the I2C Slave interface. Program data can also be downloaded through the I2C Slave to the 8051 Program Memory within. MCU Code Memory Data of CP7208 can be saved in byte units, and MCU is under Reset status while SRAM write takes place through.

- **Byte Write**

  Write operation is composed of three parts including Device Address, Index Address, and Write Data, and the success of the communication can be verified through Acknowledge Bit after the transmission of each parts. I2C slave only receives data when the Device Address matches its own.

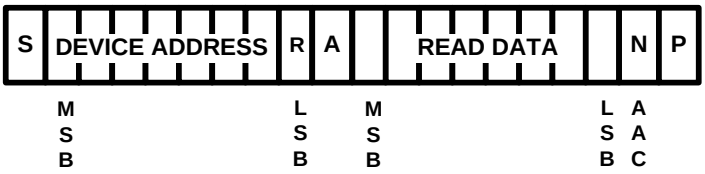
- **Random Read**

  In order to access a random register to read the register value " dummy" byte write needs to be performed. This is because internal address register automatically increases after the transmission is complete. In order to read data from a certain address register, write index address first to read the data at the relevant register.

- **Sequential Read**

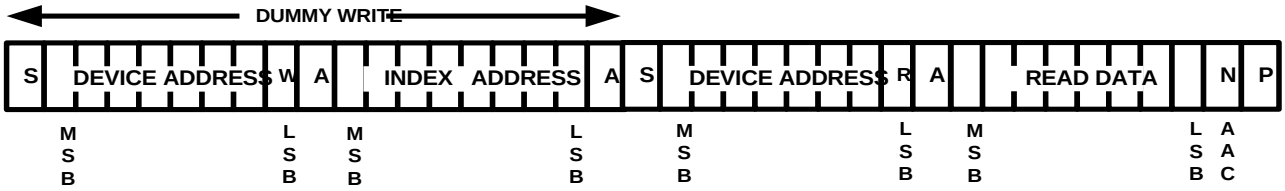
  Starts transmission together with initial Byte Read and data gets output continuously without the transmission of Device Address, Index Address to shorten communication time. I2C Master built in in CP7208 can read a maximum of 2 Bytes continuously and I2C Slave has no restrictions regarding this.

Byte Read Operation

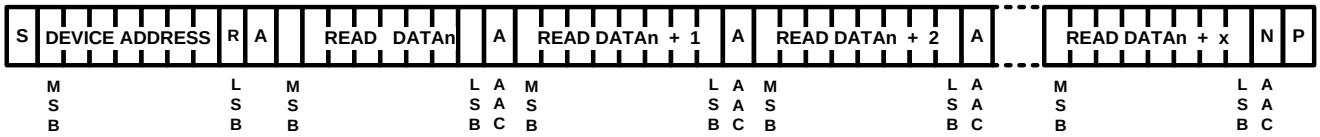


Byte Write Operation

Random Read Operation



Sequential Read Operation



S : Start Condition

P : Stop Condition

MSB : Most Significant Bit

LSB : Least Significant Bit

W : Write (1'b0)

R : Read (1'b1)

A : Acknowledge

N : No Acknowledge

AAC : Auto Address Increment

Figure 5-7 I2C Slave Read, Write Operation

5.4. GPIO Control Interface

CP7208 provides a maximum of 8 GPIOs and 4 PWMs in order to control the system control interface.

- **I/O control (system register 0x401f ~ 0x4023, 0x4055)**

  I/O control is used when sending output signals to external device, or when receiving input signal from external devices. A maximum of 8 ports can be used, and individual pull up/down control is possible through relevant registers.

5.5. PAD Control

- **PDATA Bus Control**

  PCLOCK, VSYNC, HSYNC, PDATA[9:0] pins are tri-state, pull-down control possible depending on the relevant register conditions, PDATA[2:0], HSYNC, VSYNC, PCLOCK pin output GPIO[7:2] through register control.

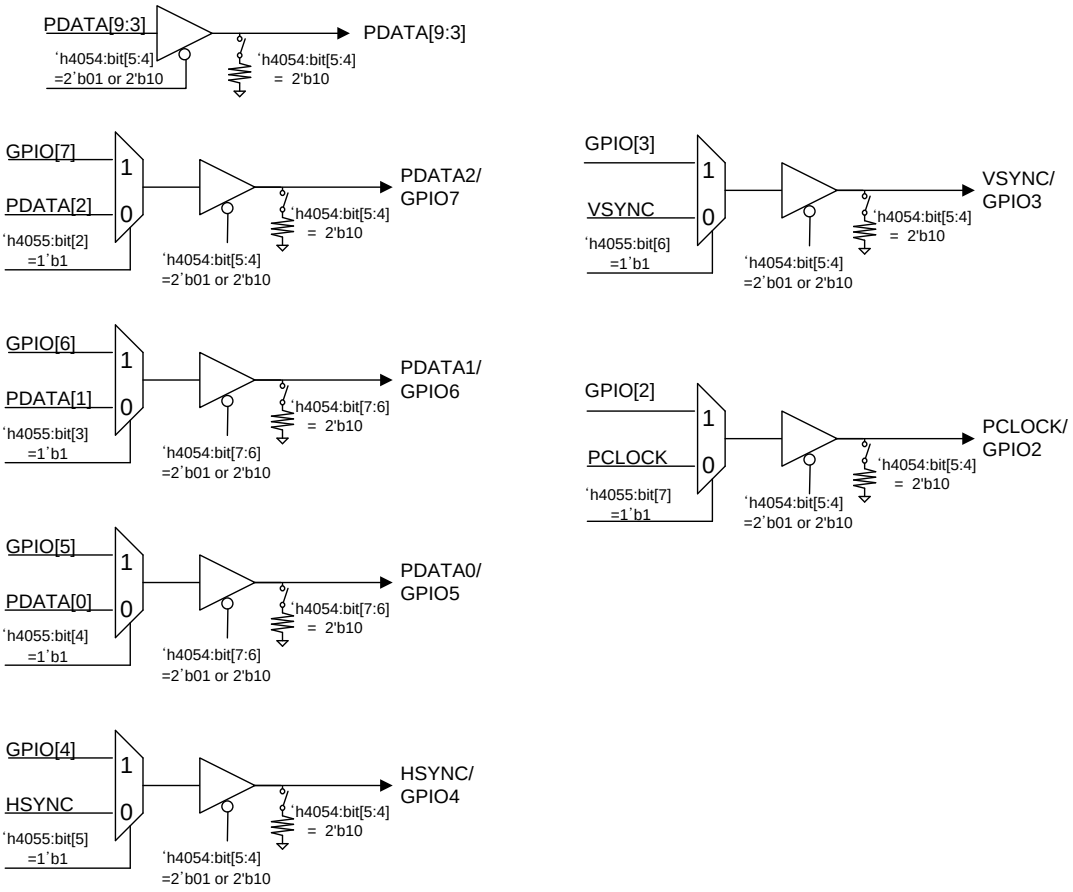


Figure 5-8 PDATA Bus Control

6. MCU interface

CP7208 has a 8bit MCU internally embedded. Memory map of the MCU block is as shown below. Code SRAM 16K byte, Data SRAM 2Kbyte are built in. CP7208 downloads the firmware using I2C master through an external EEPROM. Also, if no external EEPROM is available, the firmware can be downloaded through the system register 0x4024 ~0x4026 using I2C slave. Errors in firmware download can be checked through checksum register(0x4028 ~ 0x4029) or CRC register(0x402A ~ 0x402B). Only system register area can be accessed using I2C slave, and the other areas can be accessed using indirect mode when MCU is disabled, but the entire memory area of MCU is accessible. Interrupt Sources include VSYNC interrupt of internal Sensor and command register write interrupt.

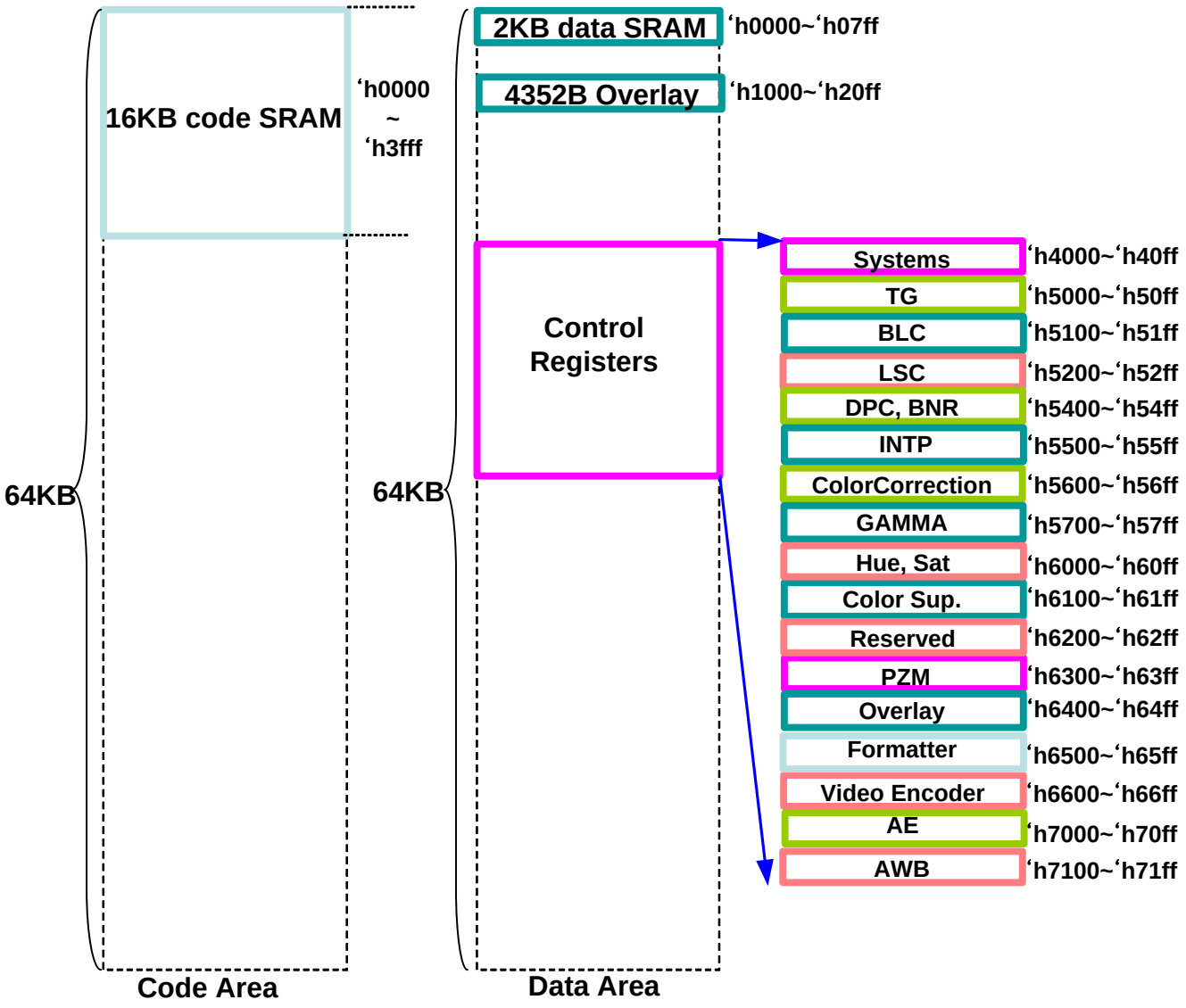


Figure 6-1 MCU Memory Map

7. EEPROM Boot Sequence

Code SRAM 16K byte and Overlay Data SRAM 4352 byte are embedded in CP7208. After initial power approval, firmware and OSD data is downloaded onto internal SRAM using I2C master through external EEPROM. Depending on the code written on certain parts of the firmware code, data size that downloaded 2 type mode can be controlled.

- **16Kbyte Code Only**

This mode uses 16K byte to code memory and does not use the OSD data. Of 16K code and address 0x3FFC and ox3FFD area of the write 0xAA and 0x55 to operate in this mode when it is.

- **16Kbyte Code + 4352byte Overlay Data**

This mode uses 16K byte to code memory and also uses 4352 byte overlay data. Of 24K code and address 0x3FFC 0x3ffD area does not have the write 0xAA and 0x55 to operate in this mode. Since 16Kbyte data automatically for overlay data is write into SRAM 4352 byte.

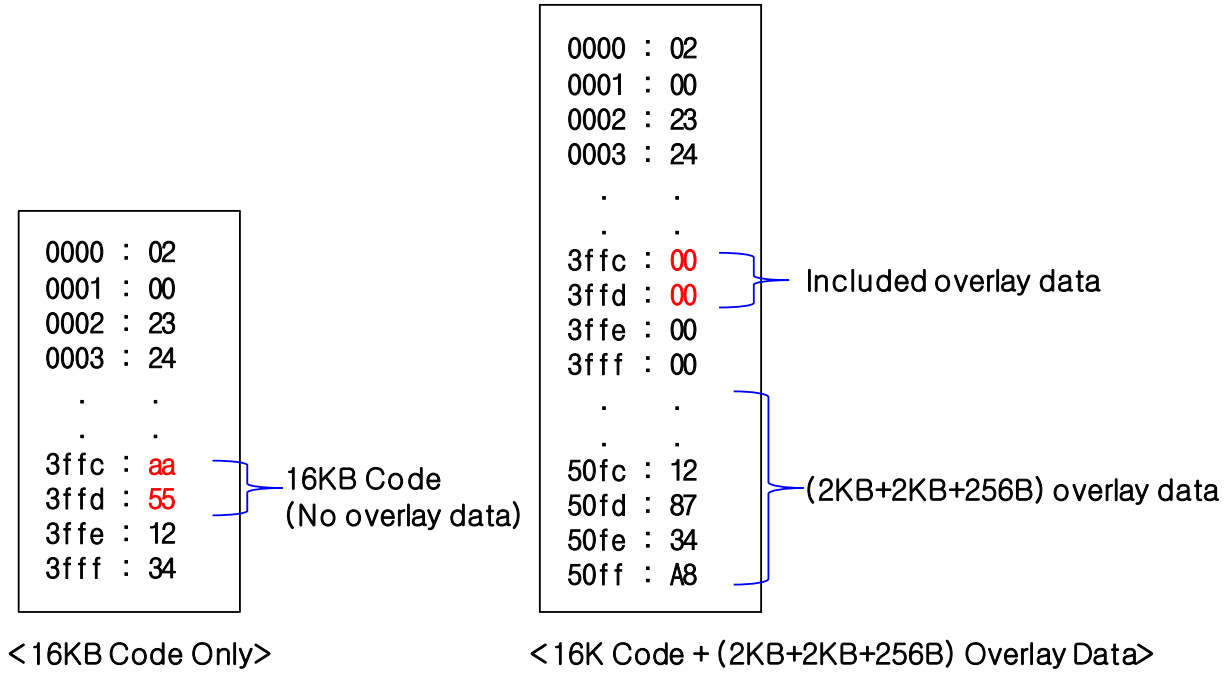


Figure 7-1 EEPROM Boot Sequence

8. TG(Timing Generator)

TG block controls the overall operation timing of the sensor and has Analog/Digital gain control, Mirror (Horizontal, Vertical) functions.

8.1. Analog/Digital Gain Control

8.1.1. Analog Gain

Register Name	RW	Bits	Register Description	
			Field Name	Field Description
A2_GAIN (Reg_0x5009)	Global Analog Gain control register **(Default 0x03)**			
	RW	[6:3]	**Cgain**	Coarse analog gain
	RW	[2:0]	**Fgain**	Fine analog gain

Analog gain can be controlled through the registers in

Register Name	RW	Bits	Register Description	
			Field Name	Field Description
A2_GAIN (Reg_0x5009)	Global Analog Gain control register **(Default 0x03)**			
	RW	[6:3]	**Cgain**	Coarse analog gain
	RW	[2:0]	**Fgain**	Fine analog gain

Table 8-1

Register Name	RW	Bits	Register Description	
			Field Name	Field Description
A2_GAIN (Reg_0x5009)	Global Analog Gain control register **(Default 0x03)**			
	RW	[6:3]	**Cgain**	Coarse analog gain
	RW	[2:0]	**Fgain**	Fine analog gain

Table 8-1 Analog Gain Control

		Fgain[2:0]							
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
Cgain[3:0]	**0000**	x0.63	x0.75	x0.88	x1.00	x1.13	x1.25	x1.38	x1.50
	0001	x1.25	x1.50	x1.75	x2.00	x2.25	x2.50	x2.75	x3.00
	0010	x1.88	x2.25	x2.63	x3.00	x3.38	x3.75	x4.13	x4.50
	0011	x2.50	x3.00	x3.50	x4.00	x4.50	x5.00	x5.50	x6.00
	0100	x3.13	x3.75	x4.38	x5.00	x5.63	x6.25	x6.88	x7.50
	0101	x3.75	x4.50	x5.25	x6.00	x6.75	x7.50	x8.25	x9.00
	0110	x4.41	x5.29	x6.18	x7.06	x7.94	x8.82	x9.71	x10.59
	0111	x5.00	x6.00	x7.00	x8.00	x9.00	x10.00	x11.00	x12.00
	1000	x10.00	x12.00	x14.00	x16.00	x18.00	x20.00	x22.00	x24.00
	1001	x15.00	x18.00	x21.00	x24.00	x27.00	x30.00	x33.00	x36.00

	1010	x30.00	x36.00	x42.00	x48.00	x54.00	x60.00	x66.00	x72.00

Table 8-2 Global Analog Gain Table

8.1.2. Digital Gain

Register Name	**RW**	**Bits**	**Register Description**	
			Field Name	**Field Description**
D_GAIN (Reg_0x500A)	Global Digital Gain control register **(Default 0x00)**			
	RW	[7:0]	**D_GAIN**	[7:5] : Global Digital Gain1 control [4:0] : Global Digital Gain2 control Gain = 2^D_GAIN[7:5]*(1 + D_GAIN[4:0]/32)

Analog gain can be controlled through the registers in

Register Name	**RW**	**Bits**	**Register Description**	
			Field Name	**Field Description**
D_GAIN (Reg_0x500A)	Global Digital Gain control register **(Default 0x00)**			
	RW	[7:0]	**D_GAIN**	[7:5] : Global Digital Gain1 control [4:0] : Global Digital Gain2 control Gain = 2^D_GAIN[7:5]*(1 + D_GAIN[4:0]/32)

Table 8-3.

Register Name	**RW**	**Bits**	**Register Description**	
			Field Name	**Field Description**
D_GAIN (Reg_0x500A)	Global Digital Gain control register **(Default 0x00)**			
	RW	[7:0]	**D_GAIN**	[7:5] : Global Digital Gain1 control [4:0] : Global Digital Gain2 control Gain = 2^D_GAIN[7:5]*(1 + D_GAIN[4:0]/32)

Table 8-3 Digital Gain Control

D_GAIN[7]	**D_GAIN[6]**	**D_GAIN[5]**	**Digital Gain1 Output**
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	X	X	x16

Table 8-4 Digital Gain 1 Table

D_GAIN[4]	**D_GAIN[3]**	**D_GAIN[2]**	**D_GAIN[1]**	**D_GAIN[0]**	**Digital Gain2 Output**

0	0	0	0	0	x1.00
0	0	0	0	1	x1.03
0	0	0	1	0	x1.06
0	0	0	1	1	x1.09
0	0	1	0	0	x1.13
0	0	1	0	1	x1.16
0	0	1	1	0	x1.19
0	0	1	1	1	x1.22
0	1	0	0	0	x1.25
0	1	0	0	1	x1.28
0	1	0	1	0	x1.31
0	1	0	1	1	x1.34
0	1	1	0	0	x1.38
0	1	1	0	1	x1.41
0	1	1	1	0	x1.44
0	1	1	1	1	x1.47
1	0	0	0	0	x1.50
1	0	0	0	1	x1.53
1	0	0	1	0	x1.56
1	0	0	1	1	x1.59
1	0	1	0	0	x1.63
1	0	1	0	1	x1.66
1	0	1	1	0	x1.69
1	0	1	1	1	x1.72
1	1	0	0	0	x1.75
1	1	0	0	1	x1.78
1	1	0	1	0	x1.81
1	1	0	1	1	x1.84
1	1	1	0	0	x1.88
1	1	1	0	1	x1.91
1	1	1	1	0	x1.94
1	1	1	1	1	x1.97

Table 8-5 Digital Gain 2 Table

9. BLC(Black Level Compensation)

Various noises are created at the image sensor which converts light into electric signals. Among those are offset form noise from heat and noise from analog circuit which processes signals. In order to measure and remove the offset form noise, create a pixel area (optical black area) which is not affected by light due to metal blocking, and change the relevant pixel value to true ‘ 0’. Such offset adjustment work is called BLC(Black Level Compensation).

10. ISP(Image Signal Processing)

10.1. Overview

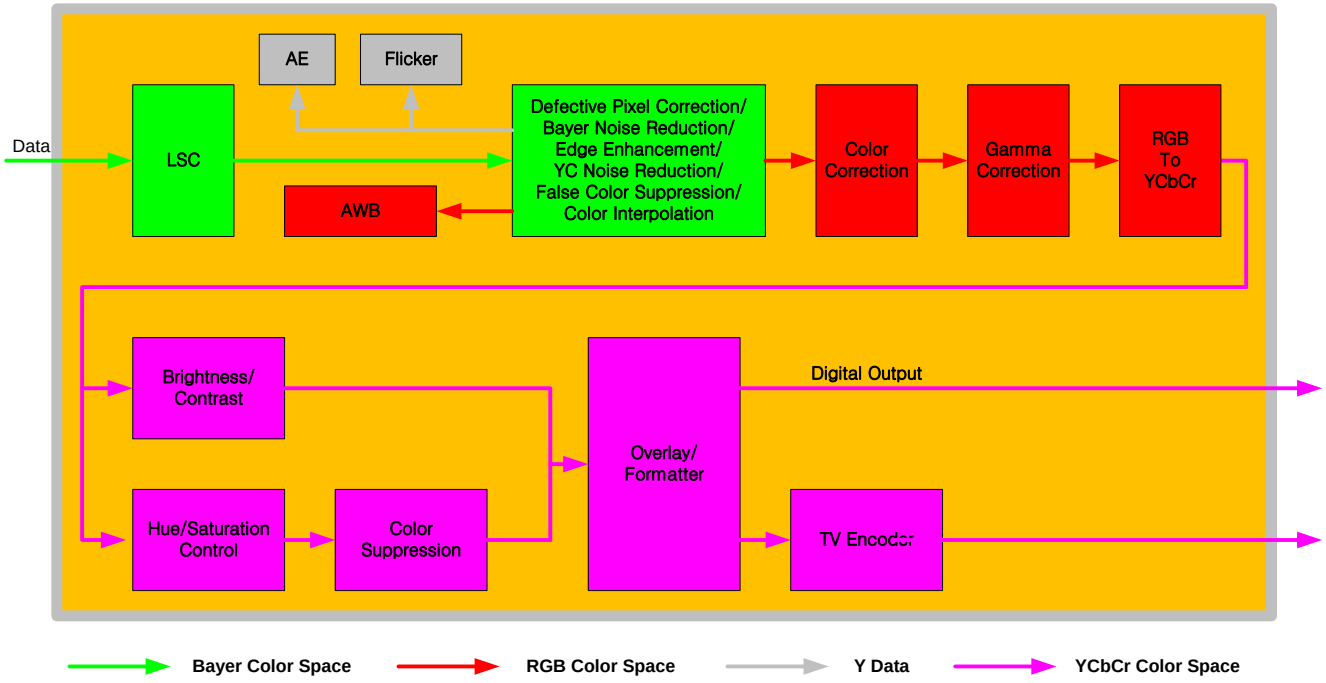


Figure 10-1 ISP Block Diagram

ISP (Image Signal Processing) carries out a function whereby the 10 bit data input from the sensor is converted into RGB and image processed to be output again. As shown in Figure 10-1 Figure 10-1 ISP Block Diagram, the input video data is processed together with Y and RGB data for Auto Exposer(AE) and Auto White Balance (AWB), through LSC and WDR blocks. Bayer format data goes through interpolation part to be converted to R[9:0], G[9:0], B[9:0].

R, G, B data interpolated are transformed into 8 bit data after color correction and gamma correction of each R, G, and B, and transformed R, G, B data are then transformed into brightness signal Y and color difference Cb, Cr signals through RGB2YC block. Therefore the bayer format video data input from the sensor is transformed into brightness and color difference singals, and that brightness (Y) and color difference(Cr/Cb) are used to enhance image quality per user request. Transformed data can be output in either of YCrCb 4:2:2, RGB565 or RGB555, Bayer formats.

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10.2. LSC(Lens Shading Compensation)

As camera modules get smaller by trend, small external lens and large f number optical devices experience image distortion due to geometrical arrangement of pixel array.

Pixels of image sensor RGB Color Filter Array (CFA) center and edges are subject to light from different directions. These minute location differences cause illumination differences, and illumination differences also affect color due to light wave and micro lens curvature differences. As a result, color distortion that forming FCA and signal size decrease dependant on the pixel location inevitably happens, and this causes the image quality fall in the original image.

10.2.1. Gain for LSC

Lens shading correction performs correction of a lens shading distortion due to gradual brightness differences from the center to the edges. Lens shading correction gain uses the ar2 function whereby r is a distance between the center and the relevant coordinates. Normally, the lens shading correction gain error increases from center to the edges, this error can be compensated by using gain. Gain control for adjusting CP7208 distortion can control each of R, Gr, Gb, B of large and small pixels. (LSC register : 0x5204 ~ 0x5207)

10.2.2. LSC Centering

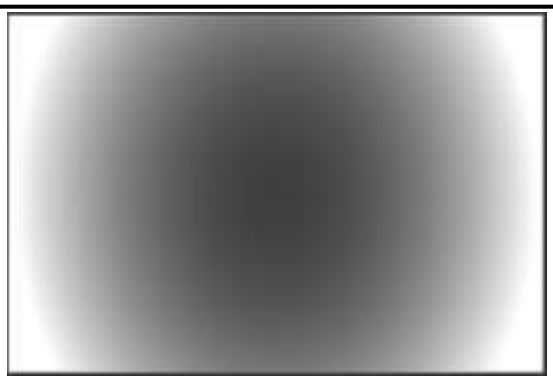
Compensates for the differnece bewween the center of the pixel array and the center of the lens. CP7208 provides register (LP:0x5201~0x5203) for LSC center.

10.2.3. LSC Weighting

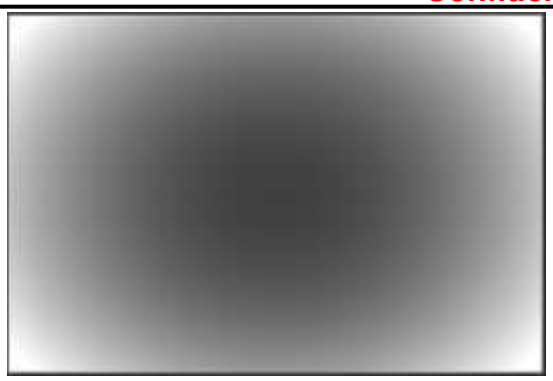
CP7208 has a width:height ratio of 1:1.12 with height being greater. Hence when compensating for shading, 1.12 of weight needs to be applied on the width or 0.88 of weight on the height. For design convenience, 1.125 or 1.0625, 1.25 of weight can be applied. Also, different weights for each of width and height can be applied.

The horizontal axis weight ratio : LSC_CON[2] = 1’b0 => 0%
=if 1’b1 => 12.5%(LSC_CON[4]: ‘0’, -12.5%)

The vertical axis weight ratio : LSC_CON[1] = 1’b0 => 0%
= if 1’b1 => 12.5% (LSC_CON[3]: ‘0’, -12.5%)



(a) Width 12.5% weighting



(b) Height 12.5% weighting

Figure 10-2 LSC Weighting

10.3. ISP1

ISP1 (Image Signal Processing1) receives Bayer format 10 bit data as input, converts it to RGB or YCbCr and outputs after image processing. Bayer format data passes through interpolation part a nd is converted into R[9:0], G[9:0], B[9:0]. RGB data is converted into YCbCr data through RGB2 YCbCr block, and the Hue/Saturation block controls Hue, Saturation, Contrast and Brightness.

10.3.1. Defect Pixel Compensation(DPC)

DPC is Blocks that finds defect pixels, and corrects it using the surrounding pixels. DPC used in CP7208 determines defect pixels by comparing color of pixels in a 5x5 window with the center pixel to correct it.

10.3.2. Color Interpolation

Color Interpolation is a block which acquires color from surrounding pixels if a pixel only has single color information. CP7208 Interpolation block, in addition to CP7208 Interpolation function has functions including YC noise reduction, Edge Enhancement, False Color Suppression, and RGB gain for White Balance.

10.3.3. YC Noise Reduction

YC noise reduction classifies between the plane section and edge section of a video to blur the plane section while maintaining the edge to reduce image noise. This function can be set on Register(0x5500).

10.3.4. Edge Enhancement

Edge enhancement function is to increase sharpness of the image. Edge Enhancement of CP7208 is controlled by 0x550C~0x550D YMGAIN and YHGAIN of register. YMGAIN controls gain of middle frequency edge of video, YHGAIN controls gain of high frequency edge of video. Corring is to set corring level to register(0x550A~0x550B) and does not allow an edge value less than corring level on the video.

10.3.5. Color Correction

Color Correction controls of color balance of acquired image to suit the target color checker. When AWB is performed, the image brightness ingredients changes and color correction needs to be performed as well.

$$\begin{bmatrix} Rout \\ Gout \\ Bout \end{bmatrix} = \begin{bmatrix} cc00 & cc01 & cc02 \\ cc10 & cc11 & cc12 \\ cc20 & cc21 & cc22 \end{bmatrix} x \begin{bmatrix} Rin \\ Gin \\ Bin \end{bmatrix}$$

Figure 10-3 Color Correction Matrix

The above equation is about the color correction. As shown above, the input color signals are adjusted to each offset values and are transformed by the color correction matrix. Each coefficient of the matrix can be set as negative value or positive value depending on the sign bit (MSB of each coefficient). In

case of a negative number, it is in a form of two's complement. The coefficients which are expressed in 6bit (except sign and overflow bytes) can be divided into 64, and each coefficient value range is -2 ~ 1.984. An appropriate coefficient is found and set depending on each image system lens, IR filter, and sensor type. When configuring each coefficients, CC_00 = {CC_01 + CC_02}, CC_11 = {CC_10 + CC_12}, CC_22 = {CC_20 + CC_21} need all to be set as same values to maintain white balance.

With actual CP7208, Color Correction Matrix of each light source are saved on the firmware and applied depending on the light source.

10.3.6. Gamma Correction

CP7208 supports the following GAMMA MODE. 19 registers are applied for gamma. Gamma control register is defined in 0x5710 ~0x5722.

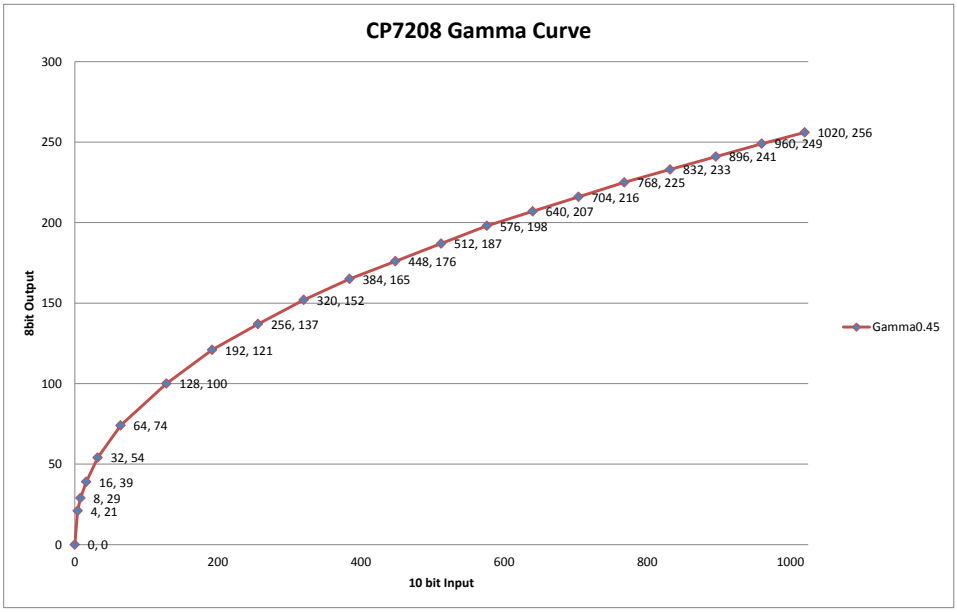


Figure 10-4 GAMMA register and GAMMA value

Figure 10-4 shows that 19 points on Y axis are mapped by the value entered in the register.

10.3.7. RGB to YCbCr

RGB to YcbCr block converts RGB to Y, Cb, Cr by below equation.

Y601 = 0.299*R + 0.587*G + 0.114*B
Cb = -0.169*R – 0.331*G + 0.500*B + 128
Cr = 0.500*R – 0.419*G – 0.081*B + 128
R,G,B are in 0~255 range
Y601 is in 0~255 range (0-255, offset=0)
Cb, Cr are in 0~255 range (+/- 127, offset=0)

Figure 10-5 SDI Equations

10.4. ISP2

ISP2 (Image Signal Processing2) receives output YC format from ISP1 block as input. The input data is performed to the image quality improvement function such as Brightness, Black Enhancement, White Enhancement, Contrast, Hue, Saturation, Color Suppression according to the user's needs.

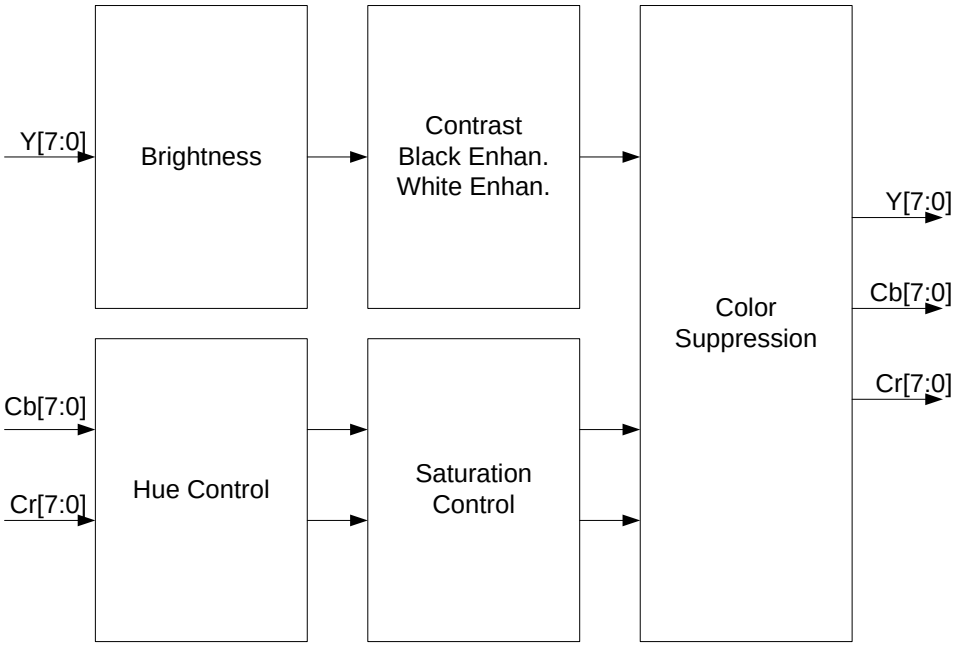


Figure 10-6 ISP2 Block Diagram

10.4.1. Brightness Control

Brightness control gives offset to the image luminance to control the brightness of the image, and the size of the offset can be chosen between -128~127.

10.4.2. Contrast Control

Contrast control block is based on the reference point luminance, and controls the contrast by reducing the luminance of areas where luminance is lower than the reference point, and increasing the luminance of areas where luminance is above the reference point. Reference point normally used is 128, and can be changed depending on the situation. Contrast gain can be applied in 0~2x ranges.

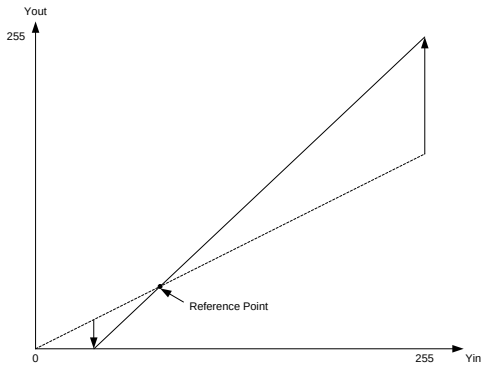


Figure 10-7 Contrast control

10.4.3. Cb/Cr Gain

Cb/Cr gain control moves current color difference information towards Cb axis or Cr axis by apply ing saturation gain on color coordinates. Cb/Cr gain can be applied in 0~2x ranges.

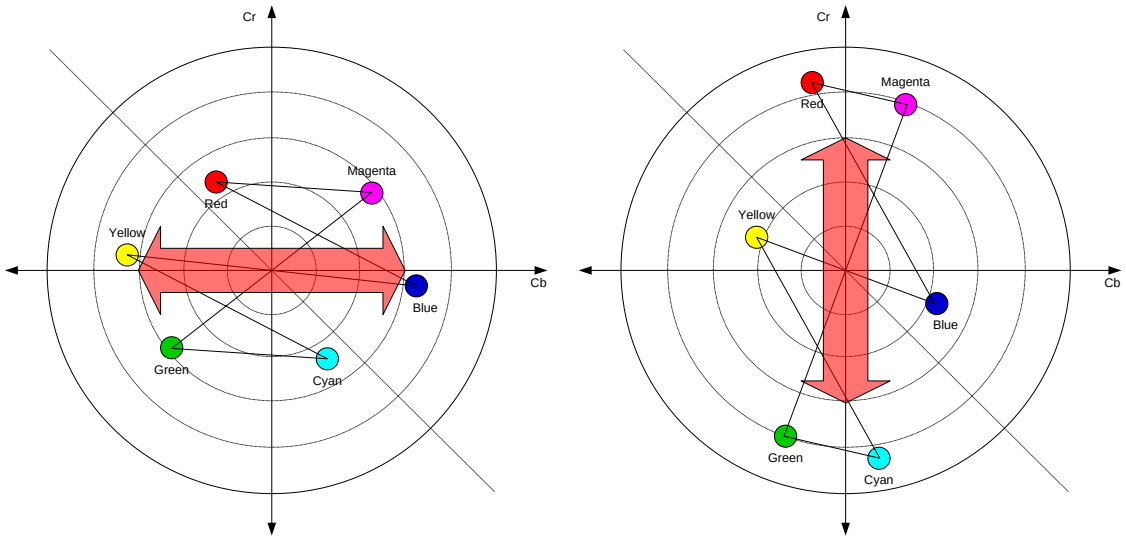


Figure 10-8 Cb/Cr gain control

10.4.4. Hue Control

Hue control is used for global or individual color information change. Hue can be changed betwe en −45°~+45° in 1° units and uses 2’s complement.

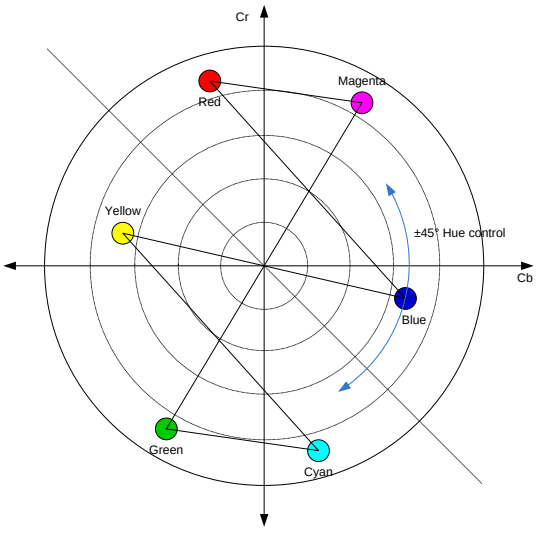


Figure 10-9 Hue control

10.4.5. Saturation Control

Saturation control is used to control the image saturation. Saturation gain can be applied in 0~2x ranges.

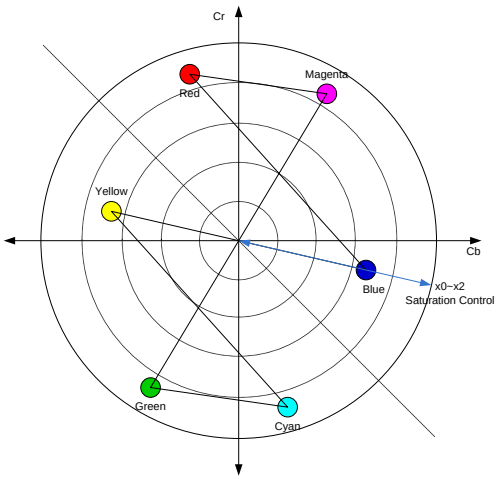


Figure 10-10 Saturation control

10.4.6. Black Enhancement

Black Enhancement makes dark areas of the image darker by making Black color level more Black, and it preserves data in the lighter areas than Contrast Control and can reduce the Minimum Black Level of the image.

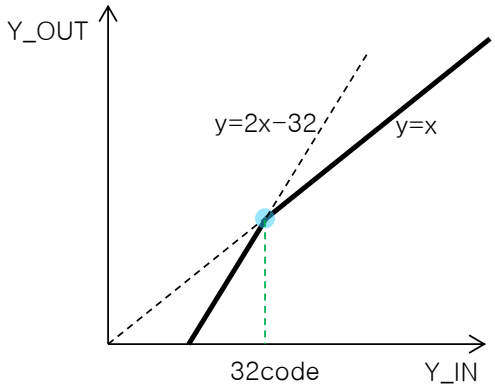


Figure 10-11 Black Enhancement Control

10.4.7. White Enhancement

White Enhancement makes bright areas of the image brighter by making White color level more White, and it preserves data in the darker areas than Contrast Control and can reduce the Minimum Black Level of the image.

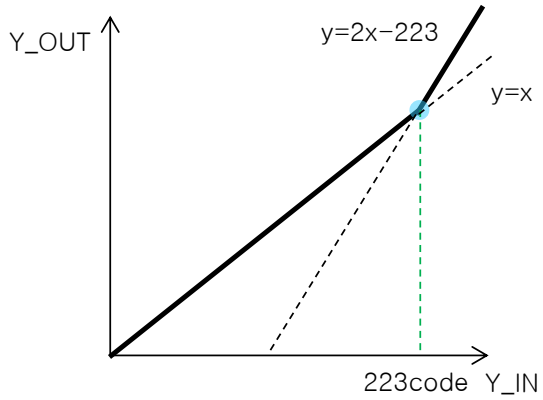


Figure 10-12 White Enhancement Control

10.4.8. Color Suppression

11. Color Suppression function is a function to reduce the color component when luminance is too high or low or if there is unwanted color noise.
12. Threshold value and gain control is possible on each of Cb and Cr.

Cb => threshold low : ‘ h6103　　thresold high : ‘ h6101
gain low : ‘ h6104　　gain high : ‘ h6102

Cr => threshold low : ‘ h6108　　threshold high : ‘ h6106
gain low : ‘ h6109　　gain high : ‘ h6107

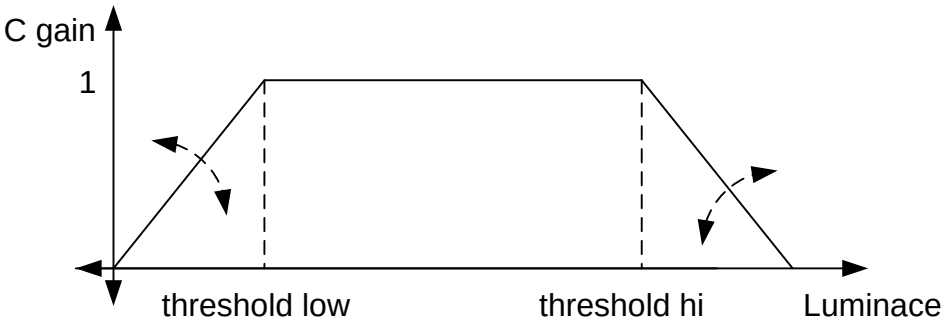


Figure 10-13 Applying Gain on Luminance Threshold

12.1. Privacy Zone

Privacy zones were designed to protect privacy in using CCTV or other.

Rectangular masks are output instead of the sensor output at user designated locations. As shown in Figure 10-14 each mask may determine the size by setting the coordinate of the top left, low right, and can be set for each color to yuv. Up to 8 of these masks can be set, and when the different color masks overlap, the mask with the smaller internal mask number takes priority.. Figure 10-15 is an example of a privacy zone set.

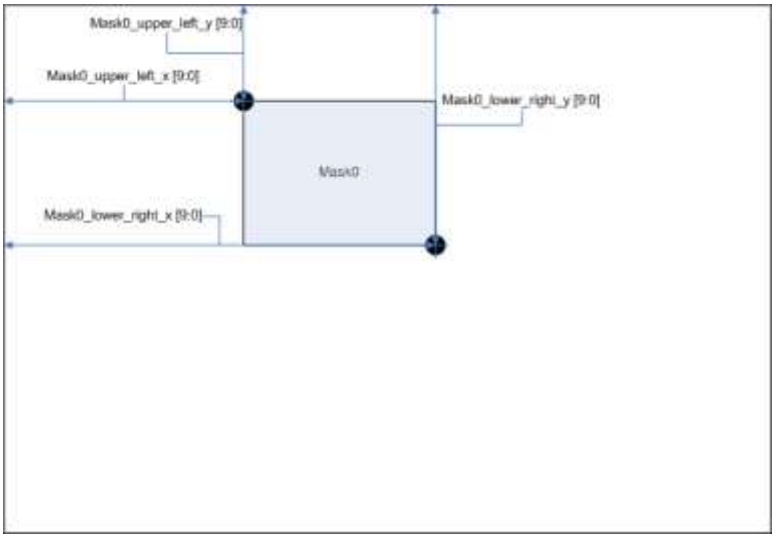


Figure 10-14 How to set position of Privacy Zone

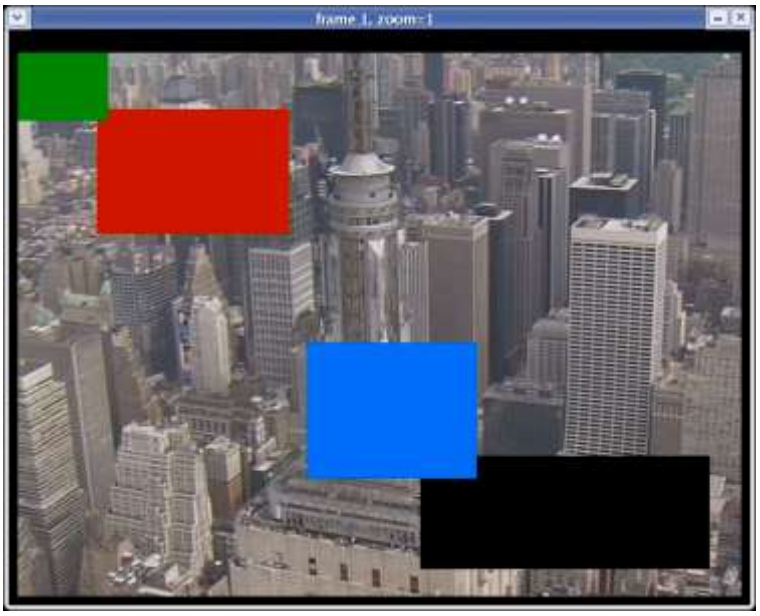


Figure 10-15 Privacy Zone Example

13. Overlay

13.1. Overlay configuration

It supports total 3 overlay plane, which uses data converted from original bitmap file to RLE(Run Length Encoding). Its overlay functions are below;

- Supports overlay data max. 2 KByte(overlay 1,2) and 256 byte(overlay 3)
- Extends max. 360x480 size overlay image to 720x480
- Can set 4 types of alpha blending (25%, 50%, 75%, 100%)
- Supports 8 color palettes for 1 bitmap
- 8 color palettes is composed Y, Cb, Cr 8 bit register
- Overlay positioning possible
- Can be set Overlay location
- Supports blink function with 1~256 frame cycle for overlay 3 image.
- Uses bitmap data
- Uses bitmap data compressed with RLE
- RLE data is expressed with odd line and the color of even line.
- Supports LUT for 4 color patters
- Uses 4 types of command through flag bit
- Available only CCIR656 and NTSC, PAL output.
- When initial booting, overlay data is downloaded from EEPROM to internal SRAM.

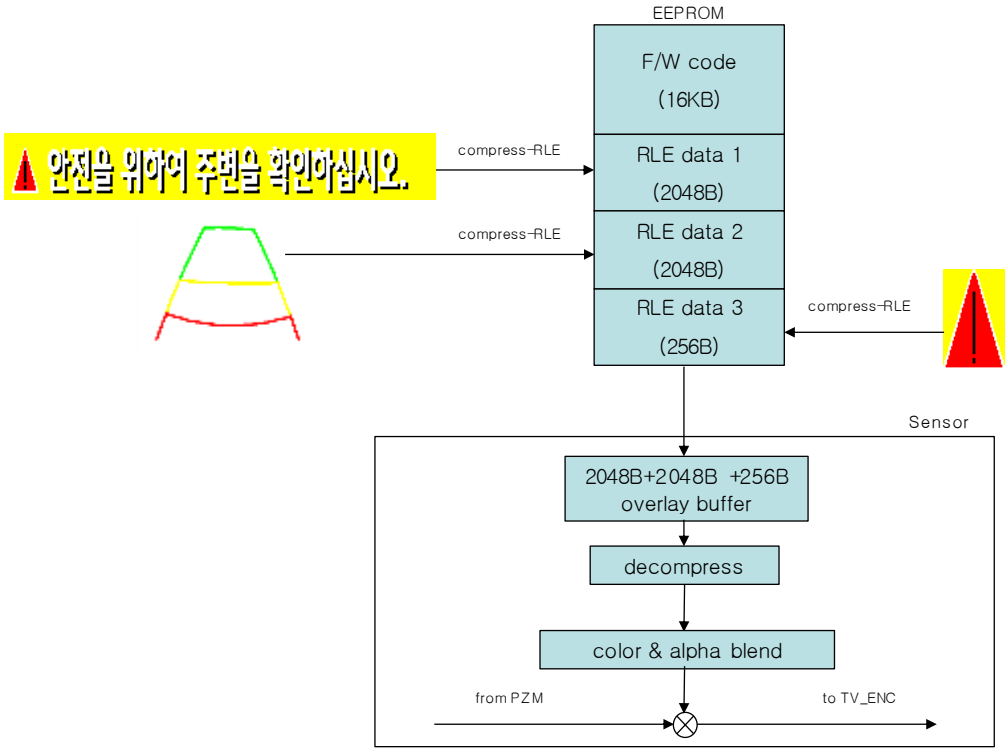


Figure 13-1 Overlay block diagram

13.2. RLE compress Command

RLE is compressed according to bitmap pattern by four commands as shown Table 13-1.

command	repetition	Command structure	Size
command_0	1pixel	1 0 | odd color[2:0] | even color[2:0]	1byte
command_1	2~32pixel & LUT pattern	0 | LUT[1:0] | Repetition[4:0]	1byte
command_2	2~64pixel or Not LUT	1 1 | Repetition[5:0] 1 0 | odd color[2:0] | even color[2:0]	2byte
command_3	65pixel ~	1 1 | Repetition[5:0] 1 1 0 | Repetition[10:6] Repetition[12:11] | odd color[2:0] | even color[2:0]	3byte

Table 13-1 RLE compress Command

Figure 13-2 is shown an example of LUT configuration including 4 color patters.

LUT color pattern

i) White(글자) :000
ii) Blank(바탕) :001
iii) Black(그림자) :010
iv) Red (이미지) :100

LUT[1:0]	Odd color	Even color
00	000	000
01	001	001
10	010	010
11	100	100

Figure 13-2 Example of LUT configuration

13.3. Setting position and size of overlay

Overlay position and size settings can be set as shown below, overlay 1,2,3, setting method is same.

- overlay start point
  : Can be set OVERLAY_START_X_H, OVERLAY_START_X_L
  OVERLAY_START_Y_H, OVERLAY_START_Y_L register
  : X point can be set to 1 pixel increments (0, 1, 2, 3 ……)
  : Y point can be set to 2 line increments (0, 2, 4, 6 ……)
- overlay X length
  : Can be set OVERLAY_LENGTH_X_H, OVERLAY_LENGTH_X_L register
  : Double set of X size of the overlay image.
- overlay Y length
  : Can be set OVERLAY_LENGTH_Y_H, OVERLAY_LENGTH_Y_L register
  : Same set of Y size of the overlay image

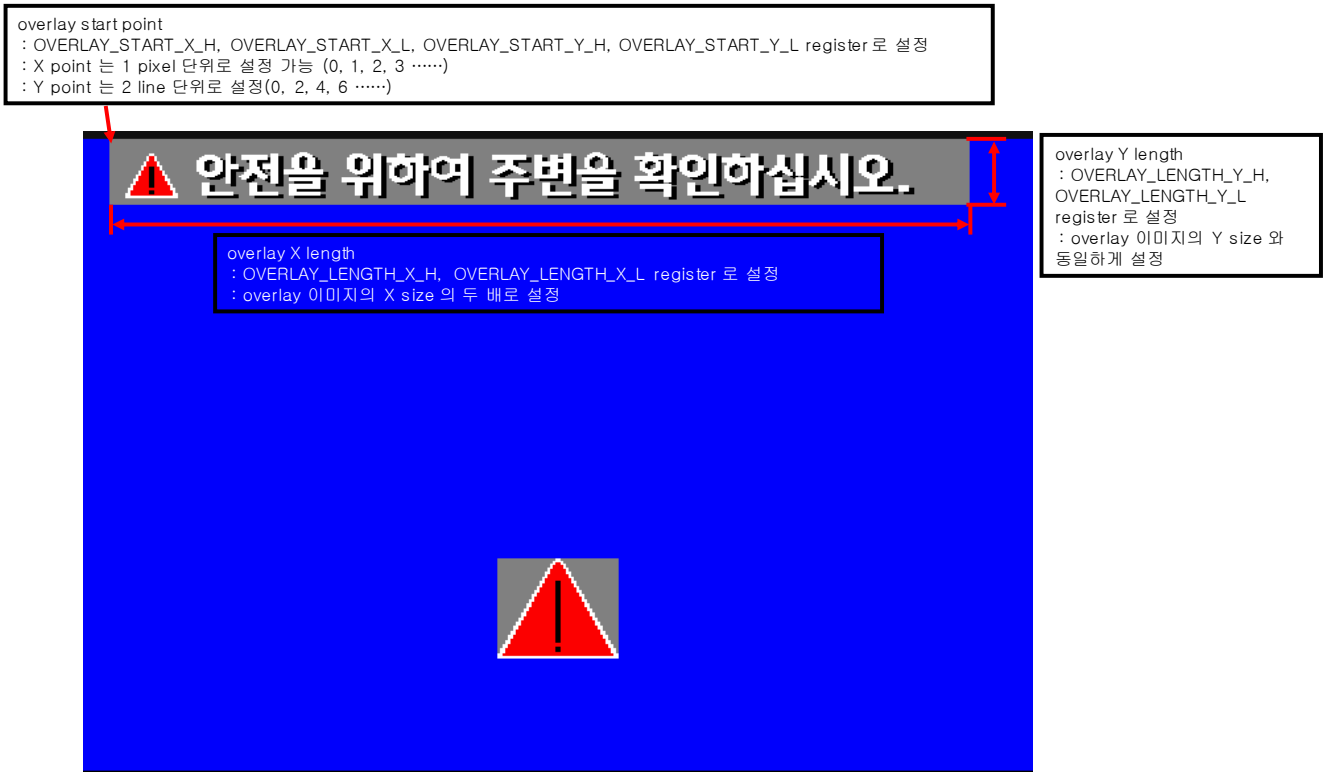


Figure 13-3 Setting position and size of overlay

14. Formatter

14.1. Overview

Major functions of formatter block are below:

- Bayer 8/10 bit
- YCbCr 4:2:2
- RGB565/555
- CCIR656
- VGA mode
- Vsync/Hsync/pclock polarity control
- Hsync control in VBLANK
- OPB(Optical Black) data output control
- Pixel data sequence control
- Bit position control when the output data is 8 bit

CP7208 receives Y, C data and can output Bayer 8/10 bit, YCbCr 4:2:2 and RGB565/555 format digital data. Digital data can be output in 720x480, 640x480 modes. In NTSC/PAL mode operation, horizontal, vertical stretch or CCIR656 output is supported to suit NTSC/PAL output format. In addition the polarity of Vsync/Hsync/pclock signals can be controlled and the output data sequences can be set in a preferred order. When in 8 bit output mode, the 8bit data MSB location can be changed.

14.2. Timing Diagram

- YCbCr 4:2:2 mode

CbCr 4:2:2 format data can be output through the PDATA[9:0] port. Since the final output is 8 bit, only 8 port out of the PDATA 10bit port is used and 8 bit data location can be changed using PDATA_CON[1:0] value. Also, depending on the DATA_FMT_CON[4:3] register value, the data sequence can be changed as shown in Figure 14-1.

Since Y and Cb or Y and Cr represent a single pixel value, the internal operation clock is to be setting 1/2 of pclock.

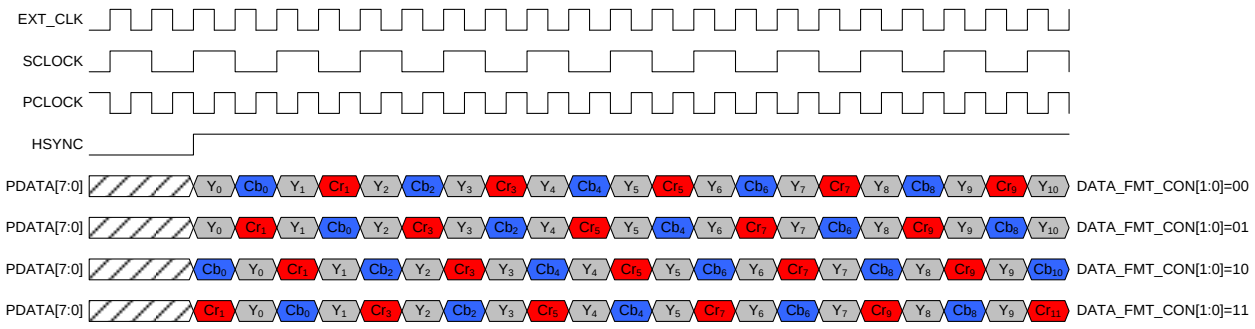
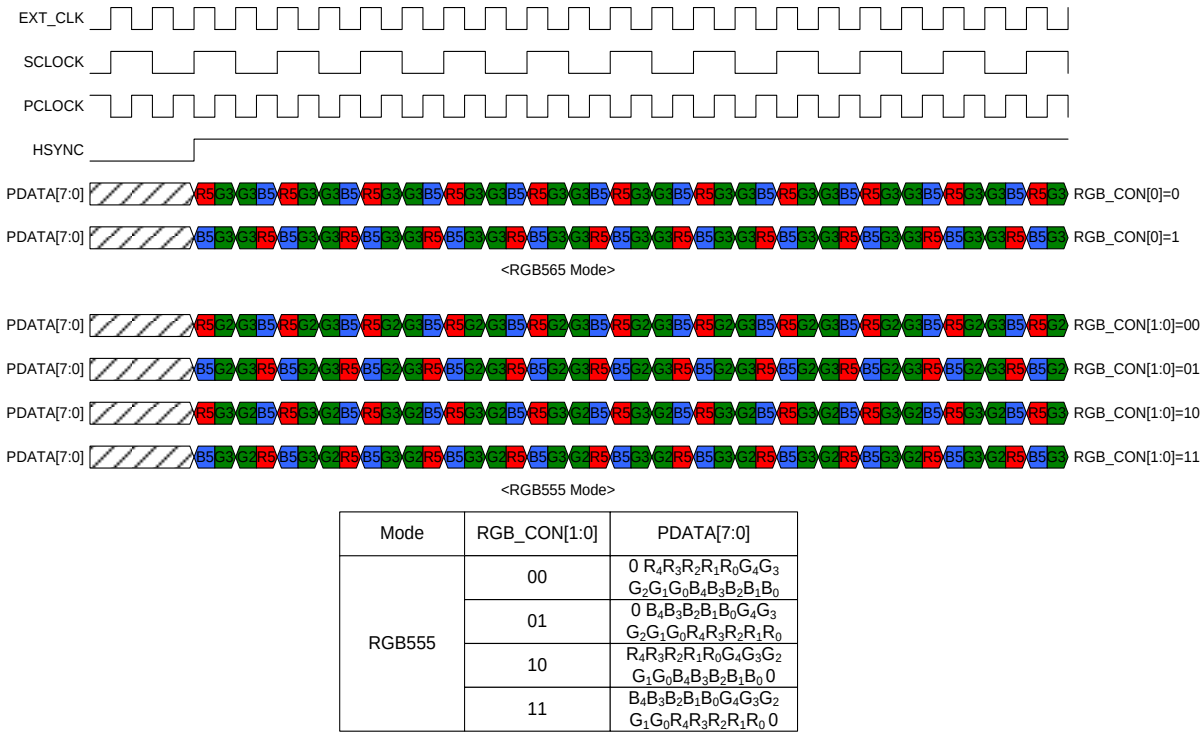


Figure 14-1 YCbCr Mode

- RGB565/555

RGB565/555 format data can be output through the PDATA[9:0] port. The final output is 8 bit in case of RGB565, and 8 or 7 bit in case of RGB555, and thus the output data location can be decided using the RGB_CON[1] value of the 10bit port PDATA. Also, depending on the RGB_CON[0] register value, the data sequence can be changed as shown below in Figure 14-2.



Mode	RGB_CON[1:0]	PDATA[7:0]
RGB555	00	0 $R_4R_3R_2R_1R_0G_4G_3$ $G_2G_1G_0B_4B_3B_2B_1B_0$
	01	0 $B_4B_3B_2B_1B_0G_4G_3$ $G_2G_1G_0R_4R_3R_2R_1R_0$
	10	$R_4R_3R_2R_1R_0G_4G_3G_2$ $G_1G_0B_4B_3B_2B_1B_0$ 0
	11	$B_4B_3B_2B_1B_0G_4G_3G_2$ $G_1G_0R_4R_3R_2R_1R_0$ 0

Figure 14-2 RGB565/555 Mode

- Bayer 8bit/10bit

Bayer 8 bit/10 bit format data can be output through the PDATA[9:0] port. Final output of Bayer 8 bit is 8 bit and so only 8 ports of 10 bit port PDATA is used and 8 bit data location can be decided using the PDATA_CON[1:0] value. Also, depending on the RGB_CON[3:2] register value, the data sequence can be changed as shown below in Figure 14-3.

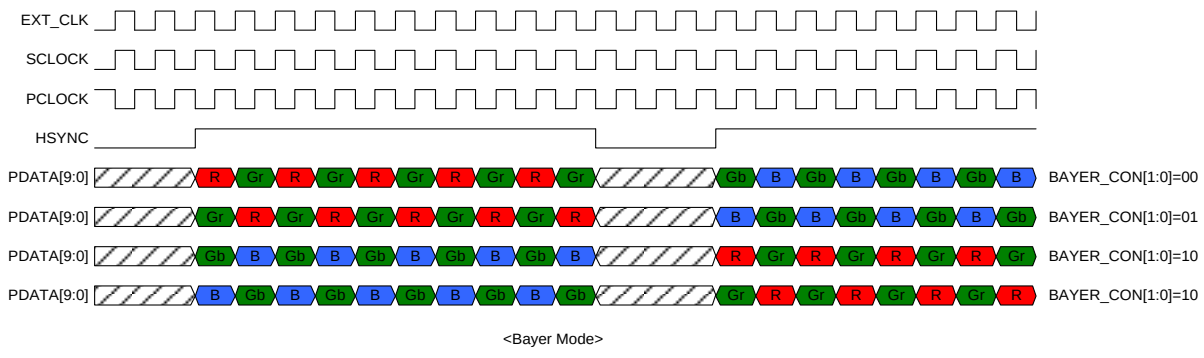


Figure 14-3 Bayer 8/10 bit Mode

14.3. Windowing

In 640x480 mode output, windowing function can be used to output the preferred section. Figure 14-4 is an example of a windowing control in 640x480 mode..

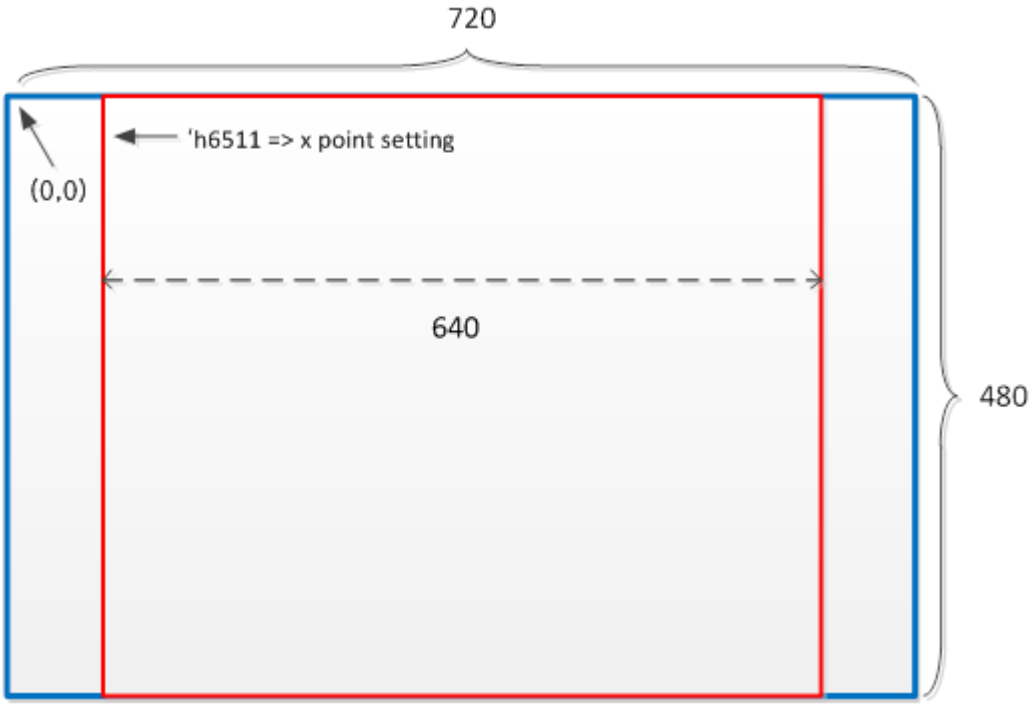


Figure 14-4 windowing control

15. Auto Control Function

CP7208has auto control functions such as AE, Anti-Flicker, and AWB. These functions are not all processed in the ISP block, but transfers the information to the MCU that can operate the auto control algorithm. As shown in Figure 15-1, the brightness(Y) data for Anti-Flicker and RGB data for AWB are transferred to the MCU and depending on the calculation results of each algorithm, expose time, and RGB gain are performed.

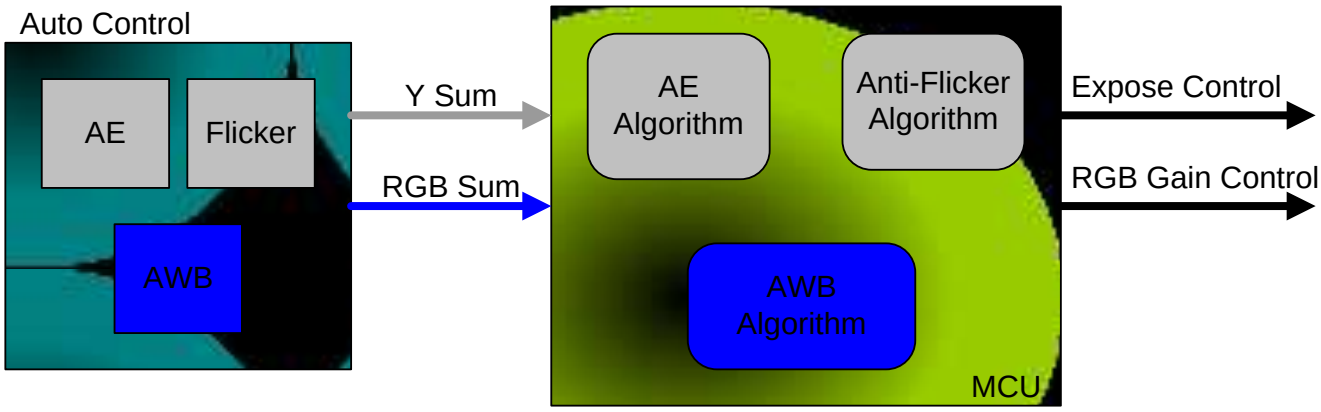


Figure 15-1 Auto Control Function

16. Register definition

16.1. System

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
0x4000	PRODUCT_ID1	R	0x72	Product ID1
0x4001	PRODUCT_ID2	R	0x08	Product ID2
0x4002	PRODUCT_ID3	R	0x10	Product ID3
0x4003	PIXEL_TYPE	R	0xA0	bit[7:0] : pixel type and revision number
0x4004	CLOCK_CONFIG	R/W	0xE5	[7] : crystal enable [6:5] : crystal output drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [4] : soft reset [3:2] : Sensor Clock 00 : Ext Clock 01 : Ext Clock / 2 10 : Ext Clock / 4 11 : reserved [1:0] : Main Clock 00 : Ext Clock 01 : Ext Clock / 2 10 : Ext Clock / 4 11 : reserved
0x4005	DEVICE_CONTROL	R/W	0x02	[7] : sleep [6] : power down mode selection [5] : pull down if powerdown at gpio & pbus [4] : TV out enable [3] : ISP enable [2] : TG enable [1] : MCU reset [0] : MCU enable
0x4006	I2C_SLAVE_ID	R/W	0x77	I2C Slave Device ID Value ID = [Value[7:1], R/W Flag[0]]
0x4007	I2C_SLAVE_LAST_INDEX	R	0x00	I2C Last Index address
0x4008	I2C_SLAVE_GLITCH	W	0x08	I2C slave glitch
0x4009	I2C_MASTER_START_REG	W	0x00	[7:1] : reserved [0] : i2c master start
0x400A	I2C_MASTER_STATUS	R	0x00	I2C Status register 0x00 : IDLE 0xAA : Transmit Success 0xBB : Transmit Fail 0xCC : I2C Line Busy
0x400B	I2C_MASTER_CONTROL	R/W	0xC0	I2C Master Control [2:0] : Transmit Byte Select 000 : 1 Byte Transfer 001 : 2 Byte Transfer 010 : 3 Byte Transfer 011 : 4 Byte Transfer 1xx : 5 Byte Transfer [3] : Dummy Write On [4] : Read Restart On [7:5] : I2C Clock Ratio Select

[7:5]	Trans	act	grap	End
3'b000	10'd100	10'd200	10'd300	10d'400

				3'b001 / 10'd150 / 10'd300 / 10'd450 / 10d'600 3'b010 / 10'd200 / 10'd400 / 10'd600 / 10d'800 3'b011 / 10'd250 / 10'd500 / 10'd750 / 10d'1000 3'b100 / 10'd50 / 10'd100 / 10'd150 / 10d'200 3'b101 / 10'd25 / 10'd50 / 10'd75 / 10d'100 3'b110 / 10'd12 / 10'd24 / 10'd36 / 10d'48 3'b111 / 10'd6 / 10'd12 / 10'd18 / 10d'24
0x400C	I2C_TARGET_ADDRESS	R/W	0x00	I2C target device id
0x400D	I2C_TARGET_INDEX	R/W	0x00	I2C target Index
0x400E	I2C_TARGET_DATA1	R/W	0x00	I2C target data1
0x400F	I2C_TARGET_DATA2	R/W	0x00	I2C target data2
0x4010	I2C_TARGET_DATA3	R/W	0x00	I2C target data3
0x4011	I2C_TARGET_DATA4	R/W	0x00	I2C target data4
0x4012	I2C_TARGET_DATA5	R/W	0x00	I2C target data5
0x4013	EEPROM_CONFIG	R/W	0x00	[7:1] : reserved [0] : eeprom disable
0x4014	I2C_TARGET_RDATA_H	R	0x00	I2C target Read data[15:8]
0x4015	I2C_TARGET_RDATA_L	R	0x00	I2C target Read data[7:0]
0x4016	LUMP_INTERVAL	R/W	0x00	Interval[3:0] / Interval decision value 4'b1111 / 11'd50 4'b1110 / 11'd100 4'b1101 / 11'd150 4'b1100 / 11'd200 4'b1011 / 11'd250 4'b1010 / 11'd300 4'b1001 / 11'd350 4'b1000 / 11'd400 4'b0111 / 11'd450 4'b0110 / 11'd500 4'b0101 / 11'd550 4'b0100 / 11'd600 4'b0011 / 11'd700 4'b0010 / 11'd800 4'b0001 / 11'd900 4'b0000 / 11'd1023
0x4017	HOST_COMMAND_FLAGS	W	0x00	[7:0] : Host command flags When write, it generates MCU interrupt. When read, it clears MCU interrupt.
0x4018	HOST_COMMAND_DATA0	W	0x00	[7:0] : Host command data 0
0x4019	HOST_COMMAND_DATA1	W	0x00	[7:0] : Host command data 1
0x401A	HOST_COMMAND_DATA2	W	0x00	[7:0] : Host command data 2
0x401B	HOST_COMMAND_RESULT0	R/w	0x00	[7:0] :Command Result 0
0x401C	HOST_COMMAND_RESULT1	R/W	0x00	[7:0] :Command Result 1
0x401D	HOST_COMMAND_RESULT2	R/W	0x00	[7:0] :Command Result 2
0x401E	HOST_COMMAND_RESULT3	R/W	0x00	[7:0]: Command Result 3
0x401F	GPIO_DIRECTION_CONTROL	R/W	0xFF	[7:0] : GPIO[7:0] direction control 0 :output 1 : input
0x4020	GPIO_IN_OUT_DATA	R/W	0x00	[7:0] : GPIO[7:0] input/output data

0x4021	GPIO_PULL_UD_CON	R/W	0xFF	[7:0] : GPIO[7:0] pull up/down control 0 :disable 1 : enable
0x4022	GPIO_PULL_UD_SEL	R/W	0x00	[7:0] : GPIO[7:0] pull up/down selection 0 : pull-down 1 : pull-up
0x4023	GPIO_DRIVE_STRENGTH_SEL	R/W	0x55	[7:6] : GPIO[7:6] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [5:4] : GPIO[5:4] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [3:2] : GPIO[3:2] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA [1:0] : GPIO[1:0] drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA
0x4024	MEM_ADDR_H	R/W	0x00	[7:0] : High byte of memory address
0x4025	MEM_ADDR_L	R/W	0x00	[7:0] : Low byte of memory address
0x4026	MEM_DATA	R/W	0x00	[7:0] : memory data
0x4027	MEM_CON	R/W	0x00	[7:4] : reserved [3] : fix index address (“1” -> i2c index address is fixed) [2] : reserved [1] : code memory write enable. [0] : code or data memory selection 0 : data 1 : code
0x4028	CHECK_SUM_H	R/W	0x00	[7:0] : High byte of code data check sum
0x4029	CHECK_SUM_L	R/W	0x00	[7:0] : High byte of code data check sum
0x402A	CRC_H	R/W	0x00	[7:0] : High byte of code data CRC
0x402B	CRC_L	R/W	0x00	[7:0] : Low byte of code data CRC
0x402C	CRC_CON	R/W	0x00	[7:1] : reserved [0] : CRC control 0 : disable 1 : enable
0x4054	PDATA_CON1	R/W	0xA0	[7:6] : P_1_0 control 00 : output PDATA[1:0] 01 : floating PDATA[1:0] 10 : floating & pull-down PDATA[1:0] 11 : reserved [5:4] : P_9_2 control 00 : output PDATA[9:2] 01 : floating PDATA[9:2] 10 : floating & pull-down PDATA[9:2] 11 : reserved [3] : DAC test mode [2] : PLL test mode [1:0]: reserved

0x4055	PDATA_CON2	R/W	0x01	[7] : GPIO[2] to PCLOCK 0 : disable 1 : enable [6] : GPIO[3] to VSYNC 0 : disable 1 : enable [5] : GPIO[4] to HSYNC 0 : disable 1 : enable [4] : GPIO[5] to PDATA[0] 0 : disable 1 : enable [3] : GPIO[6] to PDATA[1] 0 : disable 1 : enable [2] : GPIO[7] to PDATA[2] 0 : disable 1 : enable [1:0] : PDATA drive strength selection 00 : 1mA 01 : 2mA 10 : 4mA 11 : 8mA
0x4080	RESULT_0	R/W	0x00	result 0
0x4081	RESULT_1	R/W	0x00	result 1
0x4082	RESULT_2	R/W	0x00	result 2
0x4083	RESULT_3	R/W	0x00	result 3
0x4084	RESULT_4	R/W	0x00	result 4
0x4085	RESULT_5	R/W	0x00	result 5
0x4086	RESULT_6	R/W	0x00	result 6
0x4087	RESULT_7	R/W	0x00	result 7
0x4088	RESULT_8	R/W	0x00	result 8
0x4089	RESULT_9	R/W	0x00	result 9
0x408A	RESULT_10	R/W	0x00	result 10
0x408B	RESULT_11	R/W	0x00	result 11
0x408C	RESULT_12	R/W	0x00	result 12
0x408D	RESULT_13	R/W	0x00	result 13
0x408E	RESULT_14	R/W	0x00	result 14
0x408F	RESULT_15	R/W	0x00	result 15
0x4090	RESULT_16	R/W	0x00	result 16
0x4091	RESULT_17	R/W	0x00	result 17
0x4092	RESULT_18	R/W	0x00	result 18
0x4093	RESULT_19	R/W	0x00	result 19
0x4094	RESULT_20	R/W	0x00	result 20
0x4095	RESULT_21	R/W	0x00	result 21
0x4096	RESULT_22	R/W	0x00	result 22
0x4097	RESULT_23	R/W	0x00	result 23
0x4098	RESULT _24	R/W	0x00	result 24
0x4099	RESULT_25	R/W	0x00	result 25
0x409A	RESULT_26	R/W	0x00	result 26
0x408B	RESULT_27	R/W	0x00	result 27
0x409C	RESULT_28	R/W	0x00	result 28
0x409D	RESULT_29	R/W	0x00	result 29
0x409E	RESULT_30	R/W	0x00	result 30
0x409F	RESULT_31	R/W	0x00	result 31

16.2. TG, BLC

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
TG **(VSYNC SYNCHRONIZED)**				
0x5000	INT_TIME_H	R/W	0x01	[7:4] : reserved [3:0] : High byte of pixel Integration(Exposure) time
0x5001	INT_TIME_L	R/W	0xF8	[7:0] : Low byte of pixel Integration(Exposure) time
0x5002	HBLANK	R/W	0x78	[7:0] : Horizontal blank NTSC : 0x78 PAL : 0x2C
0x5003	HDUMMY	R/W	0x00	[7:5] : reserved [4] : High byte of horizontal blank NTSC : 0 PAL : 1 [3:0] : Horizontal dummy NTSC : 0x0 PAL : 0xF
0x5004	VBLANK_ODD	R/W	0x06	[7:0] : Odd Field Vertical blank NTSC : 0x06 PAL : 0x02
0x5005	VBLANK_EVEN	R/W	0x06	[7:0] : Even Field Vertical blank NTSC : 0x06 PAL : 0x02
0x5006	VDUMMY_ODD	R/W	0x03	[7:0] : Odd Field Vertical dummy NTSC : 0x03 PAL : 0x02
0x5007	VDUMMY_EVEN	R/W	0x03	[7:0] : Even Field Vertical dummy NTSC : 0x03 PAL : 0x02
0x5008	A1_GAIN	R/W	0x3F	[7:6] : reserved [5:3] : pre-amp gain C2 cap [2:0] : pre-amp gain C1 cap
0x5009	A2_GAIN	R/W	0x03	[7] : reserved [6:3] : coarse analog gain [2:0] : fine analog gain
0x500A	D_GAIN	R/W	0x00	[7:5] : Global Digital Gain1 control [4:0] : Global Digital Gain2 control Gain = 2^D_GAIN[7:5]*(1 + D_GAIN[4:0]/32)
0x500B	IMG_CON	R/W	0x00	[7:2] : reserved [1] : Vertical mirror [0] : Horizontal mirror
0x5060	TP_IMG_CON	R/W	0x00	[7:6] : reserved [5] : Test Image Enable (0 : disable, 1 : enable) [4] : reserved [3] : Test Image Data Select 0 : read out address 1 : int. address [2:0] : Test Image Type 000 : diagonal 001 : horizontal 010 : vertical 011 : single color 100 : color bar 101 : gray chart
0x5061	TP_IMG_HI	R/W	0x03	[7:6] : High byte of R color for test image [5:4] : High byte of Gr color for test image [3:2] : High byte of Gb color for test image [1:0] : High byte of B color for test image
0x5062	TP_IMG_R_LO	R/W	0x00	[7:0] : Low byte of R color value for test image
0x5063	TP_IMG_Gr_LO	R/W	0x00	[7:0] : Low byte of Gr color value for test image
0x5064	TP_IMG_Gb_LO	R/W	0x00	[7:0] : Low byte of Gb color value for test image
0x5065	TP_IMG_B_LO	R/W	0xFF	[7:0] : Low byte of B color value for test image
0x5066	SYNC_REG_UP_CON	R/W	0x02	[7:2] : reserved [1] : first frame vsync signal mask control 0 : mask disable 1 : mask enable [0] : synchronous register update control 0 : vsync rising time update 1 : immediately update

BLC (VSYNC SYNCHRONIZED)				
0x5100	BLC_MODE1	R/W	0x17	[7:5] : Reserved [4] : OB1 DPC Enable (ABLC, DBLC Area) [3] : Hold Enable [2] : Digital BLC Enable [1] : RST_CDS Enable [0] : RST1 Enable
0x5101	BLC_MODE2	R/W	0x03	[7:3] : Reserved [2] : RST_CDS low value enable (-1) [1] : DBLC Threshold Enable [0] : ABLC Threshold Enable
0x5102	BLC_MODE3	R/W	0x00	[7:6] : Reserved [5:4] : dblc moving average frame count 00 : 1frame 01: 8frame 10:16frame 11:32frame [3:2] : rst_cds moving average frame count 00 : 1frame 01: 8frame 10:16frame 11:32frame [1:0] : rst1 moving average frame count 00 : 1frame 01: 8frame 10:16frame 11:32frame
0x5103	BLC_AREA_STR	R/W	0x01	[7:5] : Reserved [4:0] : BLC area start line
0x5104	BLC_AREA_END	R/W	0x10	[7:5] : Reserved [4:0] : BLC area end line
0x5105	ABLC_TGT	R/W	0x04	[7:0] : ABLC Target
0x5106	DBLC_TGT	R/W	0x00	[7:0] : DBLC Target
0x5107	RST1_THR	R/W	0x01	[7:6] : Reserved [5:0] : ABLC RST1 Update Threshold
0x5108	ABLC_THR	R/W	0x01	[7:6] : Reserved [5:0] : ABLC RST_CDS Update Threshold
0x5109	DBLC_THR	R/W	0x01	[7:6] : Reserved [5:0] : DBLC Update Threshold
0x510A	RST_CDS	R/W	0x00	[7] : Reserved [6:0] : RST_CDS Setting or Monitoring
0x510B	RST1	R/W	0x00	[7:6] : Reserved [5:0] : RST1 Setting or Monitoring
0x510C	RST2	R/W	0x00	[7:6] : Reserved [5:0] : RST2 Setting or Monitoring
0x510D	DBLC_MAN_OFS_H	R/W	0x00	[7:2] : Reserved [1:0] : dblc manual offset[9:8]
0x510E	DBLC_MAN_OFS_L	R/W	0x00	[7:0] : dblc manual offset[7:0]
0x510F	OB_AVERAGE_H	R	0x00	[7:2] : Reserved [1:0] : OB area average[9:8]
0x5110	OB_AVERAGE_L	R	0x00	[7:0] : OB area average[7:0]
0x5111	OB_AVG_FN_L_H	R	0x00	[7:2] : Reserved [1:0] : high byte of final pixel for OB area
0x5112	OB_ AVG_FN _L_L	R	0x00	[7:0] : low byte of final pixel for OB area

16.3. LSC

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
LENS SHADING CONTROL				
0x5200	LSC_CON	R/W	0x00	[7:5] : Reserved [4] : Y axis Weight Mode 0 : subtract 1 : add [3] : X axis Weight Mode 0 : subtract 1 : add [2] : Y axis weight 0 : 0% 1 : 12.500% [1] : X axis weight 0 : 0% 1 : 12.500% [0] : LSC enable 0 : Disable 1 : Enable
0x5201	CENTER_H	R/W	0x01	[7:3] : Reserved [2] : High byte of y position [1:0] : High byte of x position
0x5202	CENTER_X_L	R/W	0x68	[7:0] : Low byte of x position
0x5203	CENTER_Y_L	R/W	0xF0	[7:0] : Low byte of y position
0x5204	C1_R	R/W	0x40	[7:0] : R pixel “c1”
0x5205	C1_GR	R/W	0x40	[7:0] : Gr pixel “c1”
0x5206	C1_GB	R/W	0x40	[7:0] : Gb pixel “c1”
0x5207	C1_B	R/W	0x40	[7:0] : B pixel “c1”

16.4. ISP 1

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
DPC				
0x5400	DPC_CON	R/W	0x24	[7] : Cluster Defect Pattern Detection Enable [6:2] : Reserved [1] : Compensation Data Selection 1’ b0: Neighborhood Similar Data 1’ b1: Neighborhood Median Data [0] : DPC Enable 1’ b0: Disable 1’ b1: Enable
0x5401	DPC_THR1	R/W	0xFF	[7:0] : DPC Threshold1
0x5402	DPC_THR2	R/W	0x20	[7:0] : DPC Threshold2
BAYER NOISE REDUCTION				
0x5420	BNR_CON	R/W	0x00	[7:6] : Reserved [5] : Pixel Position Selection [4] : Line Position Selection [3] : Red, Blue Pixel Average Type Selection 1’b0 : Average 1’b1 : Center pixel [2] : Green Pixel Average Type Selection 1’b0 : Average 1’b1 : Center pixel [1] : G_RB Position Test Enable 1’b0 : Disable 1’b1 : Enable [0] : Bayer Noise Reduction Enable 1’b0 : Disable 1’b1 : Enable
0x5421	BNR_STR	R/W	0x80	[7:0] : Strength
0x5422	BNR_THR_UPPER	R/W	0x20	[7:0] : Upper Threshold
0x5423	BNR_THR_LOWER	R/W	0x20	[7:0] : Lower Threshold
COLOR INTERPOLATION				
0x5500	INTP_CON	R/W	0x00	[7:4] : Reserved [3] : Interpolation RGB Gain Mode Selection 1’b0 : data*(1 + (gain/128)) 1’b1 : data*(0.5 + (gain/128)) [2] : Chrominance Noise Reduction Enable [1] : Luminance Noise Reduction Enable [0] : Adaptive False Color Suppression Enable
0x5501	INTP_R_GAIN	R/W	0x00	[7:0] : Interpolation R Gain
0x5502	INTP_G_GAIN	R/W	0x00	[7:0] : Interpolation G Gain
0x5503	INTP_B_GAIN	R/W	0x00	[7:0] : Interpolation B Gain
0x5504	Y_NR_GAIN	R/W	0x00	[7:2] : Reserved [1:0] : Luminance Noise Reduction Rate 2’b00 : 100% reduction 2’b01 : 50% reduction 2’b10 : 25% reduction 2’b11 : 12.5% reduction
0x5505	COLOR	R/W	0x00	[7:2] : Reserved [1:0] : First Color Selection 2’b00 : R

				2'b01 : Gr 2'b10 : Gb 2'b11 : B
0x5506	RGB_CLIP_H	R/W	0x03	[7:2] : Reserved [1:0] : High byte of RGB Clip Value
0x5507	RGB_CLIP_L	R/W	0xFF	[7:0] : Low byte of RGB Clip Value
0x5508	EDGE_TH_H	R/W	0x00	[7:2] : Reserved [1:0] : High byte of Edge Threshold
0x5509	EDGE_TH_L	R/W	0x00	[7:0] : Low byte of Edge Threshold
0x550A	Y_MID_COR	R/W	0x00	[7:0] : Middle Frequency Luminance Coring Value
0x550B	Y_HIGH_COR	R/W	0x00	[7:0] : High Frequency Luminance Coring Value
0x550C	Y_MID_GAIN	R/W	0x60	[7:4] : Middle Frequency Luminance Coarse Gain(Integer 4bit) [3:0] : Middle Frequency Luminance Fine Gain(Fraction 4bit)
0x550D	Y_HIGH_GAIN	R/W	0x10	[7]: Reserved [6:4]: High Frequency Luminance Coarse Gain(Integer 3bit) [3:0]: High Frequency Luminance Fine Gain(Fraction 4bit)
0x550E	GRGB_OFFSET	R/W	0x00	[7:0]: Gr/Gb Offset
0x550F	FC_MID_SCL	R/W	0x80	[7:0]: Middle Frequency False Color Suppression Strength(Edge)
0x5510	FC_HIGH_SCL	R/W	0x80	[7:0]: High Frequency False Color Suppression Strength(Moire)
COLOR CORRECTION				
0x5600	CC11	R/W	0x40	[7:0] : Coefficients of 1st row, 1st column in color correction matrix
0x5601	CC12	R/W	0x00	[7:0] : Coefficients of 1st row, 2nd column In color correction matrix
0x5602	CC13	R/W	0x00	[7:0] : Coefficients of 1st row, 3rd column In color correction matrix
0x5603	CC21	R/W	0x00	[7:0] : Coefficients of 2nd row, 1st column In color correction matrix
0x5604	CC22	R/W	0x40	[7:0] : Coefficients of 2nd row, 2nd column In color correction matrix
0x5605	CC23	R/W	0x00	[7:0] : Coefficients of 2nd row, 3rd column In color correction matrix
0x5606	CC31	R/W	0x00	[7:0] : Coefficients of 3rd row, 1st column In color correction matrix
0x5607	CC32	R/W	0x00	[7:0] : Coefficients of 3rd row, 2nd column In color correction matrix
0x5608	CC33	R/W	0x40	[7:0] : Coefficients of 3rd row, 3rd column in color correction matrix
GAMMA				
0x5700	GAMMA_CONTROL	R/W	0x00	[7:1] : reserved [0] : gamma enable 0 : disable 1 : enable
0x5710	GAMMA_0	R/W	0x15	[7:0] : gamma 0 (0~4)
0x5711	GAMMA_1	R/W	0x1D	[7:0] : gamma 1 (5~8)
0x5712	GAMMA_2	R/W	0x27	[7:0] : gamma 2 (9~16)
0x5713	GAMMA_3	R/W	0x36	[7:0] : gamma 3 (17~32)
0x5714	GAMMA_4	R/W	0x4A	[7:0] : gamma 4 (33~64)
0x5715	GAMMA_5	R/W	0x64	[7:0] : gamma 5 (65~128)
0x5716	GAMMA_6	R/W	0x79	[7:0] : gamma 6 (129~192)
0x5717	GAMMA_7	R/W	0x89	[7:0] : gamma 7 (193~256)
0x5718	GAMMA_8	R/W	0x98	[7:0] : gamma 8 (257~320)
0x5719	GAMMA_9	R/W	0xA5	[7:0] : gamma 9 (321~384)

0x571A	GAMMA_10	R/W	0xB0	[7:0] : gamma 10 (385~448)
0x571B	GAMMA_11	R/W	0xBB	[7:0] : gamma 11 (449~512)
0x571C	GAMMA_12	R/W	0xC6	[7:0] : gamma 12 (513~576)
0x571D	GAMMA_13	R/W	0xCF	[7:0] : gamma 13 (577~640)
0x571E	GAMMA_14	R/W	0xD8	[7:0] : gamma 14 (641~704)
0x571F	GAMMA_15	R/W	0xE1	[7:0] : gamma 15 (705~768)
0x5720	GAMMA_16	R/W	0xE9	[7:0] : gamma 16 (769~896)
0x5721	GAMMA_17	R/W	0xF1	[7:0] : gamma 17 (897~960)
0x5722	GAMMA_18	R/W	0xF9	[7:0] : gamma 18 (961~1023)

16.5. ISP 2

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
HUE / SATURATION / CONTRAST (VSYNC SYNCHRONIZED)				
0x6000	HS_CON	R/W	0x00	[7:5]: Reserved [4]: White Enhancement enable 1'b0: White Enhancement disable 1'b1: White Enhancement enable [3]: Black Enhancement enable 1'b0: Black Enhancement disable 1'b1: Black Enhancement enable [2]: Brightness enable 1'b0: Brightness disable 1'b1: Brightness enable [1]: Contrast enable 1'b0: Contrast disable 1'b1: Contrast enable [0]: Hue/Saturation enable 1'b0: Hue/ Saturation disable 1'b1: Hue/ Saturation enable
0x6001	HS_REF	R/W	0x80	[7:0]: Reference value of Hue/saturation control
0x6002	HS_Y_REF	R/W	0x80	[7:0]: Reference value of contrast
0x6003	HS_Y_CONTRAST	R/W	0x80	[7:0]: Contrast gain. Range x0(0x00)~x1.992(0xFF)
0x6004	HS_Y_BRIGHT	R/W	0x00	[7:0]: Brightness offset(2's complement)
0x6005	HS_SAT_CB	R/W	0x80	[7:0]: Saturation Cb gain. Range x0(0x00)~x1.992(0xFF)
0x6006	HS_SAT_CR	R/W	0x80	[7:0]: Saturation Cr gain. Range x0(0x00)~x1.992(0xFF)
0x6007	HS_SAT_MAG	R/W	0x80	[7:0]: Saturation Magenta gain. Range x0(0x00)~x1.992(0xFF)
0x6008	HS_SAT_RED	R/W	0x80	[7:0]: Saturation Red gain. Range x0(0x00)~x1.992(0xFF)
0x6009	HS_SAT_YEL	R/W	0x80	[7:0]: Saturation Yellow gain. Range x0(0x00)~x1.992(0xFF)
0x600A	HS_SAT_GRE	R/W	0x80	[7:0]: Saturation Green gain. Range x0(0x00)~x1.992(0xFF)
0x600B	HS_SAT_CYA	R/W	0x80	[7:0]: Saturation Cyan gain. Range x0(0x00)~x1.992(0xFF)
0x600C	HS_SAT_BLU	R/W	0x80	[7:0]: Saturation Blue gain. Range x0(0x00)~x1.992(0xFF)
0x600D	HS_HUE_MAG	R/W	0x00	[7:0]: Hue control(Magenta area) Range -45° ~ +45° (2's complement)
0x600E	HS_HUE_RED	R/W	0x00	[7:0]: Hue control(Red area) Range -45° ~ +45° (2's complement)
0x600F	HS_HUE_YEL	R/W	0x00	[7:0]: Hue control(Yellow area) Range -45° ~ +45° (2's complement)
0x6010	HS_HUE_GRE	R/W	0x00	[7:0]: Hue control(Green area) Range -45° ~ +45° (2's complement)
0x6011	HS_HUE_CYA	R/W	0x00	[7:0]: Hue control(Cyan area) Range -45° ~ +45° (2's complement)
0x6012	HS_HUE_BLU	R/W	0x00	[7:0]: Hue control(Blue area) Range -45° ~ +45° (2's complement)
Color Suppression (VSYNC SYNCHRONIZED)				
0x6100	COLOR_SUP_CON	R/W	0x00	[7:1] : Reserved [0] : Color suppress enable 1'b0: Disable 1'b1: Enable
0x6101	CB_UPPER_Y_THR	R/W	0xDC	[7:0] : Upper Threshold of Y for Cb
0x6102	CB_UPPER_SGAIN	R/W	0x20	[7:0] : Upper Suppression Gain for Cb
0x6103	CB_LOWER_Y_THR	R/W	0x40	[7:0] : Lower Threshold of Y for Cb
0x6104	CB_LOWER_SGAIN	R/W	0x20	[7:0] : Lower Suppression Gain for Cb
0x6105	CR_UPPER_Y_THR	R/W	0xDC	[7:0] : Upper Threshold of Y for Cr
0x6106	CR_UPPER_SGAIN	R/W	0x20	[7:0] : Upper Suppression Gain for Cr

0x6107	CR_LOWER_Y_THR	R/W	0x40	[7:0] : Lower Threshold of Y for Cr
0x6108	CR_LOWER_SGAIN	R/W	0x20	[7:0] : Lower Suppression Gain for Cr
0x6109	GRAY_LEVEL	R/W	0x00	[7:3] : reserved [2:0] : gray level, 111 -> full gray

16.6. PRIVACY ZONE MASK

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
PRIVACY ZONE	**(VSYNC SYNCHRONIZED)**			
0x6300	PRIV_ZONE_CON	R/W	0x00	[7] : mask7 enable (lowest priority) [6] : mask6 enable [5] : mask5 enable [4] : mask4 enable [3] : mask3 enable [2] : mask2 enable [1] : mask1 enable [0] : mask0 enable (highest priority)
0x6301	MASK0_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask0 (low)
0x6302	MASK0_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask0 (low)
0x6303	MASK0_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask0 (low)
0x6304	MASK0_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask0 (low)
0x6305	MASK0_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask0 (high) [5:4] : X-coordinate of the lowerright position of the mask0 (high) [3:2] : Y-coordinate of the upperleft position of the mask0 (high) [1:0] : X-coordinate of the upperleft position of the mask0 (high)
0x6306	MASK1_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask1 (low)
0x6307	MASK1_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask1 (low)
0x6308	MASK1_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask1 (low)
0x6309	MASK1_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask1 (low)
0x630A	MASK1_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask1 (high) [5:4] : X-coordinate of the lowerright position of the mask1 (high) [3:2] : Y-coordinate of the upperleft position of the mask1 (high) [1:0] : X-coordinate of the upperleft position of the mask1 (high)
0x630B	MASK2_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask2 (low)
0x630C	MASK2_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask2 (low)
0x630D	MASK2_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask2 (low)
0x630E	MASK2_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask2 (low)
0x630F	MASK2_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask2 (high) [5:4] : X-coordinate of the lowerright position of the mask2 (high) [3:2] : Y-coordinate of the upperleft position of the mask2 (high) [1:0] : X-coordinate of the upperleft position of the mask2 (high)
0x6310	MASK3_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask3 (low)
0x6311	MASK3_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask3 (low)
0x6312	MASK3_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask3 (low)
0x6313	MASK3_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask3 (low)
0x6314	MASK3_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask3 (high) [5:4] : X-coordinate of the lowerright position of the mask3 (high) [3:2] : Y-coordinate of the upperleft position of the mask3 (high) [1:0] : X-coordinate of the upperleft position of the mask3 (high)
0x6315	MASK4_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask4 (low)
0x6316	MASK4_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask4 (low)
0x6317	MASK4_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask4 (low)
0x6318	MASK4_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask4 (low)
0x6319	MASK4_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask4 (high) [5:4] : X-coordinate of the lowerright position of the mask4 (high) [3:2] : Y-coordinate of the upperleft position of the mask4 (high)

				[1:0] : X-coordinate of the upperleft position of the mask4 (high)
0x631A	MASK5_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask5 (low)
0x631B	MASK5_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask5 (low)
0x631C	MASK5_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask5 (low)
0x631D	MASK5_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask5 (low)
0x631E	MASK5_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask5 (high) [5:4] : X-coordinate of the lowerright position of the mask5 (high) [3:2] : Y-coordinate of the upperleft position of the mask5 (high) [1:0] : X-coordinate of the upperleft position of the mask5 (high)
0x631F	MASK6_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask6 (low)
0x6320	MASK6_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask6 (low)
0x6321	MASK6_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask6 (low)
0x6322	MASK6_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask6 (low)
0x6323	MASK6_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask6 (high) [5:4] : X-coordinate of the lowerright position of the mask6 (high) [3:2] : Y-coordinate of the upperleft position of the mask6 (high) [1:0] : X-coordinate of the upperleft position of the mask6 (high)
0x6324	MASK7_UP_LEFT_X	R/W	0x00	[7:0] : X-coordinate of the upperleft position of the mask7 (low)
0x6325	MASK7_UP_LEFT_Y	R/W	0x00	[7:0] : Y-coordinate of the upperleft position of the mask7 (low)
0x6326	MASK7_LO_RIGHT_X	R/W	0x00	[7:0] : X-coordinate of the lowerright position of the mask7 (low)
0x6327	MASK7_LO_RIGHT_Y	R/W	0x00	[7:0] : Y-coordinate of the lowerright position of the mask7 (low)
0x6328	MASK7_POS_HI	R/W	0x00	[7:6] : Y-coordinate of the lowerright position of the mask7 (high) [5:4] : X-coordinate of the lowerright position of the mask7 (high) [3:2] : Y-coordinate of the upperleft position of the mask7 (high) [1:0] : X-coordinate of the upperleft position of the mask7 (high)
0x6329	MASK01_COLOR_Y	R/W	0x00	[7:4] : Mask1 color : Y [3:0] : Mask0 color : Y
0x632A	MASK0_COLOR_C	R/W	0x88	[7:4] : Mask0 color : Cr [3:0] : Mask0 color : Cb
0x632B	MASK1_COLOR_C	R/W	0x88	[7:4] : Mask1 color : Cr [3:0] : Mask1 color : Cb
0x632C	MASK23_COLOR_Y	R/W	0x00	[7:4] : Mask3 color : Y [3:0] : Mask2 color : Y
0x632D	MASK2_COLOR_C	R/W	0x88	[7:4] : Mask2 color : Cr [3:0] : Mask2 color : Cb
0x632E	MASK3_COLOR_C	R/W	0x88	[7:4] : Mask3 color : Cr [3:0] : Mask3 color : Cb
0x632F	MASK45_COLOR_Y	R/W	0x00	[7:4] : Mask5 color : Y [3:0] : Mask4 color : Y
0x6330	MASK4_COLOR_C	R/W	0x88	[7:4] : Mask4 color : Cr [3:0] : Mask4 color : Cb
0x6331	MASK5_COLOR_C	R/W	0x88	[7:4] : Mask5 color : Cr [3:0] : Mask5 color : Cb
0x6332	MASK67_COLOR_Y	R/W	0x00	[7:4] : Mask7 color : Y [3:0] : Mask6 color : Y
0x6333	MASK6_COLOR_C	R/W	0x88	[7:4] : Mask6 color : Cr [3:0] : Mask6 color : Cb
0x6334	MASK7_COLOR_C	R/W	0x88	[7:4] : Mask7 color : Cr [3:0] : Mask7 color : Cb

16.7. OVERLAY

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
FORMATTER	**(VSYNC SYNCHRONIZED)**			
0x6400	OVERLAY_CON	R/W	0x00	[7] : reserved [6] : overlay 2 blink control 0 : disable 1 : enable [5:4] : overlay 2 alpha blending control 00 : 100% 01 : 75% 10 : 50% 11 : 25% [3:2] : overlay 1 alpha blending control 00 : 100% 01 : 75% 10 : 50% 11 : 25% [1] : overlay 2 display enable 0 : disable 1 : enable [0] : overlay 1 display enable 0 : disable 1 : enable
0x6401	OVERLAY1_START_X_H	R/W	0x00	[7:2] : reserved [1:0] : High byte of overlay 1 start X position
0x6402	OVERLAY1_START_X_L	R/W	0x00	[7:0] : Low byte of overlay 1 start X position
0x6403	OVERLAY1_START_Y_H	R/W	0x00	[7:2] : reserved [1:0] : High byte of overlay 1 start Y position
0x6404	OVERLAY1_START_Y_L	R/W	0x00	[7:0] : Low byte of overlay 1 start Y position
0x6405	OVERLAY1_LENGTH_X_H	R/W	0x00	[7:2] : reserved [1:0] : High byte of overlay 1 X length
0x6406	OVERLAY1_LENGTH_X_L	R/W	0x00	[7:0] : Low byte of overlay 1 X length
0x6407	OVERLAY1_LENGTH_Y_H	R/W	0x00	[7:2] : reserved [1:0] : High byte of overlay 1 Y length
0x6408	OVERLAY1_LENGTH_Y_L	R/W	0x00	[7:0] : Low byte of overlay 1 Y length
0x6409	OVERLAY2_START_X_H	R/W	0x00	[7:2] : reserved [1:0] : High byte of overlay 2 start X position
0x640A	OVERLAY2_START_X_L	R/W	0x00	[7:0] : Low byte of overlay 2 start X position
0x640B	OVERLAY2_START_Y_H	R/W	0x00	[7:2] : reserved [1:0] : High byte of overlay 2 start Y position
0x640C	OVERLAY2_START_Y_L	R/W	0x00	[7:0] : Low byte of overlay 2 start Y position
0x640D	OVERLAY2_LENGTH_X_H	R/W	0x00	[7:2] : reserved [1:0] : High byte of overlay 2 X length
0x640E	OVERLAY2_LENGTH_X_L	R/W	0x00	[7:0] : Low byte of overlay 2 X length
0x640F	OVERLAY2_LENGTH_Y_H	R/W	0x00	[7:2] : reserved [1:0] : High byte of overlay 2 Y length
0x6410	OVERLAY2_LENGTH_Y_L	R/W	0x00	[7:0] : Low byte of overlay 2 Y length
0x6411	OVERLAY1_PALETTE_0_Y	R/W	0x00	[7:0] : Y value of overlay 1 palette 0
0x6412	OVERLAY1_PALETTE_0_CB	R/W	0x00	[7:0] : Cb value of overlay 1 palette 0
0x6413	OVERLAY1_PALETTE_0_CR	R/W	0x00	[7:0] : Cr value of overlay 1 palette 0
0x6414	OVERLAY1_PALETTE_1_Y	R/W	0x00	[7:0] : Y value of overlay 1 palette 1
0x6415	OVERLAY1_PALETTE_1_CB	R/W	0x00	[7:0] : Cb value of overlay 1 palette 1
0x6416	OVERLAY1_PALETTE_1_CR	R/W	0x00	[7:0] : Cr value of overlay 1 palette 1
0x6417	OVERLAY1_PALETTE_2_Y	R/W	0x00	[7:0] : Y value of overlay 1 palette 2
0x6418	OVERLAY1_PALETTE_2_CB	R/W	0x00	[7:0] : Cb value of overlay 1 palette 2
0x6419	OVERLAY1_PALETTE_2_CR	R/W	0x00	[7:0] : Cr value of overlay 1 palette 2
0x641A	OVERLAY1_PALETTE_3_Y	R/W	0x00	[7:0] : Y value of overlay 1 palette 3

0x641B	OVERLAY1_PALETTE_3_CB	R/W	0x00	[7:0] : Cb value of overlay 1 palette 3
0x641C	OVERLAY1_PALETTE_3_CR	R/W	0x00	[7:0] : Cr value of overlay 1 palette 3
0x641D	OVERLAY1_PALETTE_4_Y	R/W	0x00	[7:0] : Y value of overlay 1 palette 4
0x641E	OVERLAY1_PALETTE_4_CB	R/W	0x00	[7:0] : Cb value of overlay 1 palette 4
0x641F	OVERLAY1_PALETTE_4_CR	R/W	0x00	[7:0] : Cr value of overlay 1 palette 4
0x6420	OVERLAY1_PALETTE_5_Y	R/W	0x00	[7:0] : Y value of overlay 1 palette 5
0x6421	OVERLAY1_PALETTE_5_CB	R/W	0x00	[7:0] : Cb value of overlay 1 palette 5
0x6422	OVERLAY1_PALETTE_5_CR	R/W	0x00	[7:0] : Cr value of overlay 1 palette 5
0x6423	OVERLAY1_PALETTE_6_Y	R/W	0x00	[7:0] : Y value of overlay 1 palette 6
0x6424	OVERLAY1_PALETTE_6_CB	R/W	0x00	[7:0] : Cb value of overlay 1 palette 6
0x6425	OVERLAY1_PALETTE_6_CR	R/W	0x00	[7:0] : Cr value of overlay 1 palette 6
0x6426	OVERLAY1_PALETTE_7_Y	R/W	0x00	[7:0] : Y value of overlay 1 palette 7
0x6427	OVERLAY1_PALETTE_7_CB	R/W	0x00	[7:0] : Cb value of overlay 1 palette 7
0x6428	OVERLAY1_PALETTE_7_CR	R/W	0x00	[7:0] : Cr value of overlay 1 palette 7
0x6429	OVERLAY1_LUT_0	R/W	0x00	[7:6] : reserved [5:3] : overlay 1 odd line color of LUT 0 [2:0] : overlay 1 even line color of LUT 0
0x642A	OVERLAY1_LUT_1	R/W	0x00	[7:6] : reserved [5:3] : overlay 1 odd line color of LUT 1 [2:0] : overlay 1 even line color of LUT 1
0x642B	OVERLAY1_LUT_2	R/W	0x00	[7:6] : reserved [5:3] : overlay 1 odd line color of LUT 2 [2:0] : overlay 1 even line color of LUT 2
0x642C	OVERLAY1_LUT_3	R/W	0x00	[7:6] : reserved [5:3] : overlay 1 odd line color of LUT 3 [2:0] : overlay 1 even line color of LUT 3
0x642D	OVERLAY2_PALETTE_0_Y	R/W	0x00	[7:0] : Y value of overlay 2 palette 0
0x642E	OVERLAY2_PALETTE_0_CB	R/W	0x00	[7:0] : Cb value of overlay 2 palette 0
0x642F	OVERLAY2_PALETTE_0_CR	R/W	0x00	[7:0] : Cr value of overlay 2 palette 0
0x6430	OVERLAY2_PALETTE_1_Y	R/W	0x00	[7:0] : Y value of overlay 2 palette 1
0x6431	OVERLAY2_PALETTE_1_CB	R/W	0x00	[7:0] : Cb value of overlay 2 palette 1
0x6432	OVERLAY2_PALETTE_1_CR	R/W	0x00	[7:0] : Cr value of overlay 2 palette 1
0x6433	OVERLAY2_PALETTE_2_Y	R/W	0x00	[7:0] : Y value of overlay 2 palette 2
0x6434	OVERLAY2_PALETTE_2_CB	R/W	0x00	[7:0] : Cb value of overlay 2 palette 2
0x6435	OVERLAY2_PALETTE_2_CR	R/W	0x00	[7:0] : Cr value of overlay 2 palette 2
0x6436	OVERLAY2_PALETTE_3_Y	R/W	0x00	[7:0] : Y value of overlay 2 palette 3
0x6437	OVERLAY2_PALETTE_3_CB	R/W	0x00	[7:0] : Cb value of overlay 2 palette 3
0x6438	OVERLAY2_PALETTE_3_CR	R/W	0x00	[7:0] : Cr value of overlay 2 palette 3
0x6439	OVERLAY2_PALETTE_4_Y	R/W	0x00	[7:0] : Y value of overlay 2 palette 4
0x643A	OVERLAY2_PALETTE_4_CB	R/W	0x00	[7:0] : Cb value of overlay 2 palette 4
0x643B	OVERLAY2_PALETTE_4_CR	R/W	0x00	[7:0] : Cr value of overlay 2 palette 4
0x643C	OVERLAY2_PALETTE_5_Y	R/W	0x00	[7:0] : Y value of overlay 2 palette 5
0x643D	OVERLAY2_PALETTE_5_CB	R/W	0x00	[7:0] : Cb value of overlay 2 palette 5
0x643E	OVERLAY2_PALETTE_5_CR	R/W	0x00	[7:0] : Cr value of overlay 2 palette 5
0x643F	OVERLAY2_PALETTE_6_Y	R/W	0x00	[7:0] : Y value of overlay 2 palette 6
0x6440	OVERLAY2_PALETTE_6_CB	R/W	0x00	[7:0] : Cb value of overlay 2 palette 6
0x6441	OVERLAY2_PALETTE_6_CR	R/W	0x00	[7:0] : Cr value of overlay 2 palette 6
0x6442	OVERLAY2_PALETTE_7_Y	R/W	0x00	[7:0] : Y value of overlay 2 palette 7

0x6443	OVERLAY2_PALETTE_7_CB	R/W	0x00	[7:0] : Cb value of overlay 2 palette 7
0x6444	OVERLAY2_PALETTE_7_CR	R/W	0x00	[7:0] : Cr value of overlay 2 palette 7
0x6445	OVERLAY2_LUT_0	R/W	0x00	[7:6] : reserved [5:3] : overlay 2 odd line color of LUT 0 [2:0] : overlay 2 even line color of LUT 0
0x6446	OVERLAY2_LUT_1	R/W	0x00	[7:6] : reserved [5:3] : overlay 2 odd line color of LUT 1 [2:0] : overlay 2 even line color of LUT 1
0x6447	OVERLAY2_LUT_2	R/W	0x00	[7:6] : reserved [5:3] : overlay 2 odd line color of LUT 2 [2:0] : overlay 2 even line color of LUT 2
0x6448	OVERLAY2_LUT_3	R/W	0x00	[7:6] : reserved [5:3] : overlay 2 odd line color of LUT 3 [2:0] : overlay 2 even line color of LUT 3
0x6449	OVERLAY2_BLINK_TIME	R/W	0x0F	[7:0] : overlay 2 blink time set

16.8. FORMATTER

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
FORMATTER	**(VSYNC SYNCHRONIZED)**			
0x6500	DATA_FMAT_CON	R/W	0x00	[7:5] : reserved [4:3] : YCbCr Output Order Control 00 : YCbYCr 01 : YCrYCb 10 : CbYCrY 11 : CrYCbY [2:0] : DATA Format Selection 000 : YCbCr 4:2:2 001 : RGB565 010 : RGB555 011 : Bayer 8 bit 100 : Bayer 10 bit 101 : CCIR656
0x6501	RGB_CON	R/W	0x00	[7:4] : reserved [3:2] : Bayer Output Order Control 00 : RGr-GbB 01 : GrR-BGb 10 : GbB-RGr 11 : BGb-GrR [1] : RGB555 Bit Position Control [0] : R/B Swap Control 0 : RG-GB 1 : BG-GR
0x6502	YC2RGB_RGB_MAX	R/W	0xFF	[7:0] : RGB maximum
0x6503	YC2RGB_RGB_MIN	R/W	0x00	[7:0] : RGB minimum
0x6504	FMAT_PDATA_CON	R/W	0x00	[7] : ccir656 Vsync enable [6] : Hsync enable for Vblank [5] : OPB output enable (0 : disable, 1 : enable) [4] : pclock polarity inversion [3] : Vsync polarity inversion [2] : Hsync polarity inversion [1:0] : Bit Position Control 00 : xxPDATA[7:0] 01 : xPDATA[7:0]x 1x : PDATA[7:0]xx
0x6505	VGA_WIN_CON	R/W	0x08	[7] : VGA mode enable (640x480) [6:0] : x position start point
0x6506	TV_DATA_CON	R/W	0x04	[7:4] : reserved [4] : TV Format Selection 0 : NTSC 1 : PAL [3:0] : TV Out Line Delay Control 0000 : -4 line delay 0001 : -3 line delay 0010 : -2 line delay 0011 : -1 line delay 0100 : 0 line delay 0101 : 1 line delay 0110 : 2 line delay 0111 : 3 line delay 1000 : 4 line delay

16.9. TV Encoder

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
NTSC/PAL	**(VSYNC SYNCHRONIZED)**			
0x6600	VER_STS	R	0x01	[7:3] : reserved [3:0] : VERID
0x6601	MD_CTL0	R/W	0x10	[7] : reserved [6] : Subcarrier phase reset Control 0 : Subcarrier Reset Disable 1 : Subcarrier Reset Enable (Reset to "0" at the beginning of every 4(8) field) [5] : NTSC/PAL selection 0 : NTSC 1 : PAL [4] : Pedestal setup control 0 : Pedestal SETUP Disable (NTSC-J, PAL-BDGHI, PAL-Nc, PAL60) 1 : Pedestal SETUP Enable (7.5 IRE) (NTSC-M, NTSC4.43, PAL_N, PAL-M, NTSC50) [3] : Burst Level Control 0 : BURST Level 40 IRE (NTSC-M, NTSC-J, NTSC4.43, PAL-N, PAL-M, NTSC50) 1 : BURST Level 42.86 IRE (PAL-BDGHI, PAL-N, PAL-Nc, PAL-M, PAL60) [2] : Sync Level Control 0 : Sync Level 40 IRE (NTSC-M, NTSC-J, NTSC4.43,PAL-N, PAL-M, NTSC50) 1 : Sync Level 43 IRE (PAL-BGDHI, PAL-Nc, PAL60) [1] : Vsync Width Control 0 : VSYNC 2.5 Line (NTSC-M, PAL-BDGHI, PAL-Nc, NTSC50) 1 : VSYNC 3 Line (NTSC-J, NTSC4.43, PAL-N, PAL-M, PAL60) [0] : 525/625 line format 0 : 525 line format (NTSC-M, NTSC-J, NTSC4.43, PAL-M, PAL60) 1 : 625 line format (PAL-BDGHI, PAL-N, PAL-Nc, NTSC50)
0x6602	MD_CTL1	R/W	0x00	[7:2] : reserved [1:0] : Chroma Frequency Selection 00 : 3.579545455MHz (NTSC-M, NTSC-J) 01 : 4.43361875MHz (NTSC4.43, PAL-BDGHI, PAL-N, PAL60) 10 : 3.57561189MHz (PAL-M) 11 : 3.58205625MHz (PAL-Nc)
0x6603	IF_CTL0	R/W	0x19	[7:0] : reserved
0x6604	IF_CTL1	R/W	0x0B	[7:0] : reserved
0x6605	IF_STS0	R	0x00	[7:6] : reserved [5:4] : High byte of Vertical Line Count Number per Frame (Real Number -1) [3:0] : High byte of Horizontal Count Number Status (Real Number -1)
0x6606	IF_STS1	R	0x00	[7:0] : Low byte of Vertical Line Count Number per Frame (Real Number -1)
0x6607	IF_STS2	R	0x00	[7:0] : Low byte of Horizontal Count Number Status (Real Number -1)
0x6608	IF_STS3	R	0x00	[7:0] : Current Field Count Number
0x6609	DAC_CTL0	R/W	0x10	[7:5] : reserved [4] : Video DAC power down control

				0 : active 1 : power down [3:2] : High byte of DAC data [1:0] : Encoder output selection 00 : CVBS 01 : 0x000 10 : 0x3FF 11 : DAC data
0x660A	DAC_CTL1	R/W	0x00	[7:0] : Low byte of DAC data
0x660B	ConBr_CTL0	R/W	0x80	[7:0] : Brightness Control, 2's Compliment
0x660C	ConBr_CTL1	R/W	0x00	[7:0] : Contrast Control, Max Gain = 255/128
0x660D	SatGn_CTL0	R/W	0x80	[7:0] : Cb Gain Control, Max Gain = 255/128
0x660E	SatGn_CTL1	R/W	0x80	[7:0] : Cr Gain Control, Max Gain = 255/128
0x660F	HUE_CTL0	R/W	0x00	[7:0] : Hue Control, 1 LSB = 1.40625°
0x6610	HUE_CTL1	R/W	0x00	[7:1] : reserved [0] : Video Mute Control 0 : Normal Operation 1 : Video Mute Enable
0x6611	M_PAT_CTL	R/W	0x00	[7:2] : reserved [1] : Internal Pattern Selection 0 : 100% Color Bar 1 : 75% Color Bar [0] : Internal Pattern Control 0 : Internal Pattern Disable 1 : Internal Pattern Enable
0x6612	FLTSEL_CTL0	R/W	0x00	[7:6] : reserved [5:3] : UV Filter Control 0 : Wide Bandwidth 4 : Narrow Bandwidth [2:0] : Y Filter Control 0 : Wide Bandwidth 4 : Narrow Bandwidth
0x6613	FLTSEL_CTL1	R/W	0x03	[7:4] : reserved [3] : Sync Filter Control 0 : disable 1 : enable [2:0] : Sync Filter Selection
0x6614	DTO_OS_CTL0	R/W	0x00	[7:0] : Low byte of FSC Offset Control
0x6615	DTO_OS_CTL0	R/W	0x00	[7:0] : High byte of FSC Offset Control
0x6616	M_FSC_CTL0	R/W	0x00	Manual Chroma Frequency Control. This register s are only effective when M_FSC_CTL3[7] = '1' FSCDTO = int(Fsc / CLK * 2^32 +0.5) [7:0] : Fsc[7:0]
0x6617	M_FSC_CTL1	R/W	0x00	[7:0] : Fsc[15:8]
0x6618	M_FSC_CTL2	R/W	0x00	[7:0] : Fsc[23:16]
0x6619	M_FSC_CTL3	R/W	0x00	[7] : Chroma Subcarrier Frequency Control 0 : Automatic Chroma Subcarrier Frequency Control Mode 1 : Manual Chroma Subcarrier Frequency Control Enable [6:0] : Fsc[30:24]
0x661A	SINX_CTL	R/W	0x01	[7:0] : reserved
0x661B	MY_CTL0	R/W	0x5D	[7:0] : Low byte of Manual Y gain MY = int(VMax/(219 * VFULL) * 2^18 +0.5)
0x661C	MY_CTL1	R/W	0x02	[7:3] : reserved [2] : Manual Gain Control Enable (when YCbCr to YUV Conversion) 0 : Automatic Color Space Conversion 1 : Manual Color Space Conversion [1:0] : High byte of Manual Y gain
0x661D	MCb_CTL0	R/W	0x04	[7:0] : Low byte of Manual Cb gain MCb = int(VMax*0.492*1.772/(VFULL*224)*2^18 +0.5) *VMax = 100% White Voltage Level (NTSC-M/PALM/N=0.661, NTSC-J=0.714, PAL=0.7), *VFULL=DAC Full Scale Output Voltage
0x661E	MCb_CTL1	R/W	0x02	[7:2] : reserved

				[1:0] : High byte of Manual Cb gain
0x661F	MCr_CTL0	R/W	0xD8	[7:0] : Low byte of Manual Cr gain MCr = int(VMax*0.877*1.403/(VFULL*224)*2^18+0.5)
0x6620	MCr_CTL1	R/W	0x02	[7:2] : reserved [1:0] : High byte of Manual Cr gain
0x6621	MLVL_CTL	R/W	0x00	[7:3] : reserved [2] : Manual Sync Level Control 0 : Automatic Sync Level Control 1 : Manual Sync Level Control Enable [1] : Manual Burst Level Control 0 : Automatic Burst Level Control 1 : Manual Burst Level Control Enable [0] : Manual Pedestal Set-up Level Control 0 : Automatic Pedestal Set-up Level Control 1 : Manual Pedestal Set-up Level Control Enable
0x6622	MSYNC_CTL	R/W	0xE0	[7:0] : Manual Sync Level Control . This register s are only effective when MSYNC_CTL1[0] = ”1” M_SyncLevel = int(VSync/ VFULL * 2^10 +0.5) *VSync = Sync Voltage Level (NTSC-M/J/PALM/N=0.286, PAL=0.3) *VFULL=DAC Full Scale Output Voltage
0x6623	MBST_CTL	R/W	0x70	[7:0] : Manual Burst Level Control. This register s are only effective when MBBST_CTL1[0] = ”1” NTSC : M_ Burst = int(VBurst/ VFULL * 2^9 +0.5) PAL :M_ Burst = int(VBurst/ VFULL * 2^9 * 2^-0.5 +0.5) * VBurst = Burst Voltage Level (NTSC-M/J/PALM/N=0.286, PAL=0.299) *VFULL=DAC Full Scale Output Voltage
0x6624	MSUP_CTL	R/W	0x2A	[7:0] : Manual Pedestal Set-up Level Control. This register s are only effective when MSUP_CTL1[0] =”1” & SETUP=”1” M_SetUpLevel = int(7.5*0.00715/ VFULL * 2^10 +0.5) *VFULL=DAC Full Scale Output Voltage
0x6625	MHSWd_CTL0	R/W	0x40	[7:0] : Manual HSYNC Width Control. This register s are only effective when MHSWd_CTL1[0] =”1” CLK/2 * (M_HSWd+1)
0x6626	MHSWd_CTL1	R/W	0x00	[7:1] : reserved [0] : Manual HSYNC Width Control 0 : Automatic HSYNC Width Control 1 : Manual HSYNC Width Control Enable
0x6627	MBWd_CTL0	R/W	0x40	[7:0] : Manual Burst Start Control. This register s are only effective when MBWd_CTL1[0] =”1” CLK/2 * (M_ BurstSt +1)
0x6628	MBWd_CTL1	R/W	0x00	[7:1] : reserved [0] : Manual Burst Width Control 0 : Automatic Burst Width Control 1 : Manual Burst Width Control Enable
0x6629	MBWd_CTL2	R/W	0x40	[7:0] : Low byte of Manual Burst End Control This register s are only effective when MBWd_CTL1[0] =”1” CLK/2 * (M_ BurstEnd +1)
0x662A	MBWd_CTL3	R/W	0x00	[7:1] : reserved [0] : High byte of Manual Burst End Control
0x662B	MHAV_CTL0	R/W	0x79	[7:0] : Manual Horizontal Active Start Control This register s are only effective when MHAV_CTL1[0] =”1” CLK/2 * (M_ HAVSt +1)
0x662C	MHAV_CTL1	R/W	0x00	[7:2] : reserved [1] : Slave HAV & VAV Timing Control 1 : HAV & VAV Timing is controlled by Input Timing [0] : Manual Horizontal Active Start and End Control 0 : Automatic Horizontal Active Start and End Control 1 : Manual Horizontal Active Start and End Control Enable

0x662D	MHAV_CTL2	R/W	0x49	[7:0] : Low byte of Manual Horizontal Active End Control This register s are only effective when MHAV_CTL1[0] =”1” CLK/2 * (M_ HAVEnd +1)
0x662E	MHAV_CTL3	R/W	0x03	[7:3] : reserved [2:0] : High byte of Manual Horizontal Active End Control
0x662F	MVAV_CTL0	R/W	0x12	[7:0] : Manual Vertical Active Start Control This register s are only effective when MVAV_CTL1[0] =”1” (M_ HAVSt +1) From Vsync
0x6630	MVAV_CTL1	R/W	0x00	[7:1] : reserved [0] : Manual Vertical Active Start and End Control 0 : Automatic Vertical Active Start and End Control 1 : Manual Vertical Active Start and End Control Enable
0x6631	MVAV_CTL2	R/W	0x02	[7:0] : Low byte of Manual Vertical Active End Control This register s are only effective when MVAV_CTL1[0] =”1” (M_ VAVEnd +1) From Vsync
0x6632	MVAV_CTL3	R/W	0x01	[7:1] : reserved [0] : High byte of Manual Vertical Active End Control
0x6633	VBIE_CTL	R/W	0x00	[7:0] : reserved
0x6634	VBI_STS	R/W	0x00	[7:0] : reserved
0x6635	CCF1D_CTL0	R/W	0x00	[7:0] : reserved
0x6636	CCF1D_CTL1	R/W	0x00	[7:0] : reserved
0x6637	CCF2D_CTL0	R/W	0x00	[7:0] : reserved
0x6638	CCF2D_CTL1	R/W	0x00	[7:0] : reserved
0x6639	VBIGN_CTL	R/W	0x00	[7:0] : reserved

16.10. CCP

ADDRESS (HEX)	REGISTER NAME	R/W	DEFAULT (HEX)	DESCRIPTION
AE	**(VSYNC SYNCHRONIZED)**			
0x7000	AE_WIN01_SEL	R/W	0x00	[7:2] : Reserved [1] : AE window1 display enable (1:on) [0] : AE window1 enable
0x7001	AE_WIN02_SEL	R/W	0x00	[7:2] : Reserved [1] : AE window2 display enable (1:on) [0] : AE window2 enable
0x7002	AE_WIN03_SEL	R/W	0x00	[7:2] : Reserved [1] : AE window3 display enable (1:on) [0] : AE window3 enable
0x7003	AE_WIN04_SEL	R/W	0x00	[7:2] : Reserved [1] : AE window4 display enable (1:on) [0] : AE window4 enable
0x7004	AE_WIN05_SEL	R/W	0x00	[7:2] : Reserved [1] : AE window5 display enable (1:on) [0] : AE window5 enable
0x7005	AE_WIN01_LR	R/W	0x0F	[7:4] : Left value of AE window 1 [3:0] : Right value of AE window 1
0x7006	AE_WIN01_UD	R/W	0x0F	[7:4] : Up value of AE window 1 [3:0] : Down value of AE window 1
0x7007	AE_WIN02_LR	R/W	0x0F	[7:4] : Left value of AE window 2 [3:0] : Right value of AE window 2
0x7008	AE_WIN02_UD	R/W	0x0F	[7:4] : Up value of AE window 2 [3:0] : Down value of AE window 2
0x7009	AE_WIN03_LR	R/W	0x0F	[7:4] : Left value of AE window 3 [3:0] : Right value of AE window 3
0x700A	AE_WIN03_UD	R/W	0x0F	[7:4] : Up value of AE window 3 [3:0] : Down value of AE window 3
0x700B	AE_WIN04_LR	R/W	0x0F	[7:4] : Left value of AE window 4 [3:0] : Right value of AE window 4
0x700C	AE_WIN04_UD	R/W	0x0F	[7:4] : Up value of AE window 4 [3:0] : Down value of AE window 4
0x700D	AE_WIN05_LR	R/W	0x0F	[7:4] : Left value of AE window 5 [3:0] : Right value of AE window 5
0x700E	AE_WIN05_UD	R/W	0x0F	[7:4] : Up value of AE window 5 [3:0] : Down value of AE window 5
0x700F	AE01_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 1[28:24]
0x7010	AE01_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 1[23:16]
0x7011	AE01_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 1[15:8]
0x7012	AE01_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 1[7:0]
0x7013	AE02_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 2[28:24]
0x7014	AE02_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 2[23:16]
0x7015	AE02_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 2[15:8]
0x7016	AE02_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 2[7:0]
0x7017	AE03_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 3[28:24]
0x7018	AE03_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 3[23:16]
0x7019	AE03_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 3[15:8]

0x701A	AE03_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 3[7:0]
0x701B	AE04_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 4[28:24]
0x701C	AE04_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 4[23:16]
0x701D	AE04_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 4[15:8]
0x701E	AE04_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 4[7:0]
0x701F	AE05_SUM3	R	0x00	[7:5] : Reserved [4:0] : Summation of Y data out in AE window 5[28:24]
0x7020	AE05_SUM2	R	0x00	[7:0] : Summation of Y data out in AE window 5[23:16]
0x7021	AE05_SUM1	R	0x00	[7:0] : Summation of Y data out in AE window 5[15:8]
0x7022	AE05_SUM0	R	0x00	[7:0] : Summation of Y data out in AE window 5[7:0]
AWB	**(VSYNC SYNCHRONIZED)**			
0x7100	WB_BOUND_EN	R/W	0x00	[7:4] : reserved [3] : white count zone 1 disable(1:off) [2] : white count zone 2 disable(1:off) [1] : Using pixel display enable(1:on) [0] : AWB window display enable
0x7101	WB_WIN_X_START	R/W	0x00	[7:0] : X position start value of AWB window
0x7102	WB_WIN_X_END	R/W	0xB3	[7:0] : X position end value of AWB window
0x7103	WB_WIN_Y_START	R/W	0x00	[7] : reserved [6:0] : Y position start value of AWB window
0x7104	WB_WIN_Y_END	R/W	0x77	[7] : reserved [6:0] : Y position end value of AWB window
0x7105	WB_WZONE1_P1_X	R/W	0x4B	[7:0] : White pixel zone 1 P1_X
0x7106	WB_WZONE1_P1_Y	R/W	0xAA	[7:0] : White pixel zone 1 P1_Y
0x7107	WB_WZONE1_P1_X_OS	R/W	0x0F	[7:0] : White pixel zone 1 P1_X Offset
0x7108	WB_WZONE1_P1_Y_OS	R/W	0x09	[7:0] : White pixel zone 1 P1_Y Offset
0x7109	WB_WZONE1_P2_X	R/W	0x60	[7:0] : White pixel zone 1 P2_X
0x710A	WB_WZONE1_P2_Y	R/W	0x7E	[7:0] : White pixel zone 1 P2_Y
0x710B	WB_WZONE1_SLOPE	R/W	0xA0	[7:0] : White pixel zone 1 Slope
0x710C	WB_WZONE2_P1_X	R/W	0x5C	[7:0] : White pixel zone 2 P1_X
0x710D	WB_WZONE2_P1_Y	R/W	0x74	[7:0] : White pixel zone 2 P1_Y
0x710E	WB_WZONE2_P1_X_OS	R/W	0x1F	[7:0] : White pixel zone 2 P1_X Offset
0x710F	WB_WZONE2_P1_Y_OS	R/W	0x06	[7:0] : White pixel zone 2 P1_Y Offset
0x7110	WB_WZONE2_P2_X	R/W	0x82	[7:0] : White pixel zone 2 P2_X
0x7111	WB_WZONE2_P2_Y	R/W	0x64	[7:0] : White pixel zone 2 P2_Y
0x7112	WB_WZONE2_SLOPE	R/W	0x1A	[7:0] : White pixel zone 2 Slope
0x7113	WB_WZONE3_P1_X	R/W	0x50	[7:0] : White pixel zone 3 P1_X
0x7114	WB_WZONE3_P1_Y	R/W	0x6A	[7:0] : White pixel zone 3 P1_Y
0x7115	WB_WZONE3_P2_X	R/W	0x56	[7:0] : White pixel zone 3 P2_X
0x7116	WB_WZONE3_P2_Y	R/W	0x62	[7:0] : White pixel zone 3 P2_Y
0x7117	WB_WZONE4_P1_X	R/W	0x50	[7:0] : White pixel zone 4 P1_X
0x7118	WB_WZONE4_P1_Y	R/W	0xAE	[7:0] : White pixel zone 4 P1_Y
0x7119	WB_WZONE4_P2_X	R/W	0x58	[7:0] : White pixel zone 4 P2_X
0x711A	WB_WZONE4_P2_Y	R/W	0xA4	[7:0] : White pixel zone 4 P2_Y
0x711B	WB_SAT_UP	R/W	0xFB	[7:0] : Up Threshold of RGB Data
0x711C	WB_SAT_DN	R/W	0x20	[7:0] : Down Threshold of RGB Data

0x7120	WB_RSUM3	R	0x00	[28:24] : Summation of raw Red data out in WB window
0x7121	WB_RSUM2	R	0x00	[23:16] : Summation of raw Red data out in WB window
0x7122	WB_RSUM1	R	0x00	[15:8] : Summation of raw Red data out in WB window
0x7123	WB_RSUM0	R	0x00	[7:0] : Summation of raw Red data out in WB window
0x7124	WB _GSUM3	R	0x00	[28:24] : Summation of raw Green data out in WB window
0x7125	WB_GSUM2	R	0x00	[23:16] : Summation of raw Green data out in WB window
0x7126	WB_GSUM1	R	0x00	[15:8] : Summation of raw Green data out in WB window
0x7127	WB_GSUM0	R	0x00	[7:0] : Summation of raw Green data out in WB window
0x7128	WB_BSUM3	R	0x00	[28:24] : Summation of raw Blue data out in WB window
0x7129	WB_BSUM2	R	0x00	[23:16] : Summation of raw Blue data out in WB window
0x712A	WB_BSUM1	R	0x00	[15:8] : Summation of raw Blue data out in WB window
0x712B	WB_BSUM0	R	0x00	[7:0] : Summation of raw Blue data out in WB window
0x712C	WB_WCNT2	R	0x00	[18:16] : Count of white pixel in WB window
0x712D	WB_WCNT1	R	0x00	[15:8] : Count of white pixel in WB window
0x712E	WB_WCNT0	R	0x00	[7:0] : Count of white pixel in WB window

17. Spectral Response Of Color Filter

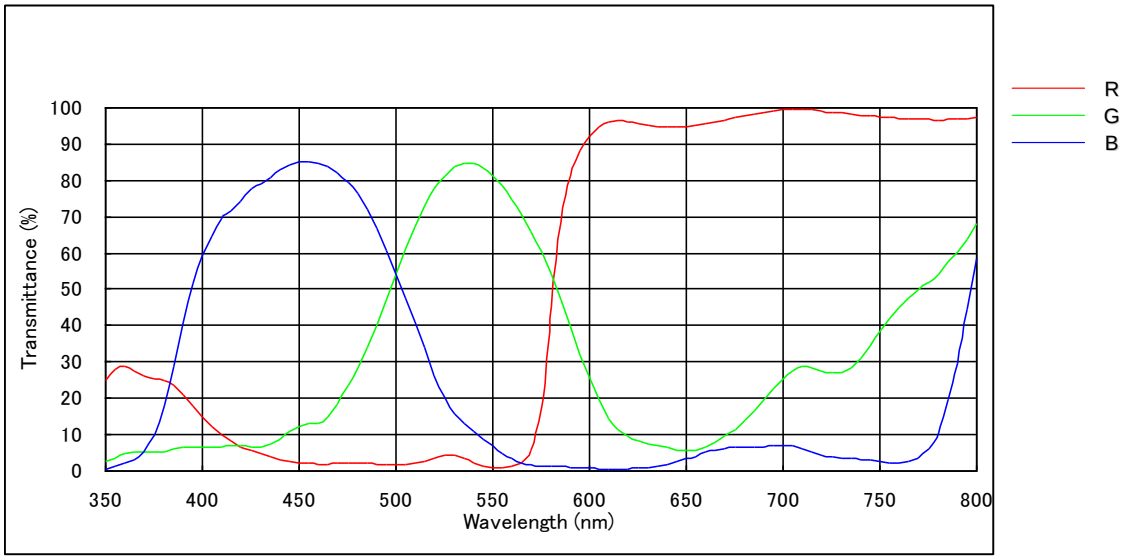


Figure 17-1 spectral response of color filter

18. Electrical Characteristics

Symbol	Parameter	Rating	Units
VDDIO	Supply Voltage for IO	4	V
VDDP	Supply Voltage for Analog	4	V
VDDL		4	V
VDDA		4	V
VDDN		4	V
T	Storage Temperature	-50 to 125	℃

Table 18-1 Absolute Maximum Ratings

Symbol	Parameter	Rating			Units
		MIN	TYP	MAX	
VDDIO	Supply Voltage for IO	2.97	3.3	3.63	V
VDDP	Supply Voltage for Analog	2.97	3.3	3.63	V
VDDL		2.97	3.3	3.63	V
VDDA		2.97	3.3	3.63	V
VDDN		2.97	3.3	3.63	V
T_A	Commercial Temperature Range	0 to 70			℃
	Industrial Temperature Range	-40 to 105			

Table 18-2 Recommended Operating Condition

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
IDDS	Quiescent Current	VDDIO = 3.3V		[T.B.D]		mW
IDD	Dynamic IDD	VDDIO = 3.3V EXT_CLK = 27MHz		[T.B.D]		mW

Table 18-3 Power Consumption

Items	VDDIO = 3.3V±10%			Unit
	MIN	TYP	MAX	
VIL			0.35*VDDIO	V
VIH	0.7*VDDIO			
IIH	-5		5	μA
IIL	-5		5	
VOL (PAD)			0.4	V
VOH (PAD)	VDDIO-0.4			
Schmitt trigger L to H Threshold	1.74		1.92	V
Schmitt trigger H to L Threshold	1.26		1.46	V

Table 18-4 DC Characteristics

19. Pin Information

Figure 19-1 and Figure 19-2 are pin maps when packaging CP7208 in 40 pin PLCC. Depending on the package kind, pin maps may change.

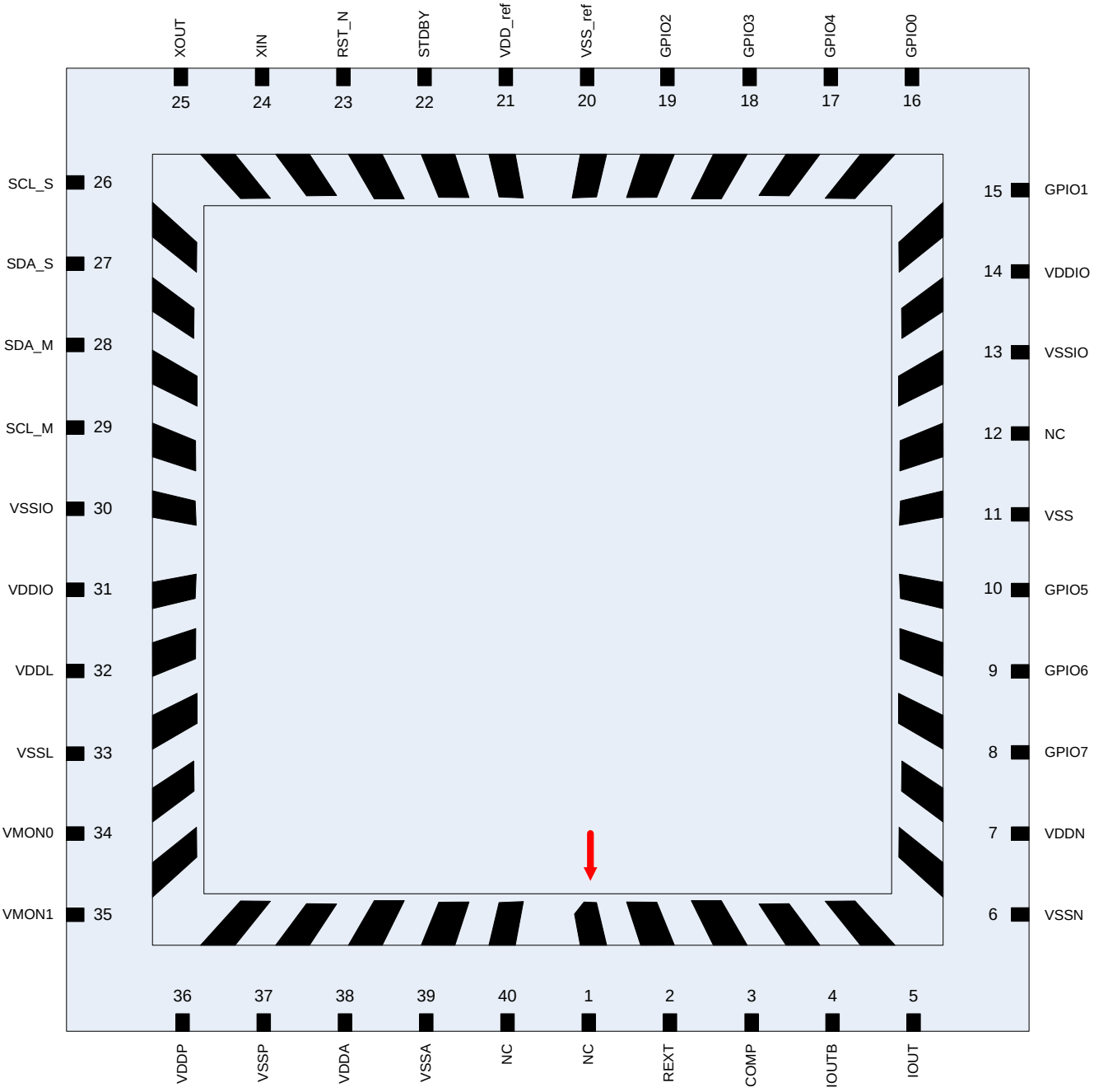


Figure 19-1 40 PLCC PKG Pin Map(Analog)

Loc	PIN Num.	PIN Name	I/O	Description	Note
BOTTOM	1	NC	–		
	2	REXT	–	External Reference Resistor	
	3	COMP	–	Compensation Pin	
	4	IOUTB	A	10bit DAC Negative Output	Analog PAD
	5	IOUT	A	10bit DAC Positive Output	Analog PAD
RIGHT	6	VSSN	G	Analog Ground for 10bit DAC	
	7	VDDN	P	Analog Power for 10bit DAC	
	8	GPIO7	I/O	GPIO 7 port	
	9	GPIO6	I/O	GPIO 6 port	
	10	GPIO5	I/O	GPIO 5 port	
	11	VSS	G	Digital ground for core	
	12	NC	–		
	13	VSSIO	G	Digital ground for IO	
	14	VDDIO	P	Digital power for IO	
	15	GPIO1	I/O	GPIO 1 port	
TOP	16	GPIO0	I/O	GPIO 0 port	
	17	GPIO4	I/O	GPIO 4 port	
	18	GPIO3	I/O	GPIO 3 port	
	19	GPIO2	I/O	GPIO 2 port	
	20	VSS_ref	G	Digital ground for core	
	21	VDD_ref	O	Digital power reference	
	22	STDBY	I	Standby input port	
	23	RST_N	I	Reset input port	
	24	XIN	I	External Clock input port	
	25	XOUT	O	External Clock output port	
LEFT	26	SCL_S	I	Slave Serial Clock port	
	27	SDA_S	I/O	Slave Serial Data port	
	28	SDA_M	I/O	Master Serial Data port	
	29	SCL_M	O	Master Serial Clock port	
	30	VSSIO	G	Digital ground for IO	
	31	VDDIO	P	Digital power for IO	
	32	VDDL	P	PLL Power	
	33	VSSL	G	PLL Ground	
	34	VMON0	A	Internal signal monitoring 0	Analog PAD
	35	VMON1	A	Internal signal monitoring 1	Analog PAD
BOTTOM	36	VDDP	P	Analog Power for Pixel	
	37	VSSP	G	Analog Ground for Pixel	
	38	VDDA	P	Analog Power for Core	
	39	VSSA	G	Analog Ground for Core	
	40	NC	–		

Table 19-1 40 PLCC Pin Information(Analog)

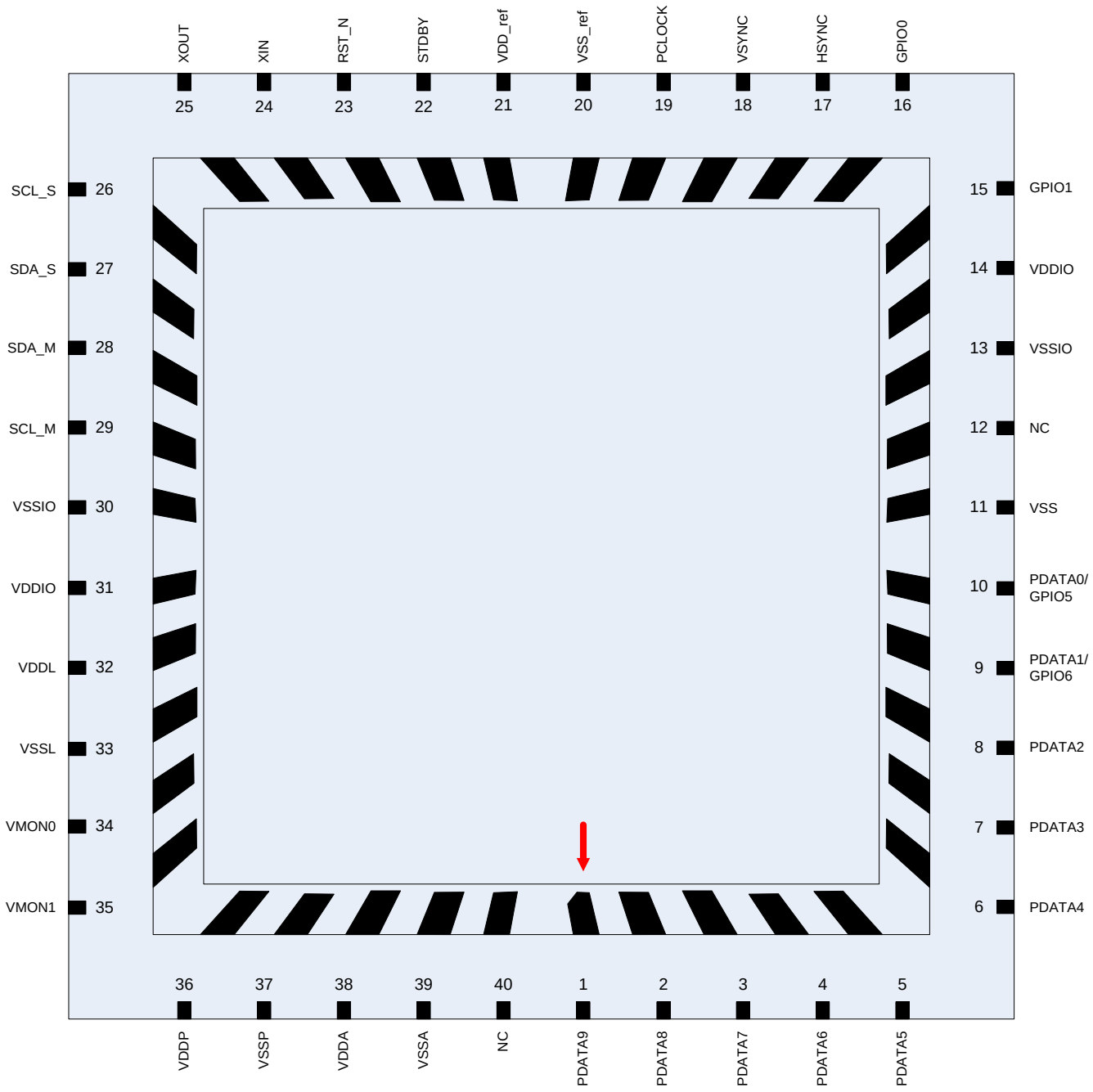


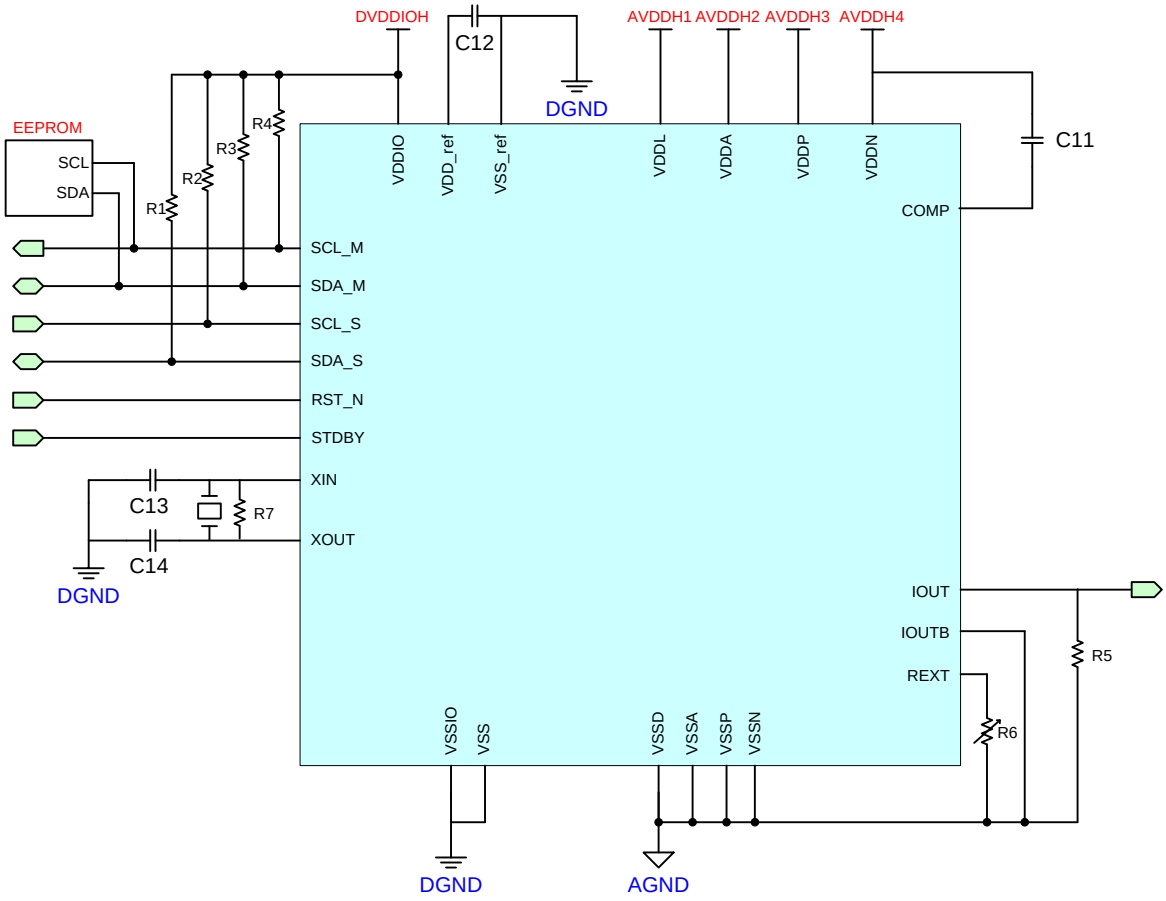
Figure 19-2 40 PLCC PKG Pin Map(Digital)

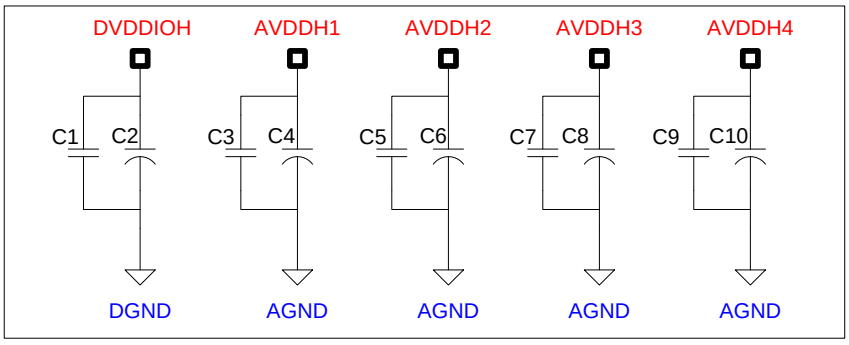
Loc	PIN Num.	PIN Name	I/O	Description	Note
BOTTOM	1	PDATA9	O	Pixel Data[9] output port	
	2	PDATA8	O	Pixel Data[8] output port	
	3	PDATA7	O	Pixel Data[7] output port	
	4	PDATA6	O	Pixel Data[6] output port	
	5	PDATA5	O	Pixel Data[5] output port	
RIGHT	6	PDATA4	O	Pixel Data[4] output port	
	7	PDATA3	O	Pixel Data[3] output port	
	8	PDATA2	O	Pixel Data[2] output port	
	9	PDATA1/ GPIO6	I/O	Pixel Data[1] output port/ GPIO 6 port	Default Pixel data[1]
	10	PDATA0/ GPIO5	I/O	Pixel Data[0] output port/ GPIO 5 port	Default Pixel data[0]
	11	VSS	G	Digital ground for core	
	12	NC	–		
	13	VSSIO	G	Digital ground for IO	
	14	VDDIO	P	Digital power for IO	
	15	GPIO1	I/O	GPIO 1 port	
TOP	16	GPIO0	I/O	GPIO 0 port	
	17	HSYNC	O	Horizontal Sync output port	
	18	VSYNC	O	Vertical Sync output port	
	19	PCLOCK	O	Pixel Clock output port	
	20	VSS_ref	G	Digital ground for core	
	21	VDD_ref	O	Digital power reference	
	22	STDBY	I	Standby input port	
	23	RST_N	I	Reset input port	
	24	XIN	I	External Clock input port	
	25	XOUT	O	External Clock output port	
LEFT	26	SCL_S	I	Slave Serial Clock port	
	27	SDA_S	I/O	Slave Serial Data port	
	28	SDA_M	I/O	Master Serial Data port	
	29	SCL_M	O	Master Serial Clock port	
	30	VSSIO	G	Digital ground for IO	
	31	VDDIO	P	Digital power for IO	
	32	VDDL	P	PLL Power	
	33	VSSL	G	PLL Ground	
	34	VMON0	A	Internal signal monitoring 0	Analog PAD
	35	VMON1	A	Internal signal monitoring 1	Analog PAD
BOTTOM	36	VDDP	P	Analog Power for Pixel	
	37	VSSP	G	Analog Ground for Pixel	
	38	VDDA	P	Analog Power for Core	
	39	VSSA	G	Analog Ground for Core	
	40	NC	–		

Table 19-2 40 PLCC Pin Information(Digital)

20. Typical Circuit Configuration

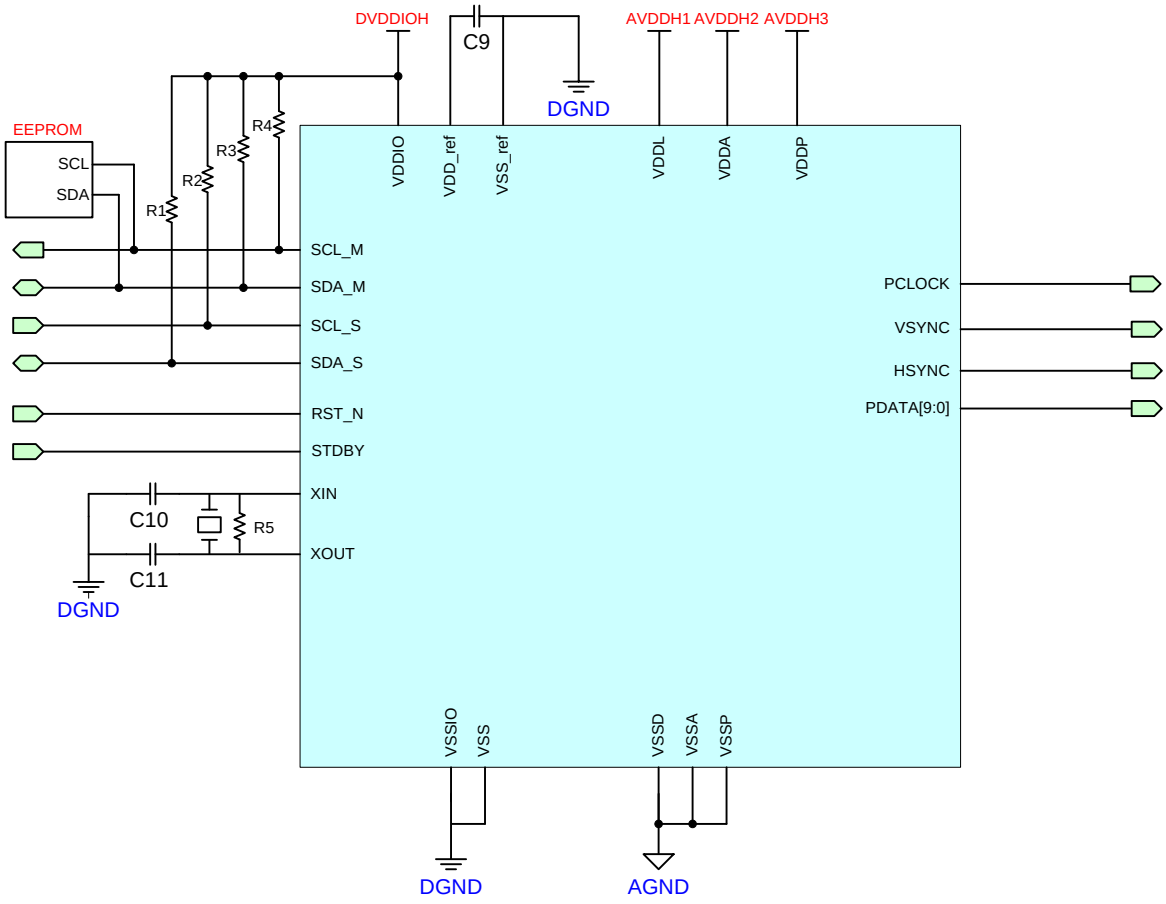
Figure 20-1 and Figure 20-2 are examples of circuit diagrams when CP7208 is packaged in 40 pin PLCC. Depending on the package kind, circuit diagrams may change.

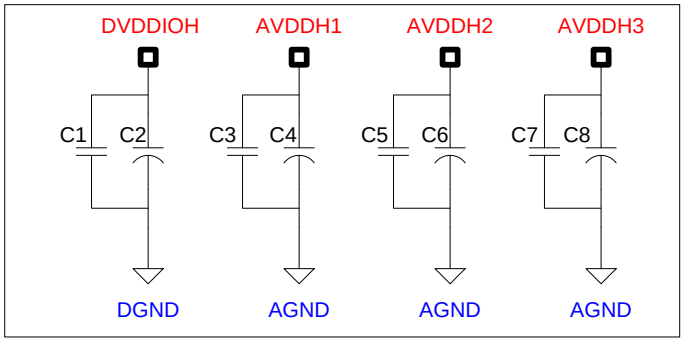




R1,R2,R3, R4 = 1.3KΩ
R5 = 75Ω
R6 = Variable resistor(~15KΩ)
R7 = 1MΩ
C1,C3,C5,C7,C9,C11 = 0.1uF
C2,C4,C6,C8,C10 = 10uF
C12 = 1uF
C13,C14 = 8pF(C_L : 9pF)

Figure 20-1 Typical Circuit Configuration(Analog)

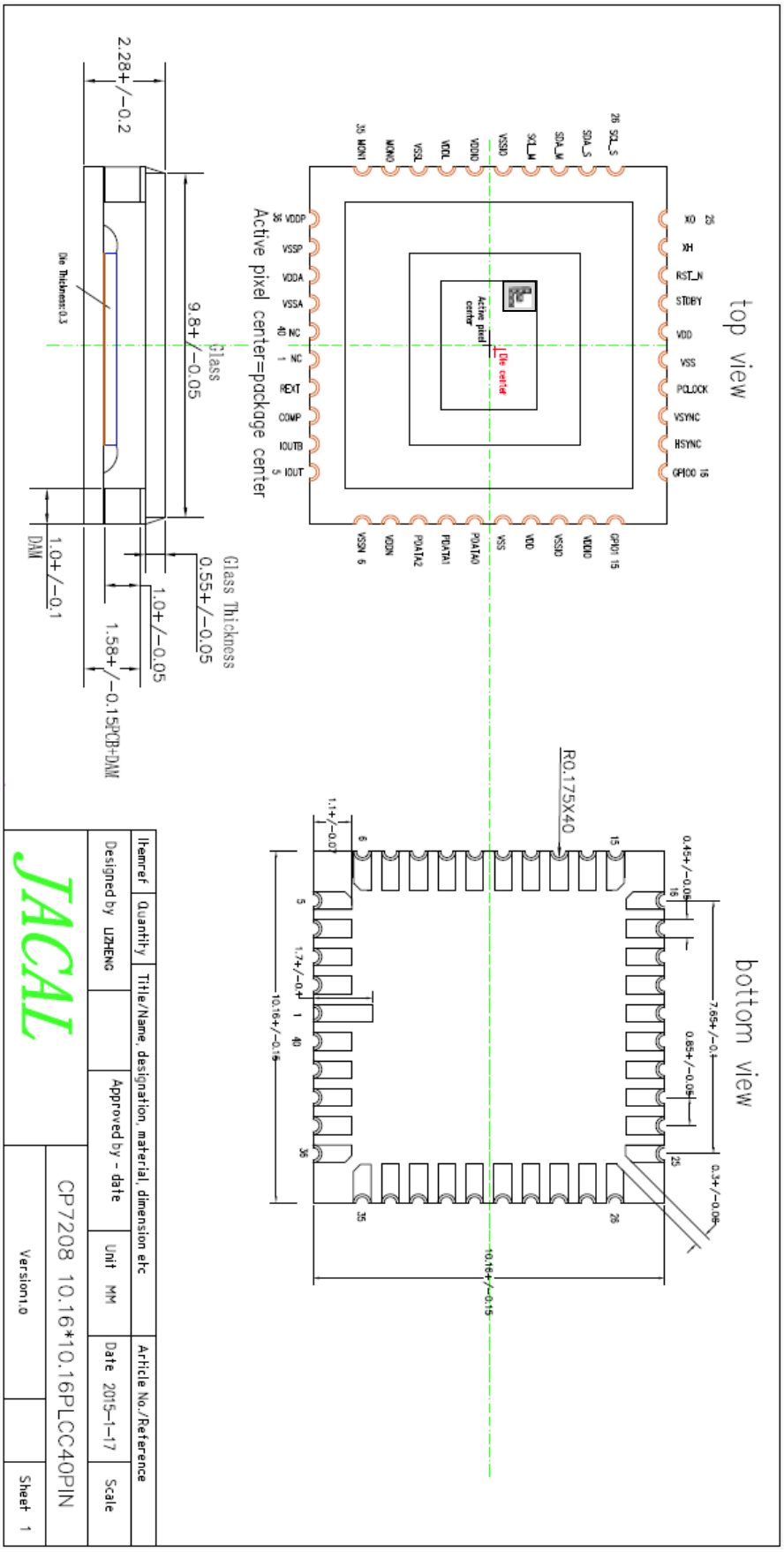


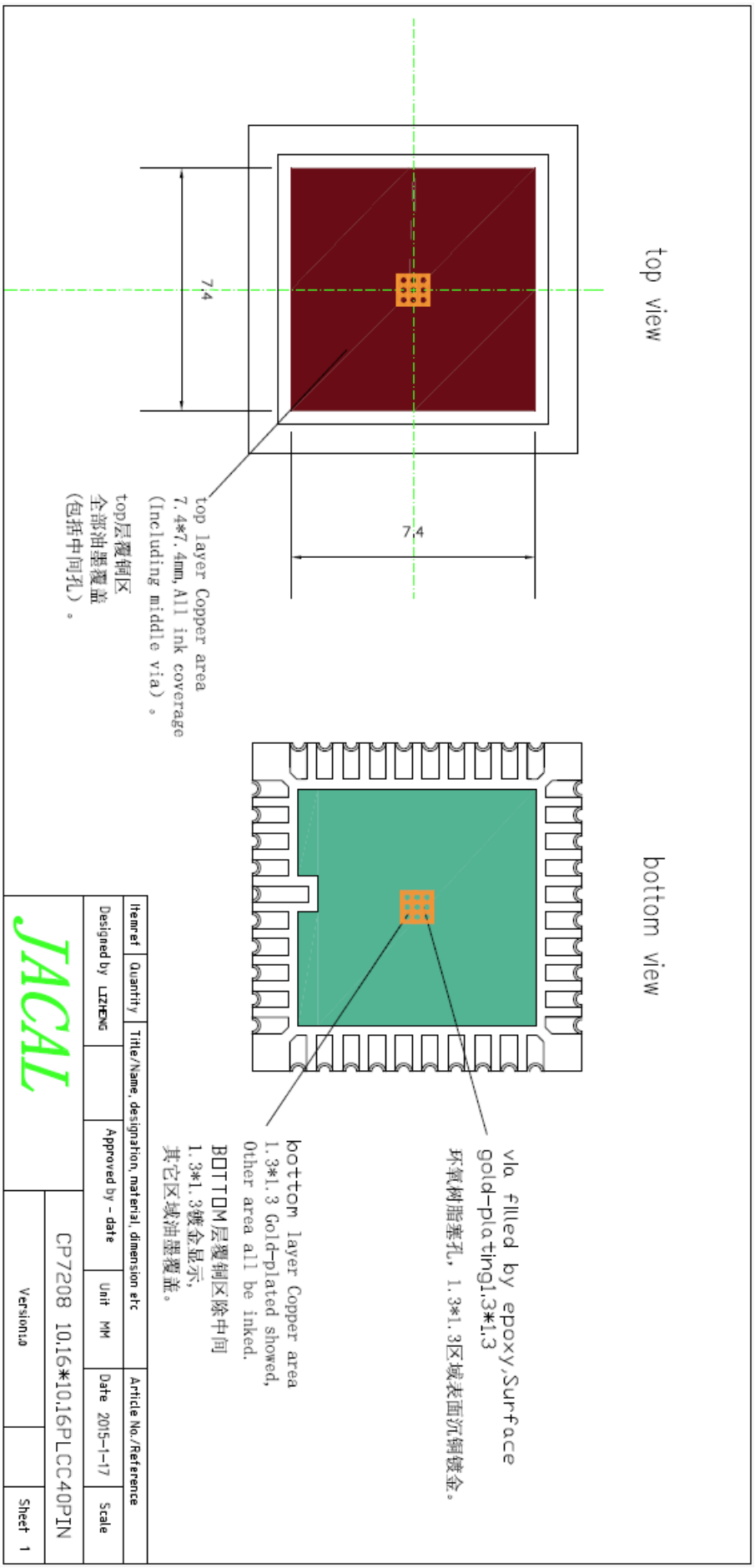


R1,R2,R3,R4 = 1.3KΩ
R5 = 1MΩ
C1,C3,C5,C7 = 0.1uF
C2,C4,C6,C8 = 10uF
C9 = 1uF
C10,C11 = 8pF(C_L : 9pF)

Figure 20-2 Typical Circuit Configuration(Digital)

21. PKG Dimension




top view
7.4
7.4
top layer Copper area
7.4*7.4mm,All ink coverage
(Including middle via) 。
top层覆铜区
全部油墨覆盖
(包括中间孔) 。
bottom view
via filled by epoxy,Surface
gold-plating1.3*1.3
环氧树脂塞孔，1.3*1.3区域表面沉铜镀金。
bottom layer Copper area
1.3*1.3 Gold-plated showed,
Other area all be inked.
BOTTOM层覆铜区除中间
1.3*1.3镀金显示,
其它区域油墨覆盖。
JACAL
Itemref
Quantity
Title/Name, designation, material, dimension etc
Article No./Reference
Designed by LIZHENG
Approved by - date
Unit MM
Date 2015-1-17
Scale
CP7208 10.16*10.16PLCC40PIN
Version.a
Sheet 1