

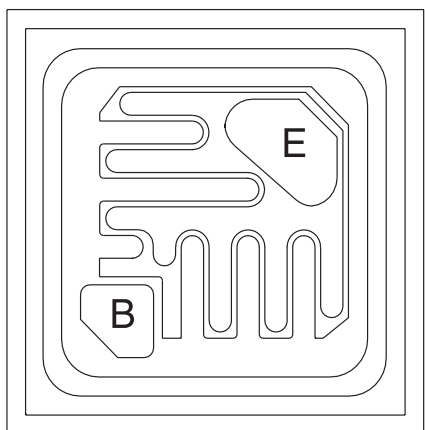
PROCESS CP716
Small Signal Transistor
PNP - High Voltage Transistor Chip

CentralTM
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	20 x 20 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	4.0 x 4.0 MILS
Emitter Bonding Pad Area	4.7 x 4.7 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 4 INCH WAFER

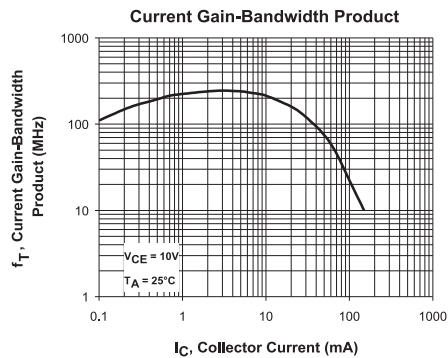
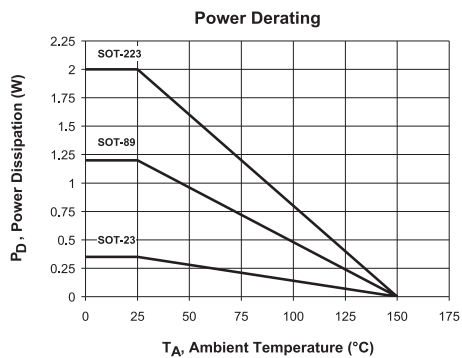
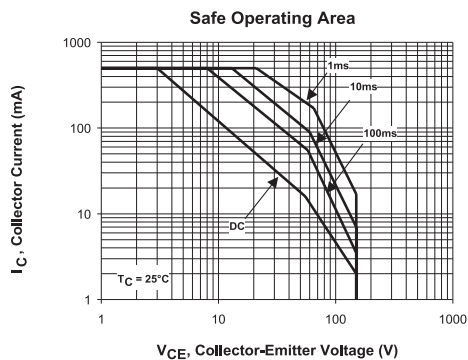
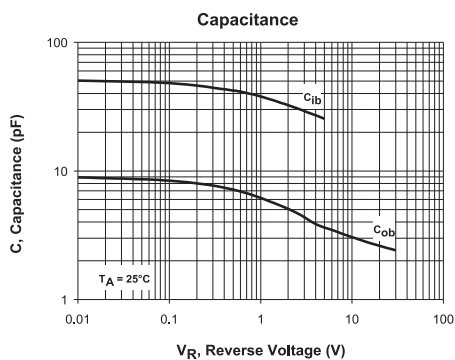
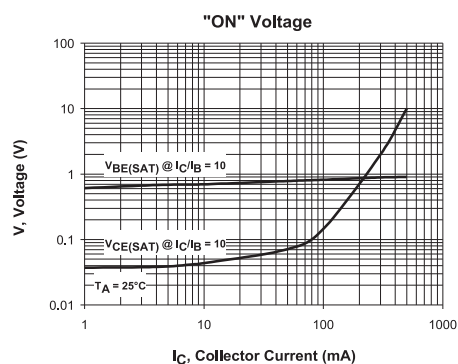
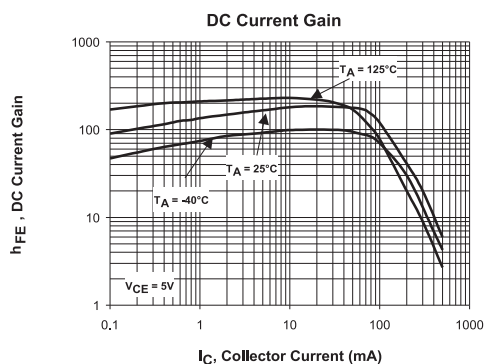
29,250

PRINCIPAL DEVICE TYPES

CMPT5401
CXT5401
CZT5401
2N5401

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centrasemi.com

R2 (1-August 2002)



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