

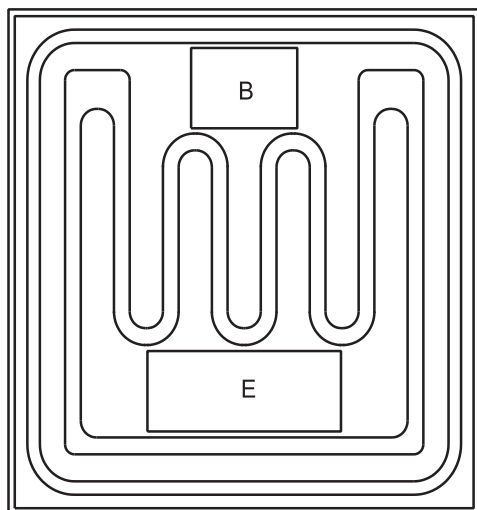
PROCESS CP712
Power Transistor
PNP - Amp/Switch Transistor Chip

CentralTM
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	75 x 75 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	17 x 12 MILS
Emitter Bonding Pad Area	31 x 12 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ti/Ni/Ag - 11,300Å

GEOMETRY



BACKSIDE COLLECTOR

R0

GROSS DIE PER 4 INCH WAFER

1,960

PRINCIPAL DEVICE TYPES

CZT7120

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

R1 (1-August 2002)



The Typical Electrical Characteristics data
for this chip is currently being revised.

For the latest updated data for this Chip Process,
please visit our website at:

www.centrasemi.com/chip

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