PROCESS CP555

Small Signal Transistor

PNP - Saturated Switch Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	15 x 10 MILS
Die Thickness	8.0 MILS
Base Bonding Pad Area	3.6 x 2.4 MILS
Emitter Bonding Pad Area	3.6 x 2.4 MILS
Top Side Metalization	Al - 20,000Å
Back Side Metalization	Au - 15,000Å

GEOMETRY

BACKSIDE COLLECTOR

R0

GROSS DIE PER 4 INCH WAFER

76,000

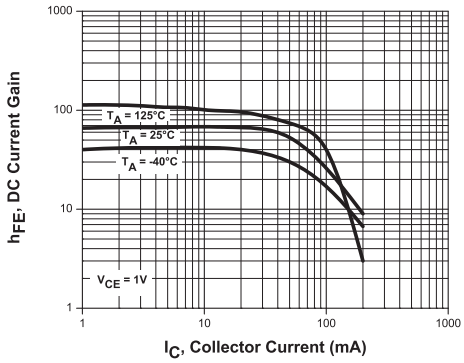
PRINCIPAL DEVICE TYPES

CMPT3640
CMPT4209
2N4209

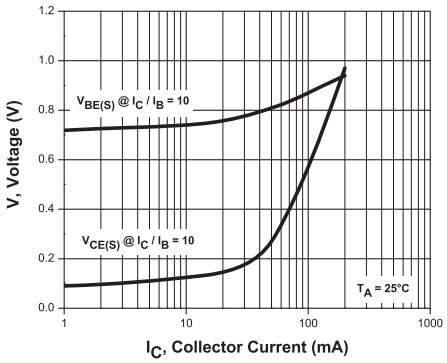
PROCESS CP555

Typical Electrical Characteristics

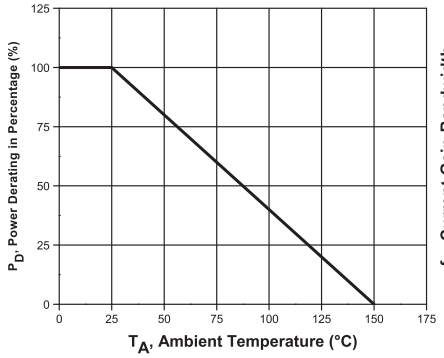
DC Current Gain



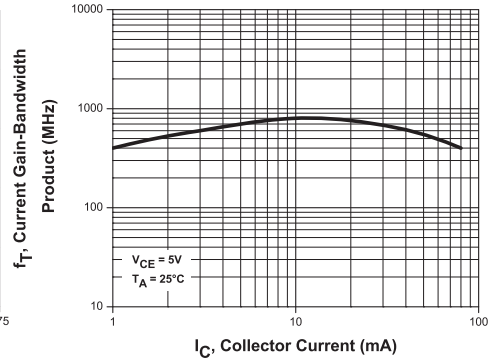
"ON" Voltage



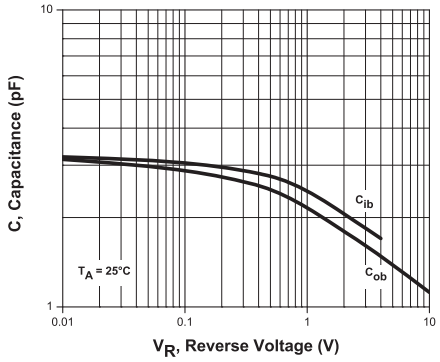
Normalized Power Derating



Current Gain-Bandwidth Product



Capacitance



R4 (22-March 2010)