PROCESS CP315V

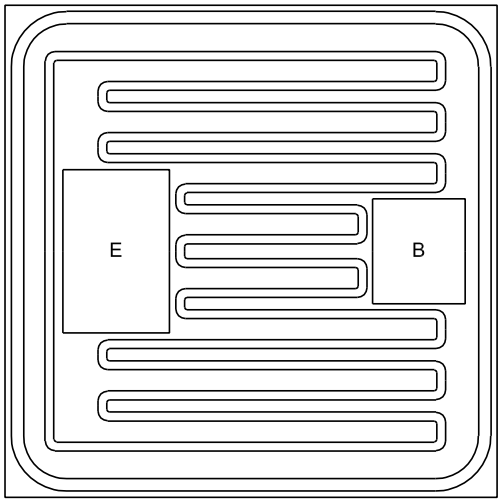
Power Transistors

NPN - High Current Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	40 x 40 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	7.9 x 8.7 MILS
Emitter Bonding Pad Area	9.0 x 14 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 12,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 4 INCH WAFER

6,936

PRINCIPAL DEVICE TYPES

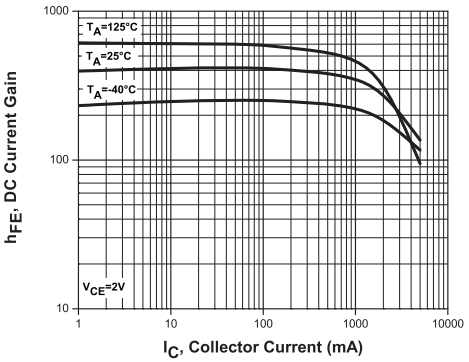
CXT3150
CZT3150

R2 (22-March 2010)

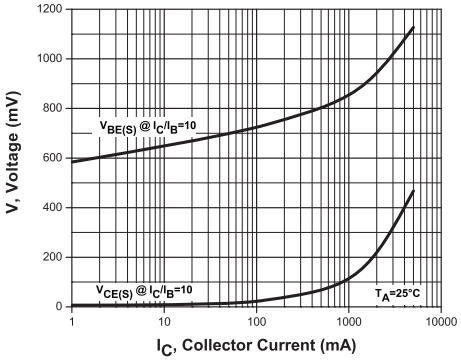
PROCESS CP315V

Typical Electrical Characteristics

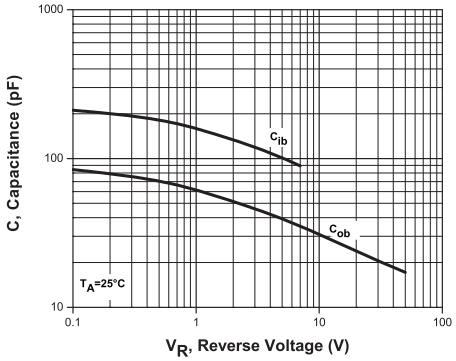
DC Current Gain



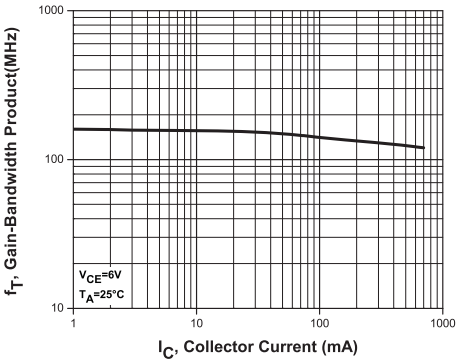
"ON" Voltage



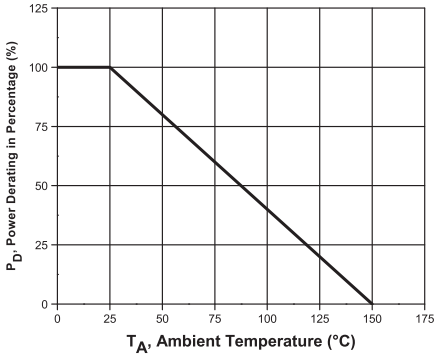
Capacitance



Current Gain-Bandwidth Product



Normalized Power Derating



R2 (22-March 2010)