PROCESS CP188

Small Signal Transistor

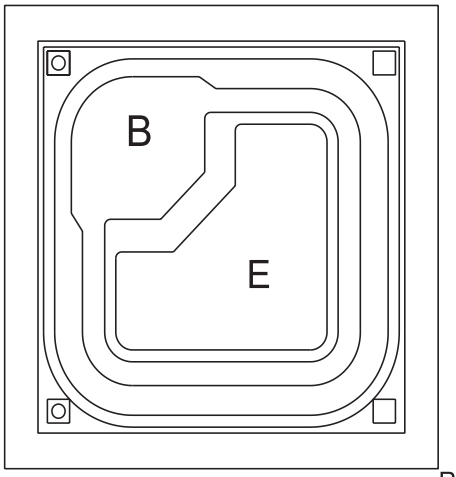
NPN - Low Noise Amplifier Transistor Chip

Central™ Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	15 x 15 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	4.0 x 4.0 MILS
Emitter Bonding Pad Area	5.5 x 5.5 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR

R1

GROSS DIE PER 4 INCH WAFER

53,730

PRINCIPAL DEVICE TYPES

CMPT2484
CMPT5088
CMPT5089
CMPT6428
CMPT6429
2N2484

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

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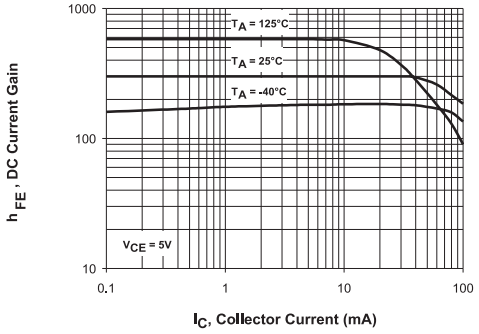
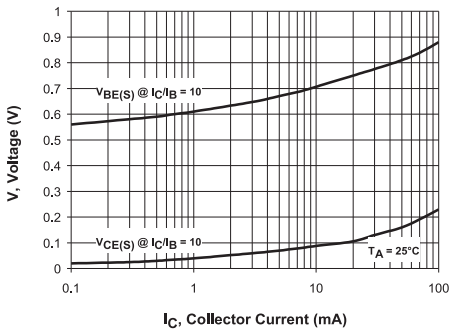
Typical Electrical Characteristics

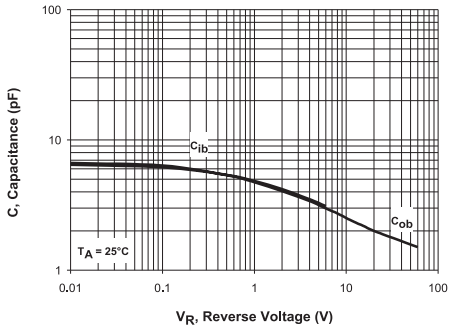
DC Current Gain



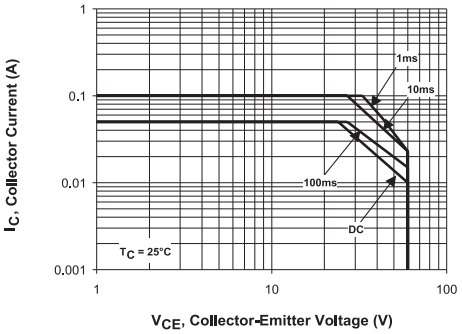
"ON" Voltage



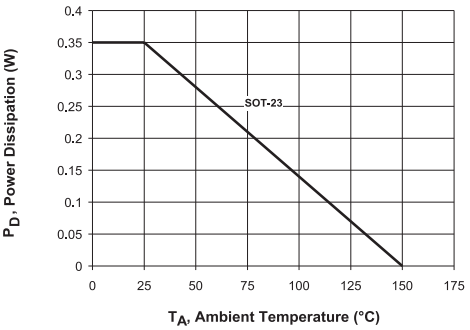
Capacitance



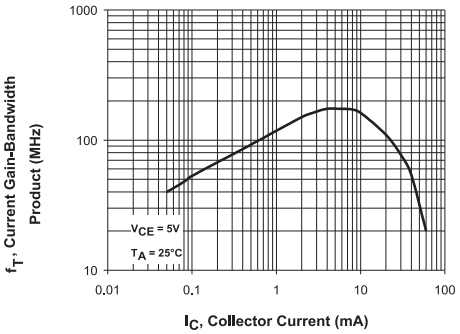
Safe Operating Area



Power Derating



Current Gain-Bandwidth Product



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