STANDARD MICROSYSTEMS CORPORATION

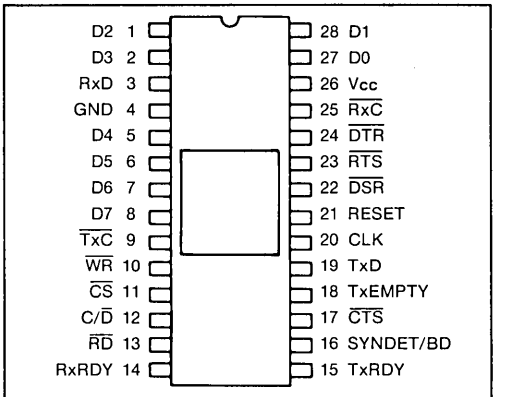
COM 8251A
μPC FAMILY

Universal Synchronous/Asynchronous Receiver/Transmitter USART

FEATURES

- ☐ Asynchronous or Synchronous Operation
  - —Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate—1, 16 or 64 X Baud Rate
    - Break Character Generation
    - 1, 1½ or 2 Stop Bits
    - False Start Bit Detection
    - Automatic Break Detect and Handling
  - —Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
    - Programmable Sync Character(s)
- ☐ Baud Rate—Synchronous—DC to 64K Baud
  —Asynchronous—DC to 19.2K Baud
- ☐ Baud Rates available from SMC's COM 8116, COM 8126, COM 8136, COM 8146, and COM 8046
- ☐ Full Duplex, Double Buffered Transmitter and Receiver
- ☐ Odd parity, even parity or no parity bit
- ☐ Parity, Overrun and Framing Error Flags
- ☐ Modem Interface Controlled by Processor
- ☐ All Inputs and Outputs are TTL Compatible

PIN CONFIGURATION



PACKAGE: 28-pin D.I.P.

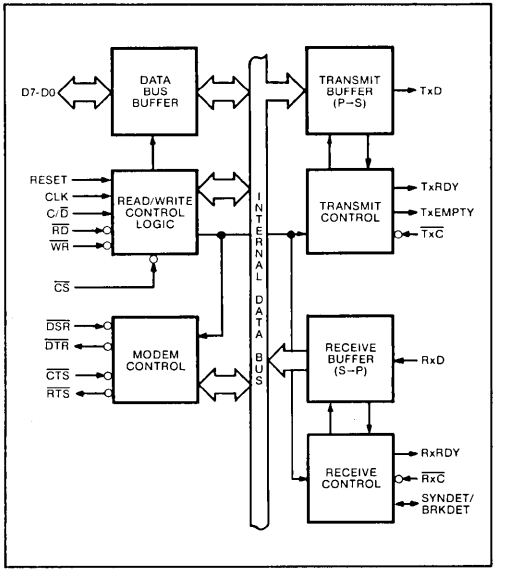
- ☐ Compatable with Intel 8251A, NEC μPD8251A
- ☐ Single +5 Volt Supply
- ☐ Separate Receive and Transmit TTL Clocks
- ☐ Enhanced version of 8251
- ☐ 28 Pin Plastic or Ceramic DIP Package
- ☐ COPLAMOS® N-Channel MOS Technology

GENERAL DESCRIPTION

The COM 8251A is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology that meets the majority of asynchronous and synchronous data communication requirements by interfacing parallel digital systems to asynchronous and synchronous data communication channels while requiring a minimum of processor overhead. The COM 8251A is an enhanced version of the 8251.

The COM 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asychronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status, including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

BLOCK DIAGRAM



PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1, 2, 27, 28, 5-8	D2, D3, D0, D1, D4-D7	DATA BUS	I/O	An 8-bit, 3-state bi-directional DATA BUS used to interface the COM 8251A to the processor data bus. Data is transmitted or received by the bus in response to input/output or Read/Write instructions from the processor. The DATA BUS also transfers Control words, Command words, and Status.
3	RxD	RECEIVER DATA	I	This input receives serial data into the USART.
4	GND	GROUND	GND	Ground
9	$\overline{TxC}$	$\overline{TRANSMITTER\ CLOCK}$	I	The $\overline{TRANSMITTER\ CLOCK}$ controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1X, 16X, or 64X the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
10	$\overline{WR}$	$\overline{WRITE\ DATA}$	I	A "zero" on this input instructs the COM 8251A to accept the data or control word which the processor is writing out to the USART via the DATA BUS.
11	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	A "zero" on this input enables the USART for reading and writing to the processor. When $\overline{CS}$ is high, the DATA BUS is in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.
12	C/$\overline{D}$	CONTROL/$\overline{DATA}$	I	The Control/$\overline{Data}$ input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the DATA BUS. 0 = Data; 1 = Control/Status
13	$\overline{RD}$	$\overline{READ\ DATA}$	I	A "zero" on this input instructs the COM 8251A to place the data or status information onto the DATA BUS for the processor to read.
14	RxRDY	RECEIVER READY	O	The RECEIVER READY output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
15	TxRDY	TRANSMITTER READY	O	TRANSMITTER READY signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information polled operaton. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the processor.
16	SYNDET/ BRKDET	SYNC DETECT/ BREAK DETECT	I/O	The SYNDET feature is only used in the Synchronous mode. The USART may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal SYNC mode, the SYNDET output will go to a "one" when the COM 8251A has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second contiguously detected SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input is sampled during the negative half cycle of $\overline{RxC}$ and will cause the COM 8251A to start assembling data character on the next rising edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the COM 8251A is in SYNC. When external SYNC DETECT is programmed, the internal SYNC DETECT is disabled.

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
16 (cont.)				The SYNDET/BRKDET pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the BREAK DETECT output will go high when an all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx Data returns to a logic one state or upon chip RESET. The state of BREAK DETECT can also be read as a status bit.
17	$\overline{CTS}$	$\overline{CLEAR\ TO\ SEND}$	I	A "zero" on the $\overline{CLEAR\ TO\ SEND}$ input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one). If either a TxEN off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART written prior to the Tx Disable command before shutting down.
18	TxE	TRANSMITTER EMPTY	O	The TRANSMITTER EMPTY output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around". The TxEN bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a SYNC character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded; an underflow condition. If the USART is operating in the two SYNC character mode, both SYNC characters will be transmitted before the message can resume. TxE does not go low when the SYNC characters are being shifted out. TxE goes low upon the processor writing a character to the USART.
19	TxD	TRANSMITTER DATA	O	This output is the transmitted serial data from the USART. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
20	CLK	CLOCK PULSE	I	The CLK input provides for internal device timing. External inputs and outputs are not referenced to CLK, but the CLK frequency must be greater than 30 times the RECEIVER or TRANSMITTER CLOCKS in the 1X mode and greater than 4.5 times for the 16X and 64X modes.
21	RESET	RESET	I	A "one" on this input forces the USART into the "idle" mode where it will remain until reinitialized with a new set of control words. RESET causes: RxRDY = TxRDY = TxEmpty = SYNDET/BRKDET = 0; TxD = $\overline{DTR}$ = $\overline{RST}$ = 1. Minimum RESET pulse width is 6 t_{CY}, CLK must be running during RESET.
22	$\overline{DSR}$	$\overline{DATA\ SET\ READY}$	I	The $\overline{DATA\ SET\ READY}$ input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
23	$\overline{RTS}$	$\overline{REQUEST\ TO\ SEND}$	O	The $\overline{REQUEST\ TO\ SEND}$ output is controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
24	$\overline{DTR}$	$\overline{DATA\ TERMINAL\ READY}$	O	The $\overline{DATA\ TERMINAL\ READY}$ output is controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
25	$\overline{RxC}$	$\overline{RECEIVER\ CLOCK}$	I	The $\overline{RECEIVER\ CLOCK}$ is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1, 16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1X, 16X or 64X or Synchronous operation at 1X the Baud Rate. Data is sampled into the USART on the rising edge of $\overline{RxC}$.
26	V_{CC}	V_{CC} SUPPLY VOLTAGE	PS	+5 volt supply

DESCRIPTION OF OPERATION—ASYNCHRONOUS

Transmission—

When a data character is written into the USART, it automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at a transmission rate of $\overline{TxC}$, $\overline{TxC}$/16 or $\overline{TxC}$/64, as defined by the Mode Instruction.

If no data characters have been loaded into the USART, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

Receive—

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge (high to low transition) at RxD signals the possible beginning of a START bit and a new character. The receiver is thus prevented from starting in a "BREAK" state. The START bit is verified by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After the STOP bit time, the input character is loaded into the parallel Data Bus Buffer of the USART and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

DESCRIPTION OF OPERATION—SYNCHRONOUS

Transmission—

As in Asynchronous transmission, the TxD output remains "high" (marking) until the USART receives the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ at the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Data Protocols require that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the USART Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until the new data characters are available for transmission. If the USART becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

Receive—

In Synchronous receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, the ENTER HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the contents of the Receive Buffer are compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the (two contiguous) SYNC character(s) programmed have been detected, the USART leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost. Under this condition the Rx register will be cleared to all "ones".

The microprocessor program controlling the COM 8251A performs these tasks:

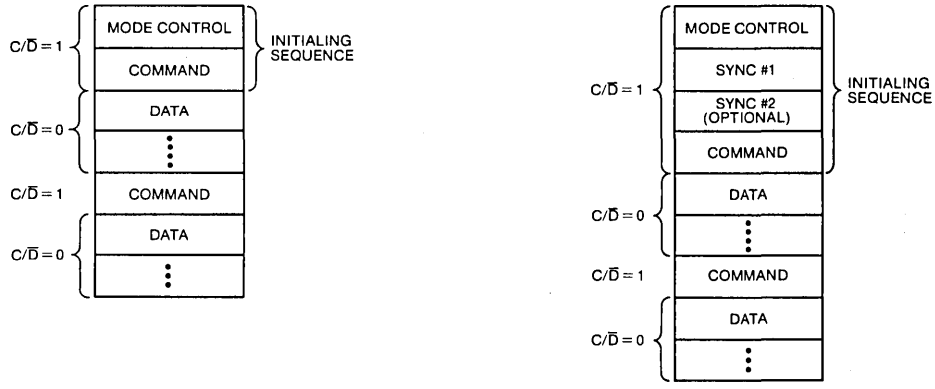
- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which has been received

Control codes determine the mode in which the COM 8251A will operate and are used to set or reset control signals output by the COM 8251A.

The Status register contents will be read by the program monitoring this device's operation in order to determine error conditions, when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.

INITIALIZING THE COM 8251A

Figure 1. Control Word Sequences for Initialization



ASYNCHRONOUS OPERATION **SYNCHRONOUS OPERATION**

The COM 8251A may be initialized following a system RESET or prior to starting a new seral I/O sequence. The USART must be RESET (external or internal) following power up and subsequently may be reset at any time following completion of one activity and preceding a new set of operations. Following a reset, the COM 8251A enters an idle state in which it can neither transmit nor receive data.

The COM 8251A is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the COM 8251A, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters, and then a command.

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a RESET (external or internal), the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following a RESET input or following an internal reset command. A reset operation (internal via IR or external via RESET) will cause the USART to interpret the next "control write", which should immediately follow the reset, as a Mode Instruction.

After receiving the control words the USART is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. Concurrently, the USART is ready to receive serial data.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	USART → Data Bus
0	1	0	0	Data Bus → USART
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

MODE CONTROL CODES

The COM 8251A interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse, as programmed. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character. In the case of a programmed character length of less than 8 bits, the least significant DATA BUS unused bits are "don't care" when writing data to the USART and will be "zeros" when reading data. Rx data will be right justified onto D0 and the LSB for Tx data is D0.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1½ or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16X or 64X baud rate factor. In these two cases, the half stop bit will be equivanlent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

COMMAND WORDS

Command words are used to initiate specific functions within the COM 8251A such as, "reset all error flags" or "start searching for sync". Consequently, Command Words may be issued by the processor to the COM 8251A at any time during the execution of a program in which specific functions are to be initialized within the communication circuit.

Figure 4 shows the format for the Command Word.

Figure 4. COM 8251A Control Command

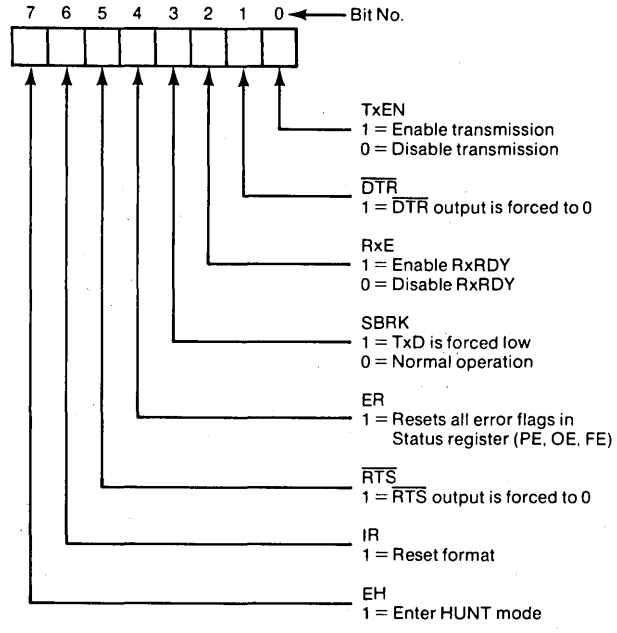


Figure 2. Synchronous Mode Control Code.

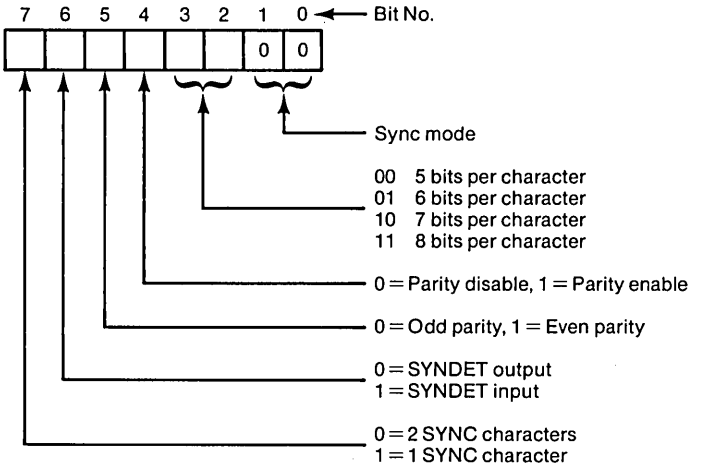
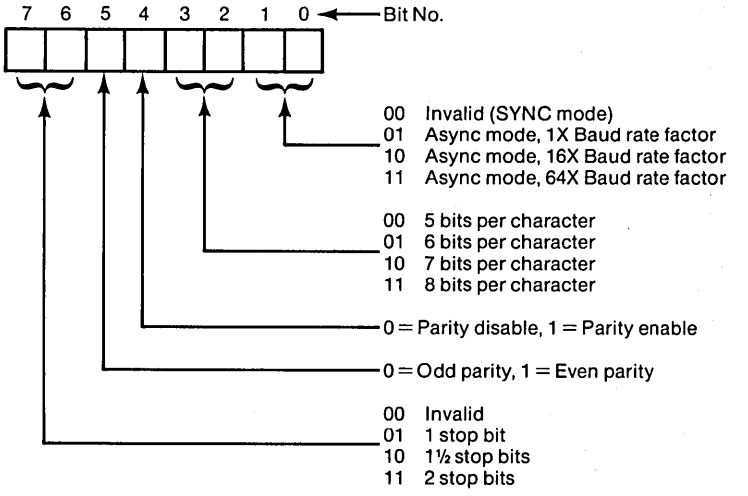


Figure 3. Asynchronous Mode Control Code.



Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission for the COM 8251A cannot take place unless TxEN is set (assuming $\overline{CTS} = 0$) in the command register. The TX Disable command is prevented from halting transmission by the Tx Enable logic until all data previously written has been transmitted. Figure 5 defines the way in which TxEN, TxE and TxRDY combines to control transmitter operations.

Bit 1 is the Data Terminal Ready ($\overline{DTR}$) bit. When the $\overline{DTR}$ command bit is set, the $\overline{DTR}$ output connection is active (low). $\overline{DTR}$ is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE, when zero, prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the Receiver Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

Figure 5.
Operation of the Transmitter Section as a Function of TxE, TxRDY and TxEN

TxEN	TxE	TxRDY	
1	1	1	Transmit Output Register and Transmit Character Buffer empty. TxD continues to mark if COM 8251A is in the asynchronous mode. TxD will send SYNC pattern if COM 8251A is in the Synchronous Mode. Data can be entered into Buffer.
1	0	1	Transmit Output Register is shifting a character. Transmit Character Buffer is available to receive a new byte from the processor.
1	1	0	Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition.
1	0	0	Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission.
0	0/1	0/1	Transmitter is disabled.

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level, (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the COM 8251A to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transferred with the ER bit set, all three error flags (PE, OE, FE) in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the COM 8251A. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit ($\overline{RTS}$), sets a latch to reflect the $\overline{RTS}$ signal level. The output of this latch is created independently of other signals in the COM 8251A. As a result, data transfers may be made by the processor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of $\overline{RTS}$.

Bit 6, the Internal Reset (IR), causes the COM 8251A to return to the Idle mode. All functions within the COM 8251A cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a processor program, the COM 8251A must first be reset. Either the RESET input can be activated, or the Internal Reset Command can be sent to the COM 8251A. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the COM 8251A when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input, clear the Rx register to all "ones", and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will continue indefinitely until EH is reset when a subsequent Command Word is sent, when the IR command is sent to the COM 8251A, or when SYNC characters are recognized. Parity is not checked in the EH mode.

STATUS REGISTER

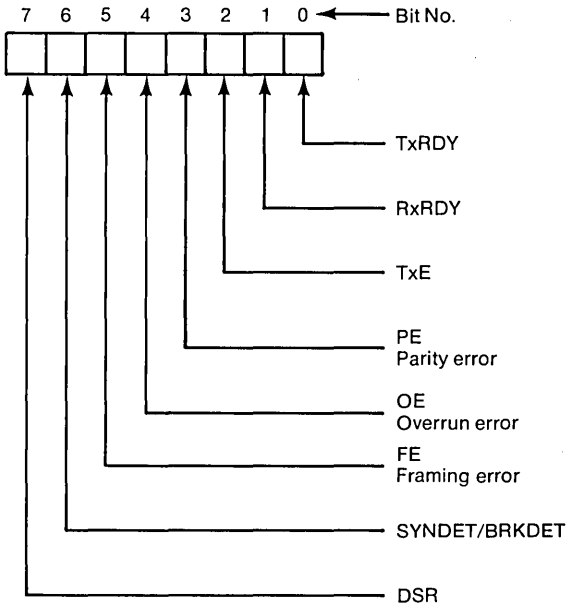
The Status Register maintains information about the current operational status of the COM 8251A. Status can be read at any time, however, the status update will be inhibited during status read. Figure 6 shows the format of the Status Register.

TxRDY signals the processor that the Transmit Character Buffer is empty and that the COM 8251A can accept a new character for transmission. The TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:

TxRDY (status bit) = Tx Character Buffer Empty
TxRDY (pin 15) = Tx Character Buffer Empty • $\overline{CTS}$ • TxEN

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

Figure 6. The COM 8251A Status Register



TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits. PE does not inhibit USART operation. PE is reset by the ER bit.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor. OE does not inhibit USART operation. OE is reset by the ER bit.

FE (Async only) is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect bit format ("0" stop bit), as specified by the current mode. FE does not inhibit USART operaton. FE is reset by the ER bit.

SYNDET is the synchronous mode status bit associated with internal or external sync detection.

DSR is the status bit set by the external $\overline{\text{Data Set Ready}}$ signal to indicate that the communication Data Set is operational.

All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset by the error reset command or the internal reset command or the RESET input. OE, FE, or PE being set does not inhibit USART operation.

Many of the bits in the status register are copies of external pins. This dual status arrangement allows the USART to be used in both Polled and Interrupt driven environments. Status update can have a maximum delay of 16 t_{CY} periods.

Note:

1. While operating the receiver it is important to realize that the RxE bit of the Command Instruction only inhibits the assertion of RxRDY; it does not inhibit the actual reception of characters. As the receiver is constantly running, it is possible for it to contain extraneous data when it is enabled. To avoid problems this data should be read from the USART and discarded. This read should be done immediately following the setting of the RxE bit in the asynchronous mode, and following the setting of EH in the synchronous mode. It is not necessary to wait for RxRDY before executing the dummy read.
2. ER should be performed whenever RxE of EH are programmed. ER resets all error flags, even if RxE = 0.
3. The USART may provide faulty RxRDY for the first read after power-on or for the first read after the receiver is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. This is not the case for the first read after hardware or software reset after the device opration has been established.
4. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through an internal flip-flop which clears itself, assuming the External Sync Detect assertion has removed, upon a status read. As long as External Sync Detect is asserted, External Sync Detect Status will remain high.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that as clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
D.C. Characteristics					
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ TO 0.45V
I_{IL}	Input Leakage		±10	μA	$V_{IN} = V_{CC}$ TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High
Capacitance					$T_A = 25°C$, $V_{CC} = GND$
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND
A.C. Characteristics					
Bus Parameters (Note 1)					
Read Cycle:					
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		200	ns	Note 3, $C_L = 150$ pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	
Write Cycle:					
t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	0		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	250		ns	
t_{DW}	Data Set Up Time for $\overline{WRITE}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	0		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4
Other Timings:					
t_{CY}	Clock Period	.320	1.35	μs	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	120	$t_{CY}-90$	ns	
$t_{\overline{\phi}}$	Clock Low Pulse Width	90		ns	

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
t_R, t_F	Clock Rise and Fall Time	5	20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse	2		μs	
t_{HRx}	Rx Data Hold Time to Sampling Pulse	2		μs	
f_{Tx}	Transmitter Input Clock Frequency				
	1X Baud Rate	DC	64	kHz	
	16X Baud Rate	DC	310	kHz	
	64X Baud Rate	DC	615	kHz	
t_{TPW}	Transmitter Input Clock Width				
	1X Baud Rate	12		t_{CY}	
	16X and 64X Baud Rate	1		t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay				
	1X Baud Rate	15		t_{CY}	
	16X and 64X Baud Rate	3		t_{CY}	
f_{Rx}	Receiver Input Clock Frequency				
	1X Baud Rate	DC	64	kHz	
	16X Baud Rate	DC	310	kHz	
	64X Baud Rate	DC	615	kHz	
t_{RPW}	Receiver Input Clock Pulse Width				
	1X Baud Rate	12		t_{CY}	
	16X and 64X Baud Rate	1		t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay				
	1X Baud Rate	15		t_{CY}	
	16X and 64X Baud Rate	3		t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		150	ns	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of last Bit		24	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		150	ns	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		24	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time Before Falling Edge of $\overline{RxC}$		16	t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Data Bit		20	t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE ($\overline{TxEn}$, $\overline{DTR}$, $\overline{RTS}$)		8	t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)		20	t_{CY}	Note 7

NOTES: 1. AC timings measured $V_{OH} = 2.0$, $V_{OL} = 0.8$, and with load circuit of Figure 1.
2. Chip Select ($\overline{CS}$) and Command/Data (C/$\overline{D}$) are considered as Addresses.
3. Assumes that Address is valid before RD↓.
4. This recovery time is for RESET and Mode Initialization. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
5. The TxC and RxC frequencies have the following limitations with respect to CLK.
   For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
   For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during RESET.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

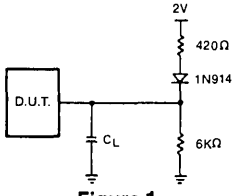
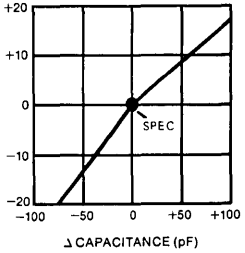


Figure 1.

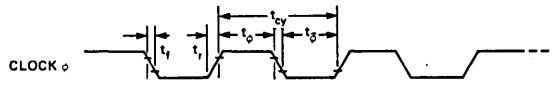
TEST LOAD CIRCUIT

Typical Δ Output Delay Versus Δ Capacitance (pF)

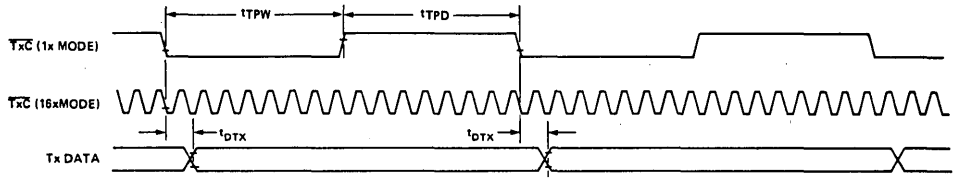


WAVEFORMS

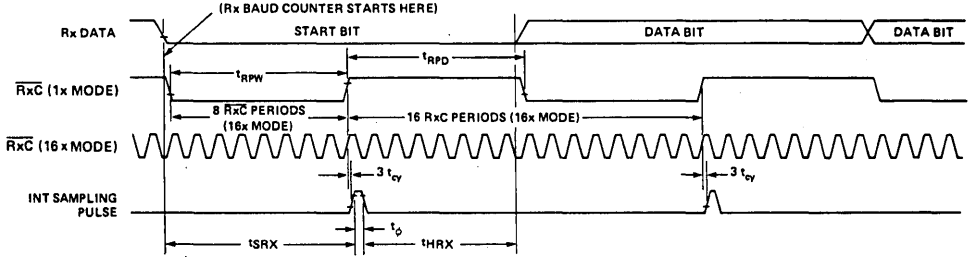
System Clock Input



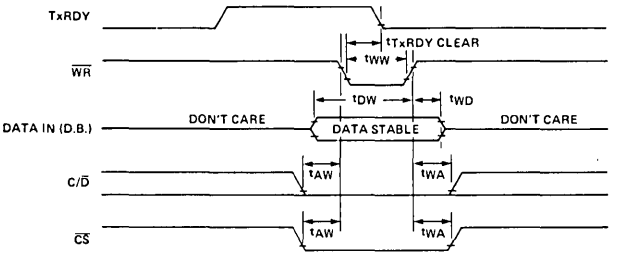
Transmitter Clock & Data



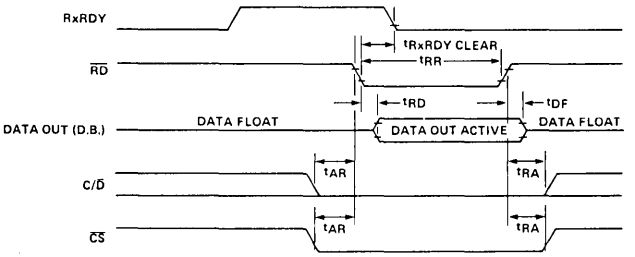
Receiver Clock & Data



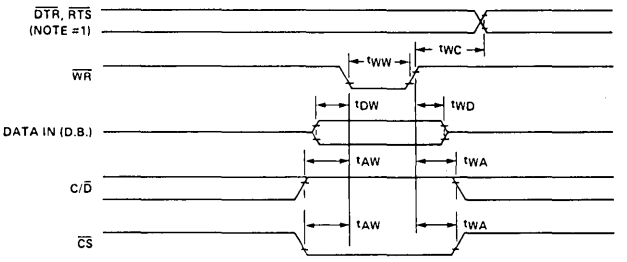
Write Data Cycle (CPU → USART)



Read Data Cycle (CPU ← USART)

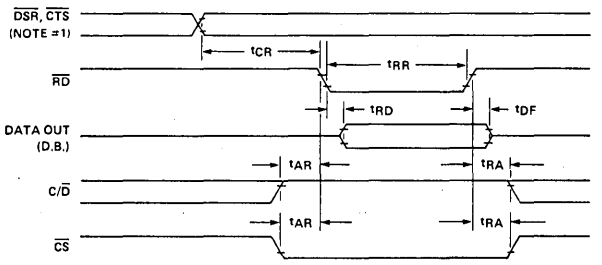


Write Control or Output Port Cycle (CPU → USART)



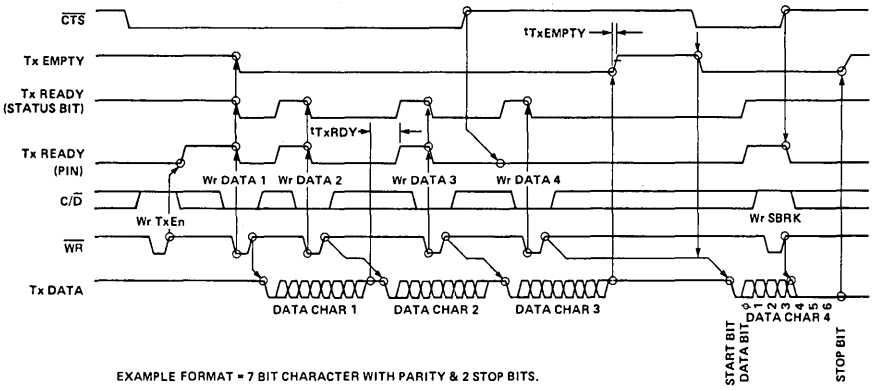
NOTE #1: T_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE.

Read Control or Input Port (CPU ← USART)



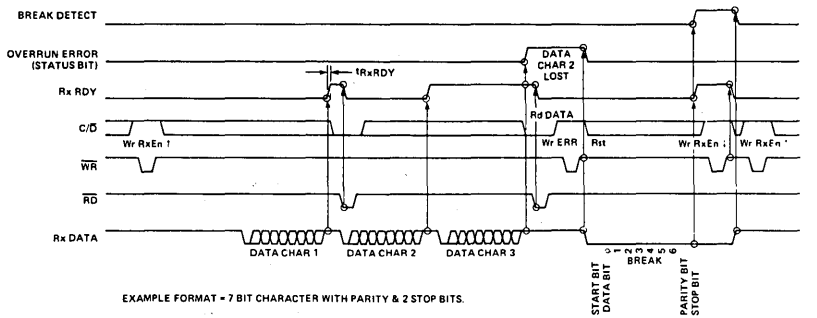
NOTE #1: T_{CR} INCLUDES THE EFFECT OF $\overline{CTS}$ ON THE TxENBL CIRCUITRY.

Transmitter Control & Flag Timing (ASYNC Mode)



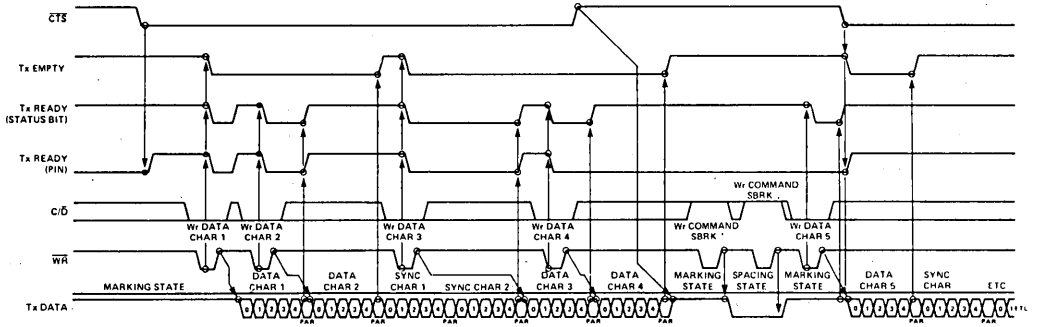
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

Receiver Control & Flag Timing (ASYNC Mode)



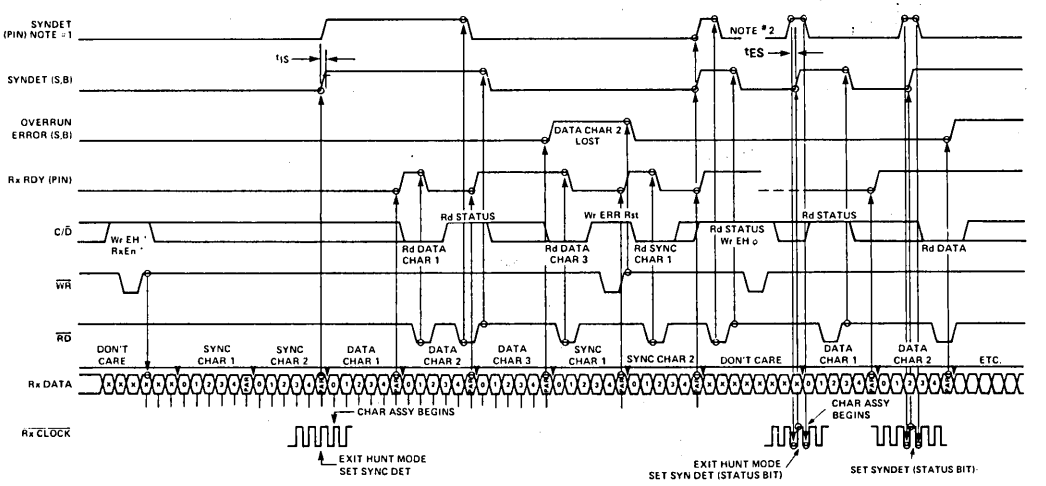
EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY & 2 STOP BITS.

Transmitter Control & Flag Timing (SYNC Mode)



EXAMPLE FORMAT = 5 BIT CHARACTER WITH PARITY, 2 SYNC CHARACTERS.

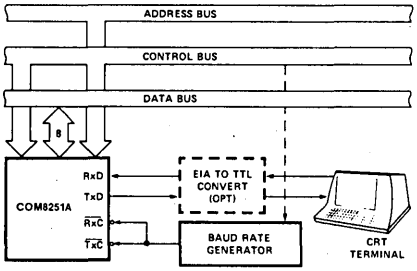
Receiver Control & Flag Timing (SYNC Mode)



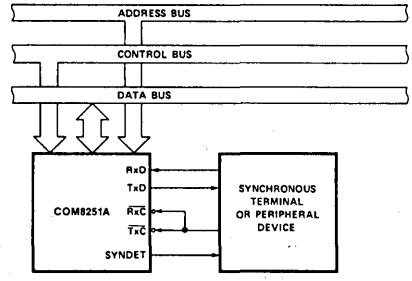
NOTE #1: INTERNAL SYNC, 2 SYNC CHARACTERS, 5 BITS, WITH PARITY
NOTE #2: EXTERNAL SYNC, 5 BITS, WITH PARITY

APPLICATION OF THE COM8251A

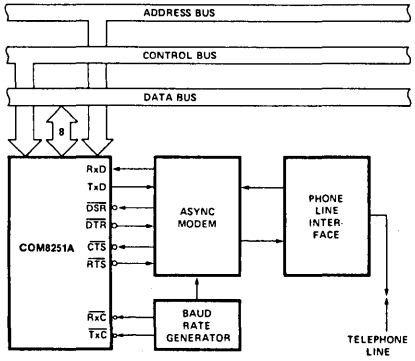
Asynchronous Serial Interface to CRT Terminal, DC to 9600 Baud



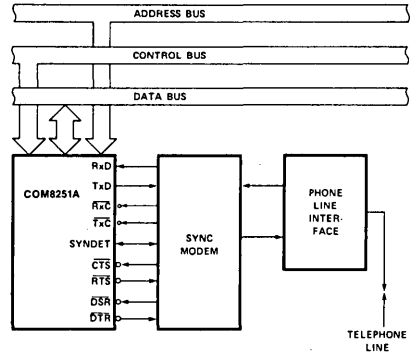
Synchronous Interface to Terminal or Peripheral Device



Asynchronous Interface to Telephone Lines



Synchronous Interface to Telephone Lines



COM8251A Interface to μP Standard System Bus