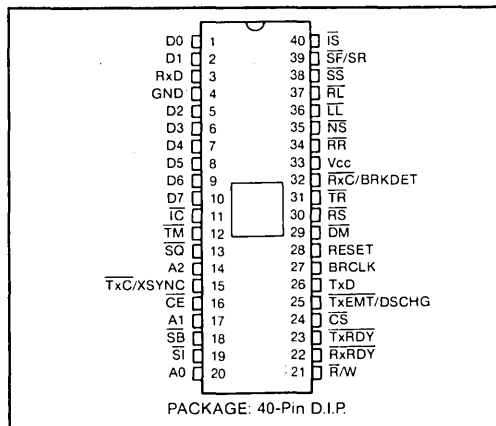


# RS-449 Programmable Communications Interface

## FEATURES

- ☐ RS-449 compatible inputs and outputs
- ☐ Maskable Interrupts for RS-449 inputs
- ☐ Synchronous and Asynchronous Full Duplex or Half Duplex Operations
- ☐ Re-programmable ROM on-chip baud rate generator
- ☐ Synchronous Mode Capabilities
  - Selectable 5 to 8-Bit Characters
  - Selectable 1 or 2 SYNC Characters
  - Internal or External Character Synchronization
  - Transparent or Non-Transparent Mode
  - Transparent mode DLE stuffing (Tx) and detection (Rx)
  - Automatic SYNC or DLE-SYNC Insertion
  - SYNC, DLE and DLE-SYNC stripping
  - Odd, Even, or No Parity
  - Local or remote maintenance loop back mode
- ☐ Asynchronous Mode Capabilities
  - Selectable 5 to 8-Bit Characters plus parity
  - 3 Selectable Clock Rates (1X, 16X, 64X the Baud Rate)
  - Line Break Detection and Generation
  - 1, 1½, or 2-Stop Bit Detection and Generation
  - False Start Bit Detection
  - Odd, Even, or No Parity
  - Parity, Overrun, and framing error detect
  - Local or remote maintenance loop back mode
  - Automatic serial echo mode (echoplex)
- ☐ Baud Rates
  - DC to 1.0M Baud (Synchronous)
  - DC to 1.0M Baud (1X, Asynchronous)

## PIN CONFIGURATION



PACKAGE: 40-Pin D.I.P.

- DC to 62.5K Baud (16X, Asynchronous)
- DC to 15.625K Baud (64X, Asynchronous)

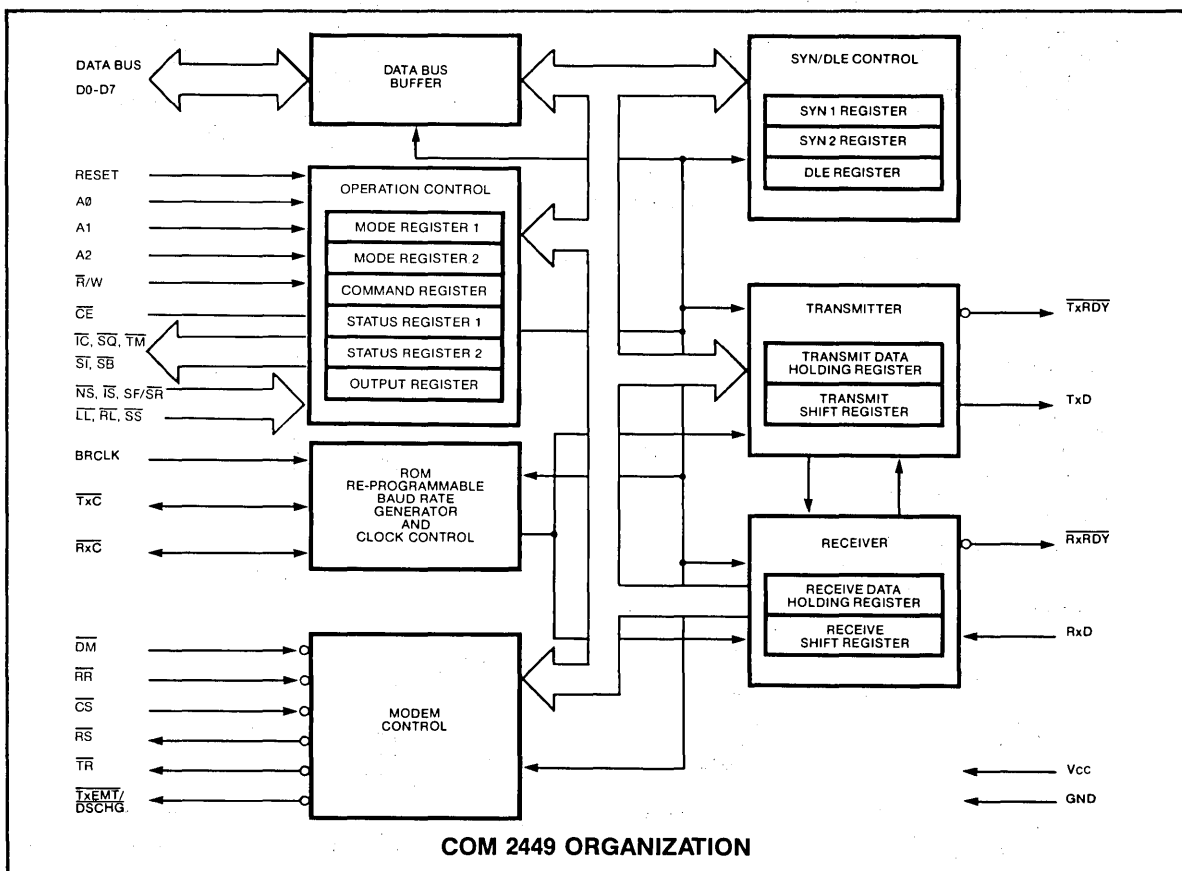
- ☐ Double Buffering of Data
- ☐ RxC and Tx C pins are short circuit protected
- ☐ Internal or External Baud Rate Clock
- ☐ 3 baud rate sets (2449-1, -2, -3)
- ☐ 16 internal rates for each version
- ☐ Single +5 volt Power Supply
- ☐ TTL Compatible
- ☐ No System Clock Required

## GENERAL DESCRIPTION

The COM 2449 is an MOS/LSI device fabricated using SMC's patented COPLAMOS® technology. It is equivalent to the COM 2661 with the additional features required to create the interface to an RS-449 compatible modem. Six new outputs are added to implement the RS-449 signals sent to the Data Communications Equipment (DCE) and five new signals are added to receive the RS-449 status signals from the DCE. A second status register and an output register have been added to allow a processor full control of the additional I/O pins. The COM 2449 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the COM 2449 (-1, -2, -3) has a different set of baud rates. Custom baud rates can be ROM reprogrammed to accommodate different baud rates

and different starting frequencies.

The COM 2449 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for microcomputer system data communications. The USART is used as a peripheral and is programmed by the processor to communicate in commonly used asynchronous and synchronous serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals is available to the processor at any time.



The COM 2449 is organized into 6 major sections. Communication between each section is achieved via an internal data and control bus. The data bus buffer allows a processor access to all internal registers on the COM 2449. The COM 2449 is a COM 2661 with 5 new inputs (readable by the processor from STATUS REGISTER 2) and 6 new outputs (written by the processor via the OUTPUT REGISTER). Each of the 5 new inputs can cause an interrupt condition on the COM 2449. The ability to enable these conditions for interrupt handling is provided. Table 1 outlines the differences between the COM 2661 and the COM 2449. It should be noted that the COM 2449 can be viewed as a general purpose communications interface device with general purpose I/O pins to allow setting output controls and interrogation of input status. This additional I/O capability, although added to allow RS-449 compatibility, can ease the interface to any communications discipline.

### Operation Control

This functional block stores configuration and operation commands from the processor and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with a processor via the data bus and contains Mode Registers 1 and 2, the Command Register, the two Status Registers, and the Output Register. Details of register addressing and protocol are presented in the COM 2449 programming section of this specification.

### Timing

The COM 2449 contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. Tables 2a, b, and c illustrate all available baud rates.

### Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and stores the "assembled" character in the receive data holding register until read by the processor.

### Transmitter

The Transmitter accepts parallel data from the processor, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

### Modem Control

The modem control provides three output signals and accepts three input signals used for "handshaking" and status indication between the COM 2449 and a modem. Five signals to and from the modem control are given names that are in accordance with the RS-449 specification. The signals, however, have an identical function to the corresponding COM 2661 RS-232 compatible signals and this correspondence is shown in Table 1.

## SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the processor. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

## Interface Signals

The COM 2449 interface signals can be grouped into two types: the processor-related signals (shown in Table 3) which interface the COM 2449 to the processor, and the device-related signals (shown in Table 4), which are used to interface to the communications equipment.

## DESCRIPTION OF PIN FUNCTIONS

TABLE 3—PROCESSOR RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
1,2,5,6, 7,8,9,10	Data	D7-D0	Bidirectional; 8 bit, three state data bus used to transfer commands, data and status between the COM 2449 and a processor. D0 is the least significant bit; D7 is the most significant bit.
14,17,20	Address	A2, A1, A0	Input; Address lines used to select COM 2449 registers.
16	Chip Enable	$\overline{CE}$	Input; when this signal is low, the operation specified by the R/W, A2, A1 and A0 will be performed. When this input is high, D7-0 are in the high impedance state.
21	Read/Write	$\overline{R}/W$	Input; Processor read/write direction control. This signal defines the direction of the data bus D7-0 when the COM 2449 is selected. D7-0 drives out (read) when this signal is low and accepts data input when this signal is high. The input only has meaning when the $\overline{CE}$ input is active.
22	Receiver Ready	$\overline{RxRDY}$	Output; This signal is the complement of Status Register 1, bit 1 (SR11). When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the processor. It goes high when the RHR is read by the processor, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the processor.
23	Transmitter Ready	$\overline{TxRDY}$	Output; This signal is the complement of Status Register 1, bit 0 (SR10). When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the processor. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the processor.
25	Transmitter empty/data set change	$\overline{TxEMT}/\overline{DSCHG}$	Output; This signal is the complement of Status Register 1, bit 2 (SR12). When low, it indicates that the transmitter has completed serialization of the last character loaded by the processor, or that a change of state of the DM or RR inputs has occurred. This signal also goes low if the SI, SB, SQ, TM or IC experience a change of state if the corresponding input is enable for interrupt. Interrupt enable bits are located in the 3 most significant bits of Status Register 2 (SR2). This output goes high when Status Register 1 is read by the processor, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the processor for this line to go high. It is an open drain output which can be used as an interrupt to the processor.
28	Reset	RESET	Input; A high on this input performs a master reset on the COM 2449. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
33	Supply Voltage	V <sub>cc</sub>	+5 volt supply.
4	Ground	GND	Ground.

TABLE 4—DEVICE RELATED SIGNALS

PIN NO.	NAME	SYMBOL	FUNCTION
3	Receive Data	RxD	Input: Serial data to the receiver. "Mark" is high, "space" is low.
11	Incoming Call	$\overline{IC}$	Input: This general purpose signal can be used for "incoming call" status from the DCE. Its complement appears in Status Register 2 bit 0 (SR20). When this input is enabled for interrupt via Status Register 2 bit 5 (SR25), a change in its state will cause a low output on TxEMT/DSCHG.
12	Test Mode	$\overline{TM}$	Input: This general purpose signal can be used for "test mode" status from the DCE. Its complement appears in Status Register 2 bit 1 (SR21). When this input is enabled for interrupt via Status Register 2, bit 6 (SR26) a change in its state will cause a low output on TxEMT/DSCHG.
13	Signal Quality	$\overline{SQ}$	Input: This general purpose signal can be used for "signal quality" status from the DCE. Its complement appears in Status Register 2 bit 2 (SR22). When this input is enabled for interrupt via Status Register 2 bit 7 (SR27) a change in its state will cause a low output on TxEMT/DSCHG.

TABLE 4—DEVICE RELATED SIGNALS (Cont'd)

PIN NO.	NAME	SYMBOL	FUNCTION
15	Transmitter Clock/External Sync	$\overline{\text{TxC}}/\text{XSYNC}$	Input or Output: If the external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X, or 64X the baud rate as programmed by mode Register 1. The transmitted data changes on the falling edge of the clock. If the internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
18	Standby Indicator	$\overline{\text{SB}}$	Input: This general purpose signal can be used for "standby indicator" status from the DCE. Its complement appears in Status Register 2 bit 3 (SR23). When this input is enabled for interrupt via Status Register 2 bit 7 (SR27), a change in its state will cause a low output on TxEMT/DSCHG.
19	Signalling Rate Indicator	$\overline{\text{SI}}$	Input: This general purpose signal can be used for "signalling rate indicator" status from the DCE. Its complement appears in Status Register 2 bit 4 (SR24). When this input is enabled for interrupt via Status Register 2 bit 7 (SR27), a change in its state will cause a low output on TxEMT/DSCHG.
24	Clear to Send	$\overline{\text{CS}}$	Input: This signal must be low in order for the transmitter to function. If it goes high during transmission, the character in the Transmit Shift Register will be transmitted before termination.
26	Transmit Data	TxD	Output: Serial data from the transmitter. "Mark" is high, "Space" is low. This signal is held in the "Mark" condition when the transmitter is disabled.
27	Baud Rate Clock	BRCLK	Input: Clock input to the internal baud rate generator (See Tables 2a, b, and c); not required if the external receiver and transmitter clocks are used.
29	Data Mode	$\overline{\text{DM}}$	Input: This general purpose signal can be used for Data Mode, Data Set Ready or Ring Indicator condition. Its complement appears as Status Register 1 bit 7 (SR17). DM causes a low output on TxEMT/DSCHG when its state changes if CR2 or CR0=1.
30	Request to Send	$\overline{\text{RS}}$	Output: This general purpose signal is the complement of the Command Register bit 5 (CR5). It is normally used to indicate Request to Send. If the Transmit Shift Register is not empty when CR5 is reset (1 to 0), then RS will go high on Tx time after the last serial bit is transmitted.
31	Terminal Ready	$\overline{\text{TR}}$	Output: This general purpose signal is the complement of the Command Register bit 1 (CR1). It is normally used to indicate Terminal Ready.
32	Receive Clock/Break Detect	$\overline{\text{RxC}}/\text{BKDET}$	Input or Output: If the external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X, or 64X the Baud rate as programmed by Mode Register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output.
34	Receiver Ready	RR	Input: This signal must be low in order for the receiver to function. The complement appears in Status Register 1 bit 6 (SR16). RR causes a low output on TxEMT/DSCHG when its state changes if CR2 or CR0=1. If RR goes high while receiving, the RxC is internally inhibited.
35	New Signal	$\overline{\text{NS}}$	Output: This signal is used to tell the DCE that a new line signal at the DTE has occurred. This output will go to its low active state when the Output Register, bit 0 (OR0) is set to a logic 1. This output will go to its high inactive state when the Output Register bit 0 (OR0) is set to a logic 0 and the RR input goes high.
36	Local Loopback	$\overline{\text{LL}}$	Output: This general purpose signal can be used to inform the DCE of a "local loopback" test condition. It is the complement of Output Register bit 1 (OR1) which has direct control over the state of this output.
37	Remote Loopback	$\overline{\text{RL}}$	Output: This general purpose signal can be used to inform the DCE of a "remote loopback" test condition. It is the complement of Output Register bit 2 (OR2) which has direct control over the state of this output.
38	Select Standby	$\overline{\text{SS}}$	Output: This general purpose signal can be used to select the normal or standby communication facilities of the DCE. It is the complement of Output Register bit 3 (OR3) which has direct control over the state of this output.
39	Select Frequency/Signal Rate Select	$\overline{\text{SF}}/\text{SR}$	Output: This general purpose signal can be used as a combined "Select Frequency" and "Signal Rate Select". It is the complement of Output Register bit 4 (OR4) which has direct control over the state of this output.
40	Terminal in Service	$\overline{\text{IS}}$	Output: This general purpose signal can be used to inform the DCE of a "Terminal in Service" condition. It is the complement of Output Register bit 5 (OR5) which has direct control over the state of this output.

Table 1 COM 2449 vs. COM 2661

NEW INPUTS		NEW OUTPUTS		I/O SIGNAL NAME EQUIVALENTS	
Symbol	Name	Symbol	Name	COM 2449	COM 2661
IC	incoming call	NS	new signal	DM	DSR
SQ	signal quality	IS	terminal in service	RR	DCD
TM	test mode	SF/SR	select frequency/ signal rate select	CS	CTS
SI	signaling rate indicator	LL	local loopback	TR	DTR
SB	standby select	RL	remote loopback	RS	RTS
		SS	standby select		

Table 2a BAUD RATE GENERATOR CHARACTERISTICS  
2449-1 (BRCLK=4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6144
0001	75	1.2	—	4096
0010	110	1.7598	-0.01	2793
0011	134.5	2.152	—	2284
0100	150	2.4	—	2048
0101	200	3.2	—	1536
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	—	256
1010	1800	28.7438	-0.19	171
1011	2000	31.9168	-0.26	154
1100	2400	38.4	—	128
1101	4800	76.8	—	64
1110	9600	153.6	—	32
1111	19200	307.2	—	16

Table 2b BAUD RATE GENERATOR CHARACTERISTICS  
2449-2 (BRCLK=4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	—	6144
0010	75	1.2	—	4096
0011	110	1.7598	-0.01	2793
0100	134.5	2.152	—	2284
0101	150	2.4	—	2048
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1200	19.2	—	256
1001	1800	28.7438	-0.19	171
1010	2000	31.9168	-0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

Table 2c BAUD RATE CHARACTERISTICS  
2449-3 (BRCLK=5.0688MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6336
0001	75	1.2	—	4224
0010	110	1.76	—	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	—	2112
0101	300	4.8	—	1056
0110	600	9.6	—	528
0111	1200	19.2	—	264
1000	1800	28.8	—	176
1001	2000	32.081	0.253	158
1010	2400	38.4	—	132
1011	3600	57.6	—	88
1100	4800	76.8	—	66
1101	7200	115.2	—	44
1110	9600	153.6	—	33
1111	19200	316.8	3.125	16

NOTE:  
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC.

## COM 2449 OPERATION

The functional operation of the COM 2449 is programmed by a set of control words supplied by the processor. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the COM 2449 Programming section of this data sheet.

After programming, the COM 2449 is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the processor to a serial bit stream. These actions are accomplished within the framework specified by the control words.

### Receiver

The COM 2449 is conditioned to receive data when the RR input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data is then transferred to the

# COM 2449 INITIALIZATION FLOW CHART

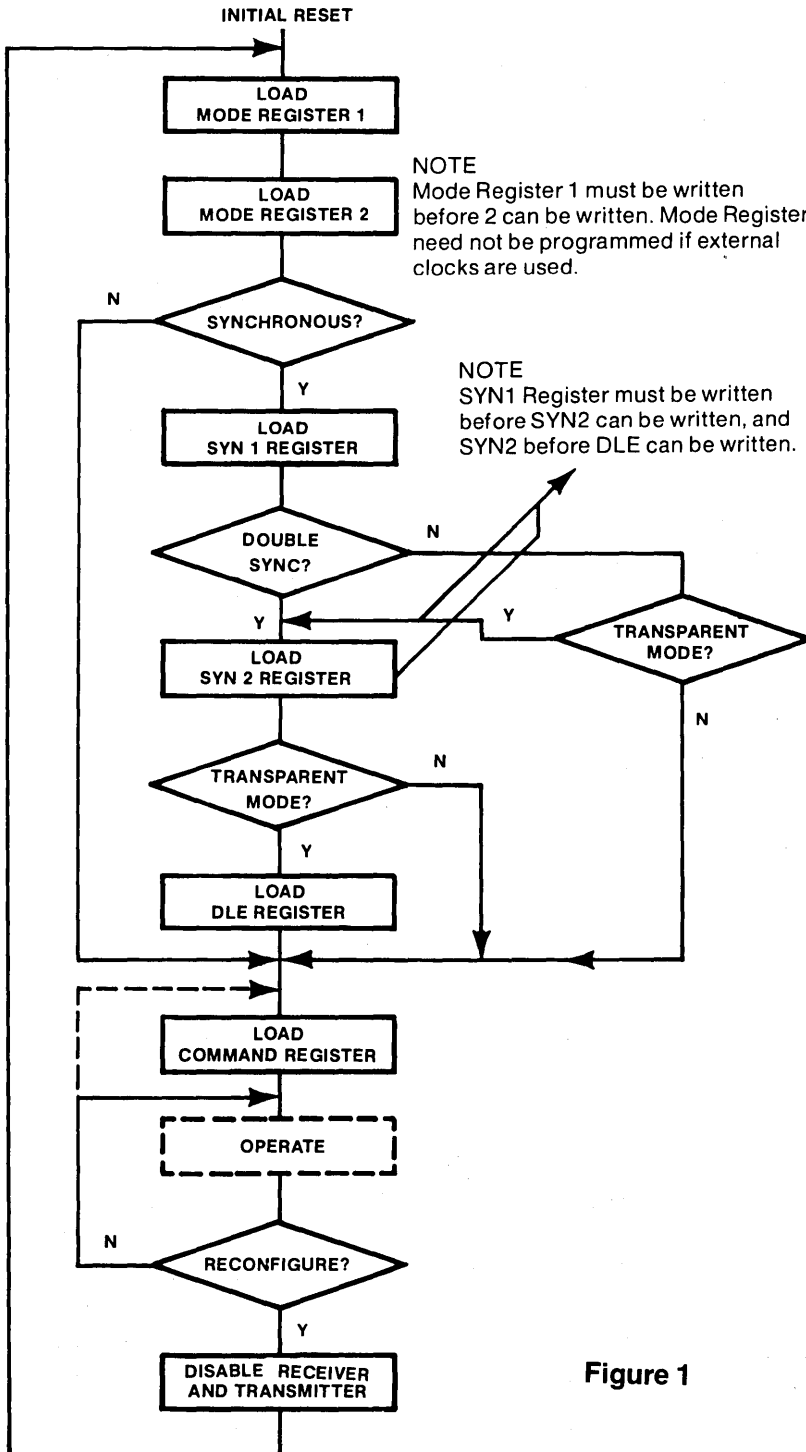


Figure 1

Receive Data Holding Register, the RxRDY bit in the status register is set, and the RxRDY output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of RxC corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the Framing error status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

When the COM 2449 is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2). In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly begins. If the single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the COM 2449 returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been achieved, the COM 2449 continues to assemble characters and transfers them to the Holding Register. The RxRDY status bit is set and the RxRDY output is asserted each time a character is assembled and transferred to the Holding Register. The Overrun error (OE) and Parity error (PE) status bits are set as appropriate. Further receipt of the proper SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled. Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

### Transmitter

The COM 2449 is conditioned to transmit data when the CS input is low and the TxEN command register bit is set. The COM 2449 indicates to the processor that it can accept a character for transmission by setting the TxRDY status bit and asserting the TxRDY output. When the processor writes a character into the Transmit Data Holding Register, the TxRDY status bit is reset and the TxRDY output is returned to a high (false) state. Data is transferred from the Holding Register to the Transmit

Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the TxEMT/DSCHG output and its corresponding status bit are asserted. Transmission resumes when the processor loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the COM 2449 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the processor. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the COM 2449 unless the processor fails to send a new character to the COM 2449 by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the COM 2449 asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the transmit holding register.

## COM 2449 PROGRAMMING

Prior to initiating data communications, the COM 2449 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The COM 2449 can be reconfigured at any time during program execution. A flow chart of the initialization process appears in Figure 1.

The internal registers of the COM 2449 are accessed by applying specific signals to the  $\overline{CE}$ ,  $\overline{R/W}$ , A2, A1 and A0 inputs. The conditions necessary to address each register are shown in Table 5.

TABLE 5—COM 2449 REGISTER ADDRESSING

CE	A2	A1	A0	$\overline{R/W}$	FUNCTION
1	X	X	X	X	Tri-state data bus
0	0	0	0	0	Read receive holding register
0	0	0	0	1	Write transmit holding register
0	0	0	1	0	Read status register 1
0	0	0	1	1	Write SYN1/SYN2/DLE registers
0	0	1	0	0	Read mode registers 1 and 2
0	0	1	0	1	Write mode registers 1 and 2
0	0	1	1	0	Read command register
0	0	1	1	1	Write command register
0	1	0	0	0	Read output register
0	1	0	0	1	Write output register
0	1	0	1	0	Read status register 2
0	1	0	1	0	Write status register 2

NOTE

See AC Characteristics section for timing requirements.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions A2=0, A1=0, A0=1, and R/W=1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 Register and

Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The COM 2449 register formats are summarized in Tables 6, 7, 8, 9, 10 and 11. Mode Registers 1 and 2 define the general operational characteristics of the COM 2449, while the Command Register controls the operation within this basic framework. The COM 2661 indicates its status in the two Status Registers. The status registers are cleared when a RESET input is applied.

## MODE REGISTER 1 (MR1)

Table 6 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and Baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character

framing of 1, 1.5, or 2 stop bits (if 1X baud rate is programmed, 1.5, stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17=1, and SYN1-SYN2 is used when MR17=0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN Detect, but the normal synchronization sequence is used. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also DLE stripping and DLE Detect (with MR14=0) are enabled.

TABLE 6—MODE REGISTER 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
<b>ASYNCH: STOP BIT LENGTH</b> 00=INVALID 01=1 STOP BIT 10=1½ STOP BITS 11=2 STOP BITS		0=ODD 1=EVEN	0=DISABLED 1=ENABLED	00=5 BITS 01=6 BITS 10=7 BITS 11=8 BITS		00=SYNCHRONOUS 1X RATE 01=ASYNCHRONOUS 1X RATE 10=ASYNCHRONOUS 16X RATE 11=ASYNCHRONOUS 64X RATE	
<b>SYNCH: NUMBER OF SYN CHAR</b> 0=DOUBLE SYN 1=SINGLE SYN	<b>SYNCH: TRANSPARENCY CONTROL</b> 0=NORMAL 1=TRANSPARENT						

NOTE Baud rate factor in asynchronous applies only if external clock is selected. Factor is 15X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

## MODE REGISTER 2 (MR2)

Table 7 illustrates mode register 2 (MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each COM 2449 version (-1, -2, -3). Version 1 and 2 specify a 4.9152 MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688 MHz input which is identical to the

COM 2651 and COM 2661-3. MR23-20 are don't cares if external clocks are selected (MR25-24=0). The individual rates are given in table 2a, b and c.

MR24-MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to table 7.

TABLE 7—MODE REGISTER 2 (MR2)

MR-27-MR24										MR23-MR20	
TxC	RxC	Pin 9	Pin 25	TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection		
0000	E	E	TxC	RxC	1000	E	E	XSYNC <sup>1</sup>	RxC/TxC	sync	See baud rates in table 2
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC <sup>1</sup>	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	
0100	E	E	TxC	RxC	1100	E	E	XSYNC <sup>1</sup>	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC <sup>1</sup>	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

### NOTES

1. When pin 9 is programmed as XSYNC input, SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled.

E=External clock  
 I=Internal clock (BRG)  
 1X and 16X are clock outputs



## COMMAND REGISTER (CR)

Table 8 illustrates the Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second RxC rising edge. Disabling the receiver causes RxRDY to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high while the TxRDY and TxEMT will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. Bits CR1 (TR) and CR5 (RS) control the TR and RS outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE—non-DLE character sequences.

Setting CR4 causes the error flags in the Status Register 1 (SR13, SR14, and SR15) to be cleared. This is a one time command. There is no internal latch for this bit. When CR5 (RS) is set, the RS pin is forced low and the transmit serial logic is enabled. A 1 to 0 transition of CR5 will cause RS to go high (inactive) one TxC time after the last serial bit has been transmitted (if the transmit shift register was not empty).

The COM 2449 can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6=00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6=01 places the COM 2449 in the Automatic Echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2=1), but the transmitter need not be enabled. Processor to receiver communications continue normally, but the processor to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1. Data assembled by the receiver are automatically

- placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. TxRDY output=1.
4. The TxEMT/DSCHG pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6=01 places the COM 2449 in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16=10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16=00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR.
3. In transparent mode (MR16=1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR13 and SR15).

Two diagnostic sub-modes can also be configured. In Local Loop Back mode (CR7-CR6=10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. TR is connected to RR and RS is connected to CS.
3. The receiver is clocked by the transmit clock.
4. The TR, RS and TxD outputs are held high.
5. The CS, RR, DM and RxD inputs are ignored.

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (TR), and CR5 (RS) must be set to 1. CR2 (RxEN) is ignored by the COM 2449.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6=11). In this mode:

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local processor, but the error status conditions (PE, OE, FE) are set.
4. The RxRDY, TxRDY, and TxEMT/DSCHG outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error	Sync/Async	Receive Control (RxEN)	Terminal Ready	Transmit Control (TxEN)
00=NORMAL OPERATION 01=ASYNCH: AUTOMATIC ECHO MODE SYNCH: SYN AND/OR DLE STRIPPING MODE  10=LOCAL LOOP BACK REMOTE LOOP BACK		0=FORCE RS OUTPUT HIGH ONE CLOCK TIME AFTER TXSR SERIAL- IZATION 1=FORCE RS OUTPUT LOW	0=NORMAL 1=RESET ERROR FLAG IN STATUS (FE, OE,  PE/DLE DETECT)	<b>ASYNCH:</b> <b>FORCE BREAK</b> 0=NORMAL 1=FORCE BREAK  <b>SYNCH:</b> <b>SEND DLE</b> 0=NORMAL 1=SEND DLE	0=DISABLE 1=ENABLE	0=FORCE TR OUTPUT HIGH 1=FORCE TR OUTPUT LOW	0=DISABLE 1=ENABLE

TABLE 8—COMMAND REGISTER (CR)

## STATUS REGISTER 1 (SR1)

The data contained in the Status Register 1 (as shown in Table 9) indicate receiver and transmitter conditions and modem/data set status.

SR10 is the Transmitter Ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the processor and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the processor. This bit is initially set when the Transmitter is enabled by CR0, unless a character has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the TxRDY output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR11, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set, it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the processor. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the processor reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the RxRDY output is low.

The TxEMT/DSCHG bit, SR12, when set, indicates a change of state of the  $\overline{DM}$  or  $\overline{RR}$  inputs (when CR2 or CR0=1), the  $\overline{SI}$ ,  $\overline{SB}$ ,  $\overline{SQ}$ ,  $\overline{TM}$  or  $\overline{TC}$  inputs (when SR25, SR26, or SR27=1) or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the Transmit Data Holding Register. The DSCHG condition is enabled when TxEN=1 or RxEN=1.

It is cleared when status register 1 is read by the processor. If status register 1 is read twice and SR12=1 while SR16 and SR17 remain unchanged, then a TxEMT condition exists. When SR12 is set, the TxEMT/DSCHG output is low.

SR13, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16=1), with parity disabled, it indicates that a character matching the DLE Register has been received, and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into the Receive Data Holding Register, when the receiver is disabled, or by a reset error command, CR4.

The Overrun Error status bit, SR14, indicates that the previous character loaded into the Receive Holding Register was not read by the processor at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

In asynchronous mode, bit SR15 signifies that the received character was not framed by a stop bit, i.e., only the first stop bit is checked. If the RHR contains all 0's when SR15=1, a break condition is present. In synchronous non-transparent mode (MR16=0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16=1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, or when Status Register 1 is read by the processor in the synchronous mode.

SR16 and SR17 reflect the conditions of the  $\overline{RR}$  and  $\overline{DM}$  inputs respectively. A low input sets the corresponding status bit and a high input clears it.

SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10
Data Mode	Receiver Ready	FE/SYN Detect	Overrun	PE/DLE Detect	TxEMT/DSCHG	RxRDY	TxRDY
0= $\overline{DM}$ INPUT IS HIGH 1= $\overline{DM}$ INPUT IS LOW	0= $\overline{RR}$ INPUT IS HIGH 1= $\overline{RR}$ INPUT IS LOW	<b>ASYNCH:</b> 0=NORMAL 1=FRAMING ERROR  <b>SYNCH:</b> 0=NORMAL 1=SYN CHAR DETECTED	0=NORMAL 1=OVERRUN ERROR	<b>ASYNCH:</b> 0=NORMAL 1=PARITY ERROR  <b>SYNCH:</b> 0=NORMAL 1=PARITY ERROR OR DLE CHAR RECEIVED	0=NORMAL 1=CHANGE IN DSR OR DCD, OR TRANSMIT SHIFT REGISTER IS EMPTY	0=RECEIVE HOLDING REG EMPTY 1=RECEIVE HOLDING REG HAS DATA	0=TRANSMIT HOLDING REG BUSY 1=TRANSMIT HOLDING REG EMPTY

TABLE 9—STATUS REGISTER 1 (SR1)

## STATUS REGISTER 2 (SR2)

The Data contained in the 5 least significant bits (SR20 to SR24) reflect the conditions of the  $\overline{IC}$ ,  $\overline{TM}$ ,  $\overline{SQ}$ ,  $\overline{SB}$  and  $\overline{SI}$  inputs respectively. A low input sets the corresponding status bit high and a high input clears the corresponding status bit low. These 5 bits are read only.

The three most significant bits (SR25 to SR27) allow interrupts to be enabled on the 5 inputs reflected in SR20 to SR24.

Setting SR25 enables an interrupt to occur when the  $\overline{IC}$

input signal experiences a change of state. Setting SR26 enables an interrupt to occur when the  $\overline{TM}$  input signal experiences a change of state. Setting SR27 enables an interrupt to occur when the  $\overline{SQ}$ ,  $\overline{SI}$ , or  $\overline{SB}$  input signals experience a change of state. All interrupts enabled in these 3 bits will be reflected in the D $\overline{SCHG}$ /TxEMT output signal and its corresponding status bit (SR12). These 3 bits can be read as well as written according to Table 5. Table 10 illustrates bit assignments of Status Register 2.

SR27 Interrupt Enable 1	SR26 Interrupt Enable 2	SR25 Interrupt Enable 3	SR24 Signal Rate Indication	SR23 Standby Indicator	SR22 Signal Quality	SR21 Test Mode	SR20 Incoming Call
1=INTERRUPT ON SQ, SI, SB STATE CHANGE	1=INTERRUPT ON TM STATE CHANGE	1=INTERRUPT ON IC STATE CHANGE	0= $\overline{SI}$ INPUT IS HIGH 1= $\overline{SI}$ INPUT IS LOW	0= $\overline{SB}$ INPUT IS HIGH 1= $\overline{SB}$ INPUT IS LOW	0= $\overline{SQ}$ INPUT IS HIGH 1= $\overline{SQ}$ INPUT IS LOW	0= $\overline{TM}$ INPUT IS HIGH 1= $\overline{TM}$ INPUT IS LOW	0= $\overline{IC}$ INPUT IS HIGH 1= $\overline{IC}$ INPUT IS LOW

TABLE 10—STATUS REGISTER 2 (SR2)

## OUTPUT REGISTER (OR)

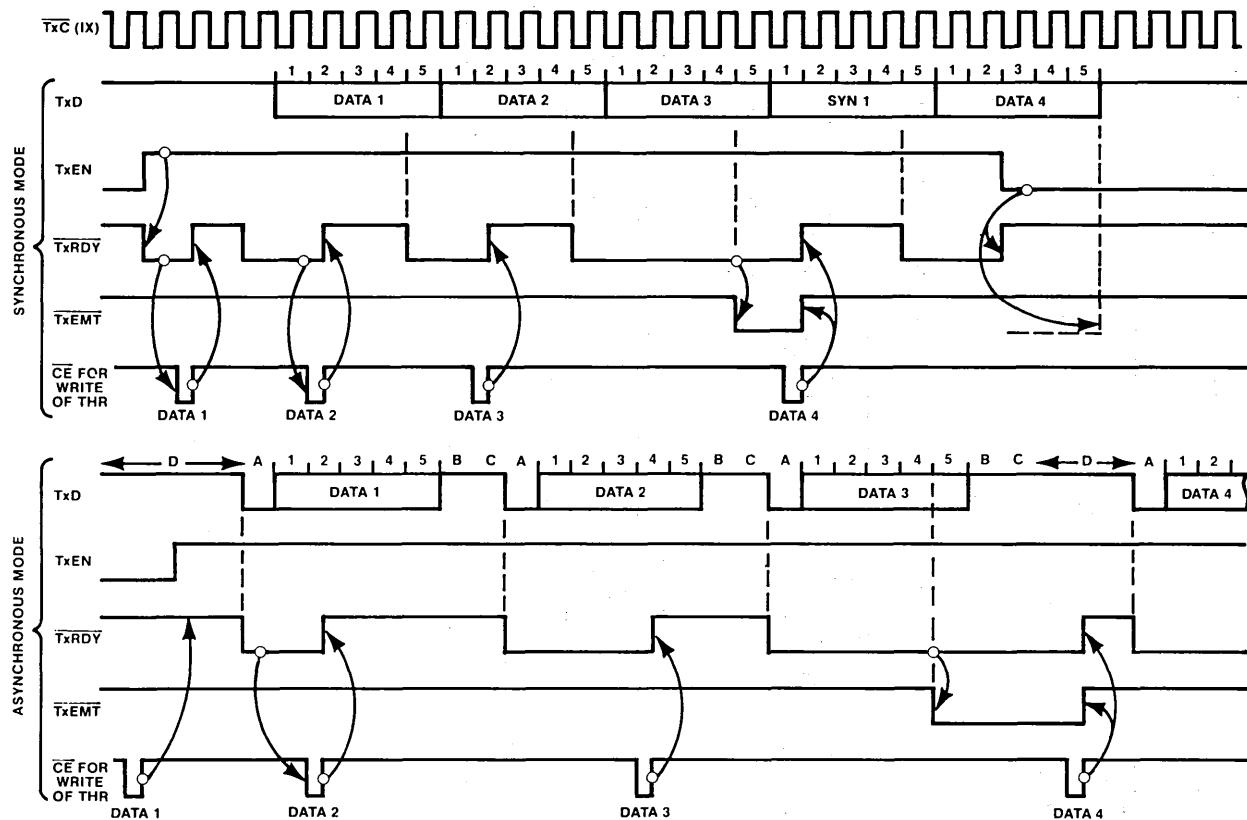
This 6 bit read write register (OR5-OR0) controls the 6 new output signals added to the COM2449. OR5-1 directly control the state of the  $\overline{IS}$ ,  $\overline{SF/SR}$ ,  $\overline{SS}$ ,  $\overline{RL}$ , and  $\overline{LL}$  respectively.

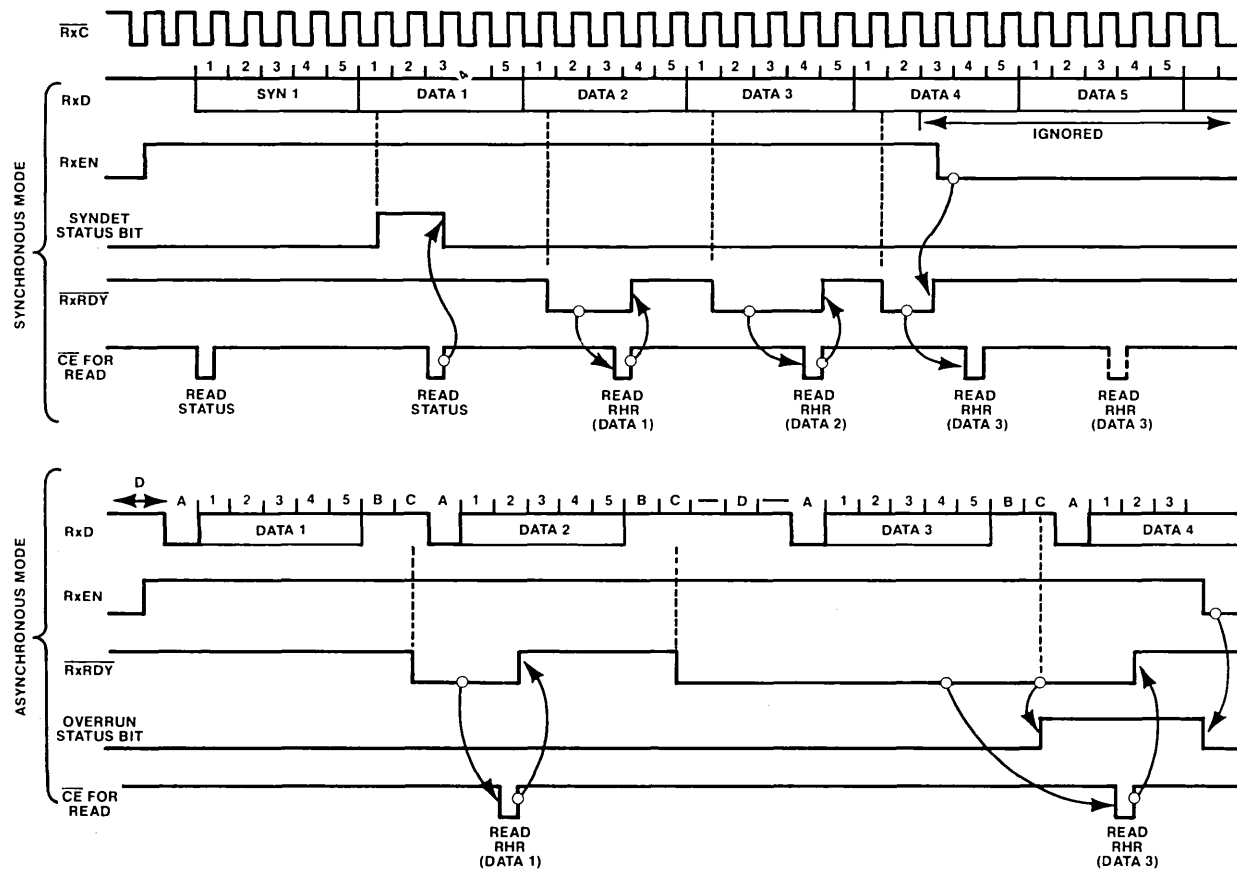
OR0 when set to a logic 1 will cause the  $\overline{NS}$  output to become low. When OR0 is set to a logic 0 the  $\overline{NS}$  output will not change until the  $\overline{RR}$  input goes high.

Table 11 illustrates bit positions of the Output Register.

OR7	OR6	OR5	OR4	OR3	OR2	OR1	OR0
		Terminal In service	Select Frequency/ Signal rate select	Select Standby	Remote Loopback	Local Loopback	New Signal
DON'T CARE	DON'T CARE	0= $\overline{IS}$ OUTPUT GOES HIGH 1= $\overline{IS}$ OUTPUT GOES LOW	0= $\overline{SF/SR}$ OUTPUT HIGH 1= $\overline{SF/SR}$ OUTPUT LOW	0= $\overline{SS}$ OUTPUT HIGH 1= $\overline{SS}$ OUTPUT LOW	0= $\overline{RL}$ OUTPUT GOES HIGH 1= $\overline{RL}$ OUTPUT GOES LOW	0= $\overline{LL}$ OUTPUT GOES HIGH 1= $\overline{LL}$ OUTPUT GOES LOW	0= $\overline{NS}$ OUTPUT GOES HIGH ONLY WHEN $\overline{RR}$ INPUT GOES HIGH 1= $\overline{NS}$ OUTPUT GOES LOW

TABLE 11—OUTPUT REGISTER (OR)





## NOTES

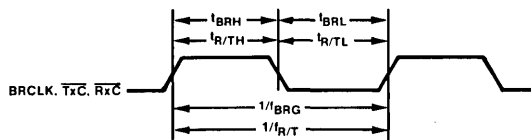
- A Start bit
- B Stop bit 1
- C Stop bit 2
- D TxD marking condition

## TIMING DIAGRAMS (Cont'd)

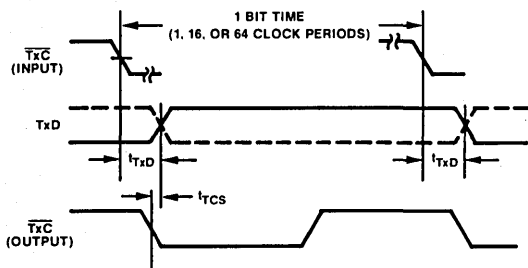
**RESET**



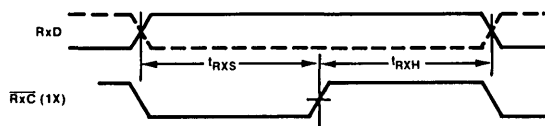
**CLOCK**



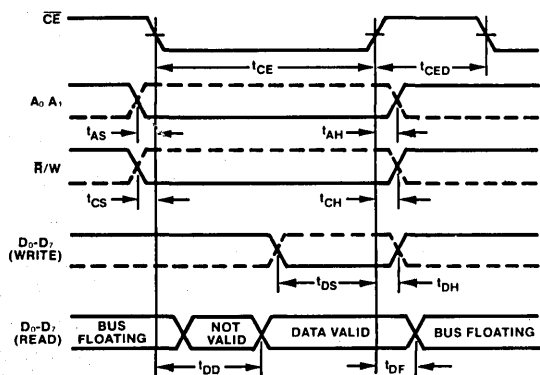
## TRANSMIT



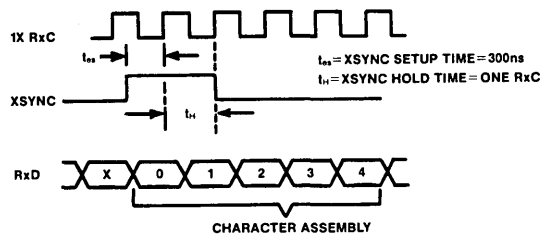
## RECEIVE



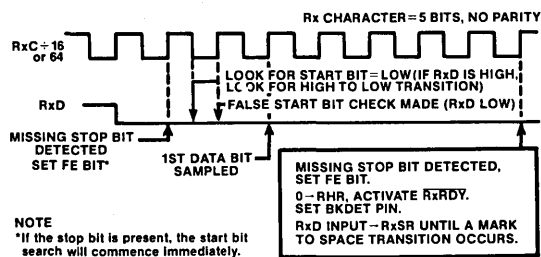
## READ AND WRITE



## EXTERNAL SYNCHRONIZATION WITH XSYNC



## BREAK DETECTION TIMING



**MAXIMUM GUARANTEED RATINGS\***

Operating Temperature Range .....	0°C to +70°C
Storage Temperature Range .....	-55°C to +150°C
Lead Temperature (soldering, 10 sec.) .....	+325°C
Positive Voltage on any Pin, with respect to ground .....	+18.0V
Negative Voltage on any Pin, with respect to ground .....	-0.3V

\*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

**DC ELECTRICAL CHARACTERISTICS**  $T_A=0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 5\%$ 

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$V_{IL}$ Input voltage Low			0.8	V	
$V_{IH}$ Input voltage High	2.0				
$V_{OL}$ Output voltage Low			0.4	V	$I_{OL}=2.2\text{mA}$
$V_{OH}$ Output voltage High	2.4				$I_{OH}=-400\mu\text{A}$
$I_{IL}$ Input leakage current			10	$\mu\text{A}$	$V_{IN}=0$ to 5.5V
$I_{LH}$ Output leakage current Data bus high			10	$\mu\text{A}$	$V_O=4.0\text{V}$
$I_{LL}$ Output leakage current Data bus low			10	$\mu\text{A}$	$V_O=0.45\text{V}$
$I_{CC}$ Power supply current			150	mA	
$C_{IN}$ Capacitance Input			20	pF	$f_c=1\text{MHz}$
$C_{OUT}$ Capacitance Output			20	pF	Unmeasured pins tied to ground
$C_{I/O}$ Capacitance Input/Output			20	pF	

**AC ELECTRICAL CHARACTERISTICS**  $T_A=0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC}=5.0\text{V}\pm 5\%$ 

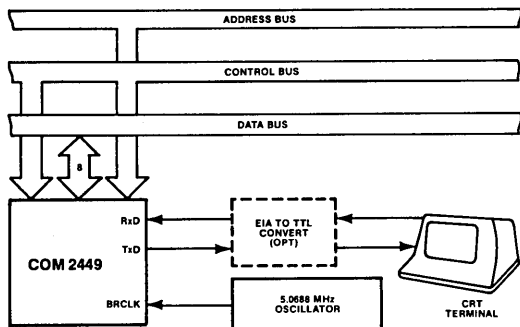
PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$t_{RES}$ Pulse width Reset	1000			ns	
$t_{CE}$ Chip enable	250			ns	
$t_{AS}$ Setup and hold time Address setup	10			ns	
$t_{AH}$ Address hold	10			ns	
$t_{CS}$ R/W control setup	10			ns	
$t_{CH}$ R/W control hold	10			ns	
$t_{DS}$ Data setup for write	150			ns	
$t_{DH}$ Data hold for write	0			ns	
$t_{RXS}$ Rx data setup	300			ns	
$t_{RXH}$ Rx data hold	350			ns	
$t_{DD}$ Data delay time for read			200	ns	$C_L=150\text{pF}$
$t_{DF}$ Data bus floating time for read			100	ns	$C_L=150\text{pF}$
$t_{CED}$ CE to CE delay	600			ns	
$f_{BRG}$ Input clock frequency Baud rate generator (2449-1, -2)	1.0	4.9152	4.9202	MHz	
$f_{BRG}$ Baud rate generator (2449-3)	1.0	5.0688	5.0738	MHz	
$f_{RT}^1$ TxC or RxC	dc		1.0	MHz	
$t_{BRH}$ Clock width Baud rate high (2449-1, -2)	75				$f_{BRG}=4.915\text{MHz}$ ; measured at $V_{IH}$
$t_{BRH}$ Baud rate high (2449-3)	70				$f_{BRG}=5.0688\text{MHz}$ ; measured at $V_{IH}$
$t_{BRL}$ Baud rate low (2449-1, -2)	75				$f_{BRG}=4.915\text{MHz}$ ; measured at $V_{IL}$
$t_{BRL}$ Baud rate low (2449-3)	70				$f_{BRG}=5.0688\text{MHz}$ ; measured at $V_{IL}$
$t_{RTH1}$ TxC or RxC high	480			ns	
$t_{RTL}$ TxC or RxC low	480			ns	
$t_{TXD}$ TxD delay from falling edge of TxC			650	ns	$C_L=150\text{pF}$
$t_{TCS}$ Skew between TxD changing and falling edge of TxC output		0		ns	$C_L=150\text{pF}$

NOTE:

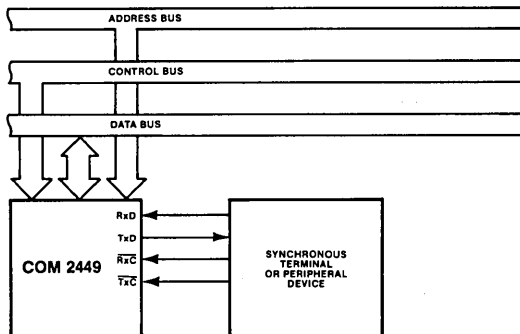
1.  $f_{RT}$  and  $t_{RTL}$  shown all modes except Local Loopback. For Local Loopback mode  $f_{RT}=0.7\text{MHz}$  and  $t_{RTL}=700\text{ns min.}$

## TYPICAL APPLICATIONS

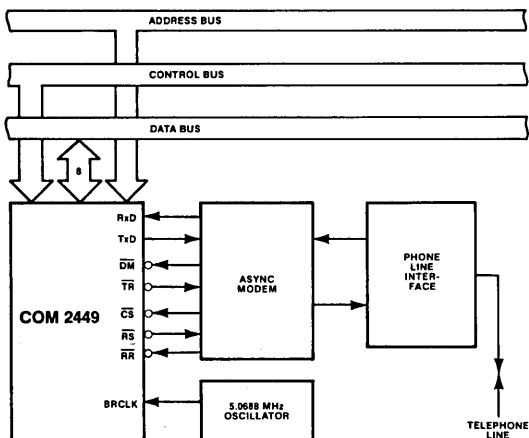
### ASYNCHRONOUS INTERFACE TO CRT TERMINAL



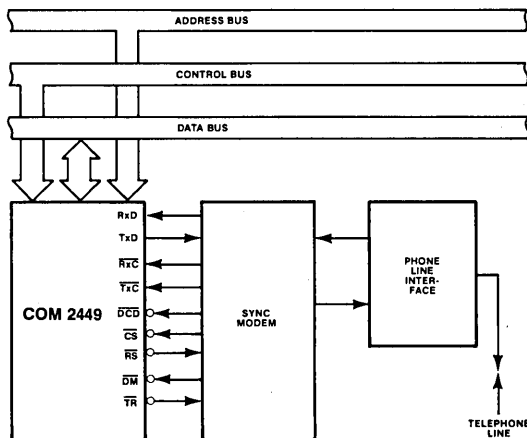
### SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



### ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



### SYNCHRONOUS INTERFACE TO TELEPHONE LINES



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