CMX7341
Marine Common Platform Processor

7341FI-6.x: MoB Marine DSC and AIS Modem with Rx I/Q Support

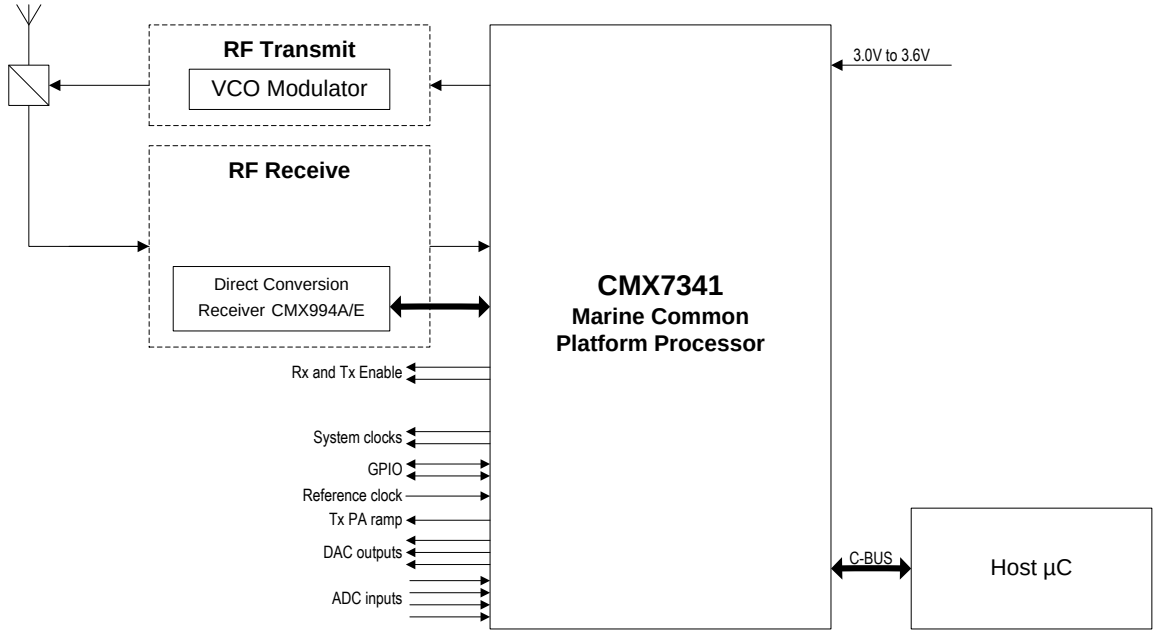
D/7341_FI6.x/4 May 2022 **DATASHEET** Advance Information

Features

- DSC Transmit modem
- DSC Receive modem
- AIS Transmit modem
- Tx Sequencer
- Direct control of CMX994A
- IEC 62369 Ed 1 compliant
- 2 Auxiliary ADCs (4 Multiplexed Inputs)
- 4 Auxiliary DACs
- 2 Auxiliary System Clock Outputs
- Tx Outputs for Two-point modulation
- Rx Inputs for CMX994 Direct Conversion (I/Q) Receiver
- C-BUS serial interface to CMX994
- C-BUS serial Interface to host micro
- Flexible powersave modes
- Low-power (3.3V) operation
- Dedicated hardware reset pin
- Differential inputs
- Available in VQFN Packages

Applications

- Man-Over-Board devices
- Personal Locator Beacon devices



1 Brief Description

The 7341FI-6.x Function Image™ (FI) implements the digital data modem functionality to support Man-Over-Board and Personal Locator Beacon devices that require both DSC and AIS signalling.

The device is optimised to use an I/Q-based direct conversion architecture utilising the built-in support for the CMX994A Direct Conversion Receiver. The CMX994A internal PLL and VCO support is used to generate both the Rx and TX Local Oscillators, so reducing device count, minimising PCB area and cost.

The device utilises CML's proprietary *FirmASIC®* component technology. On-chip sub-systems are configured by a Function Image™: This is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external serial memory or host microcontroller over the built-in C-BUS serial interface. The device's functions and features may be enhanced by future Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 7341FI-6.1.x.x

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in a VQFN package.

Note that text shown in pale grey indicates features that will be supported in future versions of the Function Image™.

This datasheet is the first part of a two-part document comprising datasheet and user manual: the datasheet/user manual combination can be obtained by registering your interest in this product with your local CML representative.

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History

Version	Changes	Date
4	References to CMX7241 removed	May 2022
3	Update to FI release 6.1.x.x: details of powersave and updated configuration / defaults	July 2021
2	Full public release	January 2021
1	First release, Advance Information	December 2020

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.

2 Block Diagram

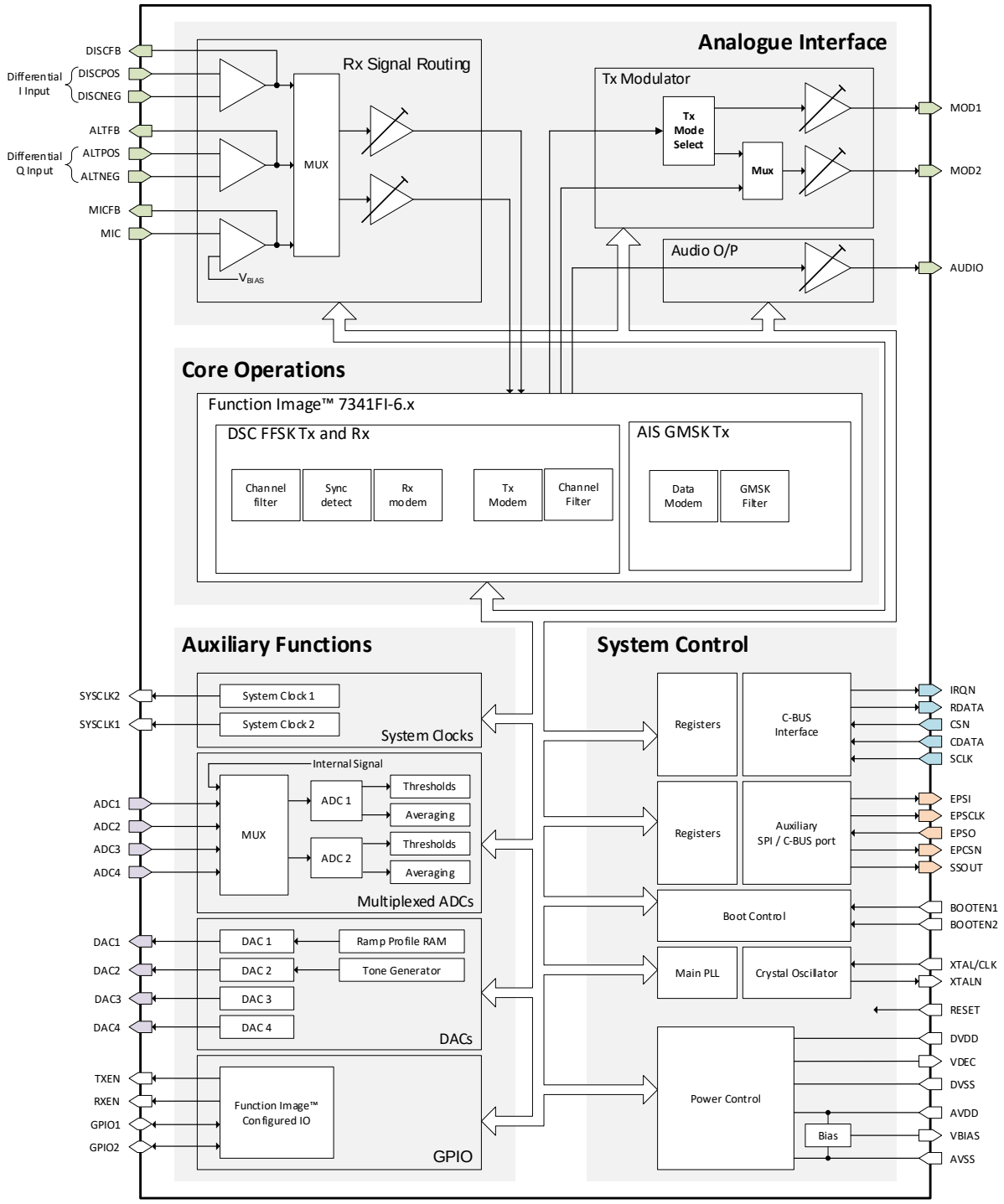


Figure 1 CMX7341 Block Diagram

3 Signal List

CMX7341 48-lead Q3	Pin Name	Type	Description	
1	EPSI	OP	Serial Data Output	Auxiliary SPI/C-BUS
2	EPSCLK	OP	Serial Clock Output	
3	EPSO	IP+PD	Serial Data Input	
4	EPCSN	OP	Serial Chip Select for CMX994A	
5	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program	
6	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program	
7	RESET	PWR	Dedicated reset function – active high. When asserted has the same effect as a power on reset. If unused, tie to DVSS	
8	IRQN	OP	A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.	Host C-BUS
9	VDEC	PWR	Internally-generated 1.8V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed. If the device is to be run from a 1.8V external supply then the VDEC pin must be connected directly to the external 1.8V regulated supply.	
10	RXENA	OP	Rx Enable – active when in Rx mode ($C1:b0 = 1)	
11	GPIOA	BI	General Purpose I/O pin	
12	GPIOB	BI	General Purpose I/O pin	
13	SYSCLK1	OP	Synthesised Digital System Clock Output 1	
14	DVSS	PWR	Digital ground	
15	TXENA	OP	Tx Enable – active when in Tx mode ($C1:b1 = 1)	
16	DISCPOS	IP	Differential input1, positive and negative. I input from CMX994	
17	DISCNEG	IP		
18	DISCFB	OP	Input1 amplifier feedback	
19	ALTPOS	IP	Differential input2, positive and negative. Q input from CMX994	
20	ALTNEG	IP		
21	ALTFB	OP	Input2 amplifier feedback	
22	MICFB	OP	Microphone input amplifier feedback	
23	MIC	IP	Microphone inverting input	
n/c	AVSS	PWR	Analogue ground	
24	MOD1	OP	Modulator 1 output	

CMX7341 48-lead Q3	Pin Name	Type	Description	
25	MOD2	OP	Modulator 2 output	
26	VBIAS	OP	Internally generated bias voltage of approx. $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed unless buffered.	
27	AUDIO	OP	Audio Output	
28	ADC1	IP	Auxiliary ADC input 1	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 6.8 for details.
29	ADC2	IP	Auxiliary ADC input 2	
30	ADC3	IP	Auxiliary ADC input 3	
31	ADC4	IP	Auxiliary ADC input 4	
32	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
33	DAC1	OP	Auxiliary DAC output 1 / RAMDAC	
34	DAC2	OP	Auxiliary DAC output 2 / Tone Generator output	
n/c	AVSS	PWR	Analogue ground	
35	DAC3	OP	Auxiliary DAC output 3. See Note 2	
36	DAC4	OP	Auxiliary DAC output 4	
37	DVSS	PWR	Digital Ground	
38	VDEC	PWR	Internally generated 1.8V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed. If the device is to be run from a 1.8V external supply, then VDEC pin must be connected directly to the 1.8V external regulated supply.	
39	XTAL/CLK	IP	Input from the external clock source or Xtal	
40	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external clock used.	
41	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.	
42	CDATA	IP	Command Data input from the µC	Host C-BUS
43	RDATA	TS OP	Reply Data tri-state output to the µC (high impedance when not sending data to the µC).	
44	SSOUT	OP	Serial Chip Select	Auxiliary SPI/C-BUS
45	DVSS	PWR	Digital ground	
46	SCLK	IP	Serial clock input from the µC	Host C-BUS
47	SYSCLK2	OP	Synthesised Digital System Clock 2	

CMX7341 48-lead Q3	Pin Name	Type	Description	
48	CSN	IP	Chip Select input from the µC (no internal pullup on this input)	Host C-BUS
Exposed Metal Pad	SUBSTRATE	~	The central metal pad (which is exposed on Q3 package only) must be connected to analogue ground (AV_{SS}). **No other electrical connection is permitted.**	

Note 1: IP = Input (+ PU/PD = internal pullup / pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

Colour Definitions:

= Aux SPI/C-BUS
= Host C-BUS
= Analogue Inputs/Outputs
= ADCs/DACs

Note 2: This is a dual-purpose pin which, for some FIs, may have an alternative configuration. However for FI-6, this pin ONLY functions as DAC3.

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DVDD by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AVDD
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

4 Component and PCB Recommendations

4.1 Recommended External Components

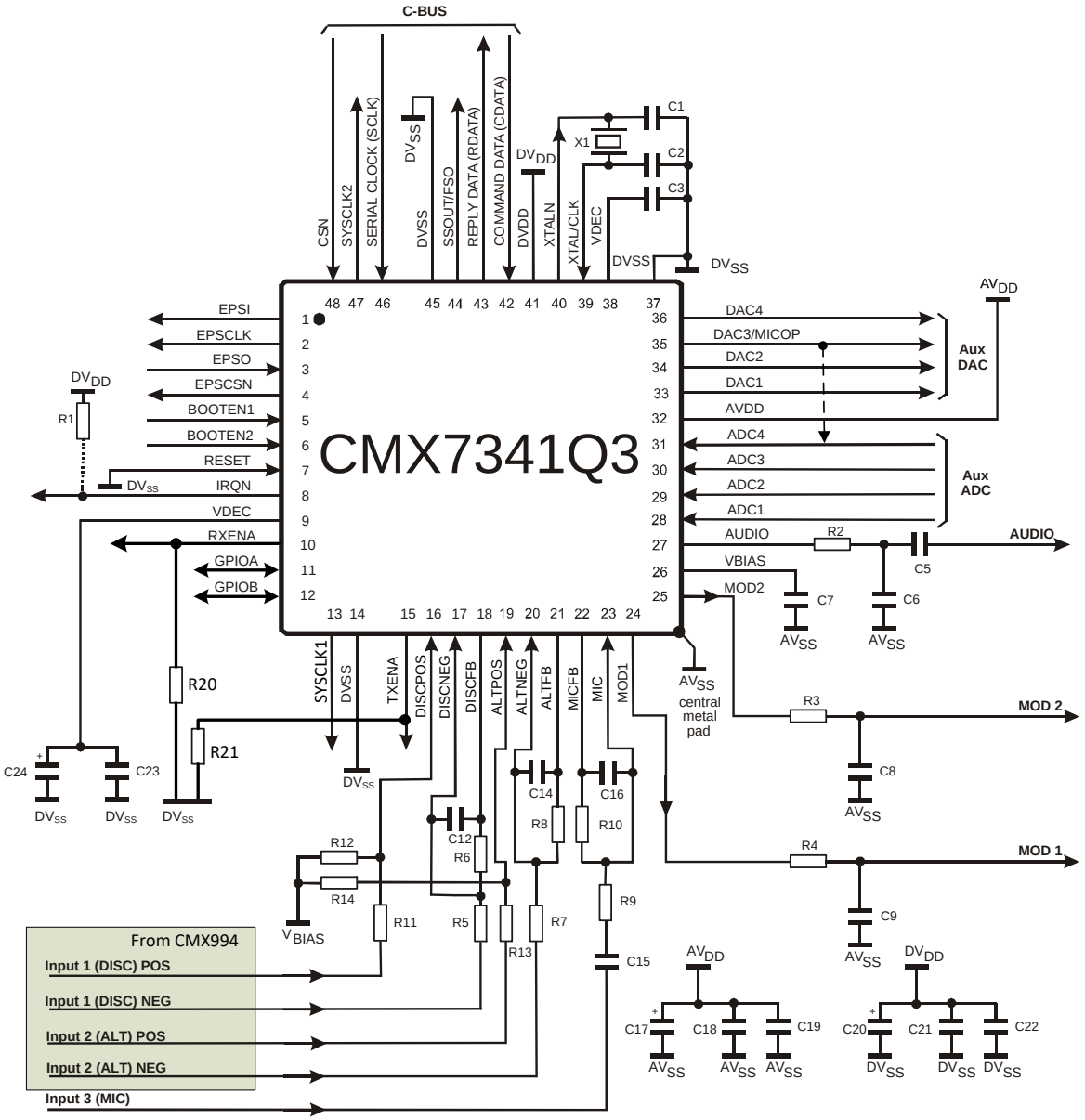


Figure 2 CMX7341 (Q3) Recommended External Components

Table 2 Recommended External Components

R1	100kΩ	C1	18pF	C11	not used	C21	10nF
R2	20kΩ	C2	18pF	C12	100pF	C22	10nF
R3	20kΩ	C3	10nF	C13	not used	C23	10nF
R4	20kΩ	C4	not used	C14	100pF	C24	10µF
R5	100kΩ	C5	1nF	C15	Not used		
R6	100kΩ (note 3)	C6	100pF	C16	Not used		
R7	100kΩ	C7	1µF	C17	10µF		

R8	Not usedSee note 4	C8	100pF	C18	10nF	X1	19.2MHz
R9	Not used100kΩ	C9	100pF	C19	10nF		See note 1
R10	100kΩ	C10	not used	C20	10µF		
R11	100kΩ						
R12	100kΩ	R20	47kΩ				
R13	100kΩ	R21	47kΩ				
R14							

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 19.2MHz oscillator is assumed (in which case C1 and C2 are not required), other values could be used if the various internal clock dividers are set to appropriate values.
2. AUDIO output is not used.
3. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the PCB with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.
4. TXENA and RXENA should be pulled down by an external resistor (R20, R21) to be directly compatible with the CMX994A (active high signals). For compatibility with earlier 7141-based FI operation, they should be pulled high (active low signals).

4.2 PCB Layout Guidelines and Power Supply Decoupling

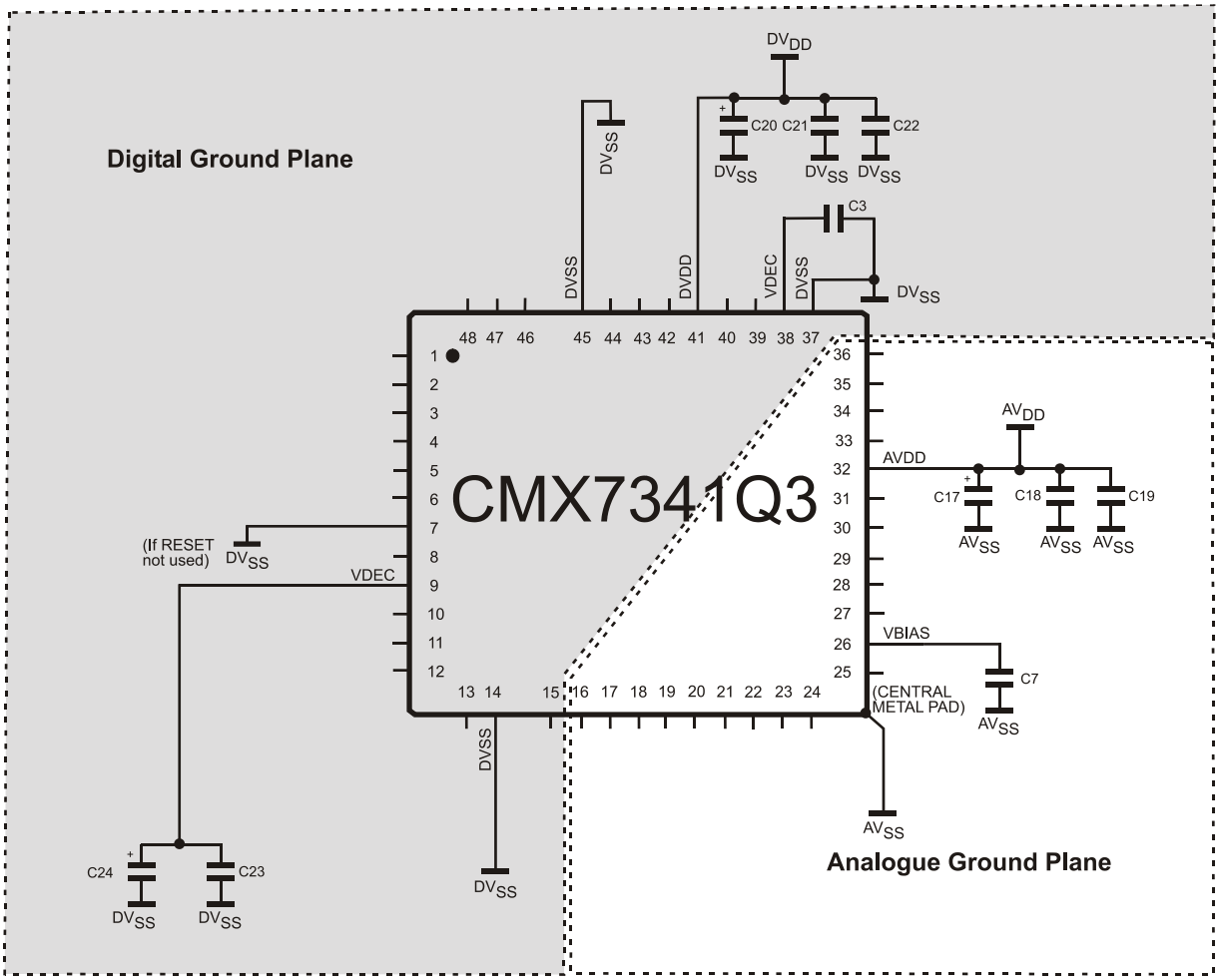


Figure 3 CMX7341 (Q3) Power Supply and De-coupling

Component Values as per Figure 2

Notes:

It is important to protect the analogue pins from extraneous in-band noise and to minimise the impedance between the CMX7341 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the CMX7341. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AVSS and DVSS supplies in the area of the device, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

VBIAS is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If VBIAS needs to be used elsewhere in the design, it should be buffered with a high input impedance buffer.

The single ended microphone input and audio output are not used.

The crystal, X1, may be replaced with an external clock source.

The device executes an internal scheduler running at 4 or 8 kHz, which may result in current “spikes” on the DVDD line, which must be taken into account when designing the power supply circuitry.

4.3 CMX994/CMX994A/CMX994E Interface

When operating the CMX7341 in I/Q mode, the interface to the CMX994A shown in Figure 4 should be used. Component values are shown in Table 3. Where values are not shown refer to the CMX994/A/E Datasheet. The CMX7341 allows for a differential interface directly to the CMX994. Resistors R20 and R21 are required to ensure that the TXENA and RXENA signals are kept in an inactive state during FI loading, and to inform the FI that these signals should be implemented active high.

The CMX994A and the CMX7341 may share the same 19.2MHz reference (however note that the CMX7341 requires a CMOS logic compatible signal).

AuxADC1 is configured to sense the Adjacent / Alternate channel power levels and so improve the performance of the CMX994A AGC system in situations where high levels of interference may be encountered.

The CMX994A should be connected to the Auxiliary SPI/C-BUS using EPCSN as the chip select.

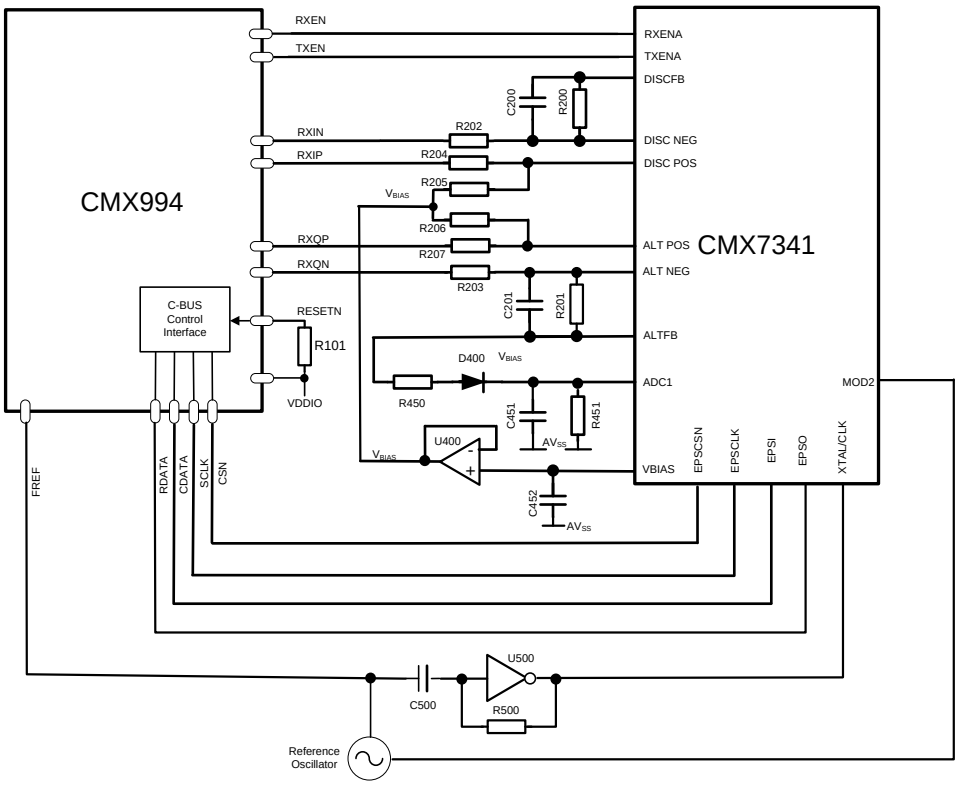


Figure 4 CMX7341/CMX994A Interface

Table 3 Recommended External Components when using CMX994

R101	100kΩ	C200	100pF	D400	MMBD1503A
R200 to R207	100kΩ	C201	100pF	U400	e.g. LMV931MG
R450	22kΩ	C400	100nF	U500	e.g. SN74AHC1G04DRL
R451	1MΩ	C451	1nF		
R500	100kΩ	C452	100nF		
		C500	1nF		

4.4 Serial Port Interfaces

A serial port is available on the device to interface to a CMX994A.

Table 4 shows the options available for the whole of the CMX7241/CMX7341 family with the only option available for FI-6 shown in **green.**

Table 4 Serial Port Assignments

configuration	pin name	7141		7241FI-1 7341FI-1		7241FI-2 Limiter/discriminator	7341FI-2 & FI-6 I/Q demod	
default	EPCSN EPSCLK EPSI EPSO SSOUT GPIOA GPIOB	CMX994	SPI-Codec or CMX 618/7262	CMX994	SPI-Codec or CMX 618/7262	SPI-Codec	CMX994	SPI-Codec
alternate	EPCSN EPSCLK EPSI EPSO SSOUT GPIOA GPIOB			CMX994	SPI-Codec or CMX 618/7262	SPI-Codec		

4.5 RESET Pin

This pin (pin 7) provides a dedicated reset function when connected to a suitable host microprocessor. To use reset the pin must be held high for a minimum of 100ns and then released. When the state of reset changes from 1 to 0, the same effect as a power-on reset is achieved.

5 General Description

5.1 7341FI-6 Features

The 7341FI-6.x Function Image™ is intended for use in Man-Over-Board or Personal Locator Beacon applications using DSC and AIS signalling in 25 kHz VHF marine band channels stated in the current version of the ITU Radio Regulations. When combined with a suitable host microcontroller and interface components, it meets or exceeds the requirements of IEC 63269 Ed 1.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with buffered output, to provide a common system clock if required. Block diagrams of the devices are shown in Figure 1. The signal processing blocks can be routed from any of the three DISC/ALT/MIC input pins.

5.2 Digital Features

A DSC raw modem (Tx and Rx) and an AIS raw transmit capability is provided:

Air Interface Physical Layer

- VHF DSC Tx and Rx 1200 bps FFSK modulation and demodulation
- AIS Tx 9600 bps GMSK modulation only
- Bit and symbol definition
- Frequency and symbol synchronisation
- Automatic control of the CMX994A

5.3 Analogue Features

- Tone generator

5.4 Auxiliary Functions

- Automatic Tx sequencer simplifies host control
- RAMDAC operation for RF PA power control
- TXENA and RXENA hardware signals
- Two-point modulation outputs
- Two programmable system clock outputs
- Two auxiliary ADCs with four selectable external input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC

5.5 Interface

- Optimised C-BUS (4-wire, high-speed synchronous serial command/data bus) interface to host for control and data transfer
- Open drain IRQ to host
- Auxiliary SPI/C-BUS interface to CMX994A with pass-through mode from host
- Two GPIO pins
- C-BUS (host) boot mode.

5.6 System Design

5.6.1 General

The system architecture has been optimised to suit the specific application:

RF receiver:

- I/Q using the CMX994A Direct Conversion Receiver

RF Transmitter:

- Two-point or single point direct VCO / reference modulation.

Local Oscillator generation:

- Uses CMX994A built-in PLL with external tank, loop filter and varactor circuit.

Host Interface:

- Raw data interface to host. All coding / decoding must be performed within the host processor.

5.6.2 Data Transfer

When transmitting, an initial block of payload data will need to be loaded from the host into the C-BUS Tx FIFO registers. The device will then transmit that data when commanded. The device will end transmission when the programmed number of bits have been sent.

When receiving, the host needs to consider that when a signal is received over the air there will be a processing delay while the device filters, demodulates the data before presenting it to the host in the C-BUS Rx FIFO registers. Reception will continue until commanded to stop by the host controller, or the FIFO becomes full. The host is responsible for terminating and possibly restarting the receiver upon detection of a message end in the decoded data.

5.6.3 CMX994A Connection (I/Q Mode)

The CMX994A can be connected via the C-BUS connection in place of the serial memory (Table 5).

Table 5 CMX994A Connections

CMX7341 Pin	CMX994A Pin
EPCSN	CSN
EPSI	CDATA
EPSCLK	SCLK
No connection	RDATA

The operation of the CMX994A is generally automatic, however specific data may be written to CMX994A registers using the pass-through mode available using register $C8. As the CMX994A PLL and VCO are used in the radio design then it is necessary to programme the appropriate frequency data to the CMX994A PLL-M Divider, PLL N-Divider and VCO Control registers using the pass-through mode before attempting reception or transmission.

The CMX994A/CMX994E devices are pin compatible with CMX994 and may be used instead. In order to make use of the advanced features Program Block P6 should be set appropriately.

The CMX994A is designed to work with the LO input operating in the divide by 2 mode. The internal PLL and VCO components are used to generate the LO at the correct frequency for the data mode in use:

- DSC: 156.525 MHz x 2 = 313.050 MHz
- AIS1: 161.975 MHz x 2 = 323.950 MHz
- AIS2: 162.025 MHz x 2 = 324.050 MHz

The CMX994A PLL settings for each frequency are:

CMX994A C-BUS register	DSC Tx and Rx	AIS1 Tx	AIS2 Tx
$20	$D4	$3C	$44
$21	$61	$65	$65
$22	$F0	$F0	$F0

Other CMX994A common settings are:

CMX994A C-BUS register	
$23	$00
$24	$06
$25	$0B

Care should be taken when designing the PCB to ensure that harmonics generated by the RF PA do not affect the on-board PLL and VCO components.

5.6.4 Hardware AGC – AuxADC1 Connection

In I/Q mode the AuxADC1 input can be used to improve the adjacent/alternate channel rejection with the addition of suitable external components (shown in Figure 2). This function provides a broadband signal detector which is used in the AGC process. This is required to prevent the DISC/ALT ADC inputs limiting internally in the presence of strong alternate channel signals, which are attenuated by the inherent filtering of the ADC.

This functionality is enabled by setting:

- Program Block P6.0:b3=1 (enable hardware AGC)
- $C0:b6 = 1 (enable BIAS)
- $93 = $xx3C (AuxADC1 Enabled, averaging = 3, Routed from AuxADC input 1)
- $95 = $0185 (hi threshold)
- $94 = $0180 (lo threshold)

Note that threshold levels may need adjustment to suit particular hardware implementations.

5.6.5 RSSI Measurement (I/Q Mode)

In I/Q mode the RSSI is calculated from the signal levels present at the I and Q inputs and the AGC levels currently in use. Figure 5 shows a typical response.

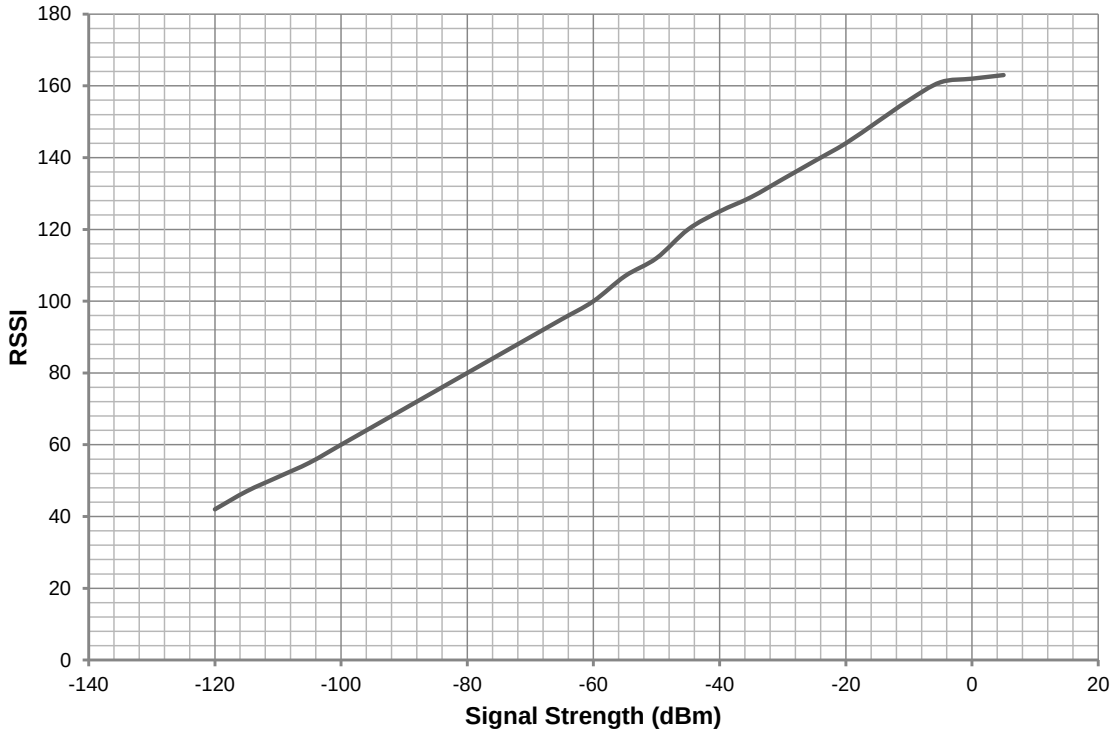


Figure 5 RSSI in I/Q Mode

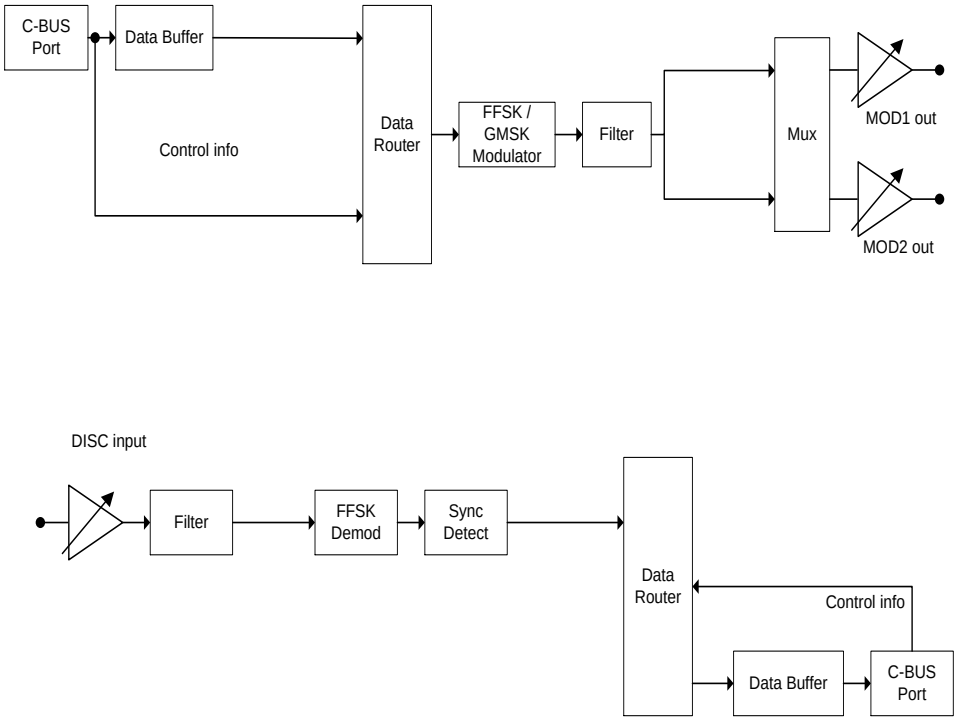


Figure 6 Internal Data Processing Blocks

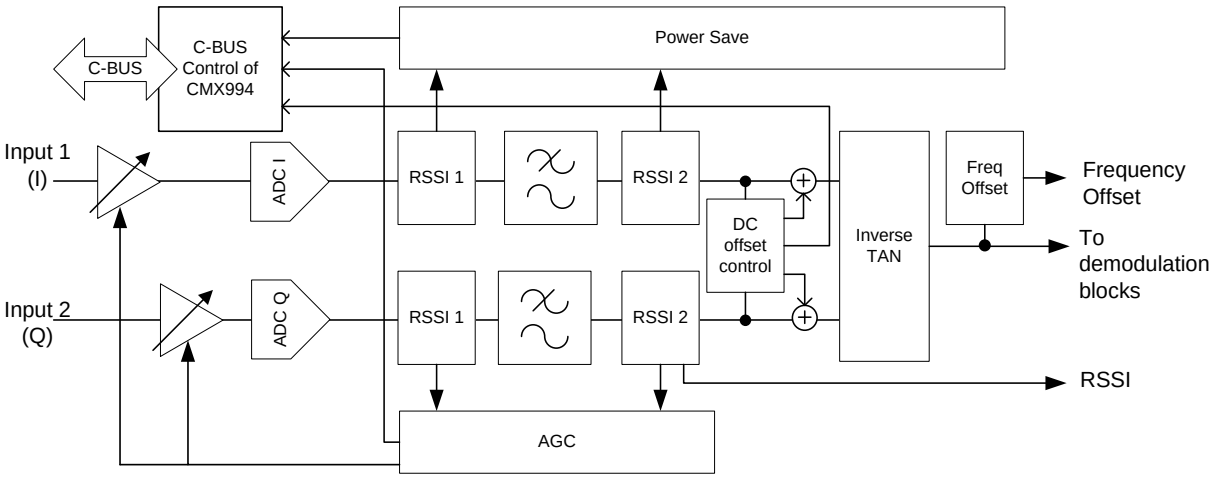


Figure 7 Additional Internal Data Processing in I/Q Mode

5.6.6 DSC / FFSK Frame Sync Detection and Demodulation

The analogue signal from the receiver is from a CMX994A I/Q interface. The signal(s) from the RF section should be applied to the CMX7341 input(s) (normally the DISC input for LD Rx and DISC and ALT inputs for I/Q Rx). The signals can be adjusted to the correct level either by selection of the feedback resistor(s) or using the CMX7341 Input Gain settings.

In I/Q mode, filtering is applied to the input signals and dc offsets are removed before an inverse tan function performs the FM demodulation function. The output of this stage has an offset depending on the frequency error of the received signal compared to the nominal frequency of the receiver. This offset is removed before RRC filtering. In I/Q mode the CMX7341 provides measurements of frequency error and RSSI.

When one of the enabled DSC Frame Sync sequences is detected the raw received data is output over the C-BUS FIFO registers to the host. The host should monitor the incoming data and disable the modem when the EOS characters have been detected or the reception of the incoming sequence is otherwise ended.

For further details of the DSC receiver operation refer to section 6.5.1

5.6.7 Radio Performance Requirements

For optimum performance, the signal should not be significantly degraded by filters that are excessively narrow and/or cause significant group delay distortion. Care should be taken in interfacing the device to the radio circuits to maintain the frequency and phase response (both low and high end), in order to achieve optimum performance. Test modes are provided to assist in both the initial design and production set-up procedures.
Further information and application notes can be found at http://www.cmlmicro.com .

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7341 is designed to work with an external frequency source of 19.2 MHz. For other values, contact CML Customer support.

Table 6 Xtal/Clock Frequency Settings for Program Block 3

Program Register			External Frequency Source (MHz)							
										19.2
P3.14	Idle	GP timer								**$0018**
P3.15		VCO output and AUX clk divide								**$0099**
P3.16	Rx or Tx	MainCLK Init								**$4F51**
P3.17		MainCLK Lock Time								**$0267**
P3.18		MainCLK0								**$43B1**
P3.19		MainCLK1								**$0019**
P3.20		MainCLK2								**$0040**
P3.21		VCO output and AUX clk divide								**$0140**
P3.22		Internal ADC/DAC clk divide								**$0008**

6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7341 and the host microcontroller; this interface is compatible with microwire and SPI. Interrupt signals notify the host microcontroller when a change in status has occurred and the microcontroller should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 6.4.2.

The CMX7341 will monitor the state of the C-BUS registers that the host has written-to every 250 µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

6.2.1 C-BUS Operation

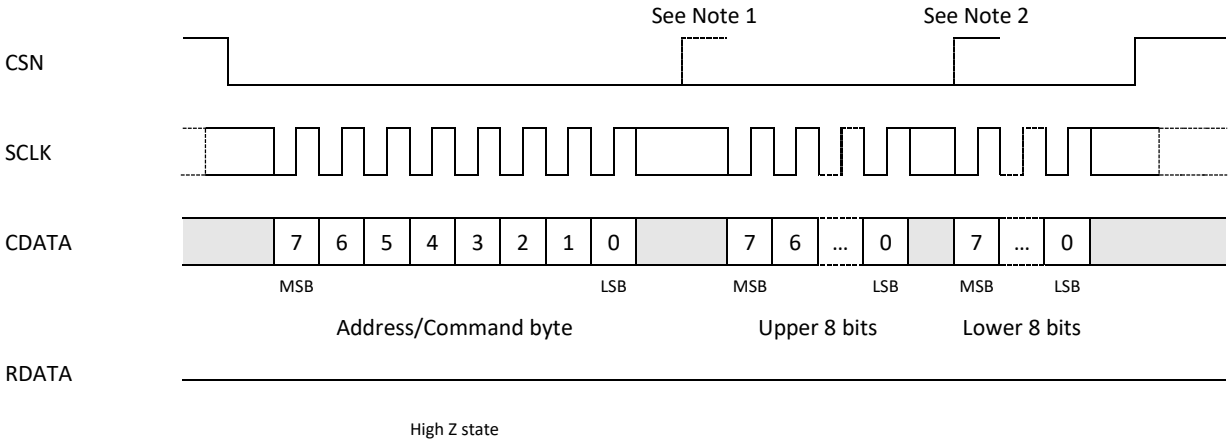
This block provides for the transfer of data and control or status information between the CMX7341's internal registers and the host microcontroller over the C-BUS serial interface. Each transaction consists of a single address byte sent from the microcontroller which may be followed by one or more data byte(s) to be written into one of the CMX7341's Write Only Registers, or one or more data byte(s) read out from one of the CMX7341's Read Only Registers, as shown in Figure 8.

Data sent from the microcontroller on the CDATA (Command Data) line is clocked into the CMX7341 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX7341 to the microcontroller is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept

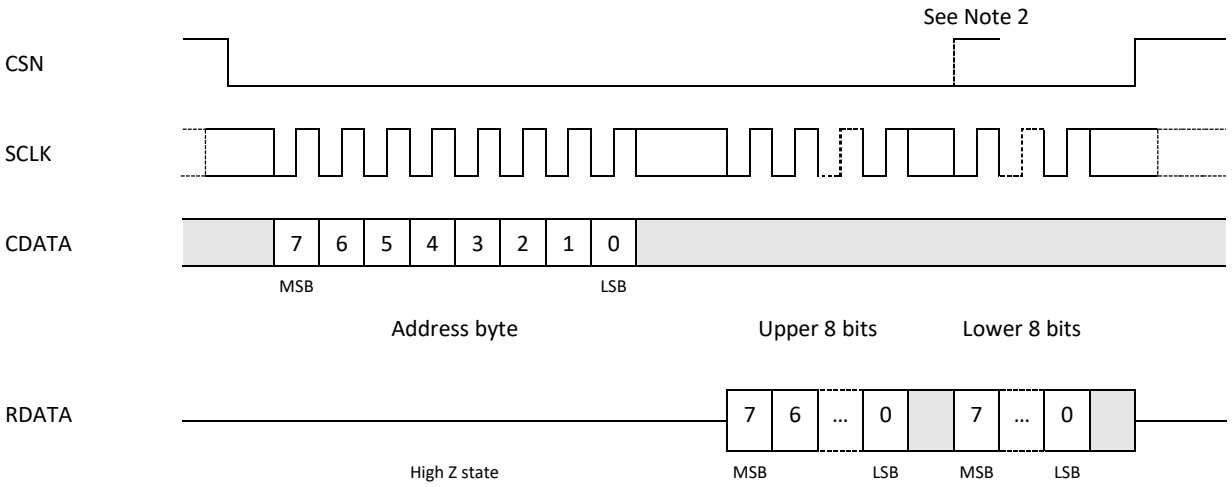
high between transfers. The C-BUS interface is compatible with most common microcontroller serial interfaces and may also be easily implemented with general purpose microcontroller I/O pins controlled by a simple software routine.

The number of data bytes following an address byte is dependent on the value of the Address byte. The most significant bit of the address or data is sent first. For detailed timings see section 7.2. Note that, due to internal timing constraints, there may be a delay of up to 250 µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:



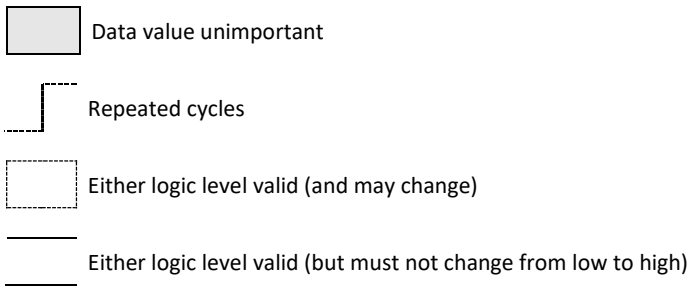


Figure 8 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

6.2.2 C-BUS FIFO operation

The 7341 implements Rx and Tx FIFOs to buffer the incoming and outgoing data. To maximise data bandwidth across the C-BUS interface, the FIFO registers are also capable of data-streaming operation. This allows a single address byte to be followed by the transfer of multiple read or write data words, all within the same C-BUS transaction. This can significantly increase the transfer rate of large data blocks, as shown in Figure 9.

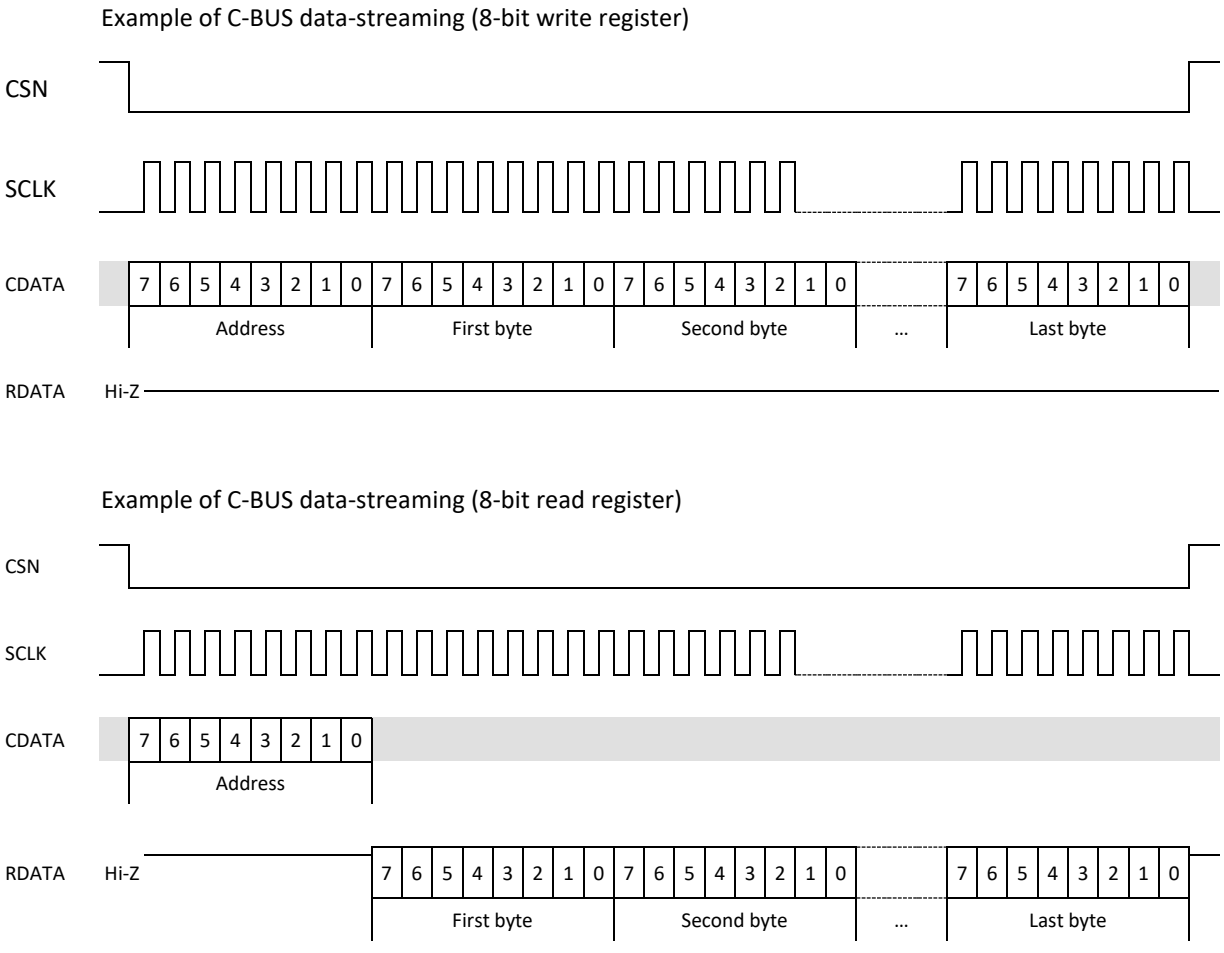


Figure 9 C-BUS Data-Streaming Operation

The Tx and Rx FIFOs are implemented as two separate 256 x 16-bit arrays. Each row of the arrays can be accessed as a 16-bit word ($79 and $7D) or an 8-bit byte ($78 and $7C - which accesses the lower byte of each row). The number of rows of each array currently in use can be read using the $7B and $7F registers.

C-BUS Address	Function		C-BUS Address	Function
$78	Tx FIFO data byte		$7C	Rx FIFO data byte
$79	Tx FIFO data word		$7D	Rx FIFO data word
$7B	Tx FIFO level		$7F	Rx FIFO Level

Table 7 C-BUS FIFO Registers

Any data in the Tx FIFO buffer is flushed on return to Idle mode ($C1 = $0000).

If data was preloaded for transmission but is no longer required this may be cleared by entering Idle Rx mode ($C1 = $0001, and returning to Idle mode to trigger the flush of the FIFO buffer.

6.3 Function Image Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software. The maximum possible size of Function Image™ is 96 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset or a reset via the RESET pin and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7341 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DVDD either directly or via a 220k resistor (see Figure 10).

Once the FI has been loaded, the CMX7341 will report the following information:

- $C5 = Product Ident Code ($7341)
- $C9 = FI version code (6xxx)
- $A9, $AA = Block 2 Checksum
- $B8, $B9 = Block 1 Checksum

The host should verify the checksum values with those published with the Function Image file downloaded from the CML Technical Portal.

The device waits for the host to load the 32-bit Device Activation Code through C-BUS register $C8. Once activated, the device initialises fully, enters idle mode and becomes ready for use, and the Programming flag (bit 0 of the Status register) will be set.

Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be reset via the dedicated RESET pin (if used) or power-cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 8 BOOTEN Pin States

	BOOTEN2	BOOTEN1	Notes:
C-BUS Host load	1	1	FIFO mode (or single word mode)

Multi-Serial Memory load	1	0	Flexible address mode
Serial Memory load	0	1	Compatible with CMX7141
No FI load	0	0	

Note: Following a reset, the contents of the device should be verified using the CRC check facility, and re-loaded if required.

6.3.1 FI Loading from Host Controller

The Function Image™ can be included with the host controller software for download into the CMX7341 at power-up over the C-BUS interface. This is done by writing the FI data into the Tx FIFO Data register ($79) which supports streaming operation. The BOOTEN1/2 pins must first be set to the C-BUS load configuration and the device then powered up or Reset before the FI data is sent over C-BUS.
When using the recommended 19.2 MHz clock source for XTALIN, the device can accommodate the host continuously streaming data to the Tx FIFO at the maximum SCLK rate of 10 MHz, therefore it is not necessary to monitor the FIFO level registers during this operation. FI download time is limited only by the clock frequency of the C-BUS. With a 10 MHz SCLK it should take less than 250 ms to complete even when loading the largest possible Function Image™.

The CMX7341 memory can be protected against brownout or other forms of corruption. This protection is applied automatically in the 7341 FIs, however when using legacy 7131/7141 FIs, this should be applied during the process of FI loading. To apply protection, the host must write the value $007F to C-BUS register $A0 after the last data block is loaded and before sending the activation block which ends the loading of the FI.

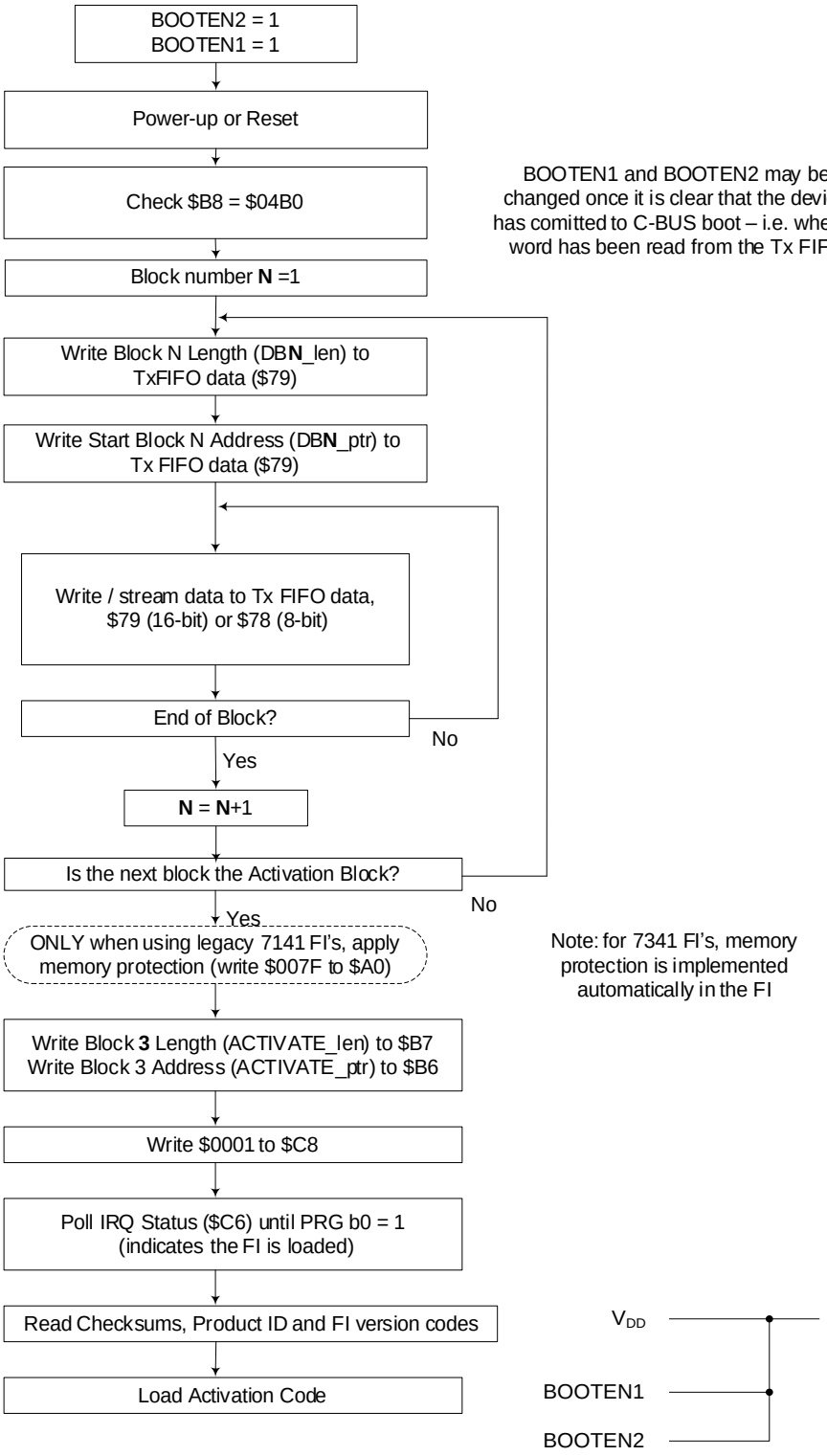


Figure 10 FI Loading from Host

If the main clock frequency (at the XTALIN pin) is slower than the C-BUS clock then the host will need to manually increase the internal MainCLK speed (contact CML Customer Support for details). The device does not take any action until BOTH length and address have been written to the FIFO, so writing the length and then polling for 'FIFO level = 0' will NOT work.

Support for the legacy mode, as used in the CMX7141 and CMX7041 series, is provided, but not recommended. Contact CML Customer Support for details.
Block 3 (Activate) may also be loaded using the Tx FIFO mechanism. However, in this case, the PRG flag will not be set when the operation has completed, so the host must implement a fixed delay or poll the $C5 register until the Device Ident Code appears, before the checksum values can be read.

6.4 Device Control

The CMX7341 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).
For basic operation:

(1) Enable the relevant hardware sections via the Power Down Control register

(2) Set the appropriate mode registers to the desired state

(3) Select the required signal routing and gain

(4) Program the CMX994A using pass-through mode

(5) If required to transmit, load the data into the Tx FIFO

(6) Use the Mode Control register to place the device into Rx or Tx mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. This will also command the CMX994A to enter powersaving mode as well. Additional powersaving can be achieved by disabling any unused hardware blocks in the CMX7341, however, care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the Input or output blocks to function.
See:

- Power Down Control - $C0 write
- Mode Control - $C1 write
- AIS/GMSK Modem Configuration - $A1 write

6.4.1 General Notes

In normal operation, the most significant registers, in addition to the Tx FIFO and Rx FIFO blocks, are:

- Mode Control - $C1 write
- IRQ Status - $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write
- Aux Data and Analogue Mode - $C2 write
- Analogue Control - $C3 write

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed. Setting the Mode register to Idle will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

Under normal circumstances the CMX7341 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

6.4.2 Interrupt Operation

The CMX7341 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the IRQ Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the IRQ Status register change from 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is

(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding IRQ Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the IRQ Status register, except the Programming Flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. The Programming Flag bit is set to 1 only when it is permissible to write a new word to the Programming register.
See:

- IRQ Status - $C6 read
- Interrupt Mask - $CE write.

Continuous polling of the Status register ($C6) is not recommended due to both the increase in response time, host loading and potential digital noise generation due to bus activity. If the host cannot support a fully IRQ driven interface then it should route the IRQ signal to a host I/O pin and poll this pin instead.

6.4.3 Signal Routing

The CMX7341 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit two-point modulation or I/Q schemes) and a single audio output.
See:

- Input Gain and Signal Routing - $B1 write
- Mode Control - $C1 write

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Attenuation control available via the Programming registers in the CMX7341.

See:

- Analogue Output Gain - $B0 write (MOD1 and 2)
- Input Gain and Signal Routing - $B1 write (DISC input, MOD1 and 2)

In common with other FIs developed for the CMX7341, this device is equipped with two signal processing paths. Input 1 and Input 2 should be routed to any of the two differential input sources (ALT, DISC) which should be connected to the I and Q outputs of the CMX994A direct conversion receiver. The internal signals Output 1 and Output 2 are used to provide two-point modulation signals and should be routed to the MOD1 and MOD2 pins as required.

6.4.4 Mode Control

The CMX7341 operates in one of these operational modes:

- Idle
- Rx with CMX994A AGC
- Tx
- Rx with CMX994A I/Q Cal.
- Rx with CMX994A Powersave

At power-on or following a Reset, the device will automatically enter Idle mode, which allows maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled). It is only possible to write to the Programming register whilst in Idle mode.

See:

- Mode Control - $C1 write

GPIO1 and GPIO2 pins (RXENA and TXENA) reflect bits 0 and 1 of the Mode Control register, as shown in Table 9. These can be used to drive external hardware without the host having to intervene. There are also two additional GPIO pins that are programmable under host control.

Table 9 Device Mode Selection

Mode Control ($C1) b3-0	Modem Mode	R20,R21connected to DVdd		R20,R21connected to DVss	
		TXENA	RXENA	TXENA	RXENA
0000	Idle – Low Power Mode	1	1	0	0
0001	Rx with CMX994A AGC	1	0	0	1
0010	Tx	0	1	1	0
0011	*reserved*	x	x	x	x
0100	*reserved*	1	1	0	0
0101	Rx with CMX994A I/Q Cal.(I/Q mode only)	1	0	0	1
1001	Rx with Powersave (I/Q mode only)	1	0	1	0
Others	*reserved*	x	x	x	x

Table 10 AIS/GMSK Modem Control Selection

Mode Control ($C1) b7-4	Rx	Tx
0000	Rx Idle	Tx Idle
0001	*reserved*	*reserved*
0010	*reserved*	Tx AIS/GMSK
0011	*reserved*	Tx AIS/GMSK PRBS
0100	*reserved*	Tx AIS/GMSK Preamble
0101	*reserved*	Tx AIS/GMSK Mod Set-up
0110	*reserved*	Tx AIS/GMSK Test
0111	*reserved*	Reset/Abort
1xxx	*reserved*	*reserved*

Table 11 Analogue Mode Selection

b15	b14	b13	b12	b11	b10	b9	b8
0	Tone	0	0	0	0	0	DSC/FFSK

In Rx, only DSC / FFSK mode can be enabled.

In Tx, only DSC/FFSK or AIS/GMSK mode should be selected at any one time.

The Modem Mode bits and the Mode Control bits should be set together in the same C-BUS write.

6.4.5 Tx Mode AIS/GMSK Raw

In Tx AIS/GMSK mode operation ($C1, Mode Control = $0022), the host should write the data block to the C-BUS TxFIFO registers and then set the Modem Mode to AIS/GMSK and the Control bits to Tx. The data in the FIFO is then transmitted automatically. The entire data burst can be loaded in one data transfer, preceded by a 16-bit control word that specifies the number of valid bits to the transmitted and with b15 = 1. The bits are transmitted msb first, so if the final byte does not contain 8 valid bits, the valid bits should be left-justified.
At the end of the burst, after the last bit has left the modulator, a 'Tx Done' IRQ will be issued. At this point it is now safe for the host to change the Mode Control and Modem Mode to Idle ($C1, Mode Control = $0000) and turn the RF transmitter off.

Alternatively, the Tx sequencer may be enabled to automatically control the RF transmitter power using the RAMDAC at the burst start and end. Refer to section 6.4.10.

The AIS format allows for a maximum of 256 bits to be sent in any single burst.

Table 12 AIS/GMSK Tx FIFO format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	Bit count (in AIS/GMSK max value = $100)											
								Data							
								Data							

6.4.6 Tx Mode AIS/GMSK PRBS

In PRBS mode ($C1, Mode Control = $0032) the preamble is transmitted automatically followed by a PRBS pattern conforming to ITU-T O.153 (para. 2.1) giving a 511-bit repeating sequence.

6.4.7 Tx Mode AIS/GMSK Preamble

In Preamble mode ($C1, Mode Control = $0042) the preamble sequence [$3333] is sent continually. This can be used to set up and adjust the RF hardware.

6.4.8 Tx Mode AIS/GMSK Mod Set-up

In Mod Set-up mode ($C1 = $0052), a repeating sequence of eight +1 symbols followed by eight -1 symbols is sent. This can be used to set up and adjust the RF hardware.

6.4.9 Tx Mode AIS/GMSK Test

In Test mode ($C1 = $0062), simple test waveforms are generated by loading the TxData4 ($CB) register with the required bit pattern. See section 8.1.39

6.4.10 Tx Sequencer

The Tx Sequencer provides an automated way of executing a sequence of actions, thus reducing timing constraints placed on the host. It is controlled by setting b15 in the AIS/GMSK Modem Configuration register ($A1) to 1. If enabled, it will automatically start executing its sequence of transmit actions when the CMX7341 is placed in Tx mode. The timing values for each action can be set in P3.0 to P3.12 and are defined in increments of 250 µs. The RAMDAC will ramp (up and down) over a period defined by the configuration in P3.13 (RAMDAC scan time configuration).

For AIS/GMSK Tx modes the CMX7341 will be prevented from modulating data until the Modulation Start Delay has elapsed. For DSC/FFSK Tx modes the signal will initially be muted for this period, at which point any buffered FFSK data will begin to modulate. Tone generation will not be possible during this start delay time therefore tone generation commands should be delayed until the Modulation Start Delay timer has expired. Expiry of the timer is indicated by the raising of the Sequencer Event IRQ ($C6:b2) and setting of the Sequencer Start event flag (b10) of the AIS/GMSK Modem Status - $C9 read register.

The Tx Sequencer may also directly take control of the GPIOA and GPIOB signals if required – setting them high for the duration of the active mode. This is enabled by selecting the appropriate bit in P6.0:b13,12. The delay timers for controlling each GPIO signal transition are set individually.

In both DSC/FFSK and AIS/GMSK Tx modes the sequencer ends automatically following the last data to be transmitted. The Tx Sequencer can also be forced to execute the “end of burst” actions by writing Tx Sequencer Release ($B000) to Aux Function Control - $A8 write. This may be used to gracefully terminate a

GMSK/AIS test pattern (such as the PRBS mode) while the Tx sequencer is in use, since these do not have a defined burst length and will remain active until cleared by the host.

Following completion of the last sequencer action (TXENA inactive) the Sequencer Event IRQ is asserted with the Sequencer End event flag (b11) being set in the AIS/GMSK Modem Status - $C9 read register and the device is automatically returned to its previous mode.

When choosing delay values, it is important that the RAMDAC ramp down completes by the end of the sequencer event. This can be confirmed by also verifying that the Ramp flag (b12) of AIS/GMSK Modem Status - $C9 read is clear when the Sequencer (End) event IRQ is raised. This can be accomplished by either increasing the “TXENA inactive delay” timer or decreasing the RAMDAC scan time.

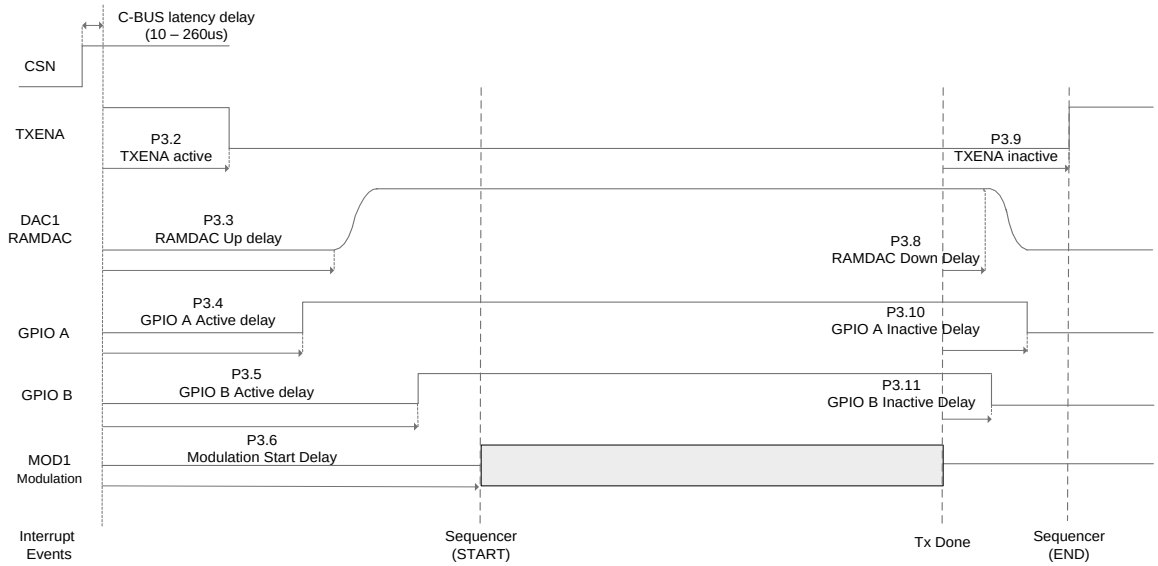


Figure 11 Tx Sequencer Delay Timers

6.4.11 Tx Mode DSC/FFSK

Transmitting DSC/FFSK data utilises the “Analogue” mode settings ($C1=$0102), the host should write the data block to the C-BUS TxFIFO registers and then set the Modem Mode to DSC/FFSK and the Control bits to Tx. The data in the FIFO is then transmitted automatically. The entire data burst can be loaded in one data transfer, preceded by a control word that specifies the number of valid bits to be transmitted and with b15 = 1. The bits are transmitted msb first, so if the final transfer contains less than 8 valid bits, the valid bits should be left-justified within the data byte.
At the end of the burst, after the last bit has left the modulator, a ‘Tx Done’ IRQ will be issued. At this point it is now safe for the host to change the Mode Control and Modem Mode to Idle ($C1, Mode Control = $0000) and turn the RF transmitter off.

Alternatively the Tx sequencer may be enabled to automatically control the RF transmitter power via the RAMDAC at the burst start and end. Refer to section 6.4.10.

The “bit count” field can hold a maximum value of 2040, defining the longest message (in bits) which can be transmitted in any single DSC/FFSK burst.

Table 13 DSC/FFSK Tx FIFO format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	Bit count (in DSC/FFSK max value = $7F8)											
								Data							
								Data							

6.4.12 Rx Mode DSC/FFSK

Receiving DSC/FFSK data utilises the "Analogue" mode settings with the CMX994A providing the I/Q signal interface ($C1 = $0101 for Rx with AGC, $C1=$0109 for Rx with Powersaving and $C1=$0105 for Rx with I/Q dc calibration). Once a Frame sequence pattern (SYNC0, SYNC1 or SYNC2) has been detected, all subsequent data will be loaded into the Rx FIFO in byte mode until it is full, or the host commands the device to leave Rx mode. Which synchronisation pattern is detected will affect the alignment of the message in the data produced, and this must be accounted for in decoding. This can be observed by reading the Analogue Status register ($CC) after the FS IRQ is raised. The data reported in the Rx FIFO will begin with the 8 bits received immediately following the detected pattern.

Table 14 DSC/FFSK Rx FIFO format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	X	X	x	x	Data							
x	x	x	x	X	X	x	x	Data							

6.4.13 Rx Mode with CMX994A AGC

When receiving in I/Q Mode ($C1 = $0101) the device will control its internal analogue gain and the gain of the CMX994A in order to keep the received I/Q signals within an acceptable dynamic range. This AGC feature may be disabled using Program Block P6.0 (I/Q AGC function), in which case any setup that the host has made of the CMX994A will determine its gain, with the input gain of the device being controlled using the Input Gain and Signal Routing - $B1 write register.

While the I/Q AGC is active this register should not be accessed by the host as this will interfere with its operation.

It is important to ensure that the dc offset on the I/Q signals is small, otherwise the AGC function will interpret the dc offset as a large received signal and may never select maximum gain. This problem can be addressed by calibrating the CMX994A as described in Section 6.4.14.

6.4.14 Rx Mode with CMX994A I/Q Cal

While receiving in I/Q mode ($C1=$0105), the device will estimate and remove the dc error present in the I/Q signals from a CMX994A receiver. However, it is necessary to calibrate the CMX994A so that the magnitude of the dc offsets presented is as small as possible. Selecting Rx mode with CMX994A I/Q Cal ($C1, Mode Control b3-0 = $5) causes the device to measure the dc offset on the DISC and ALT input pins and to control the CMX994A receiver to minimise the dc offsets.

Important note: when calibrating I/Q it is important that the I/Q signals are not swapped when interfacing to the CMX994. This can be corrected by using bits 2 to 5 of the Input Gain and Routing register ($B1).

If the CMX994A is poorly calibrated, a loss of headroom when receiving signals will result. In extreme cases, when large dc offsets are amplified, the result can be big enough to prevent the AGC from reaching maximum gain as it interprets the dc offset itself as a large signal.

Selection of some CMX994 options such as low power, or phase correction in the case of a CMX994A/CMX994E, can change the I/Q dc position. For this reason the calibration should be executed with the desired CMX994 configuration already applied and little or no RF signal at the input.

Improved resilience to RF signals present at calibration is achieved by the temporary setting of the LNA Pwr bit for the duration of the calibration process. This is accessed using the Rx Control Register on the CMX994 ($12) via pass-through mode with b5 set to disable power to the LNA. After the calibration is completed this setting must be restored before normal reception is attempted - otherwise the LNA will remain disabled and significantly reduce receiver sensitivity.

Having completed the CMX994 calibration process, the resulting value written to the CMX994 Offset correction register (or Extended Offset Register for CMX994A/E) is available to read using the Aux Data and Status ($A9, $AA) registers, once this is configured via Aux Config - $CD write. This means that having calibrated the CMX994 on a receive channel the calibration result may be stored by the host microcontroller and restored at a later time using the CMX994 pass-through mode.

The format of the dc Offset Correction register read back value differs slightly between a CMX994 and a CMX994A/CMX994E. When a CMX994A/CMX994E is connected (and configured as such) the calibration will be performed using the Extended Rx Offset Register ($17). This is a 16-bit register with a greater range of offset values than available in the CMX994 (which uses the 8 bit register $13). Because the Aux ADC Data and Status registers ($A9 and $AA) only provide 12 available bits the field is compressed when read back during this mechanism. If the host microcontroller wishes to write the values to a CMX994A/CMX994E (via CMX994 pass-through mode) it must convert the calibration result format accordingly before writing to the CMX994A/CMX994E Extended Rx Offset Register ($17). For further details about the format of the I or Q correction values please refer to the CMX994/CMX994A/CMX994E Datasheet, available from the CML website. To take advantage of the Extended Offset functionality in the calibration the device type must have previously been set via P6.2, prior to the calibration command.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Q Channel Correction Value						0	0	I Channel Correction Value					

Figure 12 - Format of CMX994A/E Extended Rx Offset register ($17)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	Q Channel Correction Value						I Channel Correction Value					

Figure 13 - Format of I/Q dc calibration reporting when CMX994A/CMX994E is selected

6.4.15 Rx Mode with CMX994A Powersave

6.4.15.1 Overview

Significant power saving may be achieved during receive operation by using the powersaving mode of the CMX7341 FI-6 and CMX994A. These are controlled by the device automatically when powersave is enabled by selecting Rx mode with powersave ($C1 = $0109). It will continue to powersave the CMX994A until a valid signal is detected, as one of the enabled DSC sync pattern. At this point a Powersave Exit IRQ will be raised and the

power-saving state will be cleared. From this point the CMX994A will remain 'on', until the powersave mode is reapplied by rewriting to the Mode Control register again. The Mode Control register may also be re-written while the powersave is still active – this will have the effect of restarting the state machine from the beginning of the off time state. An overview of the powersave states can be seen in Figure 14.

It should be noted that CMX7341 FI-6 incorporates a modified powersave state machine which operates differently to other FIs in the CMX7341 family. This is optimised for use with VHF DSC receive operations when using the built in PLL/VCO in the CMX994A and includes default values intended to optimise the power saving for reception of marine VHF DSC messages.

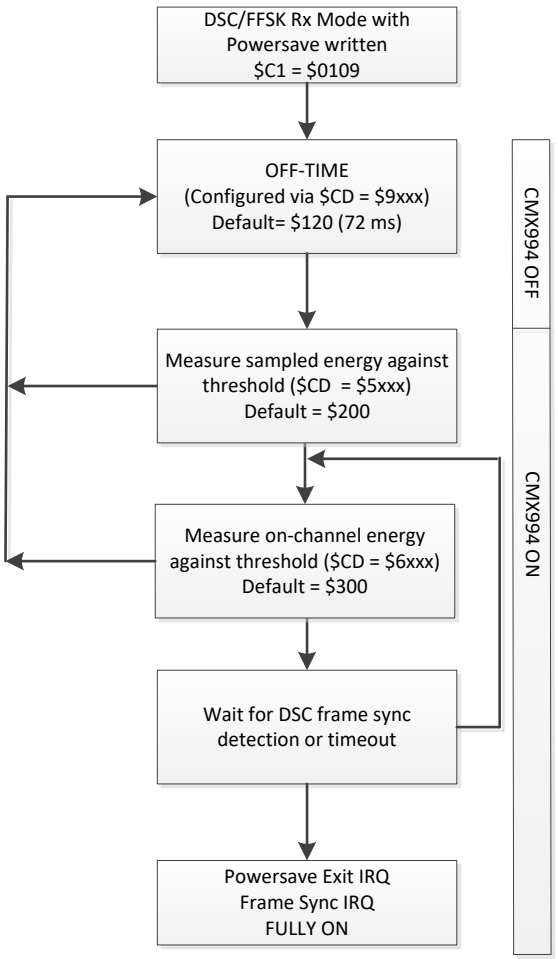


Figure 14 – FI-6 Powersave States, optimised for VHF DSC Rx

Changes to powersave related settings should be made with caution and may interfere with the reliable reception of DSC messages.

In order for the DSC frame sync detection to function during powersave the two "Phasing character" based sync patterns are required to be enabled. These detect on the later end of the DSC Phasing character sequence, either as "DX","RX-3,"DX" (SYNC1) or "RX-3", "DX", "RX-2" (SYNC2). A true detection of the dotting sequence (SYNC0) is less likely to occur during powersave operation so disabling this may reduce the chances of a false detection.

The default off-time setting of $120 (= 72ms) is chosen to allow the powersave to miss a portion of the burst start and detect the RF energy in time for the frame sync detection using the SYNC1 or SYNC2 patterns.

Once an incoming signal has been detected the normal AGC operation applies, as per the Rx with CMX994A AGC mode described in section 6.4.13.

The host microcontroller is responsible for decoding the message content. The alignment of the incoming bitstream with the DSC packet format should be determined by checking which SYNC pattern was detected. The end of the message must be determined through decoding the data and then disabling the DSC receive function ($C1 = $0001). The host may then re-apply the powersave mode and re-enable the DSC to prepare for the next DSC message on the channel ($C1 = $0109) whilst observing the C-BUS latency period between the two write commands

Powersave default parameters have been selected for reliable operation in accordance with IEC 63269. For assistance in targeting different requirements please contact CML.

6.4.15.2 CMX994A Powersave Configuration and Options

The powersave functions are compatible with three variants of the CMX994: CMX994, CMX994A and CMX994E. The device in use should be selected by writing the appropriate value to Programming Register P6.2 (see section 8.3.7).

The default settings have been designed to optimise the power saving in most situations and changing them may result in changes to the detection and decoding performance so should only be implemented with care. The defaults are intended to target IEC 63269 requirements, with the most efficient power consumption and maintaining reliable detection.

The exception to this in the default settings is the VCO/PLL control enable bit (Program Block 6.3, b12). This is off by default, but enabling it will allow the CMX994 PLL to be disabled automatically during the powersave operation with the rest of the receiver (during the “Off” state) and this can give a significant further reduction in the power consumption when no signal is present.

The VCO/PLL control is disabled by default as it requires additional support from the host microcontroller to function correctly, and possibly changes to the Tx Sequencer values: On leaving the Rx during powersaving the VCO/PLL is left in an undefined state. This can be resolved by a host write to the CMX994 General Control Register ($11) to re-write the PLLEN (b2) and VCOEN (b3) bits, along with the other required settings in this register. This write must be performed using the CMX994 pass-through function in Idle mode and can be performed alongside other CMX994 register accesses which may be required to retune the PLL to select a new channel frequency.

Because of the need to account for a possible re-locking of the PLL, this write needs to occur ahead of the desired transmission time. It can be accounted for by configuring a delay in the Tx Sequencer which will ensure that the PLL lock will have time to complete before the RAMDAC function begins. As an example a delay of 10 ms may be applied by adding an additional 40 (40 * 250 µs) to each of the “startup delays” to create an extra 10 ms delay on transmission. The host must then initiate the Tx command an additional 10 ms ahead of the slot boundary to give the expected alignment.

To produce a 10 ms delay the following values may be written (based on the default settings):

Program Block/ Word		+10 ms Delay Value
P3.2	TXENA delay	$0028
P3.3	RAMDAC Ramp delay	$0028
P3.4	GPIOA delay	$0028
P3.5	GPIOB delay	$0028
P3.6	Modulation delay	$002A

If the Tx Sequencer is not in use, the host microcontroller should schedule the PLL command ahead of the transmission by a similar amount.

6.4.15.3 Powersave Performance

Table 15 Variation in Average Current Consumption with Powersave States / Test Conditions

Test Condition	Average Current (Default config, ,CMX994A only)	Average Current (PLL/VCO control, CMX994A only)
No signal	25 mA	12 mA
+45 dB adjacent channel signal	29 mA	17 mA
DSC Message being received / powersave disabled	86 mA	86mA

6.4.16 Data Transfer

All payload data between the host and the device uses the built-in FIFO buffers. This allows the complete transmission burst to be loaded prior to enabling the RF transmitter and so minimises the C-BUS activity and any possible interference to the RF sections during transmit. Likewise in Receive, the host can monitor the level of the Rx FIFO block and wait until it has collected a suitable number of bits before reading it back in one C-BUS transfer.

The Tx and Rx FIFO's are 256 x 16 bits and can be read/written as words or bytes. In byte mode only the lower 8 bits of each word are read/written. In Tx mode, the first payload data should be preceded by a bit count value that specifies the total number of bits that are to be transmitted. In Rx mode, the device has no prior knowledge of the burst length and so will return all bits it receives following detection of the Frame Sync pattern until the host tells it to stop, or the FIFO becomes full.

See:

- Tx FIFO Data (byte mode) - $78 Write – 8-bit
- Tx FIFO Data (word mode) - $79 Write – 16 bit
- Tx FIFO Level - $7B Read – 16 bit

- Rx FIFO Data (byte mode) - $7C Read – 8 bit
- Rx FIFO Data (word mode) - $7D Read – 16 bit
- Rx FIFO Level - $7F Read – 16 bit

6.4.17 CMX994A Pass-through

To allow the host to communicate directly with the CMX994A for test and configuration purposes, a pass-through mode allows any CMX994A C-BUS register to be read or written (as appropriate) accessed as Program Block $0F (see section 8.1.45). This mode uses the Programming ($C8), Program Block Address ($C7) and RxData0 ($B8) registers on the CMX7341.

To write to the CMX994A:

- Set the device to Idle mode ($C1=$0000)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX994A C-BUS address to the Program Block Address register ($C7) with b15-8=$0F
- Write the CMX994A data value to the Programming register ($C8)
- Wait for the Program Flag to be set ($C6 b0).

Note that it is NOT possible to read data back from the CMX994A using this interface.

When using the CMX994A or CMX994E, the Extended Rx Offset Register ($17) is 16 bits wide. In order to access this register select 16-bit mode by setting b14 of the Program Block Address register ($C7) (all other registers are 8 bits wide so b14 must be left at zero for any other register).
For example, writing $4F17 to the Program Block Address register will access register $17 on the CMX994A in 16-bit mode. The full 16 bits to write should then be written to the Programming Register ($C8) in accordance with the register description.

6.5 DSC/FFSK Data Modem

The device supports 1200 baud FFSK data mode suitable for use with marine VHF Digital selective Calling to ITU-R M.493 and ETSI EN 301 025 or similar systems.
Selection of the FFSK mode is performed by bit 8 of the Mode register ($C1).

See:

- Mode Control - $C1 write
- AIS/GMSK Modem Configuration - $A1 write

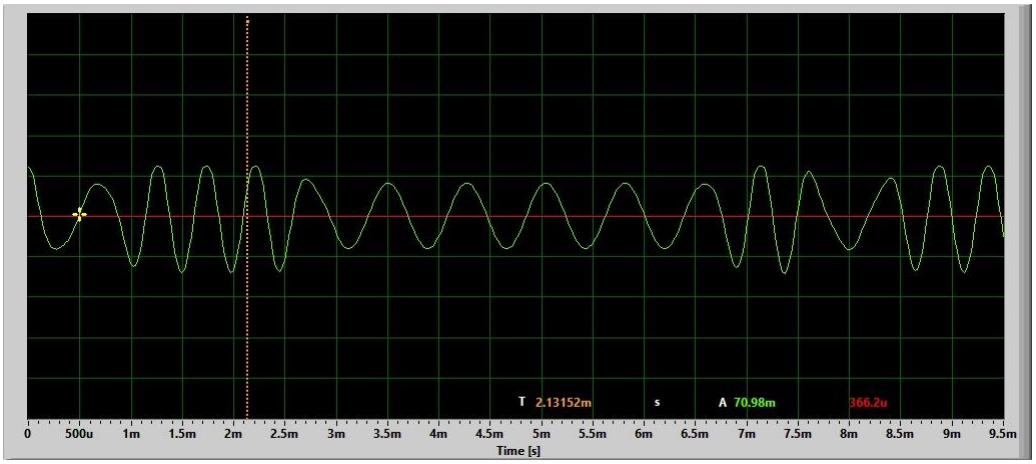


Figure 15 Modulating Waveforms for 1200 FFSK Signals

The table below shows the combinations of frequencies to represent each bit of data, for both baud rates. Pre-emphasis is applied to the transmitted signal in accordance with ITU-R M.493.

Table 16 Data Frequencies for DSC/FFSK mode

Baud Rate	Data	Frequency
1200baud	1	1300Hz
	0	2100Hz

	DX/RX	A	B	C	D	E	F	G	H	I
Dot Pattern	Phasing Sequence	Format Specifier	Called Party Address	Category	Self-Identification	Tele-command message	Frequency message	Frequency message	End of sequence	Error-check character
		2 Identical characters	5 characters	1 character	5 characters	2 characters	3 characters	3 characters	3 identical DX characters 1 RX character	1 character

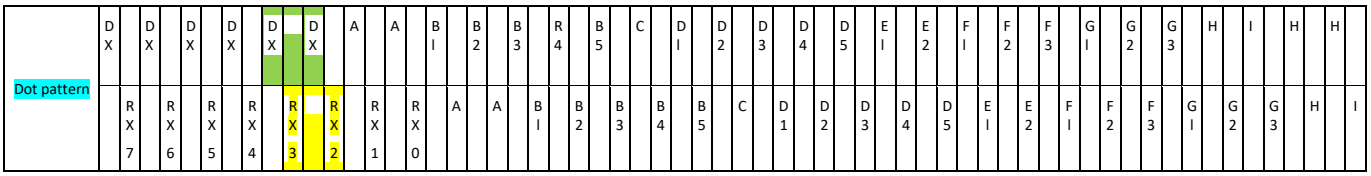


Figure 16 ITU M.493 DSC message format

The “dotting” pattern consists of 20 bits of alternating 1 and 0’s. Each subsequent DSC character consists of 7 bits of data with 3 bits of parity. The “end-of-sequence” character can be any of 117, 122 or 127, depending on the response required. See ITU-R M.493 for details. After the initial message an extended DSC messages may optionally follow it. See ITU-R M.821-1.

6.5.1 Receiving DSC/FFSK Signals

The received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The recovered data is stored in the RX FIFO and an interrupt issued to indicate received data is ready. Data is transferred via the C-BUS under host control. . The FFSK bit clock is not output externally.

Upon (re)starting the DSC/FFSK receiver the incoming signal is compared with the selected programmed Frame Sync pattern (SYNC0, SYNC1 or SYNC2). An in-band IRQ will be flagged when one of the enabled Frame Sync patterns is detected. Once a valid Frame Sync pattern has been detected the frame sync search algorithm is disabled; it may be re-started by disabling the DSC/FFSK bit of the Mode register ($C1:b8) and then re-enabling it (taking note of the C-BUS latency time). This may be combined with the restoration of the powersave state (if required) by also setting $C1:b3 in the same write.

Sync pattern sequences are available corresponding to sections of the DSC sequence as shown by the highlighted sections of Figure 16 or Table 17 below. Sync detections are reported with an in-band event IRQ and a code in the Aux Data and Analogue Status - $CC read register. At least one pattern must be enabled for the DSC Rx to function. All DSC sync patterns are enabled and subject to 1 bit of error tolerance by default. The error tolerance may be changed in Program Block P4.28.

DSC Sync	Pattern (hexadecimal)	Details
Sync 0	55555	Dotting Sequence (20 bits)
Sync 1	2F9D6AF9	Phasing - DX | RX3 | DX (30 bits)
Sync 2	35ABE55B	Phasing - RX3 | DX | RX2 (30 bits)

Table 17 - DSC Sync patterns

Immediately after the sync pattern the following data bytes will be decoded and will begin to accumulate in the Rx FIFO. When processing the data knowing which sync pattern was detected is required in order to align

the data for decoding in the reconstructed DSC message. This may be determined by reading Aux Data and Analogue Status - $CC read following the frame sync detection IRQ.

The host microcontroller must determine the end of reception and disable the demodulator at the appropriate time by decoding the message content. Restarting the DSC/FFSK demodulator will reset the RxFIFO buffer contents so the host microcontroller must ensure that the entire message data has been read before restarting or re-enabling the frame sync search. It may also be desirable to check for an extended DSC message (ITU M.821-1), following an end of sequence pattern before the detection is restarted. The MoB device is only expected to respond to ACK messages as shown in ITU-R M.493-15 Tables A1-4.2 and A1-4.7.

6.5.2 Transmitting DSC/FFSK Signals

When enabled, the modulator will begin transmitting the data in the TxFIFO. The device is configured for single or two-point modulation of an RF VCO and / or the RF PLL reference oscillator. The overall level of the FFSK signal generated can be controlled using the Audio Tone Tx Level field of the Analogue Control register ($C3) and the two MOD outputs can be independently adjusted using the MOD1 and MOD2 Fine Level Control - $80 write and Analogue Output Gain - $B0 write registers.

The device generates its own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 15 and Table 16. The binary data is taken from TxFIFO register ($76), most significant bit first. The device will indicate that the final data bit has left the chip by raising the TxDone IRQ, after which the host may power-down the RF circuitry and return the device to Idle mode as required.

6.6 AIS/GMSK Data Modem

6.6.1 Transmitting GMSK Signals

The GMSK format is specified in ITU-R M.1371 as:

Bit rate:	9600 bps
GMSK BT-product:	0.4
GMSK modulation index:	0.5

Suitable for use in the 25 kHz channels in the VHF Marine band.

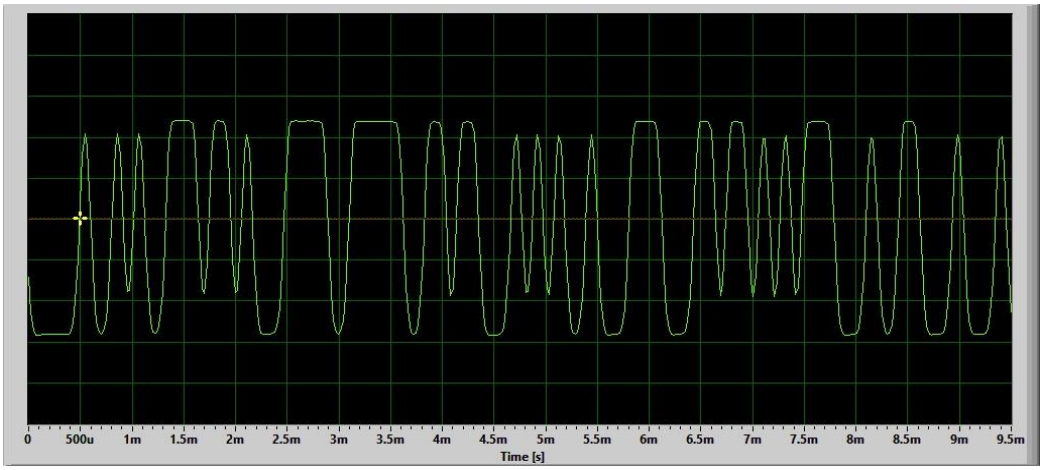


Figure 17 GMSK waveform (PRBS)

When enabled, the modulator will begin transmitting the data loaded in the TxFIFO. The device is configured for single or two-point modulation of an RF VCO and / or the RF PLL reference oscillator. The level of the two MOD outputs can be independently adjusted using the MOD1 and MOD2 Fine Level Control - $80 write and Analogue Output Gain - $B0 write registers to obtain the flat frequency response required for GMSK modulation.

The device generates its own internal data clock and converts the binary data into the appropriately filtered signal. The binary data is taken from TxFIFO register ($76), most significant bit first. The device will indicate that the final data bit has left the chip by raising the TxDone IRQ, after which the host may power-down the RF circuitry and return the device to Idle mode as required.

AIS transmissions are synchronised to UTC using 26.6 ms slots and it is recommended that the host initiates a Tx command as close to the slot boundary as possible to avoid disturbing other stations using the AIS channels. The MoB standard has a timing accuracy requirement of +/- 312 us. The maximum number of bits that can be transmitted in an AIS slot is 256, however a normal message from an MoB unit follows the AIS message 1 and message 14 format from ITU-R M.1371-5 Annexe 9 “Requirements for stations using burst transmissions” which occupy less than one slot. Note that due to the “bit-stuffing” applied to the data bits the actual length of each message will vary depending on its content, but will never exceed one slot.

All AIS Tx data supplied to the device must be NRZI encoded and HDLC formatted according to ITU-R M.1371.

Table 18 AIS Message Structure

Field:	Ramp up	Preamble	Start Flag	Message data	FCS	Stop Flag	Ramp down
Bits:	8	24	8	168 (max)	16	8	8

Table 19 AIS Message 1 format

Parameter	Number of bits	Description
Message ID	6	Identifier for this Message 1
Repeat indicator	2	Used by the repeater to indicate how many times a message has been repeated. See § 4.6.1, Annex 2; 0-3; 0 = default; 3 = do not repeat any more
Source ID	30	Number Identity (MMSI) of the source of the message (see Article **19** of the RR and ITU R M.585)
Navigational status	4	14 = locating device active 15 = locating device under test]
Rate of turn ROTAIS	8	0 to +126 = turning right at up to 708° per min or higher 0 to –126 = turning left at up to 708° per min or higher Values between 0 and 708° per min coded by $ROT_{AIS} = 4.733\ SQRT(ROT_{sensor})$ degrees per min where ROT_{sensor} is the Rate of Turn as input by an external Rate of Turn Indicator (TI). ROT_{AIS} is rounded to the nearest integer value. +127 = turning right at more than 5° per 30 s (No TI available) –127 = turning left at more than 5° per 30 s (No TI available) –128 (80 hex) indicates no turn information available (default). ROT data should not be derived from COG information.
SOG	10	Speed over ground in 1/10 knot steps (0-102.2 knots) 1 023 = not available, 1 022 = 102.2 knots or higher
Position accuracy	1	1 = high (≤10 m) 0 = low (>10 m) 0 = default
Longitude	28	Longitude in 1/10 000 min (±180°, East = positive (as per 2’s complement), West = negative (as per 2’s complement). 181 = ($6791AC0_h$) = not available = default)
Latitude	27	Latitude in 1/10 000 min (±90°, North = positive (as per 2’s complement), South = negative (as per 2’s complement). 91° (3412140_h) = not available = default)
COG	12	Course over ground in 1/10 = (0-3 599). 3 600 ($E10_h$) = not available = default. 3 601-4 095 should not be used

Parameter	Number of bits	Description
True heading	9	[Degrees (0-359) (360 – 510 should not be used) 511 = not available = default]
Time stamp	6	UTC second when the report was generated by the electronic position system (EPFS) (0-59, or 60 if time stamp is not available, which should also be the default value 61 if positioning system is in manual input mode 62 if electronic position fixing system operates in estimated (dead reckoning) mode 63 reporting last known position when the positioning system is inoperative)
Special manoeuvre indicator	2	0 = not available = default 1 = not engaged in special manoeuvre 2 = engaged in special manoeuvre (i.e. regional passing arrangement on Inland Waterway) 3 = engaged in a man overboard recovery
Spare	2	Should be set to zero. Reserved for future use.
Transmit power	1	0 = default = high power 1 = low power]
RAIM-flag	1	Receiver autonomous integrity monitoring (RAIM) flag of electronic position fixing device; 0 = RAIM not in use = default; 1 = RAIM in use. See ITU-R M.1371 Table 50
Communication state	19	See ITU-R M.1371 table 49
Number of bits	168	

Table 20 AIS Message 14 Format

Parameter	Number of bits	Description
Message ID	6	Identifier for Message 14; always 14.
Repeat indicator	2	Used by the repeater to indicate how many times a message has been repeated. See § 4.6.1, Annex 2; 0-3; 0 = default; 3 = do not repeat any more
Source ID	30	Identity (in the MMS) of the source of the message (see Article **19** of the RR and ITU-R M.585)
Spare	2	Should be set to zero. Reserved for future use
Safety related text	96 Maximum	6-bit ASCII as defined in ITU-R M.1371 Table 47
Maximum number of bits	168	Occupies up to 1 slots

The text field contains the message “MOB ACTIVE” or “MOB TEST” encoded using the 6-bit ASCII coding in ITU-R M.1371.

In active mode the MOB AIS transmits messages in a burst of 8 messages once per minute. The SOTDMA (Self-Organising Time Division Multiple Access) communication state of Message 1 is used to pre-announce its future transmissions.

Message 1 is transmitted with the navigational status set to 14 and Message 14 is be transmitted with the safety related text set to "MOB ACTIVE". In test mode the navigational status is set to 15 and the safety related text to “MOB TEST”.

Message 14 is transmitted nominally every 4 min and replace one of the position reports on both channels.

6.7 GPIO Pin Operation

The CMX7341 provides four GPIO pins: RXENA, TXENA, GPIOA and GPIOB.

RXENA and TXENA are configured to reflect the Tx/Rx state of the Mode register under control of the Tx Sequencer. These lines should be pulled to their inactive state by 47k resistors. This will ensure that the

signals are in an inactive state whilst the FI loads, and also allows the FI to determine if they should be driven active high (CMX994A compatible) or active low (for backwards compatibility with the 7141 series).

Note that RXENA and TXENA will not change state until the relevant mode change has been executed by the CMX7341. This is to allow the host sufficient time to load the relevant data buffers required prior to its transmission. There is thus a fixed time delay between the GPIO pins changing state and the data signal appearing at the MOD output pins. During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them, so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIOA and GPIOB can either be used as serial clock and data signals when separate serial ports are required (see Section 4.4 Serial Port Interfaces), can be host programmable for input or output, or can be assigned as part of the Tx sequencer operation. The mode for each pin is set in Program block 6.0.

The default state is input, high level. When set for input, the values can be read back using the Modem Status register, $C9. In output mode the value for the GPIO pin is written via the Aux Function Control register, $A8. The GPIOA and GPIOB functions can also be relocated to use the SYSCLK1 and SYSCLK2 pins. This allows the GPIOA or GPIOB functionality to still be used while the alternate SPI configuration is selected.

6.8 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed from any of the signal input pins under control of the AuxADC Control register, $93. Conversions will be performed as long as a valid input source is selected. To stop the ADCs, the input source should be set to ‘off’. Register $C0, b6, BIAS, must be enabled for auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC Control register, $93, the length of the averaging is determined by the value in the AuxADC Control register, $93, and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value.

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value
1 = 25% of the current value will be added to 75% of the last average value
.. = 12.5% etc.
7 = 0.78125% of input sample + 99.21875% of saved average
The maximum useful value of this field is 7.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated the first time a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 18. A high threshold IRQ re-arms the low threshold interrupt and vice-versa. The thresholds are programmed using $94-$97. See Figure 18.

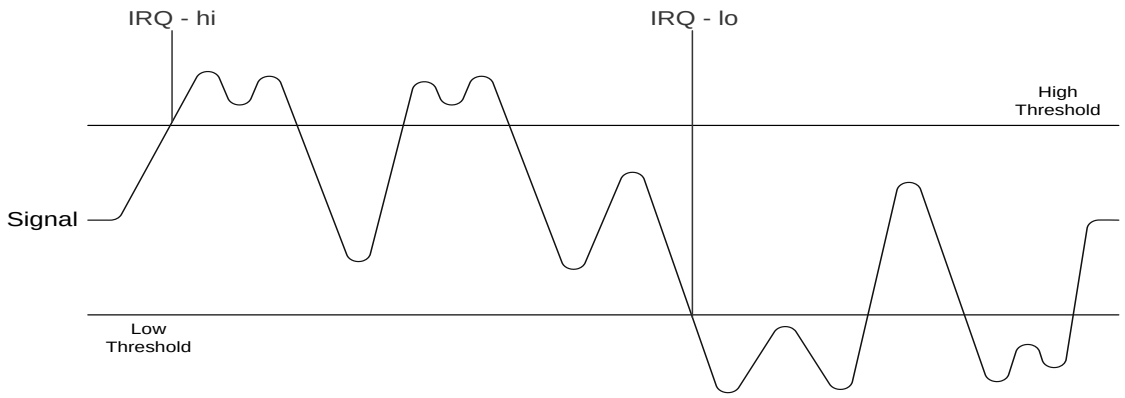


Figure 18 AuxADC IRQ Operation

Auxiliary ADC data is read back in the Aux 1 Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:

- Aux Config - $CD write
- AuxADC1 and 2 Data - $D6 and $D7 read

6.9 Auxiliary DAC/RAMDAC Operation

The three auxiliary DAC channels are programmed via the AuxDAC Data registers, $30 to $33. (Note that AuxDAC channel 1 is allocated to the RAMDAC which will automatically output a pre-programmed profile at a programmed rate under control of the Tx Sequencer. The default profile is a raised cosine (see Table 26, but this may be over-written with a user-defined profile by writing to Programming register P7.0-63. The gain of the profile may be adjusted by writing to the RAMDAC Attenuator ($84) and a fixed offset may be applied using the RAMDAC Offset ($85).

The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. An external R-C network may be required to remove any “step” noise from the output.

The RAMDAC status may be observed by checking the ramp bit (b12) in the AIS/GMSK Modem Status - $C9 read register.

AuxDAC channel 2 may optionally be set to a tone generator mode which may be used for generating simple tones or beeps for user feedback.

The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Updating an AuxDAC is performed by writing to the relevant AuxDAC register ($30-$33), however care should be taken to ensure that the AuxDAC is not currently in use by other functions (e.g RAMDAC, tone gen) as access will not be possible until the function is disabled. Any writes during this time will be discarded. On disabling RAMDAC or tone generator mode the previous enable state and level will be automatically restored by the AuxDAC.

See:

- Aux Function Control - $A8 write.
- AuxDAC1-4 Data - $30 to $33 write

6.10 Digital System Clock Generators

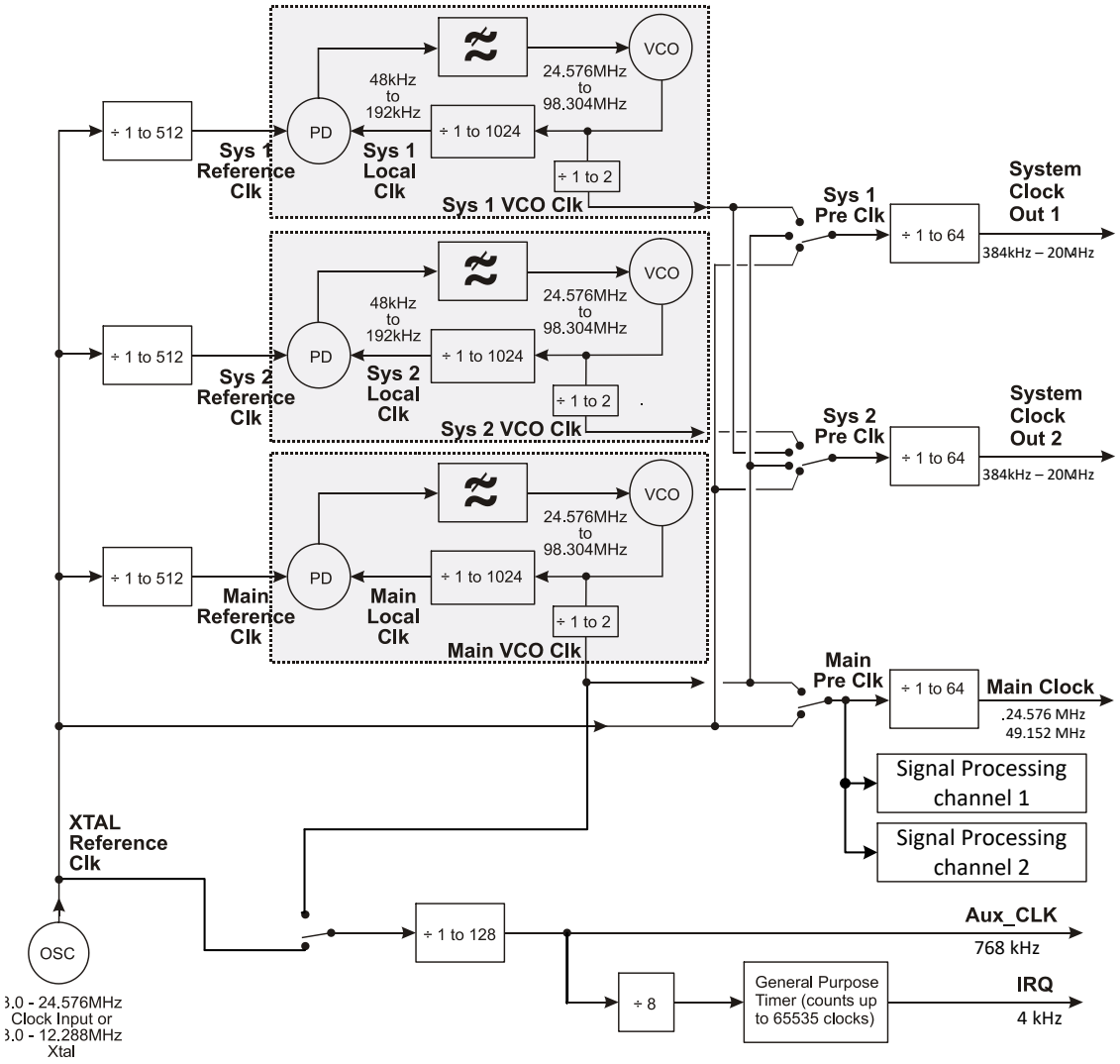


Figure 19 Digital Clock Generation Schemes

The CMX7341 includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in Section 4.1 or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 19.2MHz oscillator is assumed by default for the functionality provided in the CMX7341.

6.10.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz in Tx, 49.152MHz in Rx) for the internal sections of the CMX7341. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose (GP) Timer and the signal

processing block. In particular, it should be noted that in Idle mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX7341 defaults to the settings appropriate for a 19.2MHz oscillator, however if other frequencies are to be used then the Program Block registers P3.13 to P3.21 will need to be programmed appropriately at power-on. This flexibility allows the device to re-use an external clock source, so reducing total cost and potential noise sources. A table of common values is provided in Table 6.

See:

- Block 3: Tx Sequencer and Clock Settings
- System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96 kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 19. Note that at power-on, SYSCLK1 will be active, directly coupled to the XTALIN signal..

See:

- SYSCLK 1 and SYSCLK 2 PLL Data - $AB, $AD write
- SYSCLK 1 and SYSCLK 2 REF - $AC, $AE write.

6.11 Signal Level Optimisation

The internal signal processing of the CMX7341 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3 V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts pk-pk = 838 mV rms, assuming a sine wave signal. This should not be exceeded at any stage.

6.11.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0 dB, The MOD1 and MOD2 Fine Level Control ($80[1]) has a maximum attenuation of 1.8 dB and no gain, whereas the Analogue Output Gain ($B0) has a variable attenuation of up to +40.0 dB and no gain.

[1] Note that C-BUS register $80 is an 8-bit register.

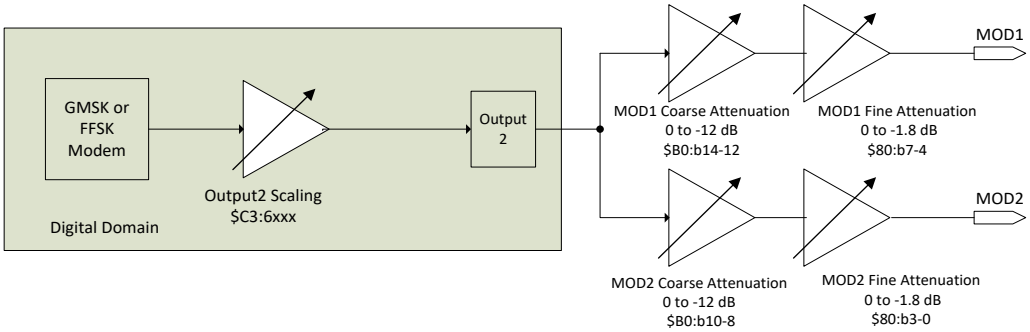


Figure 20 Tx Levels

6.11.2 Receive Path Levels

The Coarse Input adjustment ($B1) has a variable gain of up to +22.4 dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 838 mV rms. This signal level is an absolute maximum, which should not be exceeded.

7 Performance Characteristics

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	−0.3	4.0	V
AV_{DD}- AV_{SS}	−0.3	4.0	V
Voltage on any pin to DV_{SS}	−0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	−0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding BIAS) (i.e. VDEC, AVDD, AVSS, DVDD, DVSS)	−30	+30	mA
Current into or out of any other pin	−20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$V_{DEC} – DV_{SS}$	2	1.70	1.90	V
Operating Temperature		–40	+85	°C
XTAL/CLK Frequency (using an Xtal)	1	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	1	3.0	24.576	MHz

Notes: 1 Figures here represent the capability of the device. For use with this FI, however, an external CLK of 19.2MHz is required.

2 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2 and Figure 3. Maximum load on digital outputs = 30pF.

Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = −40°C to +85°C

$AV_{DD} = DV_{DD}$ = 3.0V to 3.6V

V_{DEC} = 1.8V

Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V

Signal levels track with supply voltage, so scale accordingly

Signal to Noise Ratio (SNR) in bit rate bandwidth

Input stage gain = 0dB. Output stage attenuation = 0dB

Current consumption figures quoted in this section apply to the device when loaded with 7341FI-6.x only. The use of other CMX7341 Function Images can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Idle Mode	22				
DI_{DD}		–	3.3	–	mA
AI_{DD}	23	–	0.1	–	mA
Rx Mode (I/Q Mode)	22				
DI_{DD} DSC – search for FS		–	13.2	–	mA
DI_{DD} DSC – FS found		–	13.2	–	mA
AI_{DD}		–	18.4	–	mA
Tx Mode	22				
DI_{DD} DSC – two-point		–	7.6	–	mA
DI_{DD} AIS – two point		–	8.9	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	12.9	–	mA
Additional Current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 1.8V)		–	250	–	µA
Additional Current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 1.8V)		–	50	–	µA
Additional Current for each Auxiliary DAC					

AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes:

21 T_{AMB} = 25°C: not including any current drawn from the device pins by external circuitry.

22 System Clocks: auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.

23 May be further reduced by power-saving unused sections

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input	24				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		−40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)		−1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = -5mA)		–	–	10%	DV_{DD}
'Off' State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		−1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		−1.0	–	+1.0	µA
V_{BIAS}	25				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:

24 Characteristics when driving the XTAL/CLK pin with an external clock source.

25 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters			Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input							
'High' Pulse Width			31	15	–	–	ns
'Low' Pulse Width			31	15	–	–	ns
Input Impedance (at 6.144MHz)							
	Powered-up	Resistance		–	150	–	kΩ
		Capacitance		–	20	–	pF
	Powered-down	Resistance		–	300	–	kΩ
		Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)				–	20	–	ms
System Clk 1/2 Outputs							
XTAL/CLK input to CLOCK_OUT timing:							
	(in high to out high)		32	–	15	–	ns
	(in low to out low)		32	–	15	–	ns
'High' Pulse Width			33	76	81.38	87	ns
'Low' Pulse Width			33	76	81.38	87	ns
V_{BIAS}							
Start-up Time (from powersave)				–	30	–	ms
Microphone, Alternate and Discriminator Inputs (MIC, ALT, DISC)							
Input Impedance			34	–	>10	–	MΩ
Maximum Input Level (pk-pk)			35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)				80	–	–	kΩ
Amplifier Open Loop Voltage Gain		⎫					
(I/P = 1mVrms at 100Hz)		⎭		–	80	–	dB
Unity Gain Bandwidth				–	1.0	–	MHz
Programmable Input Gain Stage			36				
Gain (at 0dB)			37	−0.5	0	+0.5	dB
Cumulative Gain Error		⎫					
(wrt attenuation at 0dB)		⎭	37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz XTAL fitted and 6.144MHz output selected (scale for 19.2MHz).

34 With no external components connected, measured at DC.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB.

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD 1, MOD 2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error ⎫ (wrt attenuation at 0dB) ⎭		−0.6	0	+0.6	dB
Output Impedance ⎫ Enabled	42	–	600	–	Ω
⎭ Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error ⎫ (wrt attenuation at 0dB) ⎭		−1.0	0	+1.0	dB
Output Impedance ⎫ Enabled	42	–	600	–	Ω
⎭ Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Zero Error	55	0	–	TBA	mV
Integral Non-linearity		–	–	TBA	LSBs
Differential Non-linearity	53	–	–	TBA	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error	56	0	–	TBA	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	TBA	LSBs
Differential Non-linearity	53	–	–	TBA	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

55 Input offset from a nominal V_{BIAS} input, which produces a $0200 ADC output.

56 Output offset from a $0200 DAC input, measured with respect to nominal V_{BIAS} output.

57 Measured at dc.

7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2. Maximum load on digital outputs = 30pF.

Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = −40°C to +85°C.

AV_{DD} = DV_{DD} = 3.0V to 3.6V. Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.

Signal levels track with supply voltage, so scale accordingly.

Signal-to-Noise Ratio (SNR) in bit rate bandwidth.

Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI-6.x only. The use of other CMX7341 Function Images can modify the parametric performance of the device.

AIS/GMSK **Modem**	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
Modem Symbol Rate		–	9600	–	symbols /s
Modulation			GMSK		
Filter (RC) Alpha		–	0.4	–	
Tx Output Level (MOD1, MOD2, two-point)	60	–	2.88	–	Vpk-pk
Tx Adjacent Channel Power (MOD1, MOD2, prbs)	61	-60	–	–	dB

Notes:

60 Transmitting continuous default preamble.

61 See user manual section 6.11.

62 Measured at baseband – radio design will affect ultimate product performance.

DSC/FFSK Modem	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
Modem Symbol Rate		–	1200	–	symbols/s
Logic 1 frequency		1298	1300	1302	Hz
Logic 0 frequency		2098	2100	2102	Hz
3rd Harmonic Distortion		–	–	3	%
Pre-emphasis		-	6	-	dB/octave
Rx Co-channel Rejection	70	-	8	–	dB
Bit Error Rate (SNR = 20dB)	73	–	<1	–	10^{-4}

Notes:

70 Transmitting continuous default preamble.

73 Combined performance of CMX7341 and CMX994 connected as shown in Figure 6.

7.2 C-BUS Timing

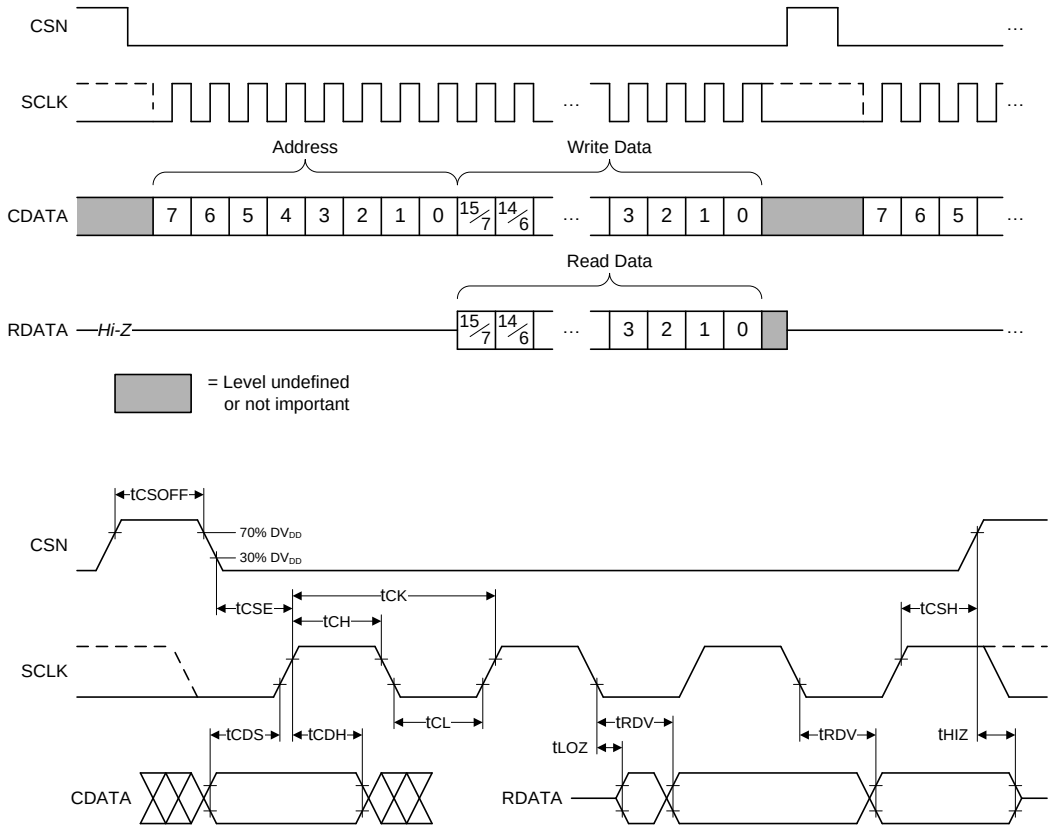


Figure 21 C-BUS Timing

AC Parameters		Notes	Min.	Typ.	Max.	Unit
C-BUS Timing						
Input pin rise/fall time (10% - 90% of DV_{DD})			–	–	3	ns
Capacitive load on RDATA and IRQN			–	–	30	pF
t_{CSE}	CSN enable to SCLK high time		40	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		40	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable time		0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	30	ns
t_{CSOFF}	CSN high time between transactions		40	–	–	ns
t_{CK}	SCLK cycle time		100	–	–	ns
t_{CH}	SCLK high time		40	–	–	ns
t_{CL}	SCLK low time		40	–	–	ns
t_{CDS}	CDATA setup time		25	–	–	ns

t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDV}	SCLK low to RDATA valid time		0	–	35	ns

Notes: 1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.

2. Data is clocked into the peripheral on the rising SCLK edge.

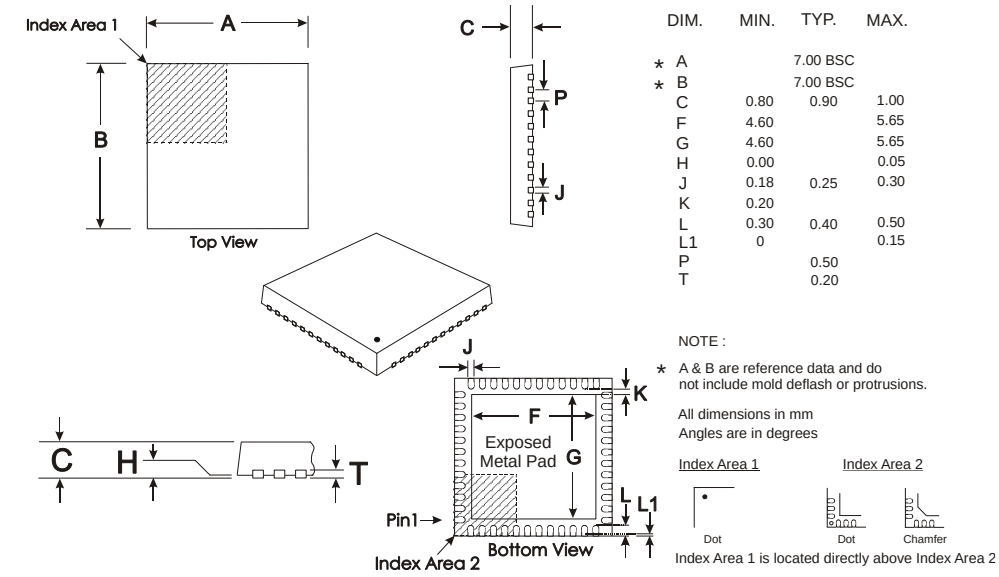
3. Commands are acted upon at the end of each command (rising edge of CSN).

4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.

5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than earlier C-BUS timing specification. The CMX7341 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 22 Mechanical Outline of 48-lead VQFN (Q3)

Order as part no. CMX7341Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

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