

GENERAL DESCRIPTION

The CMT4953G provide the designer with the best combination of fast switching , ruggedized device design , low on-resistance and cost-effectiveness.

The SOP-8 package is universally preferred for all commercial-industrial mount applications and suited for low voltage applications such as DC/DC converters.

FEATURES

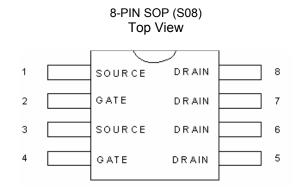
- Advanced Trench Process Technology
- ♦ High Density Cell Design For Ultra Low On-Resistance
- ♦ Fully Characterized Avalanche Voltage and Current
- Improved Shoot-Through FOM
- ♦ SO-8 Package Design

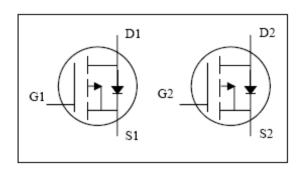
SYMBOL

APPLICATIONS

- Power Management in Notebook
- Portable Equipment
- Battery Powered System
- ♦ DC/DC Converter
- ◆ Load Switch
- ♦ DSC
- ♦ LCD Display inverter

PIN CONFIGURATION





P-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT4953G	SOP-8

*Note: G : Suffix for Pb Free Product



ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Drain- Source Voltage		V _{DS}	-30	V
Gate- Source Voltage		V _{GS}	±20	V
Continuous Drain Current ¹	T _A =25℃	ΙD	-4.5	А
Pulsed Drain Current ²		I _{DM}	-23	Α
Total Power Dissipation ¹	T _A =25℃	P _D	2	W
Operating Junction Temperature Range		TJ	-55 to150	$^{\circ}\!\mathbb{C}$
Storage Temperature Range		T _{STG}	-55 to 150	$^{\circ}\!\mathbb{C}$
Linear Derating Factor			0.02	°C/W
Thermal Resistance Junction-ambient ¹ (Max)		Rthj-amb	62.5	°C/W



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = $25\,^{\circ}\mathrm{C}_{\cdot}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V_{GS} =0V, I_D =-250uA	-30	-	-	V
2	V _{GS} =-10V, I _D =-4.6A	1	1	55	mΩ	
$R_{DS(ON)}$	Static Drain-Source On-Resistancem ²	V _{GS} =-4.5V, I _D =-3.6A	-	-	90	mΩ
V _{GS(th)}	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_{D}=-250uA$	-1	-	-2.5	V
9fs	Forward Transconductance ²	V_{DS} =-5V, I_{D} =-4.6A	-	5	-	S
I _{DSS}	Drain-Source Leakage Current (Tj=25 C)	V_{DS} =-24V, V_{GS} =0V	-	-	-1	uA
I_{GSS}	Gate-Source Leakage Current	V _{GS} =±20V	-	-	±100	nA
Qg	Total Gate Charge ²	I _D =-4.6A	-	11.7	-	nC
Q_{gs}	Gate-Source Charge	V _{DS} =-15V	-	2.1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-10V	-	2.9	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-15V	-	9	-	ns
t _r	Rise Time	I _D =-1A	-	10	-	ns
t _{d(off)}	Turn-off Delay Time	$R_G=6\Omega$, $V_{GS}=-10V$	-	37	-	ns
t _f	Fall Time	$R_D=15\Omega$	-	23	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	582	-	pF
C _{oss}	Output Capacitance	V _{DS} =-15V	-	125	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	86	_	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Units
V_{SD}	Forward On Voltage ²	I _S =-1.7A, V _{GS} =0V	ı	-0.84	-1.2	V

Notes:

1.Surface mounted on FR4 Board , $t \le 2\%$

2. Pulse width \leq 300us, duty cycle \leq 2%.



TYPICAL CHARACTERISTICS

Characteristics Curve 125°C 20 20 Ib, Drain Current (A) Ib, Drain Current (A) 25℃ 15 15 10 10 VGS 5 5 .5V 0 0 O 0.8 2,4 4.0 4.8 O. 8 10 12 -Viss, Gate-to-Source Voltage (V) -Vos, Orain-to-Source Voltage (V) Fig 1. Typical Output Characteristics Fig 2, Transfer Characteristics 10 1.8 R05(04), On-Resistance(Ohms) (Normalized) V dS = + 10 V grs, Transconductance (S) 1.6 B 1.4 б 1.2 1.0 2 0.8 15V Vos: Ō 0.6 50 D. Tj, Junction Temperature (°C) -los, Drain-5 ource Current (A) Fig 3. Transconductance v.s. Fig 4. On-Resistance v.s. Drain Current Junction Temperature Drain-Source Breakdown Voltage 1.15 20.0 lo=-250uA Vas÷0Ÿ 01.1 4s, Source-drain current (A) 10.0 1.05 1.00 0.95 0.901.0 0.85 1.3 0.4 -50 -25 25 50 **75** 100 125 -Vsp, Body Diode Forward Voltage (V)

Tj, Junction Temperature ("C)
Fig 5. Breakdown Voltage
v.s. Junction Temperature

Fig 6. Body Diode Forward Voltage v.s. Source Current

BVDSS, Normalized



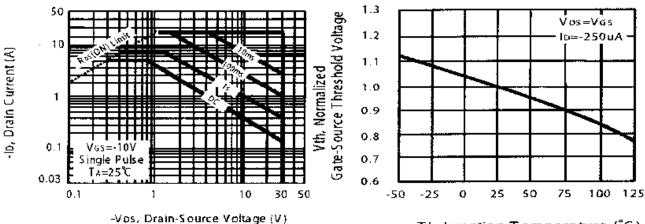


Fig 7. Maximum Safe Operating Area

(A) algorithms of the control of the

Fig 9. Gate Charge Characteristics

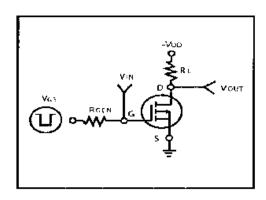


Fig 11. Switching Time Circuit

Tj. Junction Temperature (°C)
Fig 8. Gate Threshold Voltage
v.s. Junction Temperature

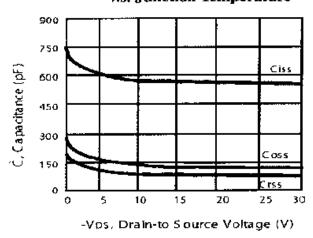


Fig 10. Typical Capacitance Characteristics

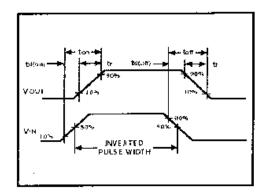


Fig 12. Switching Time Waveform



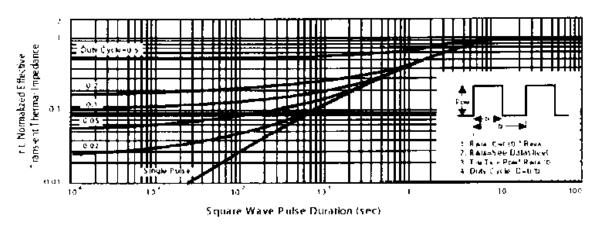
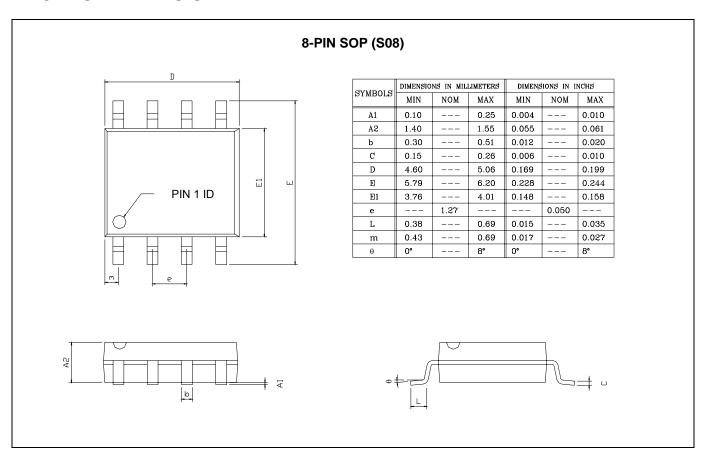


Fig 13. Normalized Thermal Transient Impedance Curve

PACKAGE DIMENSION





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