CMS66P01/02/47/22/23

8-Bit OTP MCU

Data Sheet

CMS66P01/02/47/22/23

The Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial version	18/11/2007
1.1	Modify spelling err	18/03/2008
1.2		

1. CMS66 Product Family

CMS's CMS66 family of 8-bit OTP-based microcontrollers. It uses a fully static CMOS design technology combines higher speeds with the low power and high noise immunity. On chip memory system includes 1.0K bytes of OTP ROM, and 67bytes of static RAM

2. Description

☐ On chip ROM size : 1K x14bits for CMS66P01/02/47/22/23
☐ Internal RAM size : 67 x 8 bits for CMS66P01/02/47/22/23
☐ 46 single word instructions
☐ 2-level stacks
☐ Stop Mode Wakeup when a high to low change in any pin of P0
☐ P0/P1/P2 ports Pull-up Resistor can chosed by register
☐ 8Bit x 3 channels (66P01) ADC
8Bit x 4 channels (66P02/47) ADC
8Bit x 8 channels (66P22/23) ADC
☐ 1Comparators with + input can connected to GND (66P01)
2 Comparators with + input can connected to GND(66P02/47/22/23)
☐ Operating voltage
LV XT MODE(455K): 2.1~3.6V
XT MODE(4M): 2.5 ~ 5.5V
RC MODE: 2.1 ~ 5.5 V
Internal RC: 2.5~5.5V
☐ Operating frequency
5V : 0 ~ 10 MHz
2.1V : 0 ~ 2 MHz
☐ The most fast execution time is 400ns under 10 MHz in all single cycle instructions except the branch instruction
☐ Low Votage detector Reset (LVR)
☐ Stop Mode for power saving(WDT always run and the power current less than 3uA@3V)
☐ 8-bit real time clock/counter(RTCC) with 8-bit programmable prescaler
☐ 4 types of oscillator can be selected by programming OTP ROM:
RC Low cost RC oscillator
INTRC Internal R and C oscillator
XT Standard crystal oscillator

LVXT Low voltage crystal oscillator

☐ 3 oscillator start-up time can be selected by programming OTP ROM(@VCC = 5V) :

560μs, 2.2ms, 9 ms

☐ On-chip RC oscillator based Watchdog Timer(WDT) always run

☐ All pins with their own independent direction control

5 I/O + 1 Input for CMS66P01

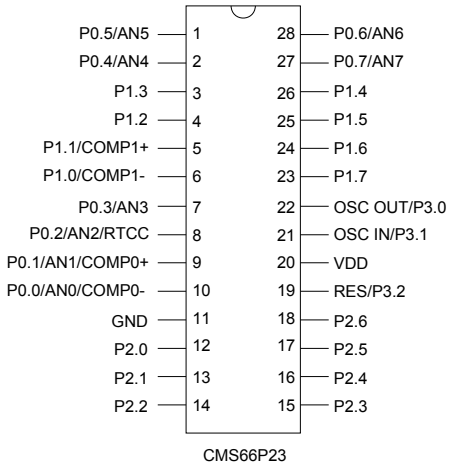
13I/O + 1 Input for CMS66P02

15 I/O + 1 Input for CMS66P47

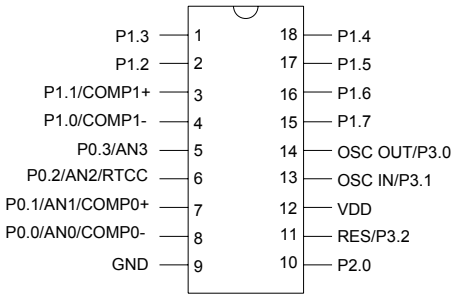
21 I/O + 1 Input for CMS66P22

25 I/O + 1 Input for CMS66P23

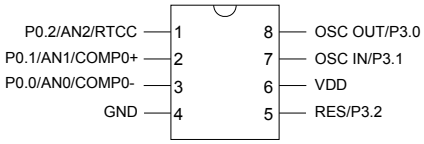
3. Pin Assignment



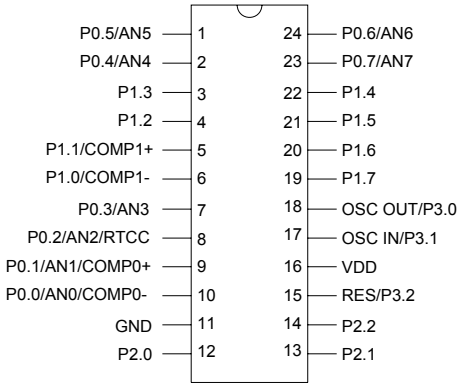
CMS66P23



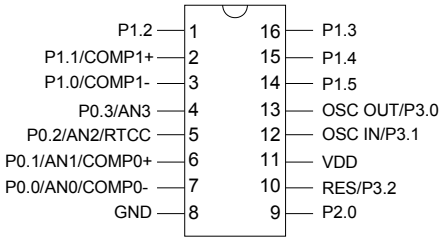
CMS66P47



CMS66P01



CMS66P22



CMS66P02

The PIN Description

Pin Name	Description
P0.0/AN0/COMP0-	Input/Ouput/AN0/Comparator0 - Input
P0.1/AN1/COMP0+	Input/Ouput/AN1/Comparator0 + Input
P0.2/AN2/RTCC	Input/Ouput/AN2
P0.3/AN3	Input/Ouput/AN3
P0.4/AN4	Input/Ouput/AN4
P0.5/AN5	Input/Ouput/AN5
P0.6/AN6	Input/Ouput/AN6
P0.7/AN7	Input/Ouput/AN7
P1.0/COMP1-	Input/Ouput and Comparator1 - Input
P1.1/COMP1+	Input/Ouput and Comparator1 + Input
P1.2	Input/Ouput
P1.3	Input/Ouput
P1.4	Input/Ouput
P1.5	Input/Ouput
P1.6	Input/Ouput
P1.7	Input/Ouput
P2.0	Input/Ouput
P2.1	Input/Ouput
P2.2	Input/Ouput
P2.3	Input/Ouput
P2.4	Input/Ouput
P2.5	Input/Ouput
P2.6	Input/Ouput
OSCOUT/P3.0	OSC Output or Input/Ouput
OSCIN/P3.1	OSC Input or Input/Ouput
RES/P3.2	RESET or Input
VCC	Power supply
GND	Ground

4. Data Memory Map

Address	Name	Descirption	Value on Power-on Reset
00h	IAR	Uses contents of FSR to address data memory (not a physical register)	xxxx xxxx
01h	TMR	Timer0 Module Register	xxxx xxxx
02h	PCL	Low 8 bits of PC	1111 1111
03h	FLAGS	Flags	0001 1xxx
04h	FSR	Indirect data memory address pointer	1xxx xxxx
05h	P0	P0 data register	xxxx xxxx
06h	P1	P1 data register	xxxx xxxx
07h	P2	P2 data register	-xxx xxxx
08h	P3	P3 data register	---- -xxx
09h	ADDATA	ADC data register	xxxx xxxx
0Ah	ADCON	ADC control register	0000 0000
0Bh	ADPORT	ADC channel register	0000 0000
0Ch		General purpose register	xxxx xxxx
0Dh	COMPCON	Comparator and Pullup Resistor Control Resgister	0000 0000
0Eh		General purpose register	xxxx xxxx
0Fh		General purpose register	xxxx xxxx
10~1Fh		General purpose registers	xxxx xxxx
20~2Fh	------	Prohibited Access	----- ----
30~3Fh		General purpose registers	xxxx xxxx
40~4Fh	------	Prohibited Access	----- ----
50~5Fh		General purpose registers	xxxx xxxx
60~6Fh	------	Prohibited Access	----- ----
70~7Fh		General purpose registers	xxxx xxxx

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0' (if applicable).

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the FLAGS Register, the I/O registers (ports) and the File Select

Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler PRESCALEs.

The General Purpose Registers are used for data and control information under command of the instructions.

FLAGS Register

This register contains the arithmetic FLAGS of the ALU, the RESET FLAG.

The FLAGS Register can be the destination for any instruction, as with any other register. If the FLAGS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the FLAGS Register as destination may be different than intended.

For example, `CLR FLAGS` will clear the upper three bits and set the Z bit. This leaves the FLAGS Register as `000u u1uu` (where `u` = unchanged).
It is recommended, therefore, that only `SETB`, `CLRB` and `LD` instructions be used to alter the FLAGS Register because these instructions do not affect the Z, DC or C bits from the FLAGS Register. For other instructions which do affect FLAGS Bits, see the Instruction Set Summary.

FLAGS REGISTER (ADDRESS: 03h)							
Bit7	Bit6	BIT5	BIT4	BIT3	BIT2	BIT1	Bit0
unused	unused	unused	TO	PD	Z	DC	C
-	-	-	R	R	R/W	R/W	R/W

bit 7-5: These bits unused.

TO : Time-out bit

`1` = After power-up, `CLRWDT` instruction, or `STOP` instruction
`0` = A WDT time-out occurred

PD$^-$: Power-down bit

`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `STOP` instruction

Z: Zero bit

`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

DC: Digit carry/borrow bit (for ADDA, ADDR, SUBA and SUBR instructions)

ADDA, ADDR

1 = A carry from the 4th low order bit of the result occurred

0 = A carry from the 4th low order bit of the result did not occur

SUBA, SUBR

1 = A borrow from the 4th low order bit of the result did not occur

0 = A borrow from the 4th low order bit of the result occurred

C: Carry/borrow bit (for ADDA, ADDR, SUBA, SUBR, and RRCA, RRCR, RLCA, RLCR instructions)

PRESCALE Register

The PRESCALE Register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0

By executing the PRESCALE instruction, the contents of the W Register will be transferred to the PRESCALE Register. A RESET sets the PRESCALE<5:0> bits.

PRESCALE REGISTER							
Bit7	Bit6	BIT5	BIT4	BIT3	BIT2	BIT1	Bit0
unused	unused	T0CKI	T0SE	PSA	PS2	PS1	PS0

bit 7-6: **Unimplemented:** Read as '0'

bit 5: **T0CKI**

1 = External P0.2/RTCC pin

0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE:** Timer0 source edge select bit

1 = Increment on high-to-low transition on T0CKI pin

0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA:** Prescaler assignment bit

1 = Prescaler assigned to the WDT

0 = Prescaler assigned to the Timer0

bit 2-0: **PS<2:0>:** Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate

000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1;64	1:32
110	1:128	1:64
111	1:256	1:128

Program Counter(PCL)

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

Instructions where the PCL is the destination, or modify PCL instructions, include LD PCL,A ADDR PCL,A and SETB PCL,5. Those Instructions can't change the Upper bits of PC.

FSR Register

The FSR is a 7-bit (CMS66P06/10/30) wide register. It is used in conjunction with the IAR Register to indirectly address the data memory area.

The FSR<6:0> bits are used to select data memory add resses 00h to 7Fh.

IAR Register

The IAR Register is not a physical register. Addressing IAR actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer).* This is indirect addressing.

EXAMPLE: INDIRECT ADDRESSING

Register file 08 contains the value 10h
Register file 09 contains the value 0Ah
Load the value 08 into the FSR Register
A read of the IAR Register will return the value of 10h
Increment the value of the FSR Register by one (FSR = 09h)
A read of the IAR register now will return the value of 0Ah.

Reading IAR itself indirectly (FSR = 0) will produce 00h. Writing to the IAR Register indirectly results in a no-operation (although FLAGS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 6-2.

EXAMPLE HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
    LDIA    H'0F'       ;initialize pointer
    LD      FSR,A       ;to RAM
LOOP：
    INCR    FSR
    SETB    FSR, 4      ;When Bit4=0   (FSR>0Fh) The Register is not definite
    CLR     IAR         ;clear IAR Register
    SZINCA  FSR
    JP      LOOP        ;NO, clear next CONTINUE
EXIT：
    ◦◦◦◦
```

P0,P1,P2,P3

As with any other register, the I/O Registers can be written and read under program control. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (WRSR P0, WRSR P1, WRSR P2) are all set.

P0 is an 8-bit I/O Register (P0<7:0>).

B7	B6	B5	B4	B3	B2	B1	B0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

P1 is an 8-bit I/O Register (P1<7:0>).

B7	B6	B5	B4	B3	B2	B1	B0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

P2 is an 7-bit I/O Register (P2<6:0>).

B7	B6	B5	B4	B3	B2	B1	B0
Always 0	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

P3 is an 3-bit I/O Register (P3<2:0>).

.7	.6	.5	.4	.3	.2	.1	.0
Always 0					RES/P3.2	OSCIN/P3.1	OSCOUT/P3.0

.2
When LVR Enable (OTP Program). This pin can be used as input port P3.2 Otherwise this pin is a reset pin.

.1 and .0
When Oscillator selected as INTRC(OTP Program), These two pins can be used as input or output, the direction can be operated by instruction WRSR P3.

Example:
```
LDIA    01h
WRSR    P3      ;then P3.0 is input and P3.1 is output
```

ADDATA

The A/D converter data register, ADDATA, is located at address 09H.

ADCON

The A/D converter control register, ADCON, is located at address 0AH,ADCON has four functions:

- Bit 0~2 select an analog input pin (AN0~AN7)
- Bit 3~4 select a conversion speed
- Bit 6 the flag of ADC finished(read only)
- Bit 7 starts the AD conversion

Only one analog input channel can be selected at a time. You can dynamically select any one of the 8 analog input pins(AN0~AN7) by manipulating the 4-bit value for ADCON.0~ADCON.2.

Bit2/Bit2/Bit0	=	000	channel selected AN0
		001	channel selected AN1
		010	channel selected AN2
		011	channel selected AN3
		100	channel selected AN4
		101	channel selected AN5
		110	channel selected AN6
		111	channel selected AN7
Bit4/Bit3	=	00	A/D clock is fosc/2
		01	A/D clock is fosc/8

10 A/D clock is fosc/32
11 A/D clock is fosc/64
Bit6 1 to 0 then the A/D begin
Bit7 = 0 A/D converter begin

ADPORT

The ADPORT register, is located at address 0BH. This register define the AN0~AN7 is analog input or normal I/O

A/D port define,B[7:0] decide AN[7:0] is analog input pin or I/O input pin.
0--- normal I/O
1--- analog input

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	P0.7 I/O	P0.6 I/O	P0.5 I/O	P0.4 I/O	P0.3 I/O	P0.2 I/O	P0.1 I/O	P0.0 I/O
1	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

Example:

```
    LDIA    B'00000111'
    LD      ADPORT,A      ;AN0、AN1、AN2 are ADC ports
    LDIA    B'00000001'
    LD      ADCON,A       ;select AN1as ADC input and fadc= fosc/2
    SETB    ADCON,7       ;set ADCON.7
    NOP
    NOP
    NOP
    NOP
    CLRB    ADCON,7       ;1 to 0 on ADCON.7   then ADC begin
WAIT：
    SZB     ADCON,6       ;waiting the ADC over
    JP      WAIT
    LD      A, ADDATA
    LD      USER_DEFINE_RAM, A
    ......
```

COMPCON Register

B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

B[7] ----- no used
B[6] ----- + Input Control bit of Comparator1
0 – the + input of comparator1 connect to GND, P1.1 can be used

as normal I/O
1 – the + input of comparator1 connect to P1.1
B[5] ----- Comparator1 enable control bit
0 –Comparator1 disable, P1.0 and P1.1 can be used as normal I/O
1 –Comparator1 enable, P1.0 used as analog – input
B[4] ----- + Input Control bit of Comparator0
0 – the + input of comparator0 connect to GND, P0.1 can be used as normal I/O
1 – the + input of comparator0 connect to P0.1
B[3] ----- Comparator0 enable control bit
0 –Comparator0 disable, P0.0 and P0.1 can be used as normal I/O
1 –Comparator0 enable, P0.0 used as analog – input
B[2] ----- Pullup Resistor of P2 Control bit
0 –Pullup Resistor of P2 Disable
1 –Pullup Resistor of P2 Enable
B[1] ----- Pullup Resistor of P1 Control bit
0 –Pullup Resistor of P1 Disable
1 –Pullup Resistor of P1 Enable
B[0] ----- Pullup Resistor of P0 Control bit
0 –Pullup Resistor of P0 Disable
1 –Pullup Resistor of P0 Enable

When any port was used as output or analog input, the Pullup Reisstor will be disable.

EXAMPLE:(How to use Comparator 0)

```
        SETB    COMPCON, 3  ;
        SETB    COMPCON, 4  ;Set P0.1 as + input of comparator 0
        NOP                 ;Delay
        NOP
        NOP
        SZB     P0, 0       ;Get the result of comparator 0
        JP      P_LT_N
N_LT_P:
        …
        JP      EXIT
P_LT_N:
        …
EXIT:
        CLRB    COMPCON, 3  ; disable comparator 0
        CLRB    COMPCON, 4
```

WRSR Registers

There have 5 WRSR Registers, Their address are the same with 2H，P0,P1,P2,P3. Those registers can only accessed by instruction WRSR.

The Output Driver Control Registers are loaded with the contents of the Acc by executing the WRSR R instruction. A '1' from a WRSR Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer

Example:

```
LDIA    0FH
WRSR    P0      ;P0.0~P0.3 input and P0.4~P0.7 output
```

5. ROM MAP

CMS66P06/10/30 memory is organized into program memory and data memory. Total OTP memory of CMS66P06/10/30 is 1K bytes.
The RESET vector for the CMS66P06/10/30 is at 3FFh. A NOP at the RESET vector location will cause a restart at location 000h.

6. OSCILLATOR CONFIGURATIONS

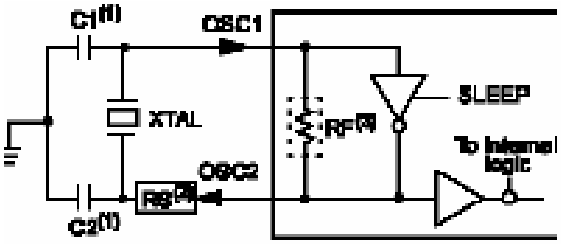
CMS66P06/10/30 can be operated in four different oscillator modes. The user can program OTP ROM to select one of these four modes:

1. EXT RC: External C and R
2. INTRC: Internal C and Internal Resistor
3. XT: High Speed Crystal/Resonator
4. LVXT: Low Speed Crystal/Resonator

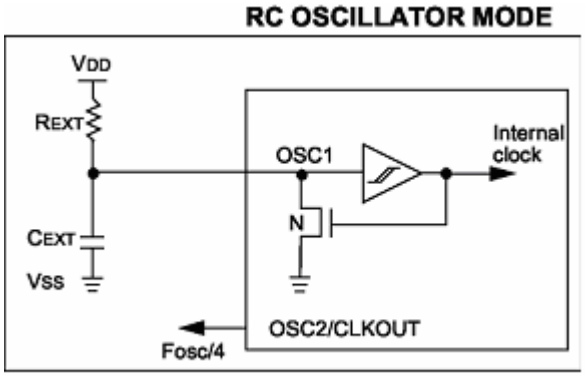
Crystal Oscillator/Ceramic Resonators

In XT, LVXT modes, a crystal or ceramic resonator is connected to the OSCIN/P3.1and OSCOUT/P3.0 pins to establish oscillation. The CMS66P06/10/30 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LVXT modes, the device can have an external clock source drive the OSCIN/P3.1pin.

XT and LV XT Mode



External RC Mode



The oscillator frequency, when in EXT RC, divided by 4, is available on the OSCOUT/p3.0 pin, and can be used for test purposes

7. RESET

CMS66P06/10/30 devices may be RESET in one of the following ways:

Power-On Reset (POR)

Low Voltage Reset (LVR)

MCLR Reset

P0 Wake-up Reset (from STOP)

WDT Reset

The bellow Table shows these RESET conditions for the PCL and FLAGS registers

Table7.1 FLAGS BITS AND THEIR SIGNIFICANCE

Condition	TO	PD
Power-On Reset	1	1
MCLR Reset (normal operation)	u	u
MCLR Wake-up (from STOP)	1	0
WDT Reset (normal operation)	0	1

WDT Wake-up (from STOP)	0	0

Legend: u = unchanged, x = unknown, — = unimplemented read as '0'

Some registers are not affected in any RESET condition. Their FLAGS is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-On Reset (POR), MCLR or WDT Reset. A MCLR or WDT wake-up from STOP also results in a device RESET, and not a continuation of operation before STOP

Table7.2 SUMMARY OF REGISTERS ASSOCIATED WITH RESET

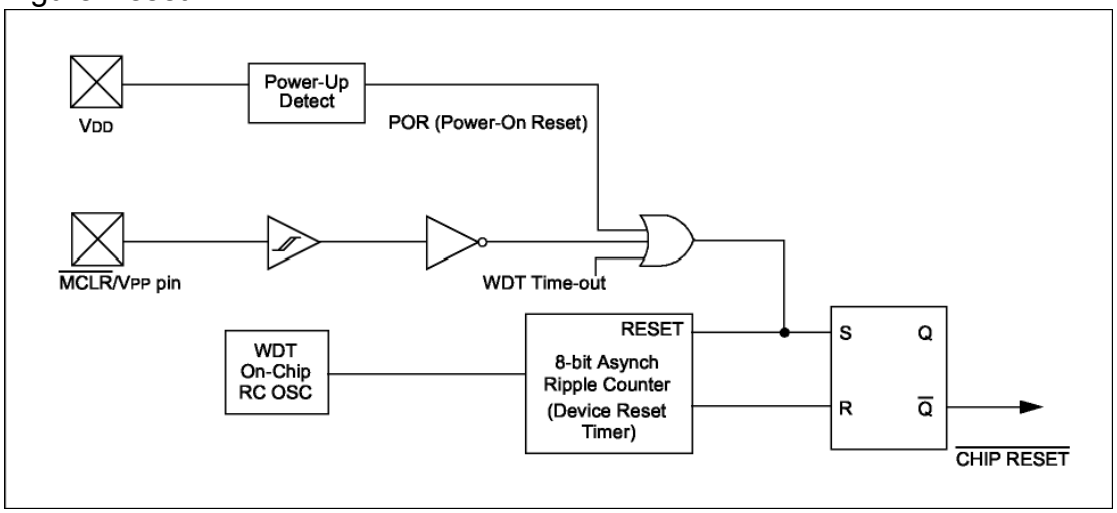
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on MCLR and WDT Reset
03h	FLAGS	--	--	--	TO	PD	Z	DC	C	0001 1xxx	000q quuu

Legend: u = unchanged, x = unknown, q = see Table 7.1 for possible values.

The TO and PD bits (FLAGS <4:3>) are set or cleared depending on the different RESET conditions (Table7.1). These bits may be used to determine the nature of the RESET

The bellow table lists a full description of RESET states of all registers. The following figure shows a simplified block diagram of the On-chip Reset circuit.

Figure Reset Pin



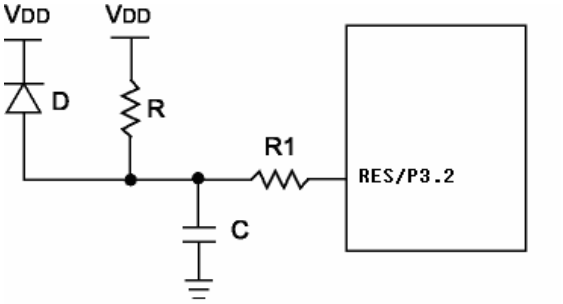
Power-On Reset (POR)

The CMS66P06/10/30 family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the RES/P3.2 pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure Reset Pin.

The Power-On Reset circuit and the Device Reset Timer circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects RES to be high. After the time-out period, which is tyCMSally 560us to 18ms@5V, it will RESET the reset latch and thus end the on-chip RESET signal

Note: When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

The POR circuit does not produce an internal RESET when VDD declines

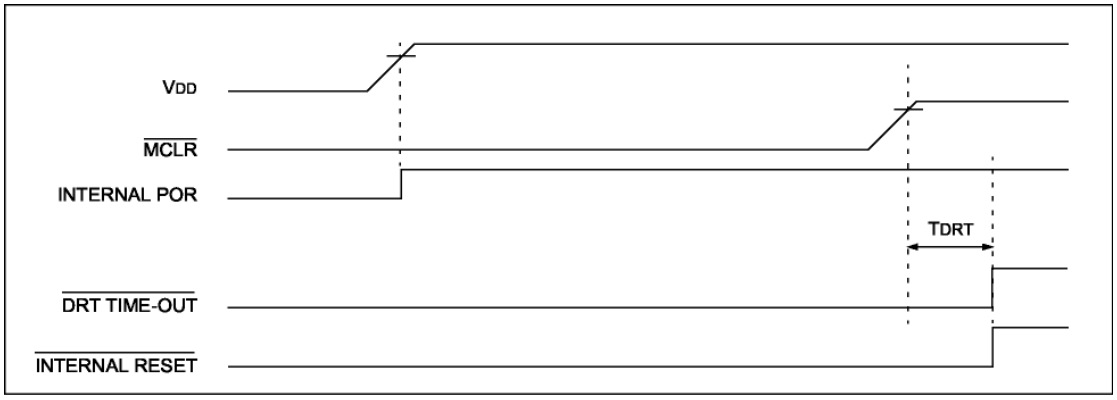


External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

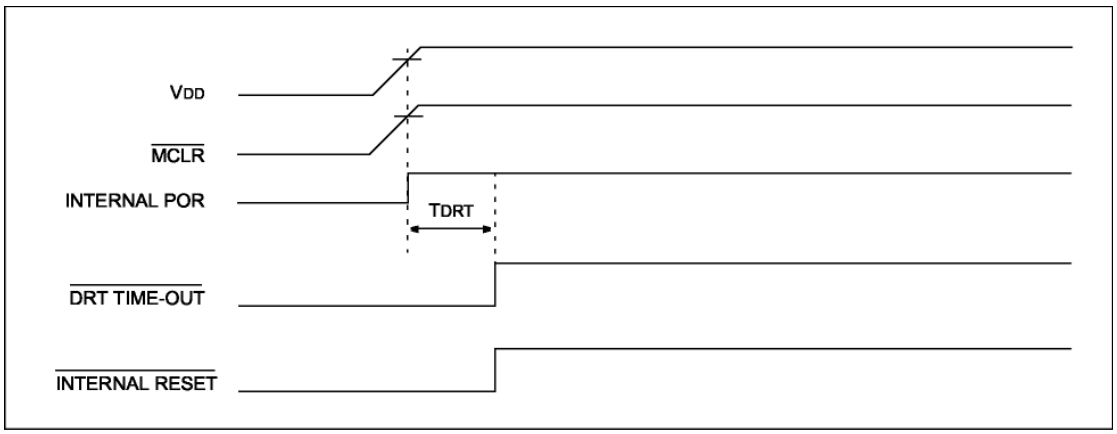
R < 40 k is recommended to make sure that voltage drop across R does not violate the device electrical specification.

R1 = 1 00 to 1 k will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Over-stress (EOS).

TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO



TIME-OUT SEQUENCE ON POWER-UP (RES NOT TIED TO)



Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 560us to 18ms (5V) nominal time-out on RESET regardless of Oscillator mode used.Those timer can be selected by program OTP ROM. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly imP0nt for applications using the WDT to wake the CMS66P06/10/30 from Stop mode automatically.

P0 Wakeup Reset

When the MCU is in STOP mode after excuted a STOP instruction, a high to low change in any pin of P0 will cause a reset of the MCU.

8. INSTRUCTION SET SUMMARY

TABLE 8-2: INSTRUCTION SET SUMMARY

Mnemonic	Description	Cycle	FLAGS Affected
SZB R,b	If R.b = 0 Then Skip	1 or 2	---
SNZB R,b	If R.b = 1 Then Skip	1 or 2	---
SZDECA R	1. [R]-1→Acc 2. If [R]-1= 0 Then Skip	1 or 2	---
SZDECR R	1. [R]-1→R 2. If [R]-1= 0 Then Skip	1 or 2	---
SZINCA R	1. [R]+1→Acc 2. If [R]+1= 0 Then Skip	1 or 2	---
SZINCR R	1. [R]+1→R 2. If [R]+1= 0 Then Skip	1 or 2	---
JP add	Jump	2	---
CALL add	Call	2	---
RET i	Return with i to Acc	2	---
LD A,R	[R] → Acc	1	z
LD R,A	Acc → R	1	---
LDR R	[R] → R	1	z
LDIA i	i → Acc	1	---
ADDA R	[R] + Acc → Acc	1	C,HC,Z
ADDR R	[R] + Acc → R	1	C,HC,Z
SUBA R	[R] – Acc → Acc	1	C,HC,Z
SUBR R	[R] – Acc → R	1	C,HC,Z
INCA R	[R] + 1 → Acc	1	Z
INCR R	[R] + 1 → R	1	Z
DECA R	[R] – 1 → Acc	1	Z
DECR R	[R] – 1 → R	1	Z
ANDA R	[R] and Acc → Acc	1	Z

ANDR R	[R] and Acc → R	1	Z
ORA R	[R] or Acc → Acc	1	Z
ORR R	[R] or Acc → R	1	Z
ORIA i	Acc or i → Acc	1	Z
XORA R	[R] XOR Acc → Acc	1	Z
XORR R	[R] XOR Acc → R	1	Z
XORIA i	i XOR Acc → Acc	1	Z
COMA R	NOT [R] → Acc	1	Z
COMR R	NOT [R] → R	1	Z
RLCA R	Rotate left with acc, the result to Acc But R no change	1	C
RLCR R	Rotate left with acc, the result to R	1	C
RRCA R	Rotate right with acc, the result to Acc But R no change	1	C
RRCR R	Rotate right with acc, the result to R	1	C
SWAPA R	Exchange R.0~R.3 and R.4~R.7 The Result to Acc (R no Change)	1	---
SWAPR R	Exchange R.0~R.3 and R.4~R.7 The Result to R	1	---
CLRB R,b	0 → R.b	1	---
SETB R,b	1 → R.b	1	---
NOP		1	---
STOP		1	TF,PF
CLRWDT	Clear Watchdog Timer	1	TF,PF
PRESCALE	Acc → Prescale Register	1	---
WRSR R	Acc → Special register	1	---
CLRA	0 → Acc	1	Z
CLR R	0 → R	1	Z

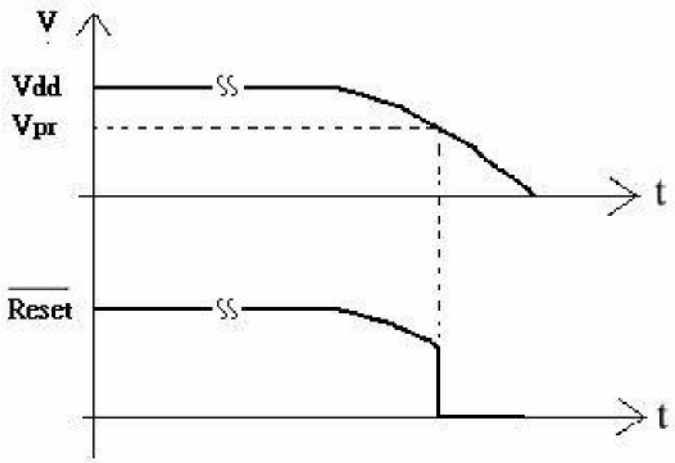
9. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings	
Ambient Temperature under bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on V_{DD} with respect to Gnd	0V to +7.5V
Voltage on RES with respect to GND(1)	0V to +14V
Voltage on all other pins with respect to GND	–0.6V to (V_{DD} + 0.6V
Total power dissipation(2)	800 mW
Max. current out of GND pin	150 mA
Max. current into V_{DD} pin	100 mA
Max. current into an input pin (T0CKI only)	±500 uA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port	40 mA
Max. output current sunk by a single I/O port	50 mA

DC Characteristics:

(A) Low Voltage Detector Reset Voltage)

V_{LVR} 1.6~1.9 V $V_{pr}V_{dd}$ (Power Supply)



(B) The basic WDT time-out cycle time @

Temperature25, the tyCMSal value as followings :

Voltage (V)	Basic WDT time-out cycle time (ms)
3.0	53
4.0	32.8
5.0	24.2

(C) The standby Current@Temperature25(NW= NO WORK)

Voltage (V)	standby Current（uA）
3.0	2.0
4.0	8.0
5.0	17

External Capacitor Selection For Crystal Oscillator

Osc. Type	Resonator Freq.	Vmin	Vmin	Vmin
		C1=C2=33P	C1=C2=47P	C1=C2=101P
LVXT	455KHz	/	1.9V	1.9V
		C1=C2=0P	C1=C2=22P	C1=C2=33P
LVXT	2 MHz	2.0V	2.2V	2.4V
	4 MHz	2.2V	2.3V	2.7V
XT	2MHz	2.4V	2.5V	2.5V
	4 MHz	2.5V	2.5V	2.7V

	6MHz	2.8V	2.9V	3.9V
	8MHZ	3.6V	3.7V	3.9V

A/D converter electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Vdd			2.7		5.5	V
Total accuracy	-	Vdd=5V CPU clock = 4M	-	-	±3	LSB
Integal linearity error	ILE	-	-	-	±2	
Differential linearity error					±1	
Offset error of top				±1	±3	
Offset error of bottom				±1	±2	
Conversion time			Fosc/2		Fosc/64	
Analog input voltage			Vss		Vdd	
Analog input inpedence			2			Mohm
Ananlog input current		Vdd=5V			10	uA
Analog block current	IADC	Vdd=5V				mA
		Vdd=2.7V				mA
		Vdd=5V Power down mode		100	500	nA

The relationship between R/C and Power Voltage:

A). RC Type OSC

@ V_{dd}=5.0 V

The IC may not oscillate properly if the resistance of rext

less than 3.3K. The minimum resistance of rext must be more than 3.3K.

Cext. (F)	Rext. (Ohm)	Frequency (MHz)
C=0P	1.5K	/
	2K	/
	3.3K	/
	4.7K	16
	5.1K	15
	5.6K	14.4
	6.8K	13.6
	8.2K	11.0
	10.0K	9.4
	15K	6.8
C=10P	1.5K	/
	2K	12.4
	3.3K	10
	4.7K	8
	5.1K	7.4
	5.6K	7
	6.8K	6
	8.2K	5.2
	10.0K	4.4
	15K	3
C=22P	1.5K	/
	2K	9
	3.3K	7
	4.7K	5.4
	5.1K	5
	5.6K	4.8
	6.8K	4
	8.2K	3.4
	10.0K	3
	15K	2
C=33P	1.5K	/
	2K	6.4
	3.3K	5
	4.7K	3.8

	5.1K	3.6
	5.6K	3.4
	6.8K	3
	8.2K	2.4
	10.0K	2
	15K	1.43

@ V_{dd}=3.0 V

The IC may not oscillate properly if the resistance of rext less than 4.7K. The minimum resistance of rext must be more than 4.7K.

Cext. (F)	Rext. (Ohm)	Frequency (MHz)
C=0P	1.5K	/
	2K	/
	3.3K	/
	4.7K	/
	5.1K	/
	5.6K	/
	6.8K	/
	8.2K	9.4
	10.0K	8.8
	15K	6.8
C=10P	1.5K	/
	2K	/
	3.3K	/
	4.7K	7.4
	5.1K	7
	5.6K	6.8
	6.8K	6
	8.2K	5.4
	10.0K	4.8
	15K	3.4
C=22P	1.5K	/
	2K	/
	3.3K	6.6
	4.7K	5.6
	5.1K	5.2
	5.6K	5
	6.8K	4.6

	8.2K	4
	10.0K	3.4
	15K	2.4
C=33P	1.5K	/
	2K	/
	3.3K	5
	4.7K	4.2
	5.1K	4
	5.6K	3.8
	6.8K	3.4
	8.2K	3
	10.0K	2.6
	15K	1.8

@ V_{dd} = 2.5V

The IC may not oscillate properly if the resistance of rext less than 8.2K. The minimum resistance of rext must be more than 8.2K.

Cext. (F)	Rext. (Ohm)	Frequency (MHz)
C=0P	1.5K	/
	2K	/
	3.3K	/
	4.7K	/
	5.1K	/
	5.6K	/
	6.8K	/
	8.2K	/
	10.0K	5.4
	15K	5.6
C=10P	1.5K	/
	2K	/
	3.3K	/
	4.7K	5.4
	5.1K	5.3
	5.6K	5.24
	6.8K	4.9

	8.2K	4.4
	10.0K	4
	15K	3.12
C=22P	1.5K	/
	2K	/
	3.3K	/
	4.7K	5.4
	5.1K	4.26
	5.6K	4.2
	6.8K	3.8
	8.2K	3.44
	10.0K	3.06
	15K	2.3
C=33P	1.5K	/
	2K	/
	3.3K	3.7
	4.7K	3.48
	5.1K	3.36
	5.6K	3.3
	6.8K	3
	8.2K	2.68
	10.0K	2.34
	15K	1.78

b). INTRC OSC (Internal C and R)

F=3.5MHZ

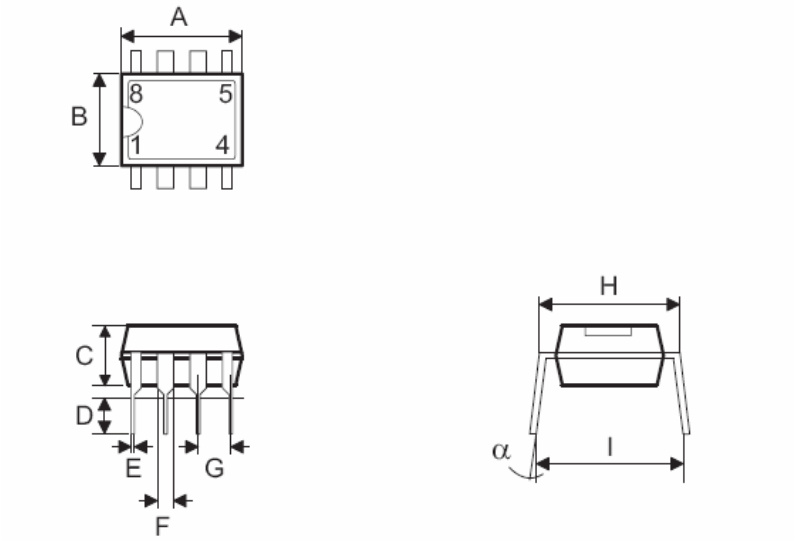
2.2v	2.3v	2.4v	2.5v	2.6v	2.8v	3.0v	3.5v	4.0v	5v	5.5v
NW	NW	3.36	3.52	3.58	3.53	3.47	3.50	3.49	3.39	3.34

NW: Not WORK

10.Package Information

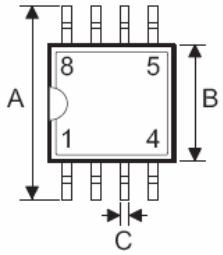
The CMS66P01 is available in a 8-pin DIP package, a 8-pin SOP package. Package dimensions are shown bellow.

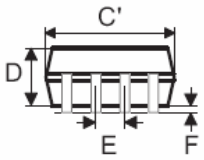
8-Pin DIP

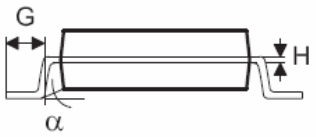


Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	355	—	375
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	335	—	375
α	0°	—	15°

8-Pin SOP





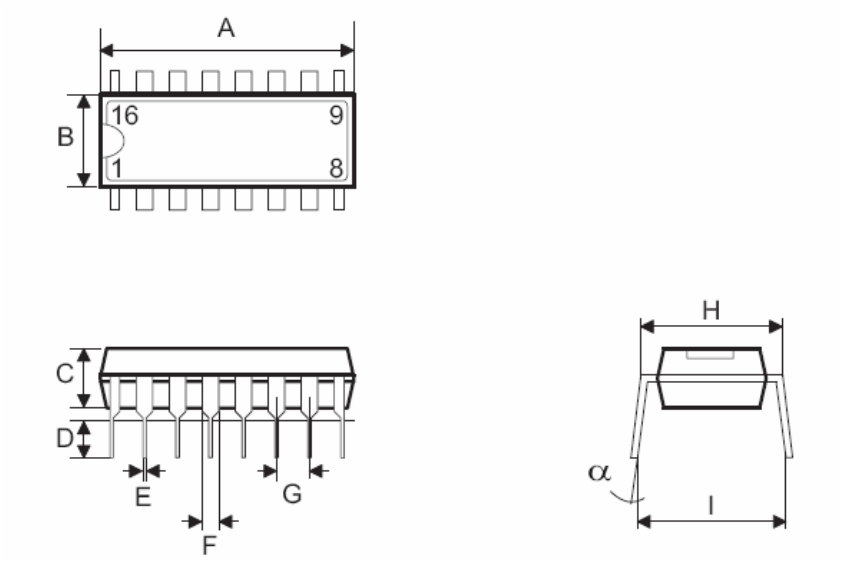


Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	149	—	157
C	14	—	20
C′	189	—	197
D	53	—	69
E	—	50	—
F	4	—	10
G	22	—	28
H	4	—	12
α	0°	—	10°

The CMS66P02 is available in a 16-pin DIP package, a 16-pin SOP

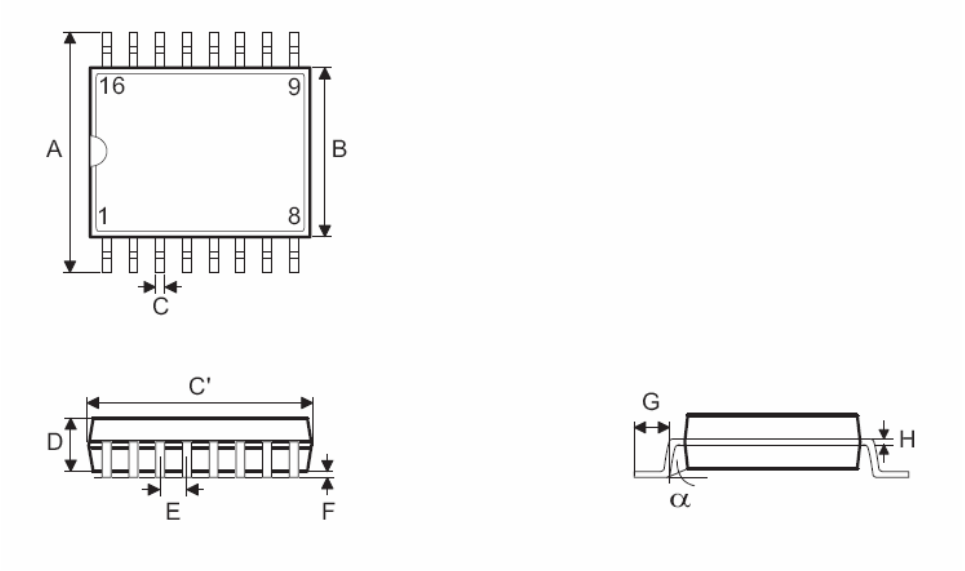
package. Package dimensions are shown bellow.

16-Pin DIP



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	745	—	775
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	335	—	375
α	0°	—	15°

16-Pin SOP

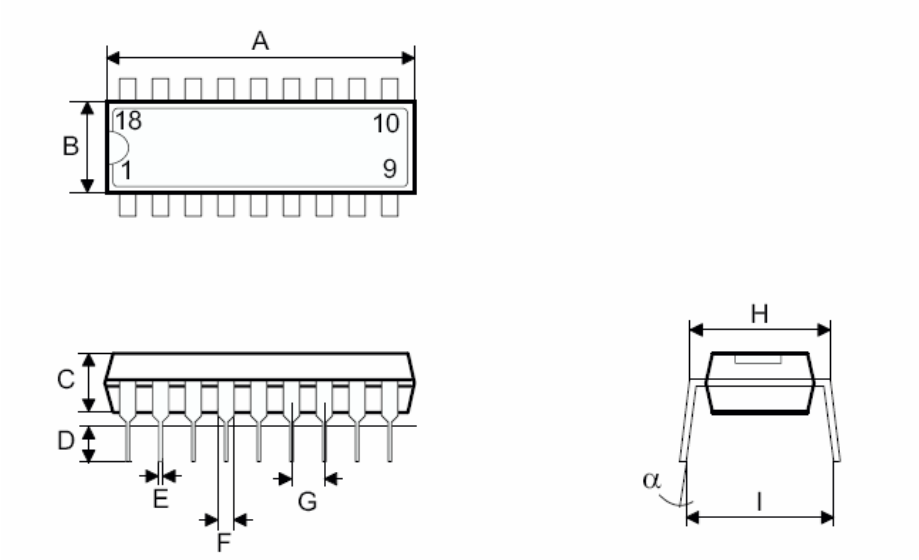


Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	228	—	244
B	150	—	157
C	8	—	12
C'	189	—	197
D	54	—	60
E	—	25	—
F	4	—	10
G	22	—	28
H	7	—	10
α	0°	—	8°

The CMS66P47 is available in a 18-pin DIP package, a 18-pin SOP

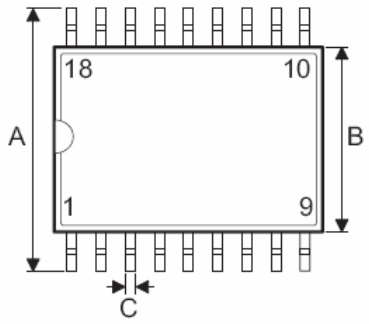
package. Package dimensions are shown bellow.

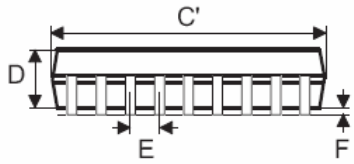
18-Pin DIP

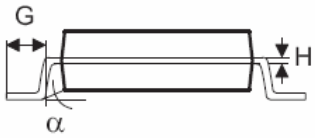


Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	895	—	915
B	240	—	260
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	335	—	375
α	0°	—	15°

18-Pin SOP



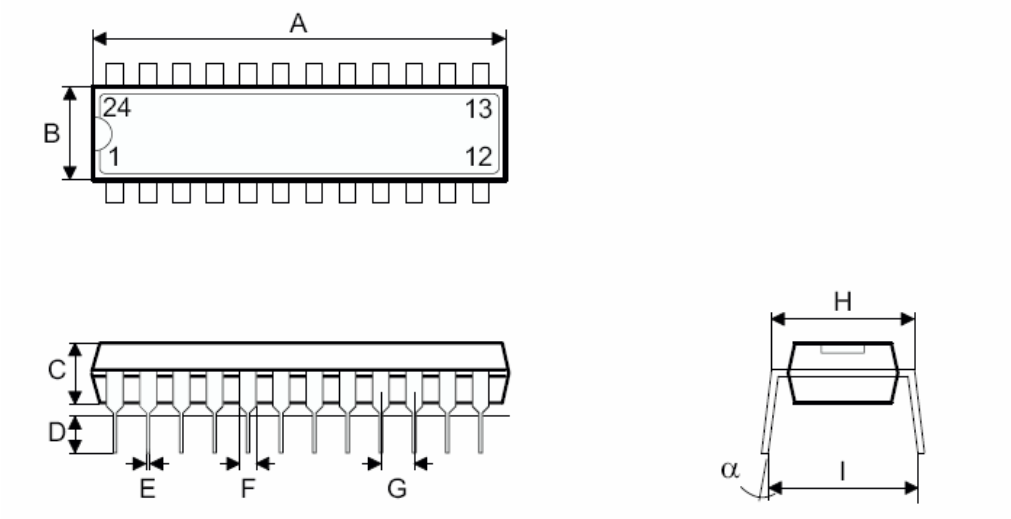




Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	394	—	419
B	290	—	300
C	14	—	20
C'	447	—	460
D	92	—	104
E	—	50	—
F	4	—	—
G	32	—	38
H	4	—	12
α	0°	—	10°

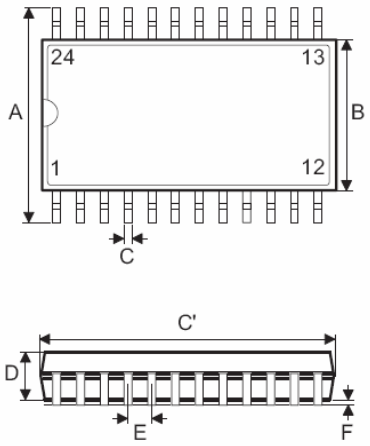
The CMS66P22 is available in a 24-Pin SKDIP package, a 24-Pin SOP package. Package dimensions are shown bellow.

24-Pin SDIP



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1235	—	1265
B	255	—	265
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	345	—	360
α	0°	—	15°

24-Pin SOP

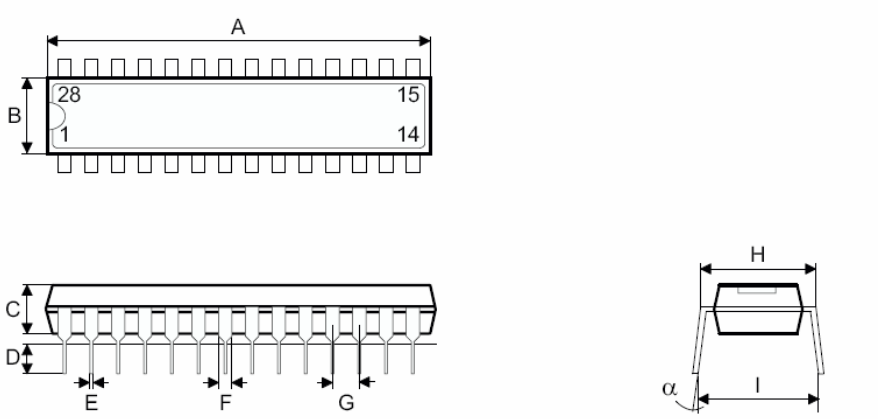


Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	394	—	419
B	290	—	300
C	14	—	20
C'	590	—	614
D	92	—	104
E	—	50	—
F	4	—	—
G	32	—	38
H	4	—	12
α	0°	—	10°

The CMS66P23 is available in a 28-pin SKDIP package, a 28-pin SOP

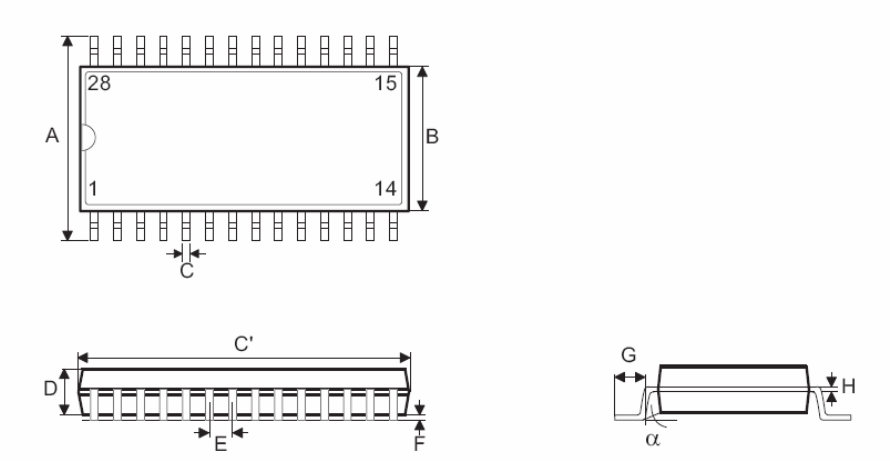
package. Package dimensions are shown bellow.

28-pin SDIP



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1375	—	1395
B	278	—	298
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	330	—	375
α	0°	—	15°

28-pin SOP



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	394	—	419
B	290	—	300
C	14	—	20
C′	697	—	713
D	92	—	104
E	—	50	—
F	4	—	—
G	32	—	38
H	4	—	12
α	0°	—	10°

11.Company Information

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