

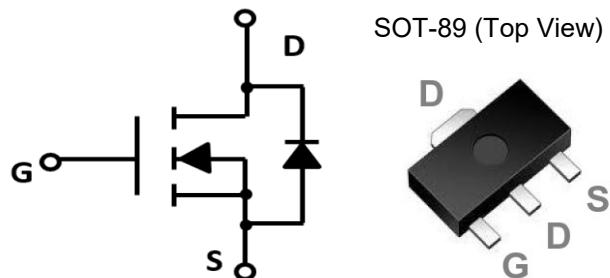
## Description

CMN4012S9 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

## Features

- V<sub>DS</sub>: 40V
- I<sub>D</sub>: 23.6A
- R<sub>DS(on)</sub> (@V<sub>GS</sub>=10V) : < 15mΩ
- R<sub>DS(on)</sub> (@V<sub>GS</sub>=4.5V) : < 23mΩ
- High density cell design for extremely low R<sub>DS(on)</sub>
- Excellent on-resistance and DC current capability

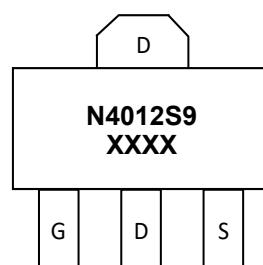
## Equivalent Circuit and Pin Configuration



## Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

## Marking Information



Device Code = N4012S9  
Date Code = XXXX

## Ordering Information

Part Number	Packaging	Reel Size
CMN4012S9	1000/Tape & Reel	7 inch

## Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V <sub>DS</sub>	40	V
Gate-source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current <sup>(1)(6)</sup>	T <sub>C</sub> =25°C	23.6	A
	T <sub>C</sub> =70°C	19	
	TA=25°C	9	
	TA=70°C	7	
Pulsed Drain Current <sup>(3)</sup>	I <sub>DM</sub>	36	A
Total Power Dissipation @ T <sub>C</sub> =25°C <sup>(4)</sup>	P <sub>D</sub>	12.5	W
Total Power Dissipation @ TA=25°C <sup>(4)</sup>		1.8	
Thermal Resistance Junction-to-Ambient <sup>(2)(5)</sup>	R <sub>θJA</sub>	70	°C/W
Thermal Resistance Junction-to-Case	R <sub>θJC</sub>	10	°C/W
Junction and Storage Temperature Range	T <sub>J,TSTG</sub>	-55 to +150	°C

**Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BVDSS	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>D</sub> =40V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>D</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>D</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2		2.5	V
Static Drain-Source on-Resistance	R <sub>D(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A		13	15	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		15	23	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =10A, V <sub>GS</sub> =0V			1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				10	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>D</sub> =20V, V <sub>GS</sub> =0V, f=1MHz		750		pF
Output Capacitance	C <sub>oss</sub>			150		
Reverse Transfer Capacitance	C <sub>rss</sub>			80		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>D</sub> =20V, I <sub>D</sub> =10A		15		nC
Gate Source Charge	Q <sub>gs</sub>			3		
Gate Drain Charge	Q <sub>gd</sub>			2.5		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>D</sub> =20V, I <sub>D</sub> =2A, R <sub>GEN</sub> =3Ω, R <sub>L</sub> =1Ω		6		ns
Turn-on Rise Time	t <sub>r</sub>			17		
Turn-off Delay Time	t <sub>D(off)</sub>			29		
Turn-off Fall Time	t <sub>f</sub>			17		

Noted: (1) Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

- (2) Performed on 40mmx40mmx1.5mm epoxy FR4 PCB with 6cm<sup>2</sup>(one layer, 70μm thick) copper area for drain connection. PCB is vertical Without blown air.
- (3) Single pulse width limited by junction temperature T<sub>J(MAX)</sub> = 150°C.
- (4) The power dissipation PD is based on T<sub>J(MAX)</sub> = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.
- (5) The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJA</sub> and case to ambient.
- (6) The maximum current rating is package limited.

## Typical Performance Characteristics

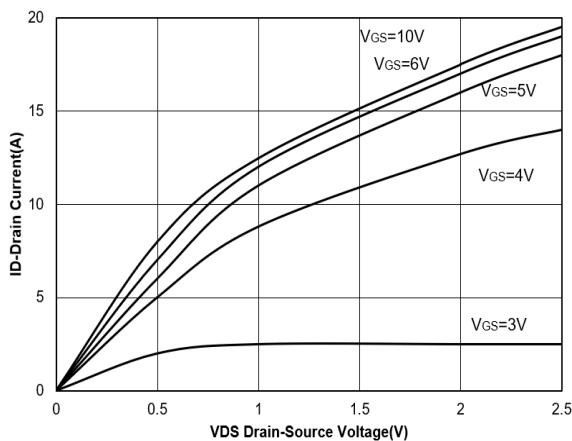


Figure 1. Output Characteristics

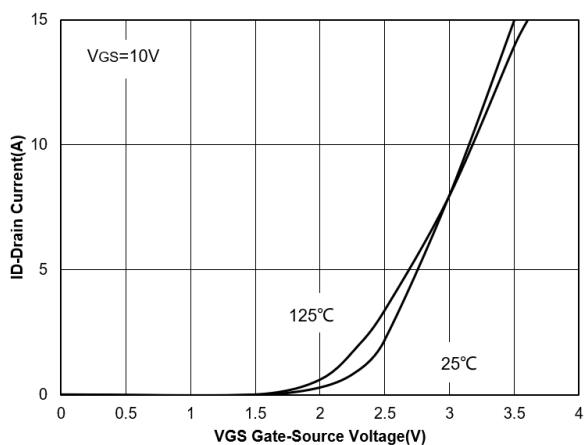


Figure 2. Transfer Characteristics

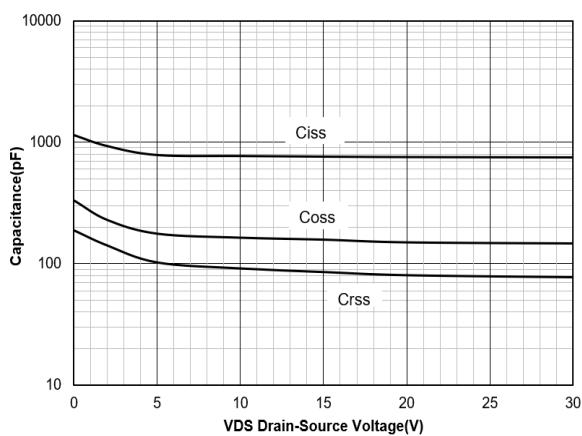


Figure 3. Capacitance Characteristics

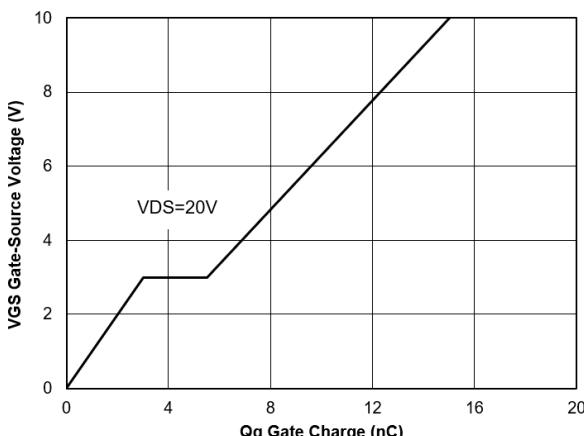


Figure 4. Gate Charge

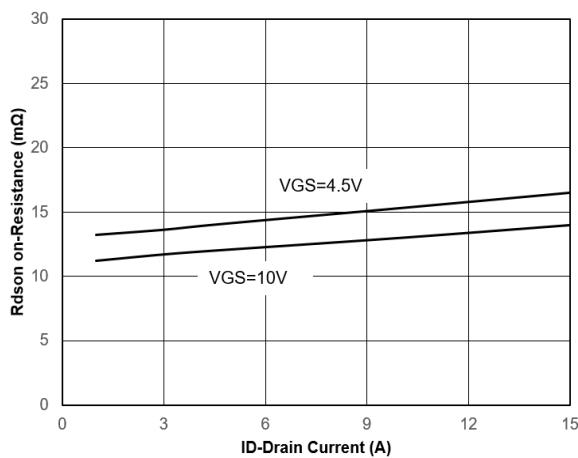


Figure 5. Drain-Source on Resistance

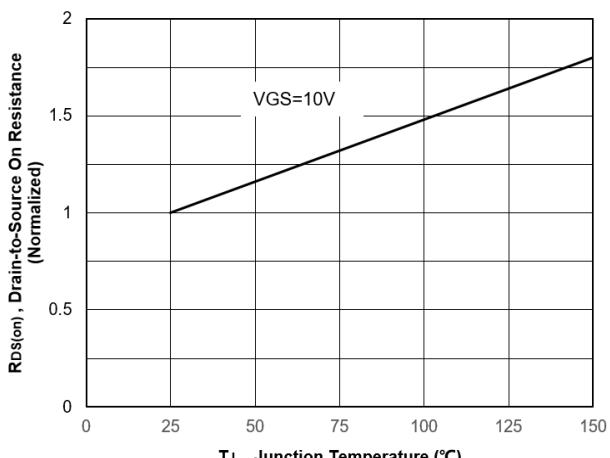


Figure 6. Normalized On-Resistance Vs. Temperature

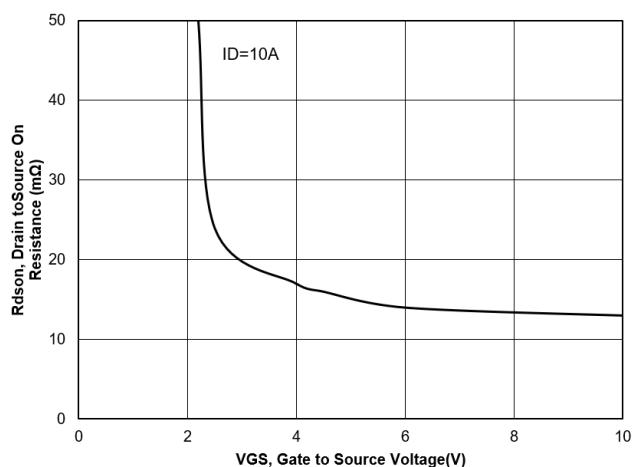


Figure 7. Typical Drain to Source ON Resistance  
VS Gate Voltage and Drain Current

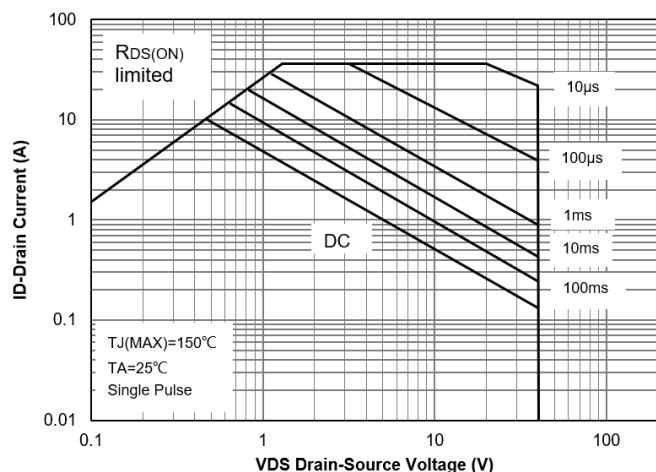


Figure 8. Safe Operation Area

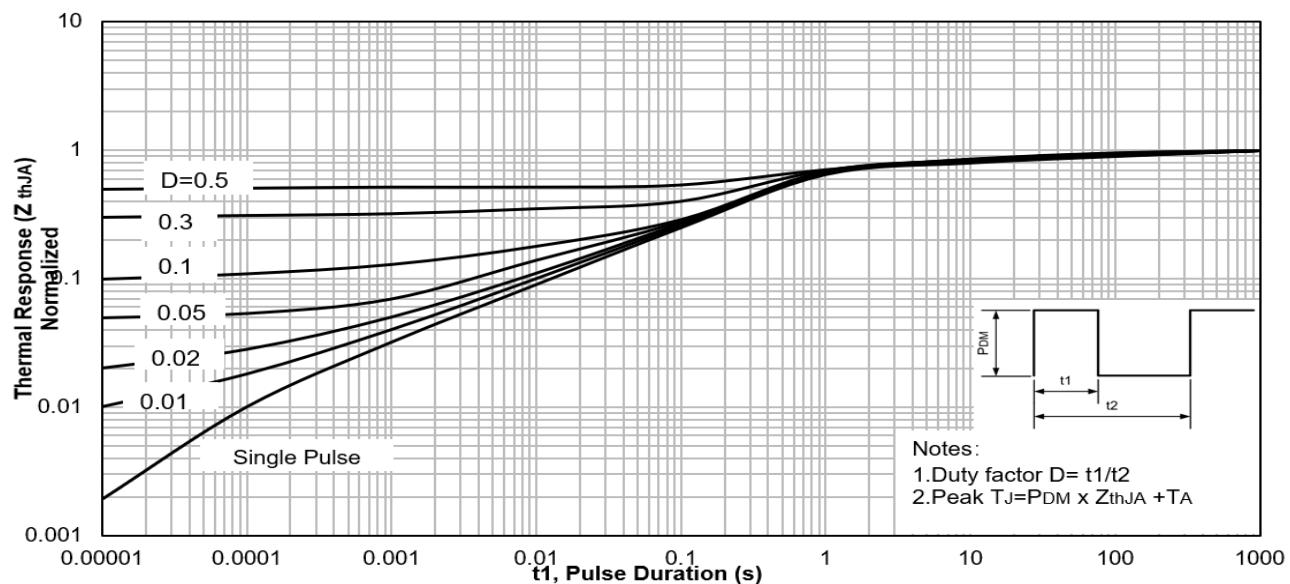


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

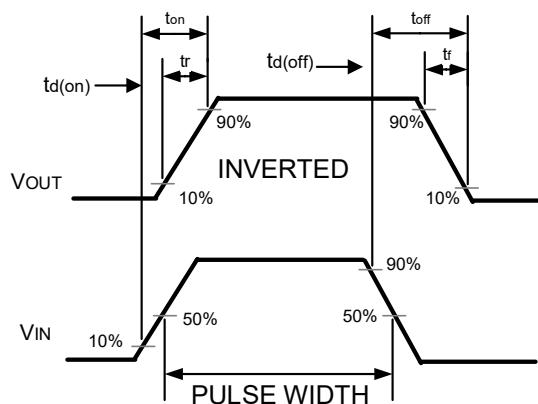
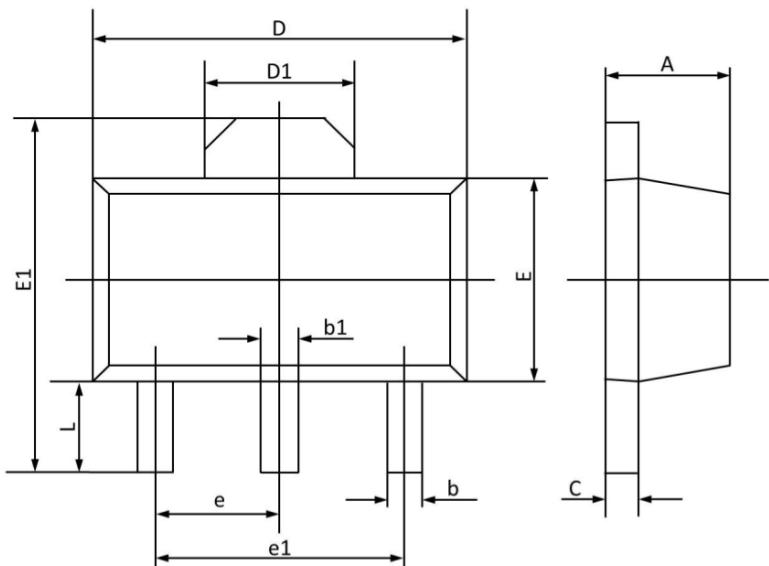


Figure 10. Switching wave

## SOT-89 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.400	--	1.600	0.055	--	0.063
b	0.320	--	0.520	0.013	--	0.020
b1	0.400	--	0.580	0.016	--	0.041
c	0.350	--	0.440	0.014	--	0.017
D	4.400	--	4.600	0.173	--	0.181
D1	1.550 REF			0.061 REF		
E	2.300	--	2.600	0.091	--	0.102
E1	3.940	--	4.250	0.155	--	0.167
e	1.500 TYP			0.060 TYP		
e1	3.000 TYP			0.118 TYP		
L	0.900	--	1.200	0.035	--	0.047

## Contact Information

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