

LCD Module Specification

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2.0 Record of revision

Rev	Date	Item	Page	Comment



3.0 General specification

Display format: 2 x 16
Character size: 5 x 7
View area: 61 x 15.8
General dimensions: 80 x 36
LCD type: STN Gray STN Yellow FSTN
Polarizer mode: Reflective Transflective Tansmissive Negative
View angle: 6 O'clock 12 O'clock Others
Backlight: LED EL CCFL
Backlight colour: Yellow green Amber Blue green White Others
Controller/Driver: KS0070B
Temperature range: Normal temperature Wide temperature Operating 0 to 50 C Operating -25 to 70 C Storage -20 to 70 C Storage -30 to 80 C
Siorage -20 to 70 C Storage -30 to 60 C



4.0 Absolute maximum rating

Vss = 0V, Ta = 25°C

NO	ITEM	SIMBOL	MIN	MAX	UNIT
1.	Power Supply voltage (Logic)	$V_{\mathrm{DD}} - V_{\mathrm{SS}}$	0	7	V
2.	Power Supply voltage (LCD Driver)	$V_{DD} - V_0$	-	12	V
3.	Operating Temperature	T_{op}	Refer p	age 3	°C
4.	Storage Temperature	T _{st}	Refer p	age 3	°C

5.0 Electrical characteristics

NO	ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
1.	Power Supply	$V_{DD}\!-V_{SS}$	-	2.75	-	5.5	V
	voltage (Logic)						
2.	Power Supply	V_{DD} - V_{0}	25°C	4.3	4.5	4.7	V
	voltage (V _{LCD})						
3.	Input Voltage	$V_{ m IH}$	-	$0.7V_{DD}$	-	V_{DD}	V
	(except OSC1)	V _{IL}	-	-0.3	-	0.4	V
4.	Current Supply	I_{DD}	$V_{DD} - V_{SS} = 5V$	-	5	-	mA

6.0 Environmental requirements

NO	ITEM	CONDITION
1.	Operating	Refer page 3
	Temperature	
2.	Storage Temperature	Refer page 3
3.	Operating Humidity	5% to 95%RH
4.	Cycle Test	0 C @ 30 min to 50 C @ 30min for 1 cycle
	-	run for 10 cycles

Note: The background on LCD has the possibility to be changed in different temperature range.

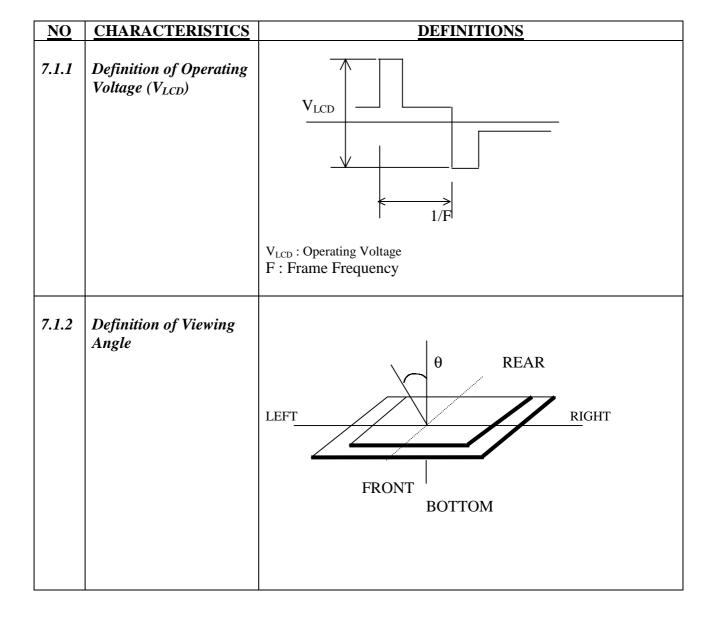




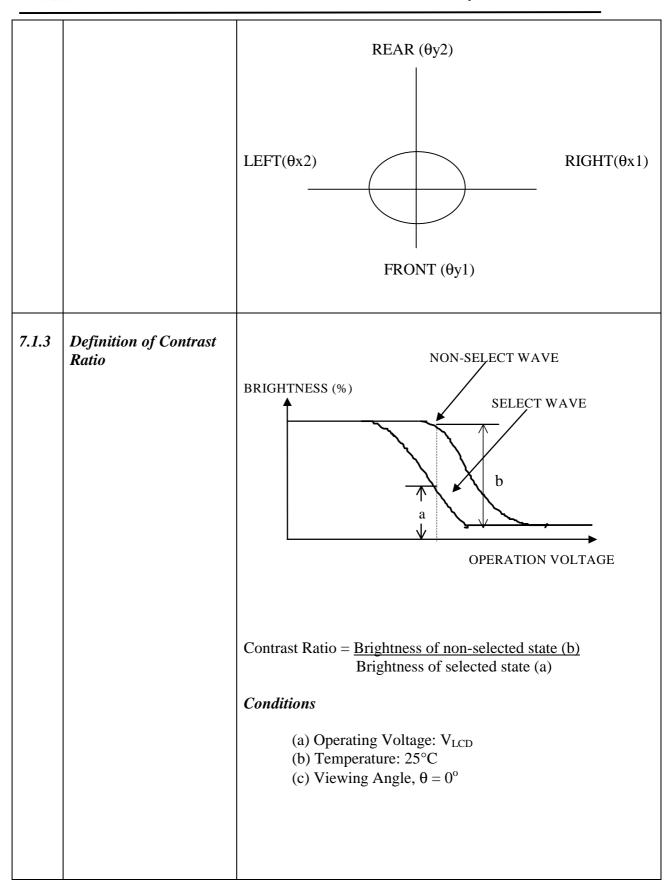
7.0 LCD specification

7.1 Electro-optical characteristics

NO	ITEM	SYMBOL	TEMP.	CONDITION	COI	MMERO	CIAL	UNIT	REF.
			°C		MIN	TYP	MAX		
1	Operating	V_{LCD}	25	$\theta = 0$	4.3	4.5	4.7	Volt	7.1.1
	Voltage			Cr = max					
2	Viewing	θ x 1	25	CR ≥ 2	-	45	-	Deg	7.1.2
		θ x 2		$V_{\rm LCD} = 4.5 V$	-	45	-		
		θу1			-	50	-		
		θу2			-	45	-		
3	Contrast	Cr	25	$\theta = 0^0, V_{LCD}$	-	10	-		7.1.3
	Ratio			=4.5V					





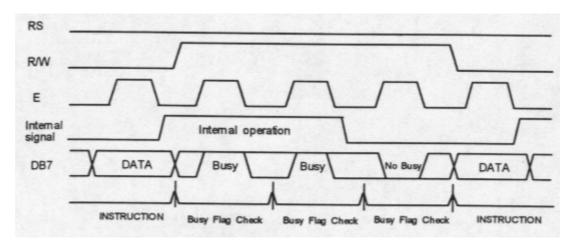


8.0 Interface

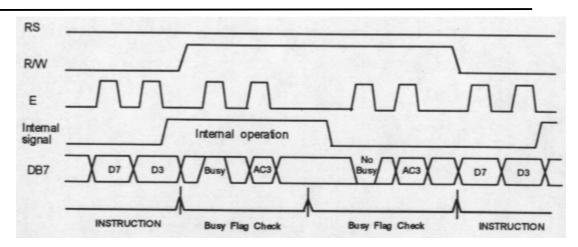
8.1	Display Driver	KS0070B	
8.2	Duty Cycle	1/16	
8.3	Pin-out Assignmen	ts	
	Pin No	Symbol	Description
	1	V _{SS}	Ground terminal of module
	2	V_{DD}	Supply terminal of module
	3	Vo	Power supply for Liquid Crystal Drive
	4	RS	Register Select: RS = 0 Instruction Register RS = 1 Data Register
	5	R/W	Read/Write: High = Read Low = Write
	6	Е	Enable
	7 to 14	D0 to D7	Bi-directional Data Bus. Data Transfer is performed once, thru D0 to D7, in the case of interface data length is 8-bits.
	15	(BL -)	LED power supply terminals
	16	(BL +)	

9.0 TIMING CHARACTERISTICS/TIMING DIAGRAMS

9.1 Timing Characteristics for KS0070B

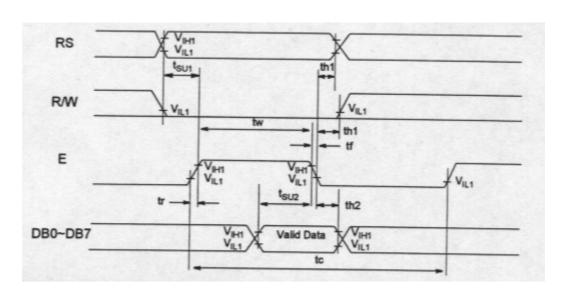


Example of 8-bitBus mode timing diagram



Example of 4-bit Bus mode timing diagram

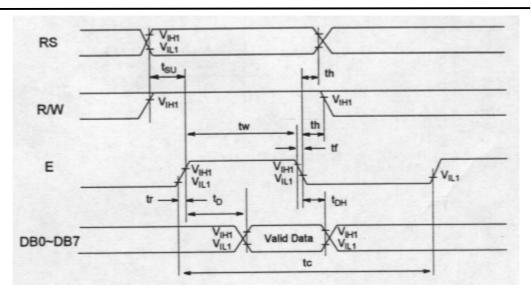
9.2 Timing Diagrams for Write Mode and Read Mode (KS0070B)



Write Mode Timing Diagram

Item	Symbol	Condition	Min	Max	Unit
Enable cycle time	t _c	$V_{\rm DD} = 4.5$ to	500	-	ns
Enable rise/fall time	t_r, t_f	5.5V	-	25	
Enable pulse width (high,	t _w	Ta = -30 to	220	-	
low)		+85C			
R/W and RS setup time	t_{su1}		40	-	
R/W and RS hold time	t_{h1}		10	-	
Data setup time	t_{su2}		60	-	
Data hold time	t _{h2}		10	-	

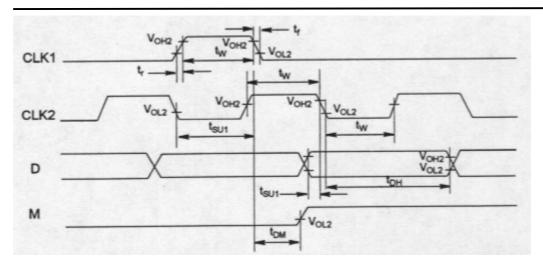




Read Mode Timing Diagram

Item	Symbol	Condition	Min	Max	Unit
Enable cycle time	t _c	$V_{\rm DD} = 4.5$ to	500	-	ns
Enable rise/fall time	t_r, t_f	5.5V	_	25	
Enable pulse width (high,	$t_{\rm w}$	Ta = -30 to	220	-	
low)		+85C			
R/W and RS setup time	t_{su1}		40	-	
R/W and RS hold time	t_{h1}		10	-	
Data setup time	t_{su2}		_	120	
Data hold time	t_{h2}		20	-	





Interface mode with extension driver timing diagram

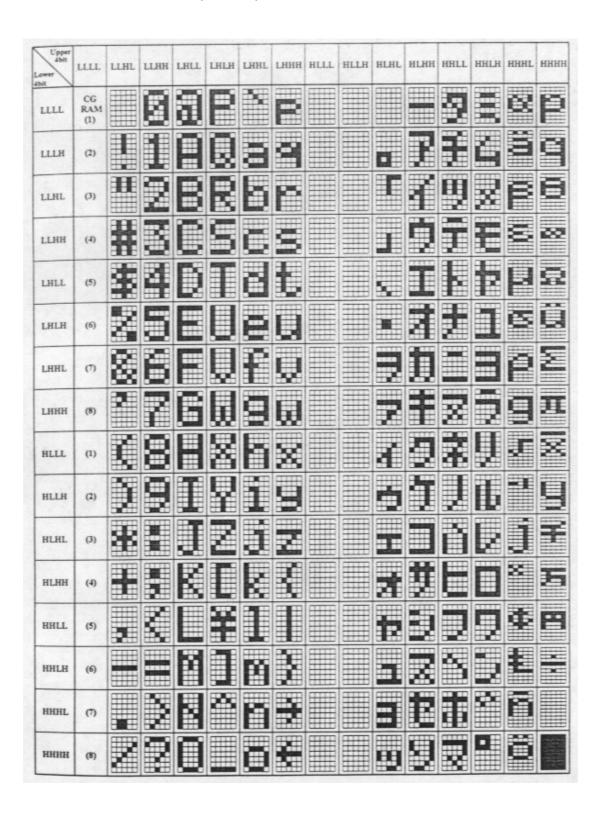
Item	Symbol	Min	Max	Unit
Clock pulse width (high, low)	t_{W}	800	-	ns
Clock rise/fall time	t_r/t_f	-	100	
Clock setup time	t_{SU1}	500	-	
Data setup time	$t_{ m SU2}$	300	-	
Data hold time	t_{DH}	300	-	
M delay time	t_{DW}	-1000	1000	

Relationship between character code (DDRAM) and character pattern (CGRAM)

Pattern number		acter Code (DDRAM data) CGRAM Address CGRAM Data										arac	Ch									
	P0	P1	P2	P3	P4	P5	P6	P7	A0	A1	A2	A3	A4	A5	D0	D1	D2	D3	D4	D5	D6	D7
pattern	0	1	15	115	0	×	×	×	0	0	0	0	0	0	0	0	0	×	0	0	0	0
	至高	0	0	0	額			18.5	1	0	0											
	33	0	0	0				5	0	1	0											
		30						14	1	1	0											
	1	0	0	0				33	0	0	1											
		0	0	0	雅			1	1	0	1											
		0	0	0	羅			3	0	1	1			-								
	0	0	0	0	0				1	1	1											
				+			37	15					3.54									
								38						1								
pattern	ESS	0	0	0	EEE S	×	×	×	0	0	0	0	0	0	1	1	1	×	0	0	0	0
		0	0	0	1			18	1	0	0										100	
	疆	0	0	0	1				0	1	0											
		201	Edition 1	500				18	1	1	0											
	餾	0	0	0				133	0	0	1											
		0	0	0				13	1	0	1											
	1	0	0	0	1			18	0	1	1											
	0	0	0	0	0			130	1	1	1			1								

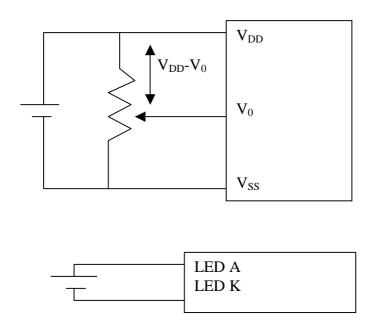


Character Generator ROM (KS0070)



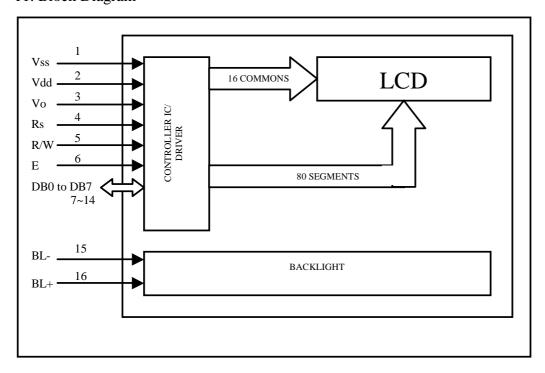


10. Power Supply



Where V_{DD} - V_0 = LCD Driving voltage

11. Block Diagram





12. Instructions

Instruction	Code										Description	Executed time(max)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	2 computer	fosc=270KHz	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clear all display and returns the cursor to the home position (Address 0)	1.53 ms	
Cursor at home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also return the display being shifted to the original position. DDRAM contents remain unchanged.	1.53 ms	
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	39 μs	
Display on/off control	0	0	0	0	0	0	1	D	С	В	Sets the ON/OFF of all display (D) cursor ON/OFF (C), and blink of cursor position character (B).	39 µs	
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing the DDRAM contents.	39 µs	
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N) and character font (F).	39 µs	
CGRAM address set	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Sets the CGRAM, data is sent and received after this setting.	39 µs	
DDRAM address set	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set the DGRAM, data is sent and received after this setting.	39 µs	
Busy Flag/ address read	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Recall Busy flag (FB) indicating internal operation is being performed and read address counter contents.	0 μs	
CGRAM/DDRAM data write	1	0	WRIT	E DATA			•	•			Writes data into DDRAM or CGRAM	43 μs	
CGRAM/DDRAM data read	1	1	READ	DATA							Reads data into DDRAM or CGRAM	43 μs	

Code		Description	Executed time (max)
I/D=1: Increment	DL= 0:4-bit	DDRAM: Display Data RAM	Fcp or fosc = 250KHz
I/D=0: Decrement	1/16 duty	CGRAM: Character Generator RAM	However, when frequency changes, execution
S=1: With display shift	1/8 duty, 1/11 duty	ACG: CGRAM Address	time also changes.
S/C=1: Display shift	F= 1:5x10 dots	ADD: DDRAM Address	
S/C=0: Cursor movement	F= 0: 5x7 dots	Corresponds to cursor address	Example
R/L=1: Shift to the right	BF=1: Internal operations is	AC: Address Counter, used for both DDRAM	If fcp or fosc is 270KHz
R/L=0: Shift to the left	being performed	and CGRAM	
DL=1: 8-bit	BF=0: Instruction acceptable	*: Invalid	



CRYSTAL CLEAR TECHNOLOGY SDN. BHD.

Spec. No: CMC216-02

8 bit operation, 8 digit 2line display example.

Step	Instruct	ion										
No	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation
1	Power	supply or	1				l l	- U				Initialized. No display
2	Function	n set										Sets to 8 bit operation and select 2
	0	0	0	0	1	1	1	0	X	X		lines display and 5x8 dot character
												font.
3	Display	on/off c	ontrol								_	Turn on display and cursor. All
	0	0	0	0	0	0	1	1	1	0		display is in space mode because
												of initialisation.
4	Entry n	node set										Sets mode to increment the
											_	address by one and to shift the
	0	0	0	0	0	0	0	1	1	0		cursor to the right at the time of
												write to the DD/CGRAM. Display
												is not shifted.
5	Write d	ata to CO	GRAM/E	DRAM								Writes C. DDRAM has already
											C_	been selected by initialisation
	1	0	0	1	0	0	0	0	1	1		when the power was turned on.
		-	-		-	-	-	-				The cursor is incremented by one
												and shifted to the right.
6												
7	Write d	ata to CO	GR AM/F	DRAM								Writes R
,	Wille C	uu to co	310/ HVI/ E	DIG IIVI							CRYSTAL CLEAR_	Willes K
	1	0	0	1	0	1	0	0	1	0	CK ISIME CLEAK_	
		Ü	U	•	Ü	•	Ü	Ü	•	Ü		
8	Sat DD	RAM ad	drace									Sets DDRAM address so that the
0	Set DD	KAWI au	uiess								CRYSTAL CLEAR	
	0	0		1	0	0	0	0	0	0	CRYSTAL CLEAR	cursor is positioned at the head of
	0	0	1	1	0	0	0	0	0	0	-	the second line.
9	W/	ata to CC	CD AM/E	NDD AM								Writes T
9	write	ata to CC	JKANI/L	DKAM			CRYSTAL CLEAR	writes 1				
	1	0	0	1	0	1	0	1	0	0		
	1	U	U	1	0	1	U	1	U	U	T_	
10												
10	***		~P + 1 + 4 =	DD 111								****
11	Write o	ata to CO	jRAM/L	DDRAM				Writes H				
											CRYSTAL CLEAR	
	1	0	0	1	0	0	1	0	0	0	TECH_	
12	Entry n	node set										Sets mode to shift display at the
						_	_				CRYSTAL CLEAR	time of write.
	0	0	0	1	0	0	0	1	1	1	TECH_	
13	Write data to CGRAM/DDRAM											Writes Y. Display is shifted to the
											CRYSTAL CLEAR	left. The first and second lines
	1	0	0	1	0	1	1	0	0	1	TECHNOLOGY	both shift at the same time.
14												
15	Return	home										Returns both display and cursor to
											<u>C</u> RYSTAL CLEAR	the original position (address 0)
	0	0	0	1	0	0	0	0	1	X	TECHNOLOGY	