DESCRIPTION

The CM6533/CM6533N/CM6533X1 is a USB 2.0 audio chip built-in 8051 for flexible applications. With integrated Tri-Colors PWM LED driver and two (2)-channel ADC/DAC and S/PDIF interface that makes it suitable for headset, docking, speaker and microphone applications. The internal 8051 can also be developed to a lot of different applications, such as Microsoft™ Lync / Skype/VoIP device, Android Phone or Tablet/Slate docking device. The CM6533 /CM6533N /CM6533X1 is compatible with USB Audio Class 1.0 and USB 2.0 Full-Speed, thus it can plug & play without any additional software installation on major operating systems. The internal DAC and ADC support from 8 ~ 96 KHz sampling rate and 16/24 bits resolution.

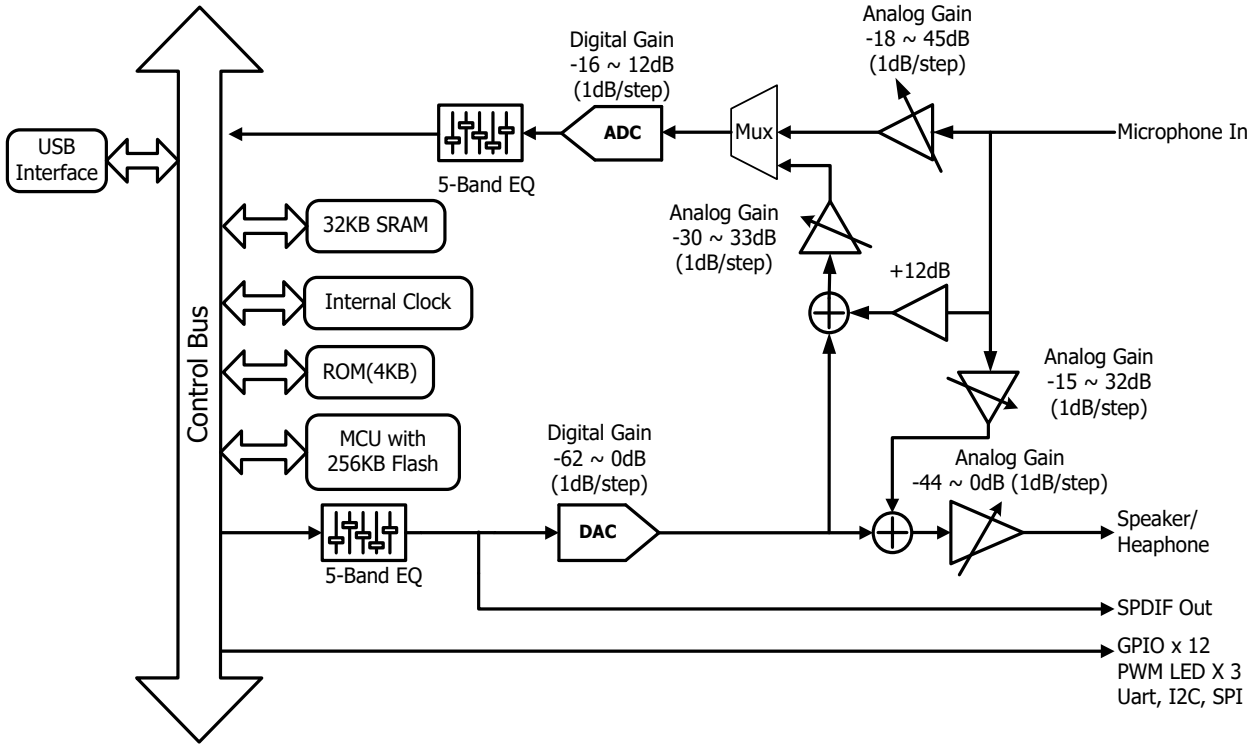
The CM6533/CM6533N/CM6533X1 integrates equalizer on both playback and recording paths to compensate the frequency response of microphone and headphone.

The CM6533/CM6533N/CM6533X1 also integrates 256K Byte flash (Including 32KB F/W programming size) and crystal but requires few passive components to make a finish product. Thus, it can save the total BOM cost and PCB area can be smaller.

FEATURES

- USB 2.0 Full-Speed compliant
- USB Audio Class 1.0 compliant
- USB Human Interface Device (HID) Class 1.11 compliant
- Two (2)-channel DAC for audio output interface
- Two (2)-channel ADC for audio input interface
- Supports Digital Microphone interface
- Built-in S/PDIF transmitter
- Built-in Equalizer on both playback and recording paths
- Supports USB suspend/resume/reset functions
- Supports control, interrupt, bulk, and isochronous data transfers
- Embedded 1T 8051 with 32K Byte SRAM and 256K Byte flash(Including 32KB F/W programming size)
- Supports OMTP and CTIA auto switch on a 4-pole jack
- Integrated Tri-Colors PWM LED driver
- Master/Slave H/W I2C/SPI/UART control interface for external audio devices or FLASH access
- Supports embedded oscillator without external crystal
- Built-in 30mW @ R=32Ω headphone amplifier
- On chip watchdog timer

BLOCK DIAGRAM



Release Notes

Revision	Date	Description
1.0	2014/07/08	First release.
1.1	2014/08/05	Modify F/W volume setting table(CH2.6).
1.2	2014/09/18	1. Modify Pin descriptions. 2. Modify Pin out diagram.
1.3	2014/09/19	1. Modify MIC_SWOUT to AO pin. 2. Modify power consumption for 12MHz MCU Clock. 3. Modify Reset diagram of CH6.13. 4. Separate CM6533/CM6533X1/CM6533DH Pin out diagram. 5. Modify flash description: 256K Byte flash(Including 32KB F/W programming size).
1.4	2015/3/30	1. Remove Microphone input impedance chart. 2. Add Xear and Dolby software function descriptions.(CH7,CH8) 3. Modify Operating ambient temperature to -15~70 °C. 4. Modify CH5.1 CH5.2 USB Topology chart. 5. Modify Block Diagram (Page1). 6. Add Cap-less cross talk performance. 7. Add CM6533N QFN Package.
1.5	2015/08/07	1. Modify CH6.7 Digital microphone descriptions.
1.6	2015/10/29	1. Modify I2C Using Example. 2. Modify SPI Using Example. 3. Modify TEST pin description.
1.7	2018/08/27	1. Modify UART TX/RX pin description 2. Correct I2C timing diagram.
1.8	2019/11/22	1. Remove dual tone generator
1.9	2020/08/28	1. Remove AGC、JTAG、CM6533DH

TABLE OF CONTENTS

1 Description and Overview

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The CM6533/CM6533N/CM6533X1 integrates equalizer on both playback and recording paths to compensate the frequency response of microphone and headphone.

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2 Features

2.1 USB Compliance

- USB 2.0 Full-Speed compliant
- USB Audio Class 1.0 compliant
- USB Human Interface Device (HID) Class 1.1 compliant
- Supports USB suspend/resume/reset functions
- Supports control, interrupt, bulk, and isochronous data transfers and overview

2.2 Integrated 8051 Microprocessor

- Embedded 8051 micro-processor to handle the command/protocol transactions
- Embedded 256K Byte SPI Flash(Including 32KB F/W programming size)
- 32K Byte RAM for firmware extension and plug-in
- HID interrupts/buttons/functions can be implemented via firmware codes
- Provides maximum hardware configured flexibility with firmware code upgrade
- VID/PID/Product String can program by firmware

2.3 Control Interface

- Master/Slave I2C control interface, bus speed supports 100 and 400kbit/s
- One 4-wire SPI mater/slave interface, bus speed supports from 150k to 12Mbit/s
- 12 GPIO pins and firmware programmable
- GPIOs are configured as HID key and LED indicators
- Tri-Colors PWM LED Driver

2.4 General

- Crystal-less (embedded crystal function)
- Single 5V power supply (embedded 5V to 1.8V regulator for digital core, 5V to 3.3V regulator for digital IO, 5V to

3.6V regulator for analog codec)

- 3.3V digital I/O pads with 5V tolerance
- Industrial standard LQFP-48 package (7x7mm)

2.5 Audio I/O

- Playback Stream:
  - ➢ Speaker/Headphone
    - Sample Rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K/88.2K/96KHz
    - Supports Bit Length: 16/24bits
    - Speaker Gain Range (Analog) is -44 ~ 0dB, 1dB/step
    - DAC Gain Range (Digital) is -62 ~ 0dB, 1dB/step
  - ➢ S/PDIF transmitter
    - Sample Rates: 44.1K/48K/88.2K/96KHz
    - Supports Bit Length: 16/24 bits

- Recording Stream:
  - ➢ Microphone
    - Sample Rates: 8K/11.025K/16K/22.05K/32K/44.1K/48K/88.2k/96KHz
    - Supports Bit Length: 16/24 bits
    - Microphone gain range (Analog) is -18 ~ 45dB, 1dB/step
    - ADC gain range (Digital) is -16 ~ 12dB, 1dB/step
  - ➢ Stereo Mixer
    - Mix stereo playback stream and stereo microphone
    - Stereo Mixer gain range is -30 ~ 33dB, 1dB/step

- A-A path Stream:
  - ➢ Microphone to playback A-A path
    - Mix mono microphone input to stereo playback both L/R channel
    - The Microphone A-A path gain range is -15 ~ 32dB, 1dB/step

**Note 1: A-A path means Analog to Analog Mixer path

**Note 2:

CM6533/CM6533N/CM6533X1 is a USB 2.0 Full Speed audio device. Since bandwidth limitation, CM6533/CM6533N/CM6533X1 cannot support 96KHz/24bits for playback and capture streams simultaneously. The possible combinations are shown below:

	Playback	Capture
Audio Format	Stereo, 96KHz/24bits	Stereo, 48kHz/24bits or below
		Mono, 96KHz/24bits or below
	Stereo, 48kHz/24bits or below	96KHz/24bits
	Mono, 96KHz/24bits or below	

2.6 General Firmware Volume Setting Value

The CM6533/CM6533N/CM6533X1 is a MCU base USB Audio Device; the default topology is different from its hardware capability.

Please refer to chapter 5.1 and 5.2 for the CM6533/CM6533N/CM6533X1 default topology while below the gain volume range.

Device	Minimum	Maximum	Default	dB/Step
Speaker	-45dB(Mute)	0dB	-10dB	1dB
Microphone in recording Volume	0dB	+30dB	+20dB	1dB
Microphone A-A path (playback)	-15dB(Mute)	+22dB	0dB	1dB

2.7 CM6533/CM6533N/CM6533X1 Compared Table

The pin out of CM6533, CM6533N, and CM6533X1 are all the same and they only differ in firmware, software and package.

		CM6533N	CM6533	CM6533X1
Package		QFN48	LQFP48	LQFP48
Firmware		Optional Jack Detection	Optional Jack Detection	--
Software	Jack Detection	●	●	--
	Xear™ Surround HP	--	--	●

For the detailed firmware and software information, please refer to its corresponding spec.

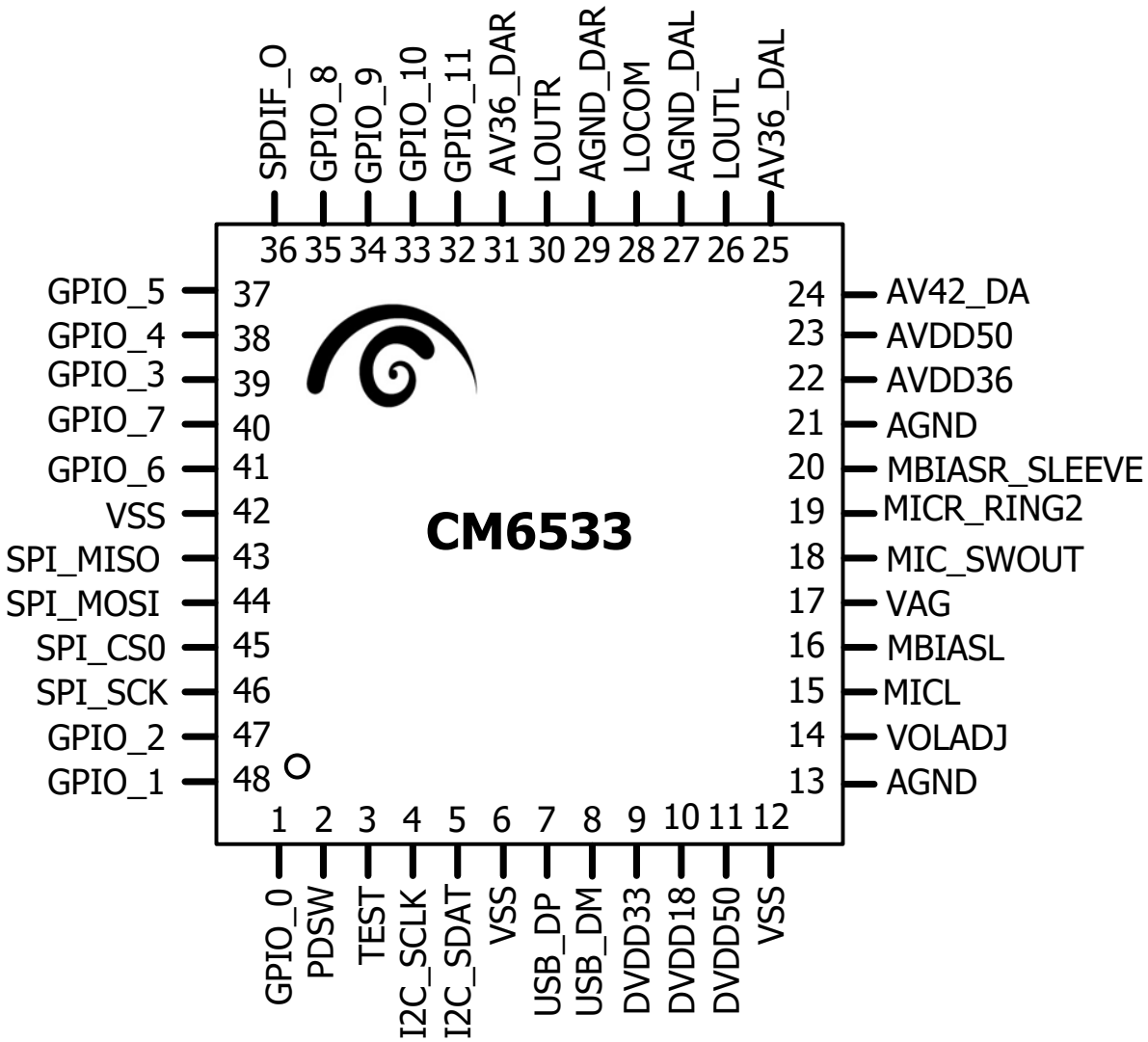
- Software Functions:
  - CM6533X1 Xear™ Sound Processing
    - Xear™ Surround Headphone
    - Xear™ Software 10 Band Equalizer
    - Xear™ Audio Brilliant
    - Xear™ Dynamic Bass
    - Xear™ Voice Clarity
    - Xear™ Smart Volume
    - Xear™ Surround Max
    - Xear™ Magic Voice
    - Xear™ Environmental Noise Cancellation

3 Applications

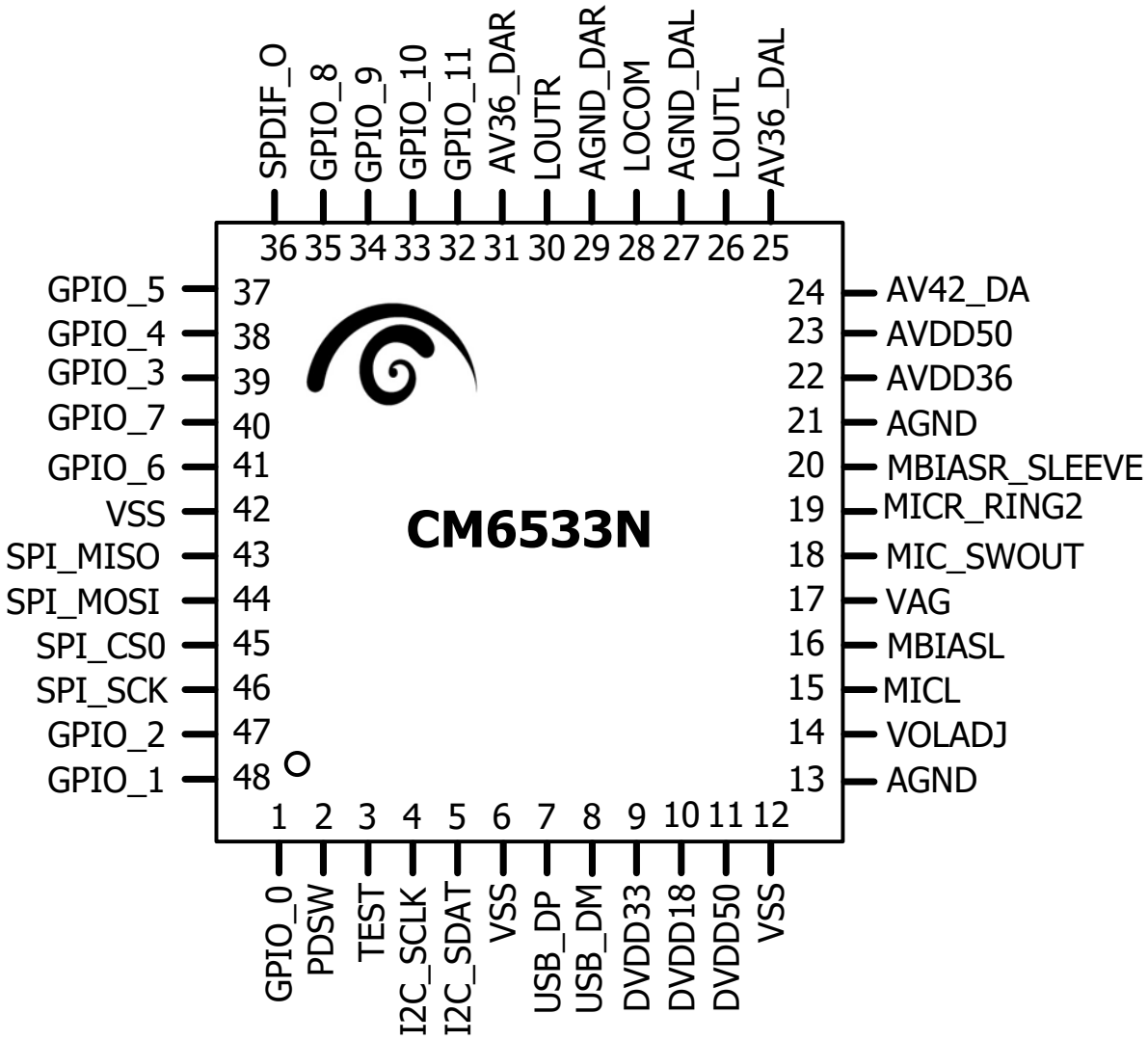
- USB Headset/Gaming Headset
- Microsoft™ Lync/Skype VoIP Headset
- Notebook/Netbook Docking
- Android Phone/Slate Docking
- USB Speaker
- USB Microphone

4 Pin Assignment

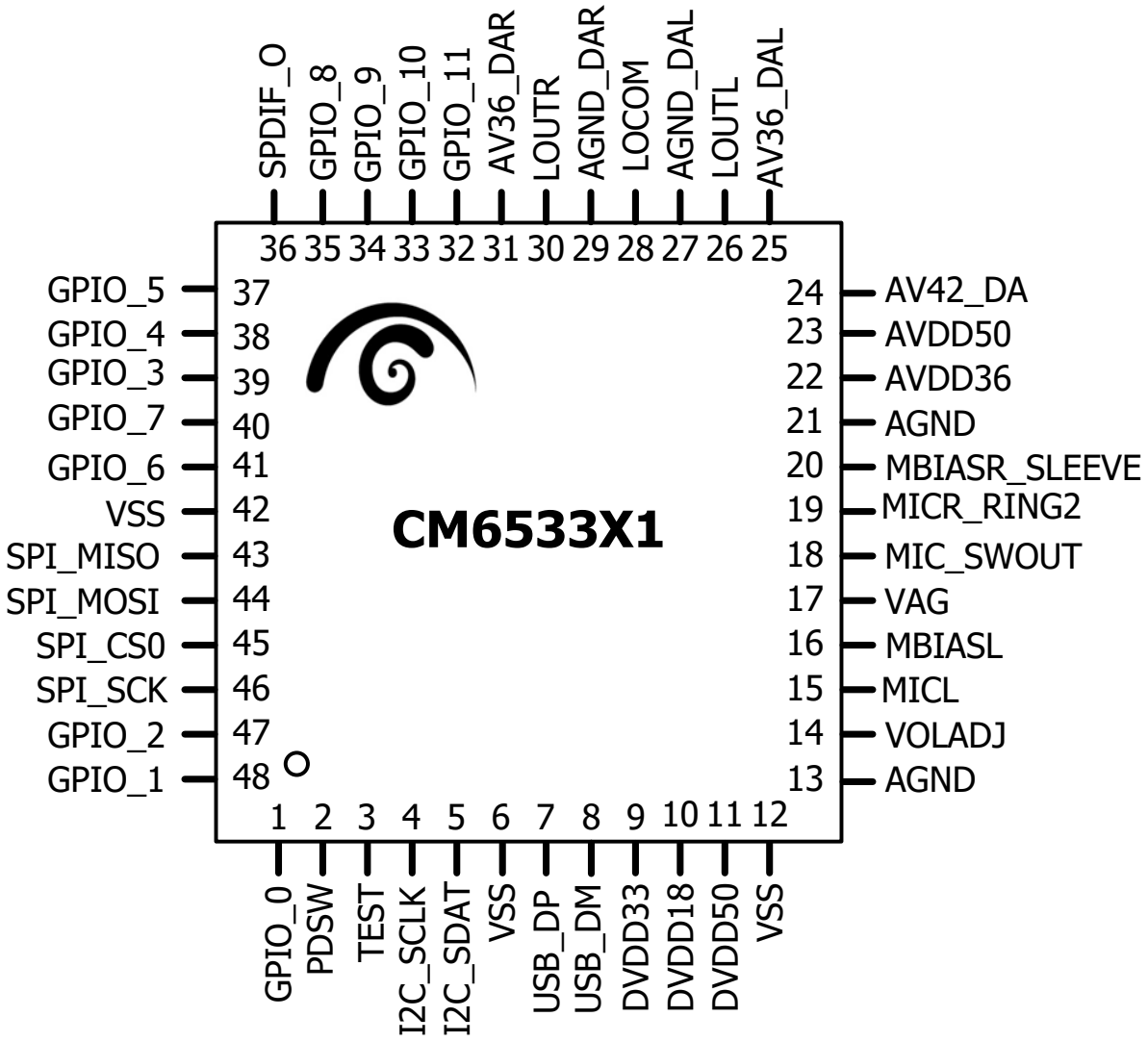
4.1 CM6533 Pin-out Diagram (LQFP48)



4.2 CM6533N Pin-out Diagram (QFN48)



4.3 CM6533X1 Pin-out Diagram (LQFP48)



4.4 Pin Description

Pin #	Symbol	I/O	Description
USB2.0 BUS Interface			
7	USB_DP	AIO	USB 2.0 data positive (USB D+ signal).
8	USB_DM	AIO	USB 2.0 data negative (USB D- signal).
Power/Ground			
9	DVDD33	AO	Regulator 3.3V output, drive capacity 10mA.
10	DVDD18	AO	Regulator 1.8V output, no current drive capacity.
11	DVDD50	PWR	5V digital power for 5/3.3/1.8V regulator.
22	AVDD36	AO	Analog 3.6V regulator for ADC, no current drive capacity.
23	AVDD50	PWR	5V analog power for 4.2/3.6V regulator.
24	AV42_DA	AO	Analog 4.2V regulator for Analog 3.6V regulator, no current drive capacity.
25	AV36_DAL	AO	Analog 3.6V regulator for DAC left channel, no current drive capacity.
31	AV36_DAR	AO	Analog 3.6V regulator for DAC right channel, no current drive capacity.
6	VSS	GND	Digital Ground.
12	VSS	GND	Digital Ground.
42	VSS	GND	Digital Ground.
13	AGND	GND	Analog Ground.
21	AGND	GND	Analog Ground.
27	AGND_DAL	GND	Analog Ground.
29	AGND_DAR	GND	Analog Ground.
Audio Interface			
18	MIC_SWOUT	AO	Combo jack detect and auto switch, detect combo jack type and switch to MICR_RING2 or MBIASR_SLEEVE.
15	MICL	AI	Microphone in left channel.
19	MICR_RING2	AI	Microphone in right channel or combo jack Ring2 pin input.
16	MBIASL	AO	Microphone bias (2.75V) for Left channel.
20	MBIASR_SLEEVE	AO	Microphone bias (2.75V) for Right channel or combo jack Sleeve pin input.
17	VAG	AO	Voltage reference cap filter.
26	LOUTL	AO	Line out left channel.
28	LOCOM	AO	Line out common reference for cap-less connection. Suggested connections: Cap-less: 10uF None use: floating
30	LOUTR	AO	Line out right channel.
14	VOLADJ	AI	Analog control voltage input for playback volume control. SAR ADC digital input range: SARAD<5:0> 000000:Maxium------27.3mV 111111:Minium-------1.75V (27.3mV/1step)
S/PDIF I/O			
36	SPDIF_O	DO	S/PDIF transmitter SPDIF_O is an output buffer with 8mA Tri-state.
GPIO			
1	GPIO_0	DIO	General purpose input/output (default Volume Up button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.
48	GPIO_1	DIO	General purpose input/output (default Volume Down button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.
47	GPIO_2	DIO	General purpose input/output (default Play Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.

39	GPIO_3	DIO	General purpose input/output (default Rec Mute button). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
38	GPIO_4	DIO	Programmable 2 in 1 I/O interface. GPIO / PWM select by firmware. General purpose input/output (default PWM LED Blue). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
37	GPIO_5	DIO	Programmable 2 in 1 I/O interface. GPIO / PWM select by firmware. General purpose input/output (default PWM LED Green). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
41	GPIO_6	DIO	Programmable 2 in 1 I/O interface. GPIO / PWM select by firmware. General purpose input/output (default PWM LED Red). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
40	GPIO_7	DIO	General purpose input/output . 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default EQ disable and weak pull-up for input.	There are 4 kinds of preset EQ, GPIO7 and 8 are used to determine in which mode. The combinations are shown below. GPIO[8:7]=0,0: Normal mode GPIO[8:7]=0,1: Gaming mode GPIO[8:7]=1,0: Communication mode GPIO[8:7]=1,1: Movie mode EQ function can enable via configuration tool or firmware.
35	GPIO_8	DIO	General purpose input/output 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default EQ disable and weak pull-up for input.	
34	GPIO_9	DIO	General purpose input/output (default Rec Clip Indicator). 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
33	GPIO_10	DIO	Programmable 3 in 1 I/O interface. GPIO / Digital MIC Clock (DMIC_CLK) / UART_RX select by firmware. GPIO (Default MIC Jack Detect): 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
32	GPIO_11	DIO	Programmable 3 in 1 I/O interface. GPIO / Digital MIC Data (DMIC_DAT) / UART_TX select by firmware. GPIO (Default Headphone Jack Detect): 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
4-Wire SPI Serial Bus				
43	SPI_MISO	DIO	SPI data master in/slave out, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-down for input.	
44	SPI_MOSI	DIO	SPI data master out/slave in, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-down for input.	
45	SPI_CS0	DIO	SPI chip select, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
46	SPI_SCK	DIO	SPI clock, 3.3V I/O, 5V tolerance, bidirectional buffer with 8mA driving current, Default weak pull-down for input.	
2-Wire Serial Bus (I2C)				
5	I2C_SDAT	DIO	2-wire serial data, 3.3V I/O, 5V tolerant, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	
4	I2C_SCLK	DIO	2-wire serial clock, 3.3V I/O, 5V tolerant, bidirectional buffer with 8mA driving current, Default weak pull-up for input.	

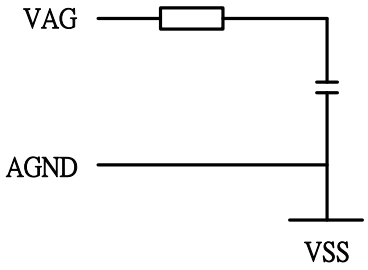
Miscellaneous			
2	PDSW	DO	Power Down Switch is an output buffer with 8mA Tri-state output. Normal mode: 0 Suspend mode: 1
3	TEST	DI	The TEST pin is used for IC test, another one is in the situation when F/W was crash or USB was not recognized, Set TEST pin to 3.3V before USB connect can force MCU into boot loader mode and able to update F/W via configuration tool, Default weak pull-down for input. 1: Boot loader mode 0: Normal operation

**Note1: GPIOs, I2C, SPI, SPDIF, MIC_SWOUT, MICL, MICR_RING2, MBIASL, MBIASR_SLEEVE, VAG, LOUTL, LOCOM, LOUTR, VOLADJ, PDSW pins can be left floating if not in use.

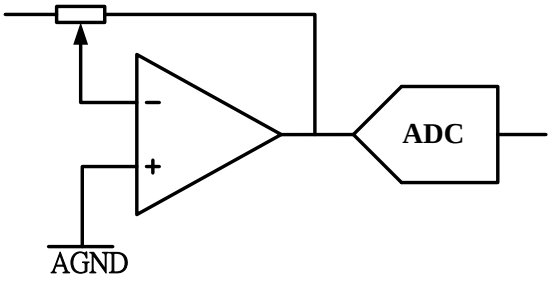
**Note2: Suggest connect TEST pin to GND by default setting.

4.5 Pin Circuit Diagrams

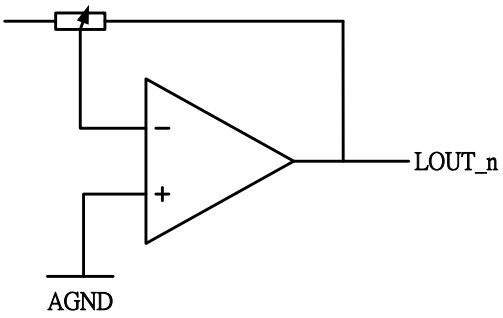
VAG, MIC_BAIS



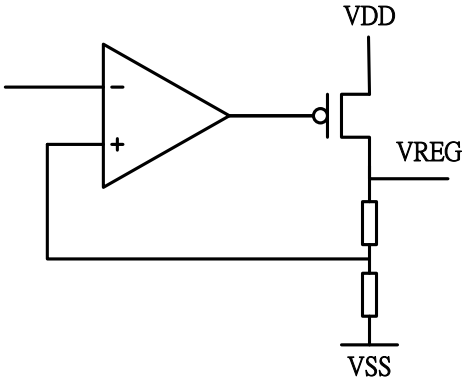
Analog input pins LINE, MIC



Output pins LOUTL, LOUTR

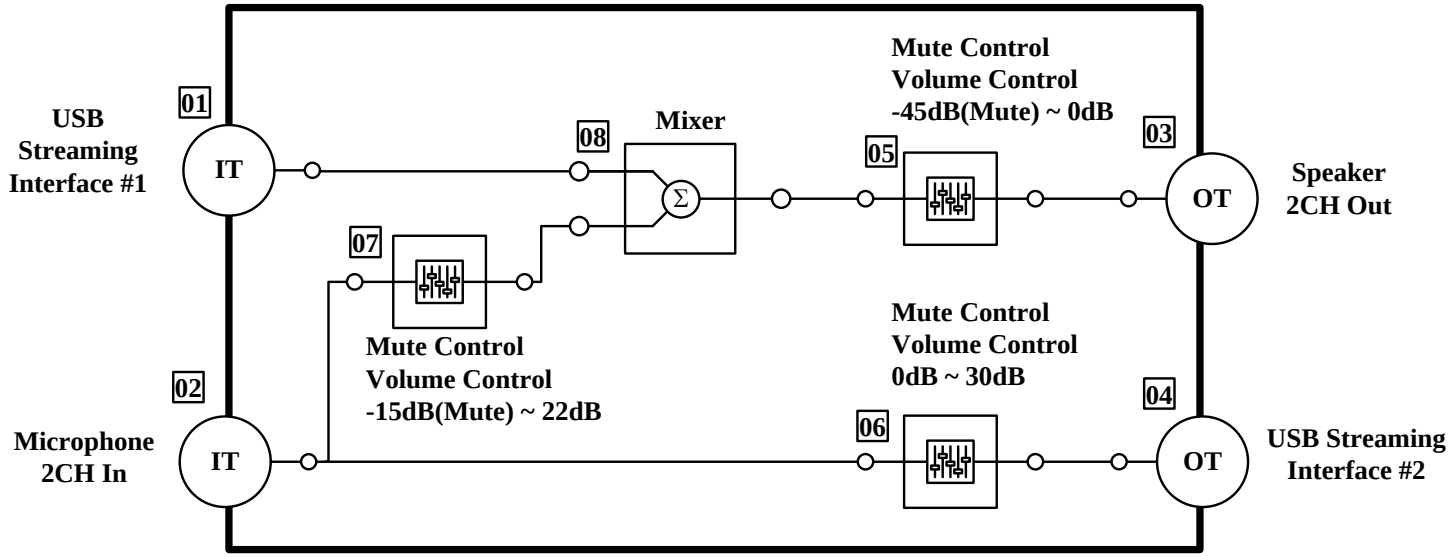


Output pins LOUTL, LOUTR



5 USB Audio Topology

5.1 CM6533N/CM6533 Headset Topology



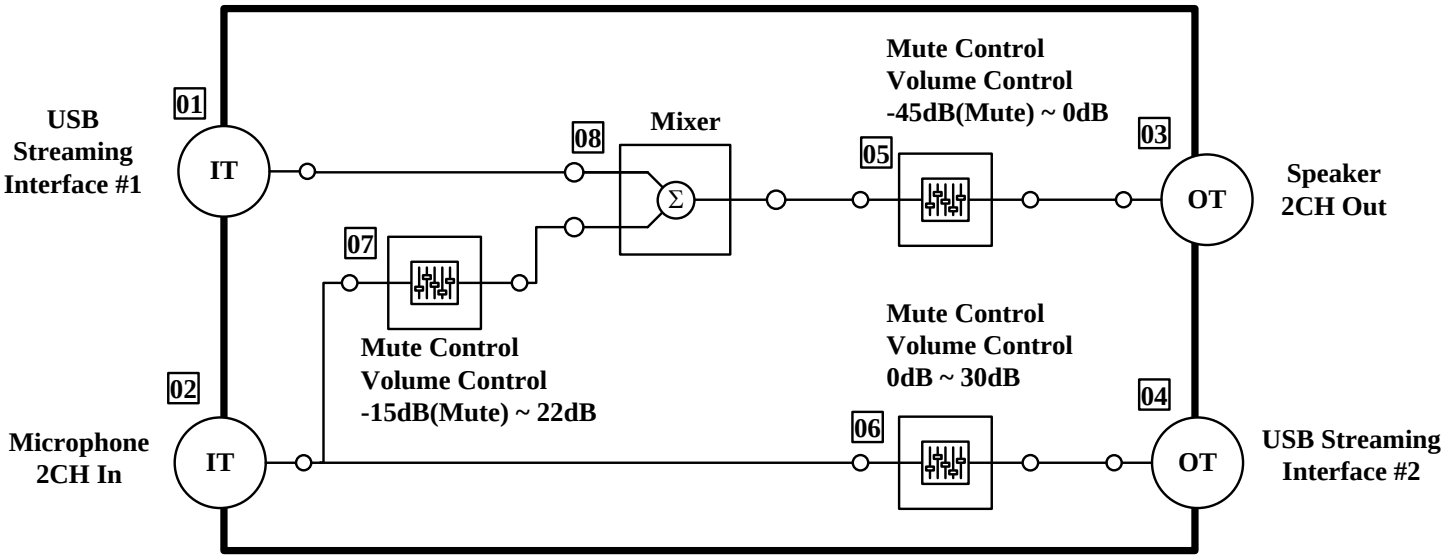
USB Interfaces List

	Interface Description	Endpoint
Interface 0	Audio Control Interface	
Interface 1	Audio Stream Interface for Playback	0x01
Interface 2	Audio Stream Interface for Record	0x82
Interface 3	HID Interface	0x87(Interrupt In 16 bytes)

Audio Stream Interfaces' Alternate Setting List

Interface 1 (Speaker)	Alt 1	2CH, 16Bits PCM	8K,11.025K,16K,22.05K,32K,44.1K,48K
	Alt 2	2CH, 24Bits PCM	8K,11.025K,16K,22.05K,32K,44.1K,48K
	Alt 3	2CH, 16Bits PCM	88.2K,96K
	Alt 4	2CH, 24Bits PCM	88.2K,96K
Interface 2 (MIC In)	Alt 1	2CH, 16Bits PCM	8K,11.025K,16K,22.05K,32K,44.1K,48K
	Alt 2	2CH, 24Bits PCM	8K,11.025K,16K,22.05K,32K,44.1K,48K
	Alt 3	2CH, 16Bits PCM	88.2K,96K
	Alt 4	2CH, 24Bits PCM	88.2K,96K

5.2 CM6533X1 Headset Topology



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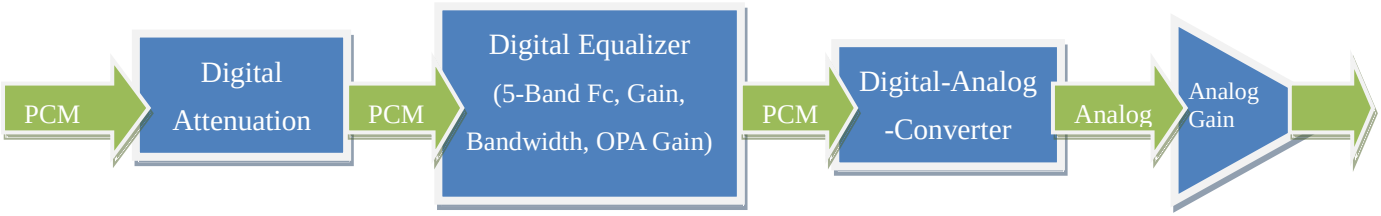
	Alt 3	2CH, 16Bits PCM	88.2K,96K
	Alt 4	2CH, 24Bits PCM	88.2K,96K
	Alt 5	2CH, 16Bits AC3	44.1K,48K
Interface 2 (MIC In)	Alt 1	2CH, 16Bits PCM	8K,11.025K,16K,22.05K,32K,44.1K,48K
	Alt 2	2CH, 24Bits PCM	8K,11.025K,16K,22.05K,32K,44.1K,48K
	Alt 3	2CH, 16Bits PCM	88.2K,96K
	Alt 4	2CH, 24Bits PCM	88.2K,96K

6 Function Description

6.1 Playback Equalizer

6.1.1 5-band equalizer

CM6533/CM6533N/CM6533X1 has integrated five (5)-band hardware digital equalizer (EQ) engine inside the chips to fulfill various application usages. It provides up to four (4)-preset modes on client's product design for different user scenarios including default/music, movies, gaming and communication modes. Clients could also change the gain parameters for each of the preset application EQ mode via embedded FLASH coding. Also, the EQ engine could also be utilized for compensating and fine-tuning the headphone driver for Sound Pressure Level (SPL) performance to a specific preference. In this case, clients could fully customize all EQ coefficients such as center frequency, gain values, and bandwidth to one optimized frequency response curve and setting in terms of the headphone driver and housing's acoustics characteristics, also via embedded FLASH programming.



The EQ engine contains five (5) frequency bands (Fc) of digital filters to conduct transfer functions of the frequency response over the audio band. It allows maximum +-12dB digital gain (Gain) for each band with 0.5dB adjustment per step. Each filter will have its bandwidth (BW) factor between 0 and 1.0.

Fc: Center Frequency, F1~F5, 20<Fc<20K (Hz)

Gain: Digital Frequency Gain, -12dB <= Gain <=+12dB, 0.5dB/step

BW: Filter Bandwidth Factor, 0<BW<1

OPA Gain: Analog Gain Compensation setting for each equalizer mode

The EQ engine already provides four (4)-preset modes/settings based on the same preset F1~F5 center frequencies and OPA gain:

F1 (Bass)= 100Hz

F2 = 350Hz

F3 = 1KHz

F4 = 3.5KHz

F5 (Treble) = 13KHz

With the four (4)-preset EQ modes, clients could use embedded FLASH parameters to change the gain values for each band of the center frequency and hence customize the four (4)-preset EQ curves based on the preset center frequencies and bandwidth. Alternatively, clients could also skip the four (4) preset modes and create a customized EQ curve by changing the center frequencies, gain values and even the bandwidth factors in embedded FLASH parameters to make the headphone sound better or meet some frequency requirements. However, in this case, the product will always use one optimized EQ setting and could not allow users to dynamically change into different preset modes. Clients could also consider reporting Treble/Bass feature unit by embedded FLASH to Windows UAA driver to allow end-users to adjust Bass (F1) and Treble (F5) by themselves. Therefore there are three usage/application scenarios as shown by the summary table below:

3 EQ Usage/Application Scenarios

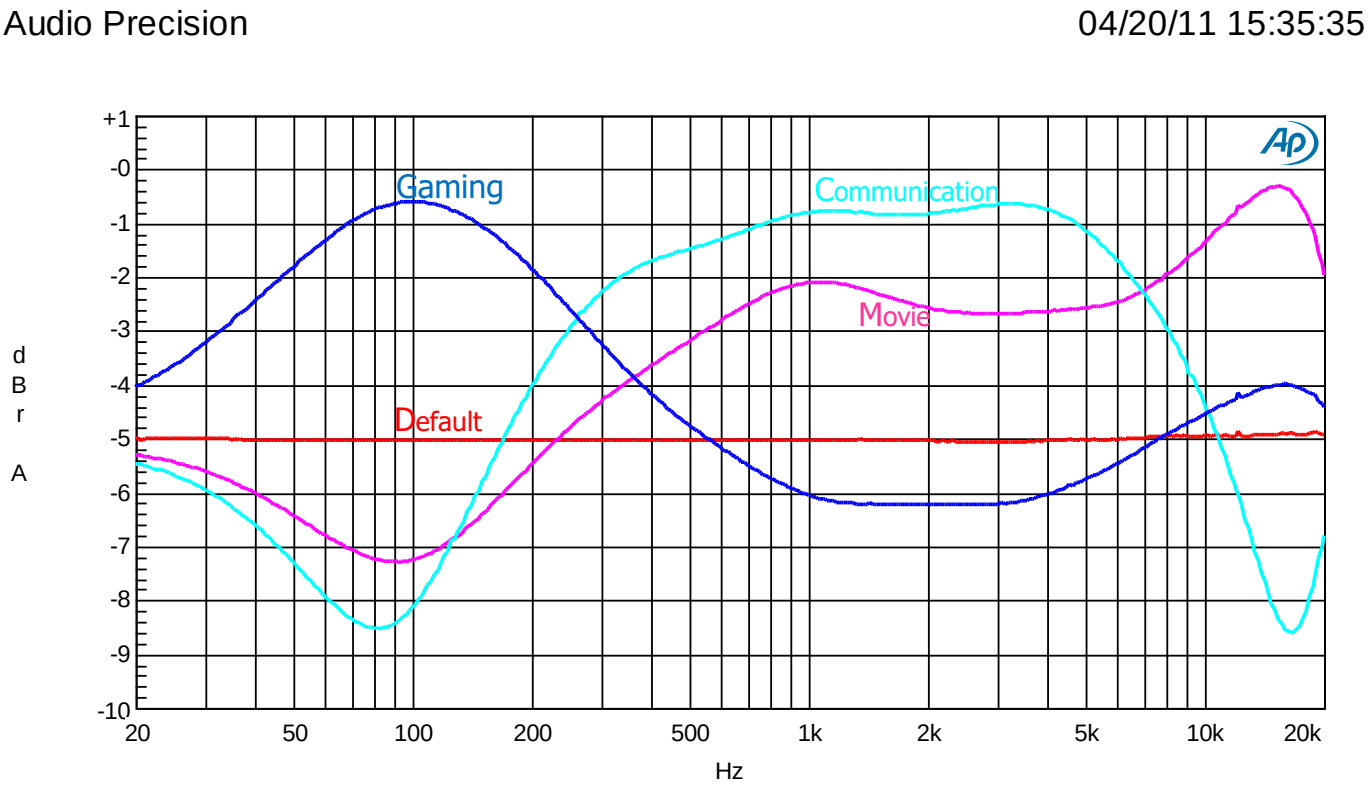
No	Scenario	Gain Value	Center Frequency / Bandwidth Factor	Number of Modes	User Control Type
1	**4 Switchable Presets**	Configurable	Fixed	4	Hardware
2	**Full-Customized EQ**	Configurable	Configurable	1	N.A.
3	**Treble/Bass Feature Unit**	Configurable	Configurable	1	Software

**Note: Hardware user control type means end-users could select which EQ mode they are going to use by a hardware switch/button on the product; software control means they could control the treble/bass gain values by GUI in Windows OS sound device advanced settings.

6.1.2 Four (4) Preset EQ Mode

As mentioned above, EQ engine already provides four (4)-preset EQ modes for different user scenarios/applications. The EQ function default was disable but it can enable via configuration tool or firmware, End users could use the hardware switch on the product (determined by 2 EQ configuration input pins) to dynamically change to different EQ modes. The following shows the frequency response of each mode.

Mode	GPIO8	GPIO7	Color
Default	0	0	----------
Gaming	0	1	----------
Communication	1	0	----------
Movie	1	1	----------



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	2	Anlr.Ampl	Left	00
2	1	Magenta	Solid	2	Anlr.Ampl	Left	11
3	1	Cyan	Solid	2	Anlr.Ampl	Left	10
4	1	Blue	Solid	2	Anlr.Ampl	Left	

DA-EQ-SPDIF_In_DA_Out.at27

6.2 Recording Equalizer

CM6533/CM6533N/CM6533X1 also provide five (5)-band equalizer for the input. It can be used to compensate the frequency response of microphone unit. Clients could fully customize all EQ coefficients (center frequency, gain values, and bandwidth) through embedded FLASH.

6.3 HID Function

6.3.1 HID Interrupt in

Input Data Format:

byte0	always 1 for org HID event report ID
byte1	for defined HID event, each event occupies one bit
byte2	
byte3	start address of returned data (H-start_addr)
byte4	start address of returned data (L-start_addr)
byte5	bit7
	bit6:UART_INT
	bit5:GPI_INT
	bit4:SPIS_INT(slave mode int)
	bit3: SPIM_INT(master mode int)
	bit2:I2CS_INT(slave mode int)
	bit1:I2CM_INT(master mode int)
	bit0: IR_INT
byte6	read data of [start_addr]
byte7	read data of [start_addr+1]
byte8	read data of [start_addr+2]
byte9	read data of [start_addr+3]
byte10	read data of [start_addr+4]
byte11	read data of [start_addr+5]
byte12	read data of [start_addr+6]
byte13	read data of [start_addr+7]
byte14	read data of [start_addr+8]
byte15	read data of [start_addr+9]

6.3.2 HID get_input_report

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h A1	8'h 01 (Get_Report)	16'h 01 01 (Rpt Type + Rpt ID)	16'h 00 03 (Interface)	16'h 00 10 (16 bytes)	Report

**Note: The Start_Addr value in the input reported is put in the Internal Register Address 0xff. Software must set the value of Start_Addr Register to make sure get_input_report can read the proper data desired.

Input Data Format:

byte0	always 1 for org HID event report ID
byte1	for defined HID event, each event occupies one bit
byte2	
byte3	start address of returned data (H-start_addr)
byte4	start address of returned data (L-start_addr)
byte5	bit7
	bit6:UART_INT
	bit5:GPI_INT
	bit4:SPIS_INT(slave mode int)
	bit3: SPIM_INT(master mode int)
	bit2:I2CS_INT(slave mode int)
	bit1:I2CM_INT(master mode int)
	bit0: IR_INT
byte6	read data of [start_addr]
byte7	read data of [start_addr+1]
byte8	read data of [start_addr+2]
byte9	read data of [start_addr+3]
byte10	read data of [start_addr+4]
byte11	read data of [start_addr+5]
byte12	read data of [start_addr+6]
byte13	read data of [start_addr+7]
byte14	read data of [start_addr+8]
byte15	read data of [start_addr+9]

6.3.3 HID set_output_report

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 21	8'h 09 (Set_Report)	16'h 02 01 (Rpt Type + Rpt ID)	16'h 00 03 (Interface)	16'h 00 10 (16 bytes)	Report

**Note: Byte5 is the beginning address of this write sequence.

Output Data Format:

byte0	always 1 for org HID event report ID
byte1	start address of write reg (H-start_addr)
byte2	start address of write reg (L-start_addr)
byte3	effective write/read data length (<=12)
byte4	write data to [start_addr]
byte5	write data to [start_addr+1]
byte6	write data to [start_addr+2]
byte7	write data to [start_addr+3]
byte8	write data to [start_addr+4]
byte9	write data to [start_addr+5]
byte10	write data to [start_addr+6]
byte11	write data to [start_addr+7]
byte12	write data to [start_addr+8]
byte13	write data to [start_addr+9]
byte14	write data to [start_addr+10]
byte15	write data to [start_addr+11]

6.4 Vendor Command Definition

6.4.1 Vendor Command Read

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h C3	8'h 02 (Command 2)	16'h -- -- (Start Address of input Data)	16'h 00 00	16'h 00 - (<=64 bytes)	Data

Input Data Format:

Byte 0	Data of Reg[wValue]
Byte 1	Data of Reg[wValue + 1]
Byte 2	Data of Reg[wValue + 2]
…	…
Byte 63	Data of Reg[wValue + 63]

6.4.2 Vendor Command Write

Command Format:

bmRequestType	bRequest	wValue	wIndex	wLength	Data
8'h 43	8'h 01 (Command 1)	16'h -- -- (Start Address of Output Data)	16'h 00 00	16'h 00 - (<=64 bytes)	Data

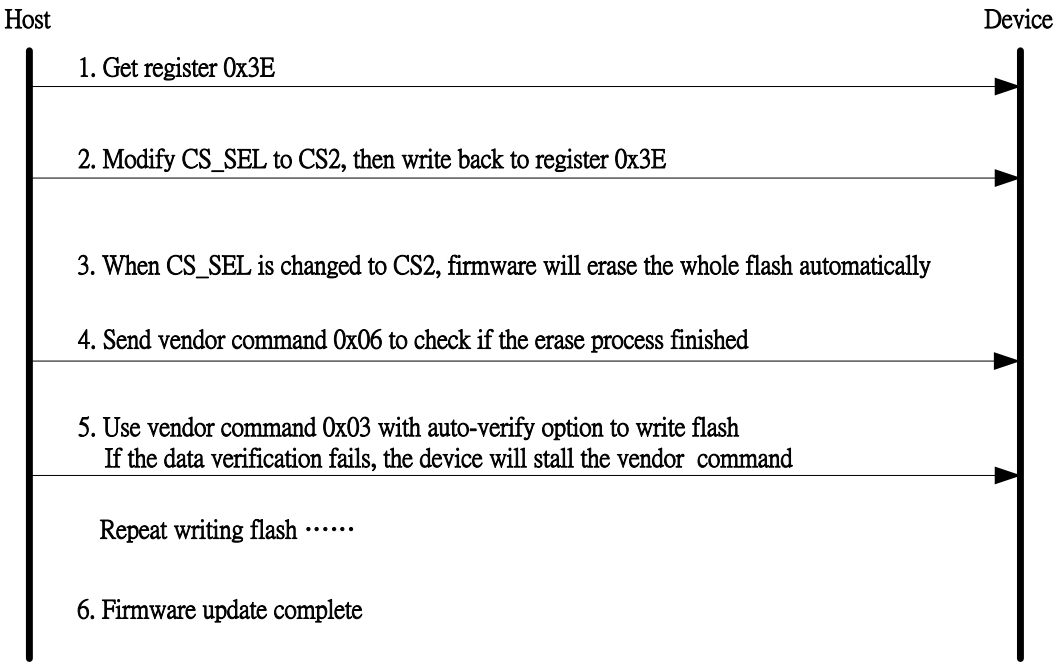
Output Data Format:

Byte 0	Data of Reg[wValue]
Byte 1	Data of Reg[wValue + 1]
Byte 2	Data of Reg[wValue + 2]
…	…
Byte 63	Data of Reg[wValue + 63]

6.4.3 USB Vendor Requests

bmRequestType	bRequest	wValue	wIndex	wLength	Data
0x43 (Vendor Other)	0x01 Register Write	Address	0x0000	Data Length (<=64 bytes)	Data
0xC3 (Vendor Other)	0x02 Register Read	Address	0x0000	Data Length (<=64 bytes)	Data
0x43 (Vendor Other)	0x03 Flash Write	Address	0x0000: Write only 0x0001: Auto Verify	Data Length (<=64 bytes)	Data
0xC3 (Vendor Other)	0x04 Flash Read	Address	0x0000	Data Length (<=64 bytes)	Data
0x43 (Vendor Other)	0x05 Flash Control	0x0000	0x0001: Chip Erase	0x0000	None
		Address	0x0002: Sector Erase		
0xC3 (Vendor Other)	0x06 Flash Control - Get Status	0x0000	0x0000	0x0001	1-byte data 0x01: Erasing 0x00: Ready

6.4.4 Simple Process of Firmware Update



6.5 SPDIF Control Description

6.5.1 SPDIF Frame Description

- Audio format: linear 16 bit default.
- Allowed sampling frequencies (Fs) of the audio:
  - 96KHz from DVD
  - 88.2KHz from DVD
  - 48 kHz from DAT
  - 44.1kHz from CD
- One-way communication: from a transmitter to a receiver.
- Control information:
  - V (validity) bit: indicates if audio sample is valid
  - U (user) bit: user free coding i.e. running time song, track number
  - C (channel status) bit: emphasis, sampling rate and copy permit
  - P (parity) bit: error detection bit to check for good reception

- Coding format: biphase mark except the headers (preambles), for sync purposes
- Bandwidth occupation: 100kHz up to 6Mhz (no DC)
- Signal bitrate as following table:

Sampling Rate (KHz)	SPDIF Bit Rate (MHz, 64*Fs)
96	6.144
88.2	5.6448
48	3.072
44.1	2.8224

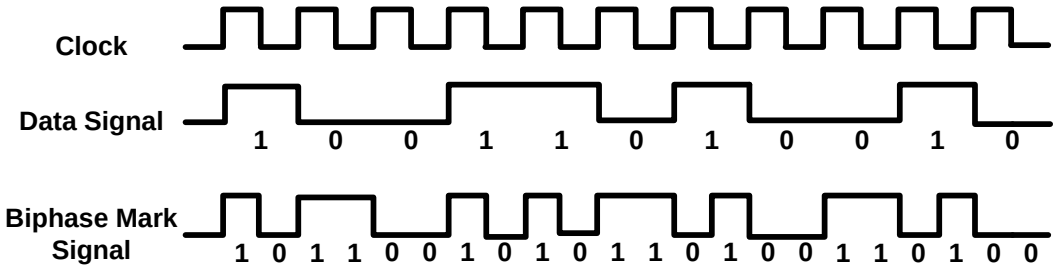


Figure -17 Biphase Mark signal of SPDIF

Preamble	cell-order (last cell "0")	cell-order (last cell "1")
"B"	11101000	00010111
"M"	11100010	00011101
"W"	11100100	00011011

Preamble “B”:

Marks a word containing data for channel A (left) at the start of the data-block.

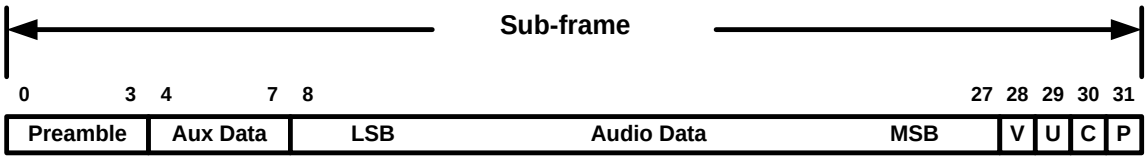
Preamble “M”:

Marks a word with data for channel A that is not at the start of the data-block.

Preamble “W”:

Marks a word containing data for channel B (right, for stereo). When using more than 2 channels, this could also be any other channel (except for A).

The number of subframes that are used depends on the number of channels that is transmitted. A CD-player uses Channels A and B (left/right) and so each frame contains two subframes. A block contains 192 frames and starts with a preamble "B":



V: Valid, U:User-Data, C:Channel-Status-Data, P:Parity-Bit

Figure -1 SPDIF Subframe Description

In each block, 384 bits of channel status and subcode info are transmitted. The Channel-status bits are equal for both subframes, so actually only 192 useful bits are transmitted:

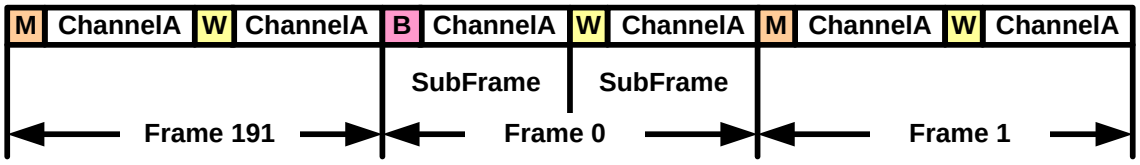


Figure -2 Preamble Description of 192 SPDIF frame

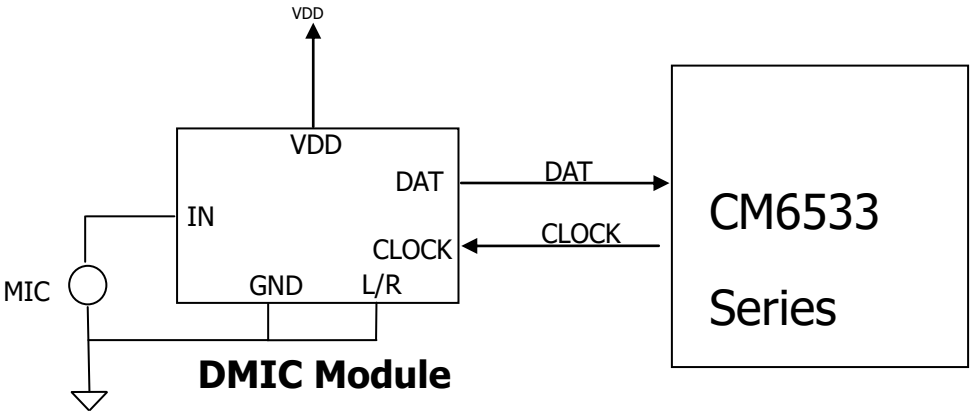
6.5.2 SPDIF Out Channel Status

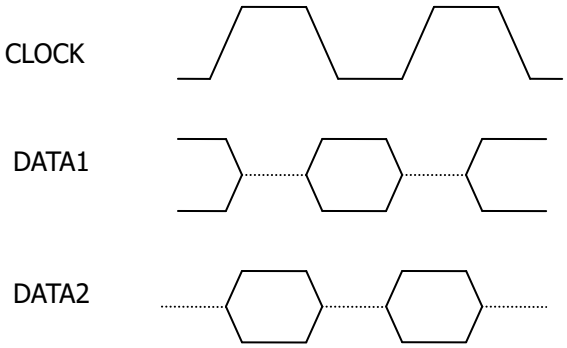
	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7
byte0	**consumer /professional**	**audio/ non-audio**	**copyright**	**pre-emphasis**			**mode**	
default	0(P)	0(P)	1(P)	0(P)	0(fixed)	0(fixed)	0(fixed)	0(fixed)
byte1	**category code**							**L**
default	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)	0(P)
byte2	**source number**				**channel number**			
default	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)	0(fixed)
byte3	**sampling frequency**				**clock accuracy**		**reserved**	
default	0(P)	0(P)	0(P)	0(P)	0(fixed)	0(fixed)	0(fixed)	0(fixed)

**Note: (P) These bits can be programmed by USB HID or USB vendor command

6.6 Digital Microphone

CM6533/CM6533N/CM6533X1 series IC provide digital microphone interface for recording. There are two microphone signals transmitted on a single DATA line from DMIC module. The oversampling bit stream output from DMIC module connects to internal decimation filter to generate PCM output.

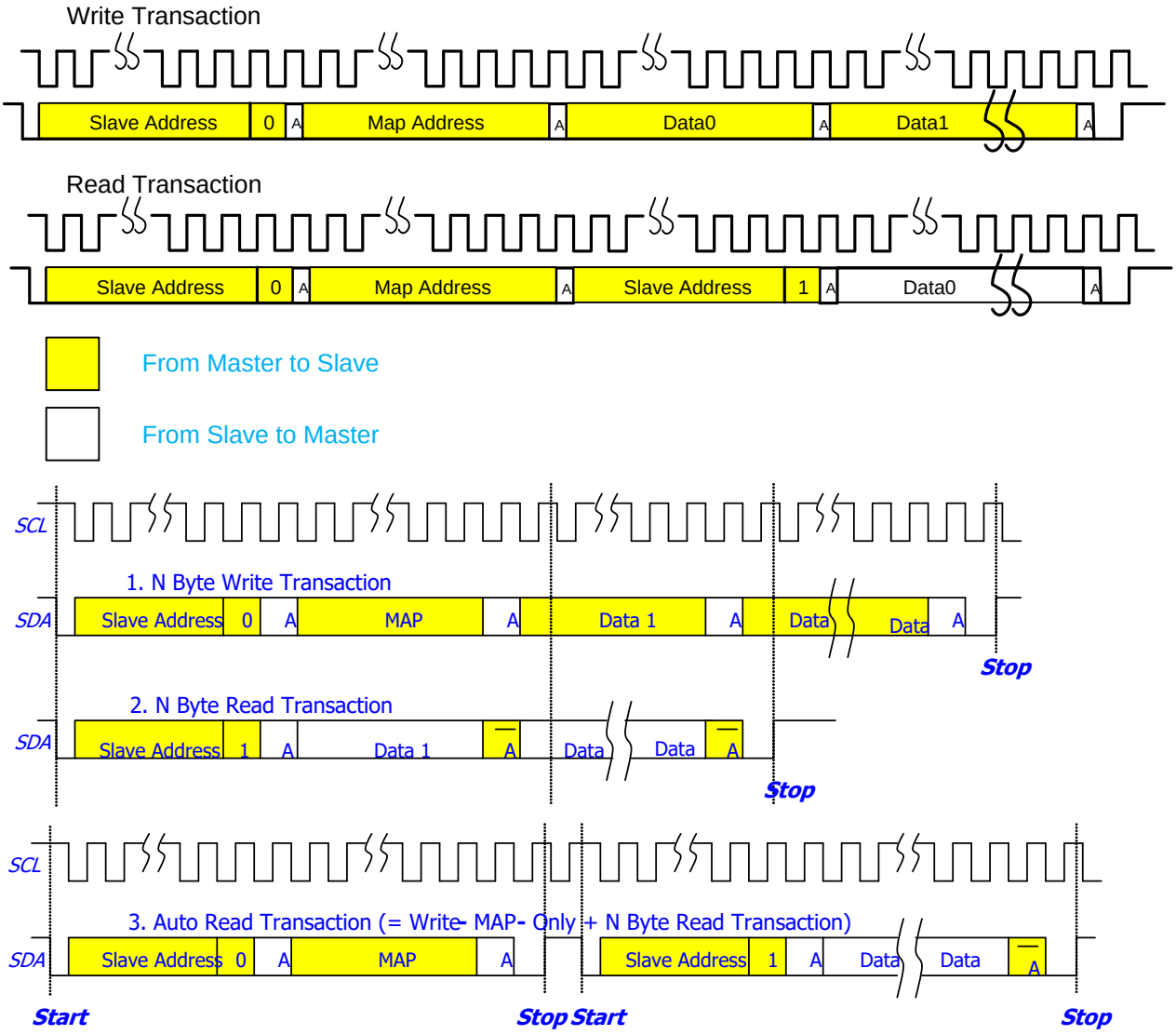




6.7 I2C Interface

6.8.1I2C Master Mode

I2C protocol timing



from master to slave

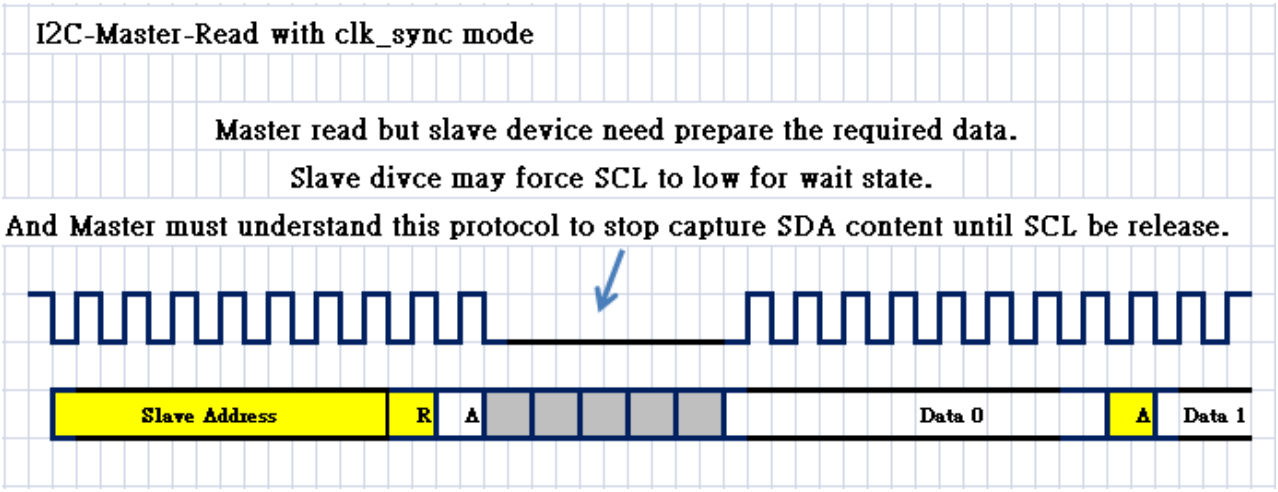
from slave to master

$A =$ *acknowledge* (*SDA Low*)

$\overline{A} =$ *not acknowledge* (*SDA High*)

MAP: Memory Address Pointer
(the target register address
in slave device)

6.8.2I2C-Master Read with clk_sync mode



6.8.3 I2C Master Device Address and Control Register

Address: 0x80

Bits	R/W	Bit Mnemonic	Description	Default
7-1	R/W	SA_reg	The target slave device address.	0xA8 (POR)
0	R/W	SA_reg	1: read, 0: write	1'b0 (POR)

6.8.4 I2C Master Memory Address Pointer (MAP) Register

Address: 0x81

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	MAP_reg	The register low byte address of salve device to be read or written.	8'b0 (POR)

6.8.5 I2C Master Memory Address Pointer (MAP2) Register

Address: 0x82

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	MAP2_reg	The register high byte address of salve device to be read or written.	8'b0 (POR)

6.8.6 I2C Master Data Register

Address: 0x83 ~ 0x92

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	data0~ data15	The data read from or written to the slave device.	8'b0 (POR)

6.8.7 I2C Master Control and Status Register 0

Address: 0x93

Bits	R/W	Bit Mnemonic	Description	Default
7-0	R/W	i2c_ctrl_reg1	Data length of read/write command 8'h1: 1 byte, minimum length 8'h2: 2 bytes … 8'hFE: 254 bytes 8'hFF: 256 bytes, maximum length	0x14 (POR)

6.8.8 I2C Master Control and Status Register 1

Address: 0x94

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	i2c_start	Trigger I2C read/write command 0->1: trigger I2C read/write command. 1->0: I2C interface had completed current task. 0 : I2C interface is idle and ready for work. 1 : I2C interface is running.	1'b0 (POR)
6	R/W	i2c_reset	Reset I2C interface 0 : Not reset I2C interface 1 : Reset I2C interface	1'b0 (POR)
5	R/W	map_len	MAP length 0 : 8-bit MAP 1 : 16-bit MAP	1'b0 (POR)
4	R/W	clk_sync	Clock Synchronization 0: off 1: on, when slave pull-down SCLK, master would pause	1'b1 (POR)
3	R/W	fast_std	I2C speed mode 0 : Standard mode, 100kHz 1 : Fast mode, 400kHz	1'b0 (POR)
2	R/W	map_only	MAP only write command 0 : Write command. 1 : MAP only write command.	1'b0 (POR)
1	R/W	auto_rd	Auto read command 0 : Read command. 1 : Auto read command.	1'b1 (POR)

0	R	i2c_ctrl_reg2	Slave NACK error occur 1 : No error 2 : Slave NACK error occur	1'b0 (POR)

*Note: Write-MAP-Only: An operation which only writes the register MAP the salve device

6.8.9 I2C Master Download Control and Status Register

Address: 0x95

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	I2c_mas_sel	I2C master/slave select	1'b1 (POR)
6	RO WO	Flag_8byte Flag_ready	Flag_8byte (RO): Flag to status I2C is transmitting at 1st 8 bytes data or 2nd 8 bytes data. If the flag index it's transmitting the 2nd 8 bytes data, then F/W can prepare the next 8 bytes data into 1st 8byte buffer. Flag_ready (WO): Flag to index F/W has prepared next data ready. After prepare done, F/W need set this bit to index the data had been written. If F/W didn't catch on when all data has been transmitted, the I2C clock would be keep low to till it ready.	1'b0 (POR)
5:4	R/W	LD_BLOCK	Download to which block of SRAM. 00: Load to 1st 8KB block. 01: Load to 2nd 8KB block. 10: Load to 3rd 8KB block. 11: Load to 4th 8KB block.	2'b00 (POR)
3	RO	CHKSUM_ERR	Check sum Error 1. If in LD_PHASE, the check sum value was calculated by I2C load data. 2. If in CHK_PHASE, the check sum value was calculated by SRAM read content.	1'b0
2	RO	CHK_FINISH	CHECK phase done 1: finish download data CHECK	1'b0
1	R/W	CHK_PHASE	MCU select CHECK phase to read SRAM data for check-sum check. 1: enable (after disable LD_PHASE) 0: set 0 after complete	1'b0 (POR)
0	R/W	LD_PHASE	MCU select LOAD phase to access SRAM from download. 1: enable 0: set 0 after complete	1'b0 (POR)

6.8.10 I2C Master Clock Period Setting Register

Address: 0x96

Bits	R/W	Bit Mnemonic	Description	Default
7	W	CHG_ENABLE	MCU can program I2C clock; 1'b1: enable	1'b0 (POR)
6	R/W	LD_SEL	MCU download select 1'b0 : SPI download 1'b1 : I2C download	1'b0 (POR)
5-0	W	CHG_FREQ	Set I2C-master clock period. The clock period=83.3*5*(CHG_FREQ+1) Ex: CHG_FREQ = 6'd48 I2C Clock Period=83.3*5*(48+1)=20408ns HW limitation CHG_FREQ >= 6'h3	6'h0 (POR)

6.8.11 I2C Slave Mode

"7-bit slave address = 7'b0001000 to 7'b0001011"

CM6533/CM6533N/CM6533X1 can serves as a slave device with bit rate up to 400Kbps (fast mode). External MCU can write data to CM6533/CM6533N/CM6533X1 or read data from CM6533/CM6533N/CM6533X1 (No Size limitation in I2C Interface). Since host side and MCU can both access to all the internal registers.

CM6533/CM6533N/CM6533X1 will transfer an interrupt to internal MCU until the INT bit of I2C control Register have been clean by internal MCU. The interrupt will be trigger when write transaction done or detect read-slave-address.

The main usage of 2-wire slave bus is to become the interface between the CM6533/CM6533N/CM6533X1 and a external micro control unit (EMCU).

6.8.12 I2C Slave Data Register

Address: 30~33h

Bits	R/W	Bit Mnemonic	Description	Default
31:0	R/W	MCU_data0~F	The data received from or transmitted to master device. This register cannot be written when 2-wire slave serial bus status is busy.	0000h (POR)

6.8.13 I2C Slave Status Register

Address: 34~35h

Bits	R/W	Bit Mnemonic	Description	Default
15			Reserved	1b
14:12	R		Reserved	0h
11	R/W	Thld_int_mask	Threshold interrupt mask: 1: mask; 0: non-mask ; default :0	0b (POR)
10	R	Write_data_ready	Interrupt happened, auto-cleared after read	0b (POR)
9	R/W	I2c_s_reset	0: 2-wire serial bus in normal operation (default) 1: 2-wire serial bus in reset state	0b (POR)
8	R/W	Dri_tran_st	**initiated transaction status** 1: The last initiated transaction failed, write 1 to clear.	0b (POR)
7	R/W	Rd_tran_st	**Read transaction status** 1: a new read transaction received, write 1 to clear.	0b (POR)
6	R/W	Wr_tran_st	**Write transaction status** 1: a new write transaction received, write 1 to clear.	0b (POR)
5:1	R	Data_len	The data length of the last write transaction received, 00000: 1 byte (MAP only) 00001: 2 byte (MAP + 1 byte data) 00010: 3 byte (MAP + 2 byte data) 00011: 4 byte (MAP + 3 byte data) 00100: 5 byte (MAP + 4 byte data) … 01111: 16 byte (MAP + 15 byte data) . 10000: 17 byte (MAP + 16 byte data) Others: Reserved	0b (POR)

0	R	busy	The 2-wire serial bus status, 0: idle, 1: busy	0b (POR)

**Note: When I2C issue interrupt to MCU, MCU needs to read the data numbers that threshold data count specified. And waits another interrupt until the total data transfer completed.

6.8.14 I2C Slave Memory Address Pointer(MAP) Register

Address: 36h

Bits	R/W	Bit Mnemonic	Description	Default
7:0	R/W	MCU_MAP	The memory addresses of the read or write transactions from MCU. Address 0 is reserved for initiated transaction.	00h (POR)

6.8.15 I2C Slave Status Register

Address: 37h

Bits	R/W	Bit Mnemonic	Description	Default
7	R/W	Sync_en	**Synchronization Enable** 1: enable (the synchronization selection bit will decide the method adopted). 0: disable (MCU and ARC should guarantee no data lost themselves).	1b (POR)
6	R/W	Int_polarity	The polarity control of pin INT_OUT (initiated transaction interrupt), 0: high active, 1: low active	0b (POR)
5:4	R/W	Slave_addr	Slave Device Address 00: select 0001000 (10h) as slave address 01: select 0001001 (12h) as slave address 10: select 0001010 (14h) as slave address 11: select 0001011 (16h) as slave address	01b (POR)
3	R/W	Sync_sel	**Synchronization Method Selection** 1: Data synchronization. When this bit is one, if the current transaction has not been serviced by ARC, the clock line of the 2-wire serial bus will be pulled low. Under this situation, the MCU cannot start a new transaction or continue the current read transaction until the clock line goes back to high. 0: Ready pin synchronization. If the MCU cannot support open drain 2-wire serial bus, this bit should be set to zero. Under this situation, the MCU cannot start a new transaction or continue the current read transaction until the pin XSLAVE_RDY goes high to signal that the driver has serviced the current transaction. Driver should use “driver acknowledge” to signal the processing of the current transaction is completed.	1b (POR)
2	R/W	Int_mask	**Interrupt Mask** 0: interrupt will happen at a read/write transaction received or a driver initiated transaction failed 1: interrupt will not happen	0b (POR)
1	R/W	Dri_init_tran	**Driver initiated transaction** Write 1 to start Driver initiated transaction. This bit is cleared automatically, after ARC initiated transaction starts. The ARC initiated transaction should be issued only when the 2-wire slave serial bus is idle. Otherwise, it will be ignored. The ARC initiated transaction will cause pin INT_OUT to send out an interrupt for MCU.	0b (POR)

			After MCU responded with a Write-MAP-Address-0-Only transaction and a subsequent read transaction, interrupt INT_OUT will be de-asserted. However, if the MCU does not act as what is expected (a write MAP-Address-0-Only transaction and a subsequent read transaction), the interrupt INT_OUT will be still de-asserted, but the ARC initiated transaction status is used to signal a fail status to ARC. In this case, the driver should consider to repeat the failed Driver initiated transaction again.	
0	R/W	ack	Driver Acknowledge means driver has processed the current transaction. Write 1 to acknowledge. This bit will be cleared automatically.	0b (POR)

I2C example for Master mode:

Write 2 bytes:

(Slave address = 92, MAP address = 01, Data = 55, AA)

Write 0x80 = 92 (Slave address)

Write 0x81 = 01 (MAP address)

Write 0x83~0x84 = 55 AA (Data register)

Write 0x93 = 02 (Data length 2 bytes)

Write 0x94 = 92 (I2C start)

Read 2 bytes:

(Slave address = 92, MAP address = 01)

Write 0x80 = 93 (Slave address)

Write 0x81 = 01 (MAP address)

Write 0x93 = 02 (Data length 2 bytes)

Write 0x94 = 92 (I2C start)

Read 0x83~0x84 (Data register)

6.9 SPI Interface

The SPI interface is used to transfer control data between the CM6533/CM6533N/CM6533X1 and external codec.

In a SPI interface there is only one central clock source producing a reference clock to which SPI data processing is synchronized. This clock is often referred to as the MCU clock, e.g. for SPI clock 12Mhz, When the MCU clock equal 48Mhz and SPI clock div4.

Example	MCU CLK 0xB5[2:0]	48M(3'b100)	24M(3'b011)	12M(3'b010)	6M(3'b001)	3M(3'b000)
SPI clock 0x3D[4:3]=00(div4)	SPI CLK	12M	6M	3M	1.5M	750k
SPI clock 0x3D[4:3]=01(div12)	SPI CLK	4M	2M	1M	500k	250k
SPI clock 0x3D[4:3]=10(div16)	SPI CLK	3M	1.5M	769k	375k	187.5k
SPI clock 0x3D[4:3]=11(div20)	SPI CLK	2.4M	1.2M	625k	300k	150k

6.9.1 SPI Registers Descriptions

Address: 38~3bh

Bits	R/W	Bit Mnemonic	Description	default
31-0	R/W	Data0~Data3	The data (which include address, r/w, and data bits) written to or read from the codec. The bits in this register should be interpreted according to the individual codec. The content of this register, after a write operation completes, has no meaning. The content of this register, after a read operation completes, should reference the document of individual codec to see how many bits in this register is valid.	0x0000 0000 (POR)

6.9.2 SPI Control Register 0

Address: 3ch

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	slv_mst	SPI master/slave mode 0: master mode 1: slave mode	1'b1 (POR)
6	R/W	long_mode	SPI slave address length 0: 1-byte address 1: 2-byte address	1'b1 (POR)
5	--	--	Reserved	1'b0 (POR)
4	--	--	Reserved	1'b0 (POR)
3	R/W	si_mode	Serial interface mode 0: normal SPI mode 1: Serial interface mode	1'b0 (POR)
2	R/W	si_mode_rs	Serial interface RS/A0 output 0: RS/A0==0 for 8th bit 1: RS/A0==1 for 8th bit	1'b0 (POR)
1	RO	flag_rd	Flag read 0: mcu can't read spi data 1:mcu need to read spi data	1'b0
0	RO	flag_wr	Flag write 0: mcu can't write spi data 1:mcu need to write spi data	1'b0

6.9.3 SPI Control Register 1

Address: 3dh

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	spi_start	Trigger SPI read/write command 0->1: trigger SPI read/write command. 1->0: SPI interface had completed current task. 0 : SPI interface is idle and ready for work. 1 : SPI interface is running.	1'b0 (POR)
6	R/W	spi_lh_edge	SPI CEN control 0: codec latch control data at SPI clock low (default) 1: codec latch control data at SPI clock high	1'b1 (POR)
5	R/W	Spi_flash_rd_wr	SPI Flash Read/Write 0:spi flash read (default) 1:spi flash write	1'b0 (POR)
4-3	R/W	frq_sel	SPI clock period 2'b00: by MCU clk div 4 2'b01: by MCU clk div 12 2'b10: by MCU clk div 16 2'b11: by MCU clk div 20	2'b0 (POR)
2	R/W	first_leading_bit	First data bit of 2-bit leading mode	1'b0(POR)
1	R/W	second_leading_bit	Second data bit of 2-bit leading mode	1'b0(POR)
0	R/W	leading_bit_mode	RA8815 2-bit leading mode 0: No leading bits 1: 2-bit leading for each transaction	1'b0 (POR)

6.9.4 SPI Interrupt

Address: 3eh

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	CPOL	Clock Polarity	1'b1(POR)
6	R/W	CPHA	Clock Phase	1'b1(POR)
5-4	R/W	CS_SEL	SPI CS Select 00: CS0 01: CS1 10: CS2(Default) 11: CS2	2'b10(POR)
3	RO	slv_hid	SPI slave flag to HID interrupt 0: access to internal register 1: flag to HID interrupt	1'b0 (POR)
2	RO	slv_rw	SPI slave read/write flag 0: read 1: write	1'b0 (POR)
1	R/W	slv_int_en	SPI slave interrupt 0: no interrupt 1: interrupt (Default) Ext MCU can program this bit to make slave mode interrupt	1'b1 (POR)
0	R/W	mst_int_en	SPI master interrupt enable 0: disable 1: enable (Default) Control HW to make master mode interrupt	1'b1 (POR)

**Note:
1. Bit [1]: When SPI interface is slave mode, SPI interrupt happened when bit [1] ==1, which is written by external MPU via SPI. Interrupt (HID) would be cleaned once address 0x10 was written.
2. Bit [0]: When SPI interface is master mode, SPI interrupt happened when bit [0] ==1 and every SPI master command completed. Interrupt (HID) would be cleaned once address 0x10 was written.

6.9.5 SPI Control Register 3

Address: 3fh

Bits	R/W	Bit Mnemonic	Description	default
7-0	R/W	data_len	The data length of read/write, 0000_0000: Reserved 0000_0001: 1 bytes 0000_0010: 2 bytes 0000_0011: 3 bytes . . . 1111_1111:255 bytes	8'd0 (POR)

SPI example for master mode:

Write 3 bytes:

(Address = 92, DATA = 55,AA)

Write 0x38~0x3A = 92 55 AA (Data register)

Write 0x3F = 03 (Write 3 bytes length)

Write 0x3D = A0 (SPI start)

Read 3 bytes:

(Address = 92)

Write 0x38= 92 (Data register)

Write 0x3F = 03 (Read 3 bytes length)

Write 0x3D = 80 (SPI start)

Read 0x38~0x3A

6.9 GPIO

6.9.1GPO Data Register

Address Offset: C0-C1h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPO_0_reg GPO_1_reg	GPO data register which represents	16'h0 (POR)

6.9.2GPI Data Register

Address Offset: C2-C3h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R		GPI data register which represents	16'h0 (POR)

6.9.3GPIO Direction Control Register

Address Offset: C4-C5h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPOE_0 GPOE_1	GPIO output enable register which represents for pin XGPIO[15:0] 1: the corresponding pins are used as output 0: the corresponding pins are used as input	16'h0 (POR)

6.9.4GPIO Interrupt Enable Mask Register

Address Offset: C6-C7h

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPI_EN	GPIO_E, GPIO interrupt enable mask which represents for pins, XGPIO[15:0] 1: enable, 0: disable	16'h0 (POR)

6.9.5GPIO Debouncing Register

Address Offset: C8-C9h
Default Value: 0000h (MSB -> LSB)

Bits	R/W	Bit Mnemonic	Description	Default
15:0	R/W	GPI_Deb	Enable the clock scale of mini-second (32 ms) for de-bouncing, default 1 1: enable, 0: disable	16'h0 (POR)

6.9.6GPI Remote Choose

Address Offset: 0xE2~E3h

Bits	R/W	Bit Mnemonic	Description	default
15:0	R/W	GPI_RWL GPI_RWH	D0==1'b1:GPI[0] remote wake up enable D1==1'b1:GPI[1] remote wake up enable D2==1'b1:GPI[2] remote wake up enable D3==1'b1:GPI[3] remote wake up enable D4==1'b1:GPI[4] remote wake up enable D5==1'b1:GPI[5] remote wake up enable D6==1'b1:GPI[6] remote wake up enable D7==1'b1:GPI[7] remote wake up enable D8==1'b1:GPI[8] remote wake up enable D9==1'b1:GPI[9] remote wake up enable D10==1'b1:GPI[10] remote wake up enable D11==1'b1:GPI[11] remote wake up enable D12==1'b1:GPI[12] remote wake up enable D13==1'b1:GPI[13] remote wake up enable D14==1'b1:GPI[14] remote wake up enable D15==1'b1:GPI[15] remote wake up enable	16'h0 (POR)

6.9.7GPIO Pull-up/Down

Address Offset: 0xE4

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	GPIO_PD0[7]	GPIO_7 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
6	R/W	GPIO_PD0[6]	GPIO_6 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD0[5]	GPIO_5 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD0[4]	GPIO_4 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD0[3]	GPIO_3 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD0[2]	GPIO_2 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD0[1]	GPIO_1 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD0[0]	GPIO_0 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)

Address Offset: 0xE5

Bits	R/W	Bit Mnemonic	Description	default
7	R/W	GPIO_PD1[7]	GPIO_15 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1 (POR)
6	R/W	GPIO_PD1[6]	GPIO_14 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD1[5]	GPIO_13 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD1[4]	GPIO_12 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD1[3]	GPIO_11 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD1[2]	GPIO_10 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD1[1]	GPIO_9 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD1[0]	GPIO_8 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)

Address Offset: 0xE6

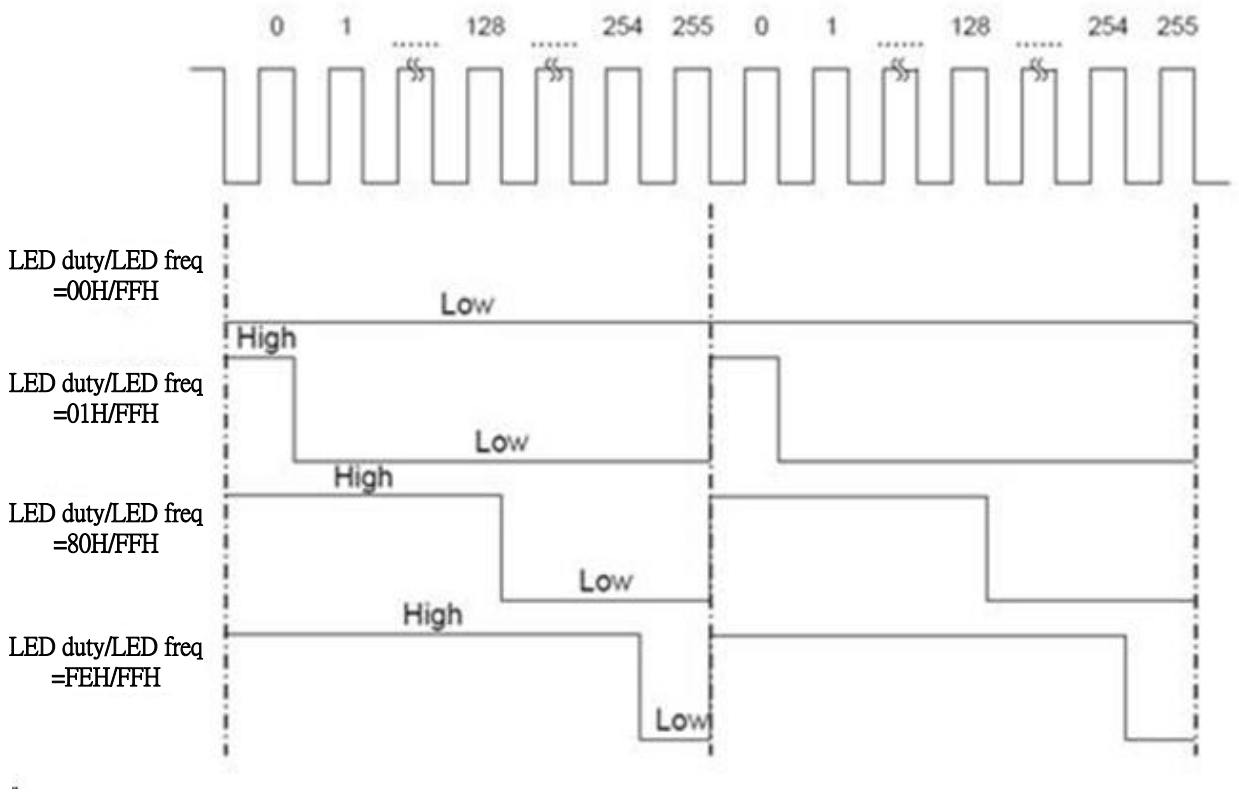
Bits	R/W	Bit Mnemonic	Description	default
7	R/W	GPIO_PD2[7]	GPIO23 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1 (POR)
6	R/W	GPIO_PD2[6]	GPIO_22 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
5	R/W	GPIO_PD2[5]	GPIO_21 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
4	R/W	GPIO_PD2[4]	GPIO_20 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
3	R/W	GPIO_PD2[3]	GPIO_19 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
2	R/W	GPIO_PD2[2]	GPIO_18 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
1	R/W	GPIO_PD2[1]	GPIO_17 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)
0	R/W	GPIO_PD2[0]	GPIO_16 pad control 1'b1 : floating ; 1'b0 : 75k pull up	1'b1(POR)

6.10 Tri-Colored LED Control Setting

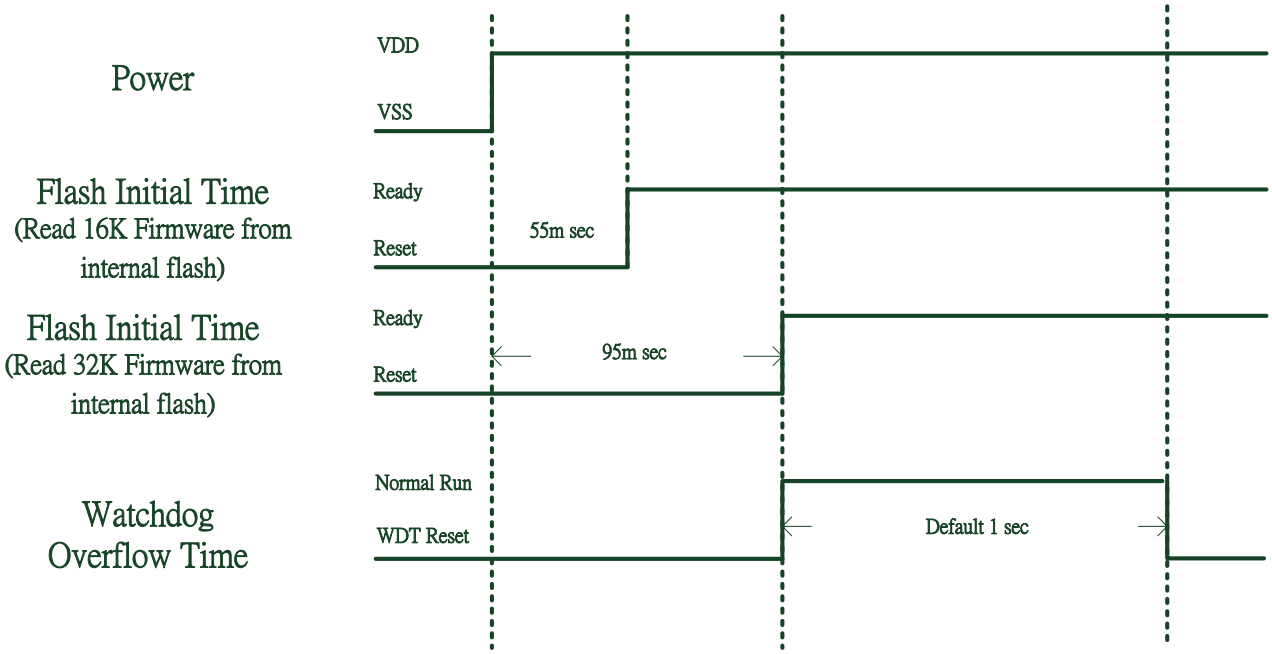
PWM function is generated by LED counter and output the PWM signal to GPIO pin. The 8-bit counter counts modulus 256 controlled by LED freq, LED duty register. The LED unit register controls PWM resolution. When the LED freq register value is equal to the LED duty register (high), the PWM output also goes high. When the LED freq, LED duty register reaches zero, the PWM output is forced to go low. The low-to-high ratio (duty) of the PWM output is LED duty/LED freq.

LED duty	LED freq	LED unit (256 step)	PWM duty range
00H	FFH	00:10.5ms 01:5.45ms 10:2.73ms 11:1.36ms	00H/FFH ~FEH/FFH
01H	FFH		
80H	FFH		
FEH	FFH		

The Output Duty of PWM has different timings. Duty range is from 0/256~255/256.



6.11 Reset



6.11.1 Watchdog Reset Timer

The watchdog timer is a 15-bit counter that is incremented every 24 or 384 clock cycles. It is used to provide the system supervision in case of software or hardware upset. If the software was not able to refresh the Watchdog Timer after 786336 or 12581376 clock cycles (65ms or 1s when using 12MHz clock), an internal reset is generated.

7 CM6533X1 Xear™ Sound Processing

Xear™ is the core name of C-Media sound effect technology; it includes audio and voice processing. These sections describe the main sound processing on CM6533X1.

7.1 Xear™ Surround Headphone

Xear™ Surround Headphone creates a realistic 5.1/7.1CH surround sound field over stereo headphones. Combined with 3D sound processing in games, gamers could enjoy amazing 3D gaming sound experience and combat advantages. It also delivers natural sound space for stereo music as real as playback on speakers for longer listening on headphones without fatigue.

Xear Surround Headphone provides music/gaming and movie modes for different applications. User can switch the surround mode to get the best effect in different situation.

7.2 Xear™ Software 10 Band Equalizer

It provides 10-band EQ function, User will able to adjust the EQ band by manual and create customize preset items or click on the preset EQ mode. There are 12 preset modes such as Bass, Treble, Live, Rock, Jazz, etc.

7.3 Xear™ Audio Brilliant

Xear™ Audio Brilliant restores the clarity and details of compressed audio in music, movies and games (MP3, WMA, AAC, AC3, etc.). Make the sound more dynamic and brilliant. Audio compression algorithms will usually sacrifice some audio frequency signals. It might result in flat, thin, and lifeless sounds. Audio Brilliant recreates the subtleties of the original performance.

7.4 Xear™ Dynamic Bass

Xear™ Dynamic Bass reproduces the deep and vibrating bass in music, games, and movies, and music even over small speaker/headphone drivers and enclosures. Applying psychoacoustic techniques to make users feel stronger bass signals of drums, bass guitars, explosions, automobile engines, etc.

It can overcome small speaker driver's poor bass limitation without damage.

7.5 Xear™ Voice Clarity

Xear™ Voice Clarity can increase the clarity, intelligibility, and prominence of receiving voice in games, VOIP, music, or movies without suppressing or changing other background audio. Adjustable voice clarity levels make you hear the voice more clearly or learn language more easily.

Optional background stationary noise suppression in communication simultaneously.

7.6 Xear™ Smart Volume

Xear™ Smart Volume normalizes sound levels of music, Internet AV clips, and movies to reduce the probabilities that require volume adjustments on Docking Speakers and PCs.

7.7 Xear™ Surround Max

Xear Surround Max can expand stereo audio content to each output channel.

When you playing mp3 music file and enable this function, you can hear music from each speaker (8 speakers).

7.8 Xear™ Magic Voice

Xear™ Magic Voice is a great feature for disguising your voice (using cartoon/monster/male/female effects) for VOIP and online gaming Applications.

7.9 Xear™ Environmental Noise Cancellation

Xear™ VoClear Environmental Noise Cancellation (ENC) utilizes dual microphone signal capturing via gaming headset, which could effectively identify the dynamic ambient noises, and cancel them out significantly even in noisy gaming environments (Internet Café, game champion spot, living room, etc.) to ensure the far-end teammate could hear your voice clearly over the Internet or LAN, and create team gaming advantages.

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Test conditions: DV50 = 5V, AV50 = 5V, DGND =0V, TA=+25°C

Parameter	Symbol	Min.	Typ	Max.	Unit
Storge temperature	T_S	-25	-	150	°C
Operating ambient temperature	T_A	-15	25	70	°C
Digital supply voltage(DV50)		4.5	5.0	5.5	V
Analog supply voltage(AV50)		4.5	5.0	5.5	V
I/O pin voltage	-	GND	-	3.3	V
ESD (Body mode)			±4000		V
ESD (Machine mode)			±200		V

8.2 Recommended Operation Conditions

Parameter	Symbol	Min.	Typ	Max.	Unit
Digital supply voltage(DV50)	-		5		V
Analog supply voltage(AV50)			5		V
Operating ambient temperature			25		°C
MCU Clock	-		12.000		MHz

8.3 Power Consumption

Test Conditions: DV50=5V, AV50 = 5V, DGND =0V, TA=+25°C, MCU Clock = 12MHz.
Sample Rate=48kHz, 16Bits, Operation: HP-Out Playback+Mic-In Recording, EQ disable, Spdif out disable, No loading

Parameter	Min.	Typ	Max.	Unit
Total power consumption (including Playback and Recording)	-	65.9 = Digital 27.9mA + Analog 38mA	-	mA
Standby power consumption (excluding Playback and Recording)	-	64	-	mA
Suspend mode power consumption	-	2.4	-	mA

8.4 DC Characteristics

Test Conditions: DV50=5V, V_{DD} = 3.3V, DGND =0V, TA=+25°C, V_{DD} = 3.3V

Parameter	Symbol	Min.	Typ	Max.	Unit
Operation Voltage range	DVDD	4.5	5	5.5	V
DC Input voltage range (GPIO,I2C,SPI,SPDIF)	DCVin	-0.3		5.5	V
Input High-level voltage (GPIO,I2C,SPI,SPDIF)	Vih	2	2		V
Input Low-level voltage (GPIO,I2C,SPI,SPDIF)	Vil		0.8	0.8	V
Output High-level voltage (GPIO,I2C,SPI,SPDIF)	Voh	2.4	-	3.6	V
Output Low-level voltage (GPIO,I2C,SPI,SPDIF)	Vol	0	-	0.4	V
Output source current (GPIO, I2C,SPI,SPDIF)	IOH		8		mA
Output sink current (GPIO, I2C,SPI,SPDIF)	IOL		8		mA
VREG33 driver current	IVREG			10	mA

**Note: DVDD18,AVDD36,AV42_DA,AV36_DAL,AV36_DAR without current drive capacity

8.5 Analog Audio

Parameter	Symbol	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max		
Signal Reference Voltage	XVAG	XVAG	1.65	1.75	1.85	V	RLoad>> 10 MΩ
Microphone Input Clipping Level (at minimum input volume, i.e., 0 dB)	VMI	XMICL XMICR			2.828	Vpp	Volume = 0 dB
Analog Output Voltage AC	VAO	XLNOUTL XLNOUTR			2.828	Vpp	
Microphone Input Impedance	MII	XMICL XMICR	20		45	kΩ	
Microphone A-A Input Impedance	MAII	XMICL XMICR		20		kΩ	
Headphone Output Impedance	HPOI	XLNOUTL XLNOUTR		32		Ω	Volume = 0 dB

8.6 USB Transceiver

Parameter	Symbol	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max		
Regulator Voltage	XV33	XV33	3.0	3.3	3.6	V	CL =10uF
Driver Output Impedance including the 22ΩExternal Serial Resistor	RO	D+/D−	24		40	Ω	static, LOW or HIGH
Rise and Fall Times	tr/tf		3	10	19	ns	CL = 50 pF, driver mode
Rise/Fall Time Matching	MA_TRTF		90		110	%	CL = 50 pF, driver mode
Crossover Voltage	VXOVER		1.30	1.75	2.0	V	CL = 50 pF, driver mode
Differential Receiver Common-Mode Range	VCM_DREC		0.8		2.5	V	
Single-ended Receiver Threshold Voltage	VT_SREC		0.8		2.0	V	
Switchable Pull-up Resistor	RPU	VREG, D+		1.5		kΩ	

8.7 Microphone Bias

Parameter	Symbol	Pin Name	Limit Values			Unit	Test Conditions
			Min.	Typ.	Max		
Open Circuit Voltage Microphone Bias	VMICBIAS	MICBIAS	2.55	2.75	2.95	V	
Output Current Microphone Bias	IMICBIAS	MICBIAS			1.25	mA	RMIN=2.2kΩ
Output Impedance Microphone Bias	ROUTMICB	MICBIAS	600	650	700	Ω	
Power Supply Rejection Ratio for Microphone Bias	PSRRMICB	AVDD, MICBIAS		100		dB	Internal regulators active, at maximum load current (0.5 mA), 1 kHz sine wave at 100 mVrms

9 Audio Performance

9.1 DAC Audio Quality

TA=25℃, DV50=5V, AV50=5V, Equalizer disabled, Typical Fs/Bit-depth=48KHz/16bit (except remarked in Test Conditions), Master Volume= 0dB, Platform=DELL Desktop 32BWS02, 4G RAM, Windows 8.1 CHT

Items	Test Conditions	Test Values			Unit
		Min.	Typ.	Max.	
Full Scale Output Voltage	10KΩ loading		1.04		Vrms
	32Ω loading		0.99		Vrms
THD+N @ -3dB Full Scale	10KΩ loading, 20~20KHz		-87		dB
	32Ω loading, 20~20KHz	-86.7	-71 (@1KHZ)		dB
Dynamic Range (with -60dBFs Output Signal)	10KΩ loading, A-Weighted		91		dB
	32Ω loading, A-Weighted		92		dB
Noise Level (SNR, with -96dBFs Output Signal)	10KΩ loading, A-Weighted		93		dB
	32Ω loading, A-Weighted		93		dB
Inter-Channel Phase Delay	100Hz ~ 20kHz	+0.01		+1.01	Deg
Sampling Frequency Accuracy	10KΩ loading	-0.0046		+0.0078	%
Channel Separation(Crosstalk)	10KΩ loading, 20~20KHz		-95		dB
	32Ω loading (Normal Jack), 20~20KHz		-60		dB
	32Ω loading (4-ring Combo Jack), 20~20KHz	-61	-53 (@1KHz)	-52	dB
Frequency Response	10KΩ loading, Fs=48kHz/16bits, 20~20KHz	-0.064 (20Hz)		-0.949 (20KHz)	dB
	10KΩ loading, Fs=96kHz/24bits, 20~48KHz	-0.017 (20Hz)		-3 (42KHz)	dB
Passband Ripple Range	10KΩ loading, 20~20KHz			0.278	dB

9.2 ADC Audio Quality

TA=25℃, DV50=5V, AV50=5V, input test signal is 997Hz sine wave, measure bandwidth is 120Hz to 20kHz, Equalizer disable, Mic Gain= 0dB, Typical Fs/Bit-depth=48KHz/16bit (except remarked in Test Conditions)

Platform=DELL Desktop 32BWS02, 4G RAM, Windows 8.1CHT

Items	Test Conditions	Test Values			Unit
		Min.	Typ.	Max.	
Full Scale Input Voltage			0.74		Vrms
THD+N @-3dB Full Scale Input	20~20KHz	-85	-83 (@1KHz)		dB
Dynamic Range (with -60dBFs Input Signal)	A-Weighted		88		dB
Sampling Frequency Accuracy	Fs=48kHz/16bits	-0.0032		-0.0069	%
	Fs=96kHz/24bits	-0.0057		-0.0078	
Channel Separation(Crosstalk)	20~20KHz		-80		dB
Frequency Response	Fs=48kHz/16bits, 20~20KHz	-0.043 (20Hz)		-0.512 (20KHz)	dB
	Fs=96kHz/24bits, 20~48KHz	-0.005 (20Hz)		-3 (43KHz)	dB
Passband Ripple Range	20~20KHz			0.265	dB

9.3 Analog Monitoring / Side tone (A-A) Path Audio Quality

TA=25℃, DV50=5V, AV50=5V, Microphone-In to Line-Out, 10Kohms loading, Master Volume=0dB, Mic Gain=0dB

Platform=DELL Desktop 32BWS02, 4G RAM, Windows 8.1 CHT

Items	Test Conditions	Test Values			Unit
		Min.	Typ.	Max.	
Full Scale Output Voltage			1.05		Vrms
THD+N @ -3dB Full Scale Input	20~20KHz	-90	-89 (@1KHz)		dB
Dynamic Range (with -60dBFs Input Signal)	A-Weighted		92		dB
Channel Separation (Crosstalk)	20~20KHz		-90		dB
Frequency Response	20~20KHz	-0.036 (20Hz)		-0.133 (20KHz)	dB
Passband Ripple Range	20~20KHz			0.002	dB

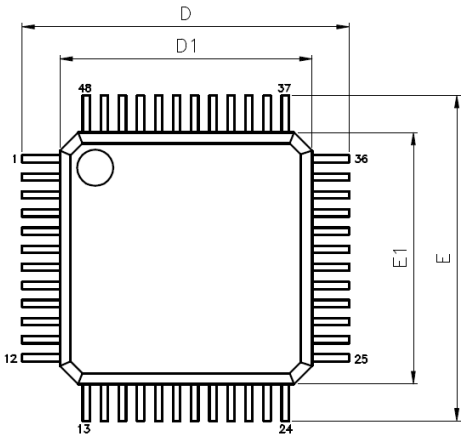
10 Package Dimension

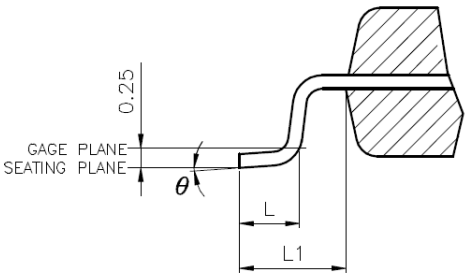
Model Number	Package	Operating Ambient Temperature	Supply Range
CM6533	48-Pin LQFP 7mm×7mm×1.4mm (Plastic)	-15°C to +70°C	DVdd = 5V, AVdd = 5V
CM6533N	48-Pin QFN 7mm×7mm×0.85mm (Plastic)	-15°C to +70°C	DVdd = 5V, AVdd = 5V
CM6533X1	48-Pin LQFP 7mm×7mm×1.4mm (Plastic)	-15°C to +70°C	DVdd = 5V, AVdd = 5V

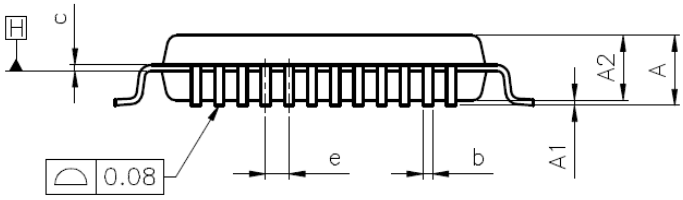
Outline Dimensions *Dimensions shown in inches and (mm)

11.1 Package Dimension of CM6533/6533X1

48-Lead Thin Plastic Quad Flatpack (LQFP)







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

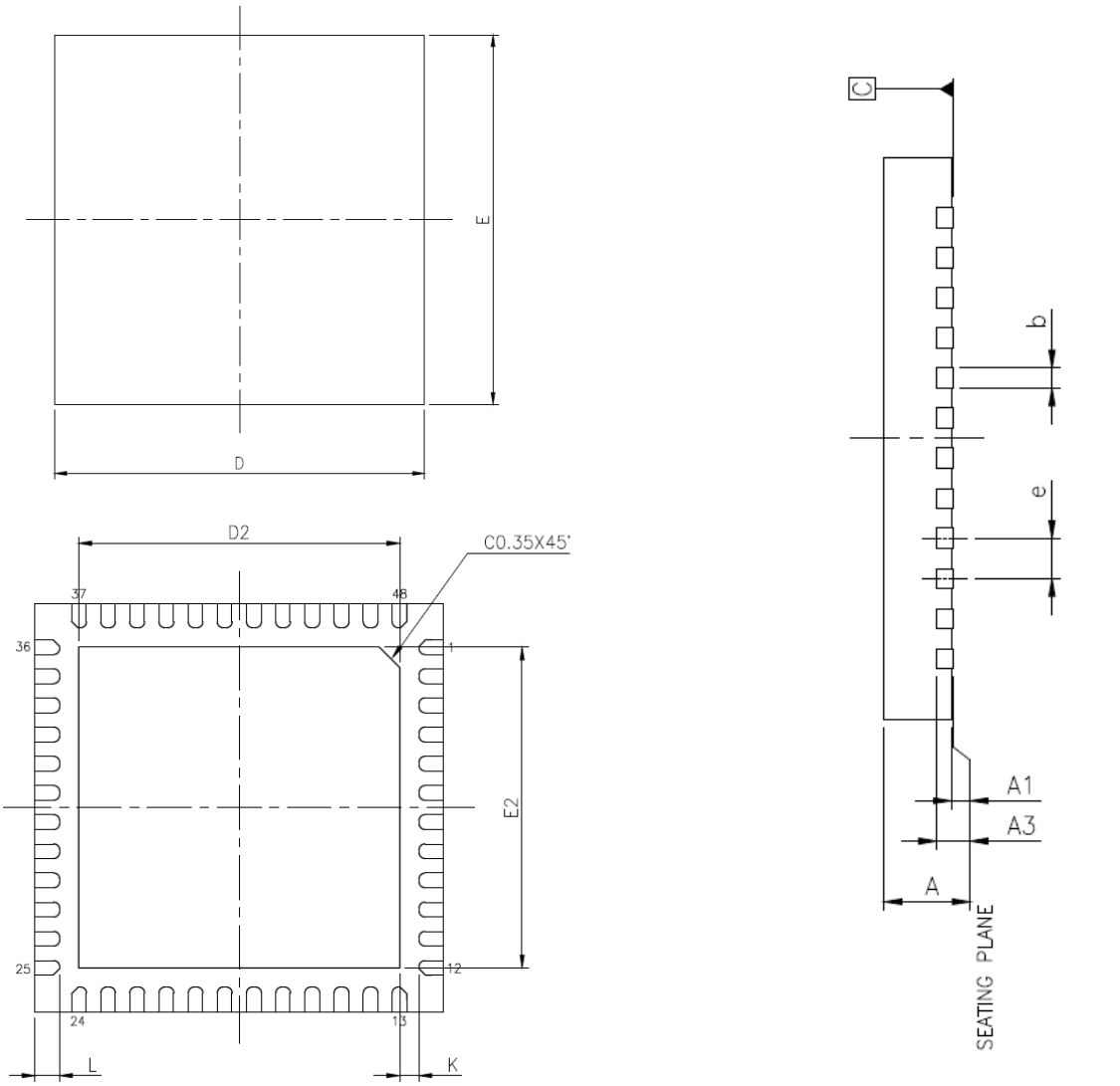
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:
1.JEDEC OUTLINE :
MS-026 BBC

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

11.2 Package Dimension of CM6533N

48-Lead Thin Plastic Quad Flatpack (QFN)



	PACKAGE TYPE		
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN(Y748)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
K	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
224X22* MIL	5.25	5.30	5.35	5.25	5.30	5.35	0.35	0.40	0.45	V	X	N/A

"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

—End of Datasheet—

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