CM6306 USB Audio Single Chip Specification

Preliminary Release
Version 1.1

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1. Descriptions and Overview

CM6306 is a highly integrated single chip USB audio solution which comprises more USB audio controller and applications. According to coming more experiences in PC USB Audio peripheral from Vendors' recommend, C-Media aggressively design one single chip to let vendors to come more integration products, and increase more revenues.

CM6306 is C-Media's new Audio SOC IC family. It combines the highly performance ADC, and also integrates I2C and SPI interfaces with external Micro processor or DSP to communicate it. Expecially in USB Microphone , Array Microphone applications , CM6306 could give you low noise but high quality speech input solution , thus, when it comes to conference or public speech , it would be wonderful choice for you.

All essential analog and digital modules are embedded in in the CM6306, including 4-Channel ADC, Linear microphone gain control, PLL, regulator, USB transceiver, 12 MHz crystal, and power on reset circuit. The CM6306 supports sampling rates of 8KHz, 16KHz, 44.1KHz and 48KHz, with high quailty 16 bit resolution. It has friendly General purpose inputs and outputs connect the CM6306 to peripheral hardware, like LED, keypads and buttons, there are many features could be programmable with external EEPROM and MCU. External MCU/EEPROM/GPIO can easily be controlled through the HID software interface. 2 LED indicator pins supported provide more flexible behavior with device On / Off / Operation / recording mute / and controllable flash times (with PWM Function).

Instant messaging and VoIP software are gaining widespread popularity, as they provide real-time audio/video communication in a cost-effective manner. C-Media not only provides the single chip hardware solution for audio peripherals, but also software middleware that enhances instant messaging programs.

We additional come this SOC to cooperate with 3rd party or vendors as having more intelligent solution, not only in low cost consideration, but also to be easy integration or modification.

2. Features

- USB spec. 2.0 Full speed compatible and USB IF certification
- USB audio device class spec. 1.0 and USB HID class spec. 1.1 compliant
- Supports control, interrupt and isochroous data transfers
- USB suspend/resume and remote wake-up support
- Embedded USB transceiver and power-on reset circuit
- Single 12MHz Crystal Input with On-chip PLL
- High-power (500mA) and Low-power (100mA) mode options supported
- Support series number string (16 Bytes) for operation system detect
- Serial EEPROM programming interface supports customized VID/PID/Product string/ Manufacture string for device name changed and configuration
- EEPROM interface support 24C02 data format
- 4CH ADC Input

  ADC sampling rate from 8KHz, 16KHz, 44.1KHz to 48KHz with 16-bit resolution

  Dynamic Range: 88db, THD+N: -79~-84db

  Digital Linear Microphone Gain Control function (-6db~33db)

  1.0 Vrms biased at 2.25V input swing Supported Stereo Mixer function
- Support Microsoft HID Record_Mute function
- Support I2C & SPI (Master/Slave) control interface for external controller used
- MCU read/write support 8 bytes data transfer bandwidth
- I2C interface support extra interrupt pin INT
- MCU / EEPROM / GPIO control via HID / Vender command interface
- USB audio topology has 1 Input Terminals, 1 Output Terminals, 1 Selector Unit, and 1 Feature Units
- Support 2 LED indicator pins:
  1. On / Off / Operation
  2. Recording mute
- Support Digital Mic interface

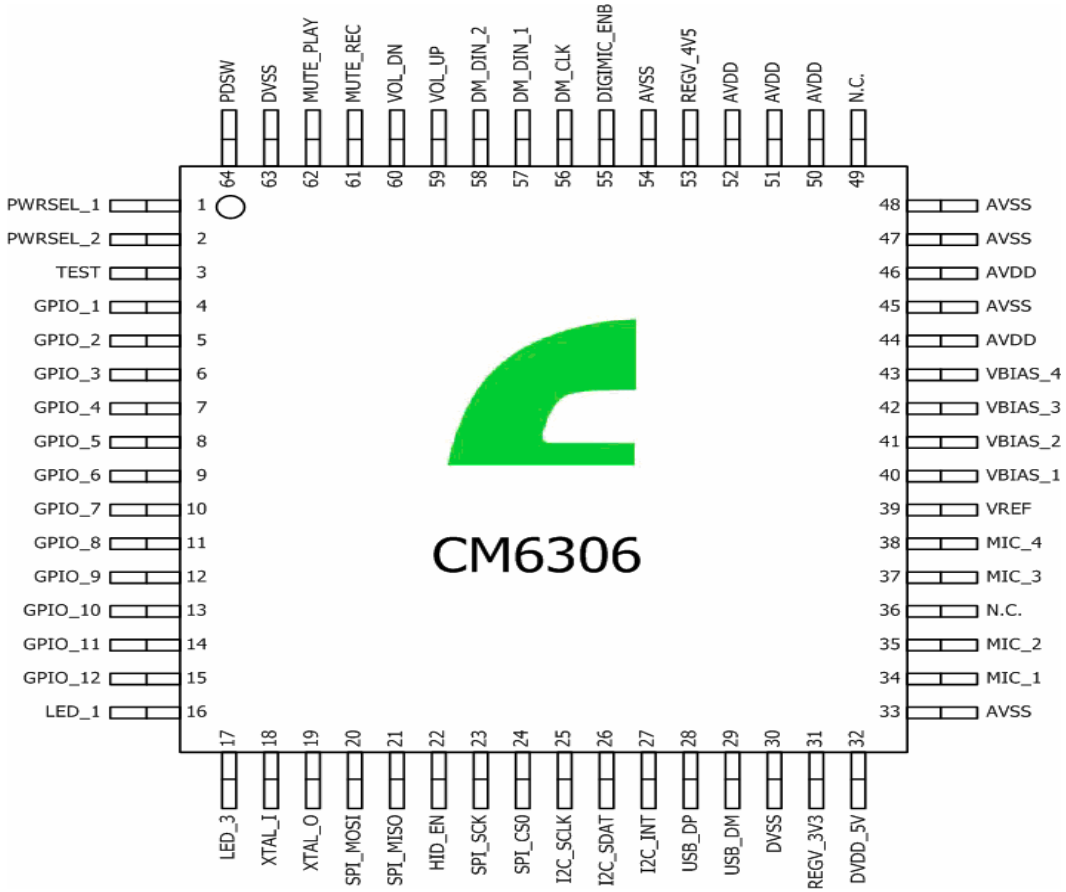
- Supported 12 GPIO pins
- Isochronous transfer uses Adaptive Mode with Internal PLL for Synchronization
- Embedded Power-On-Reset Block
- Single 5V power supply with embedded 5V to 3.3V regulator
- Industry standard LQFP-64 Pin package
- Compatible with Win2000 / WinXP / Vista without additional driver
- Support Linux Red Hat and Fedora with plug in play
- Support Hardware SDK tool for third-party software or soft-phone development

3. Pin Descriptions

3.1 PIN ASSIGNMENT BY PIN NUMBER

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	PWRSEL_1	17	LED_3	33	AVSS	49	N.C.
2	PWRSEL_2	18	XTAL_I	34	MIC_1	50	AVDD
3	TEST	19	XTAL_O	35	MIC_2	51	AVDD
4	GPIO_1	20	SPI_MOSI	36	N.C.	52	AVDD
5	GPIO_2	21	SPI_MISO	37	MIC_3	53	REGV_4V5
6	GPIO_3	22	HID_EN	38	MIC_4	54	AVSS
7	GPIO_4	23	SPI_SCK	39	VREF	55	DIGIMIC_ENB
8	GPIO_5	24	SPI_CS0	40	VBIAS_1	56	DM_CLK
9	GPIO_6	25	I2C_SCLK	41	VBIAS_2	57	DM_DIN_1
10	GPIO_7	26	I2C_SDAT	42	VBIAS_3	58	DM_DIN_2
11	GPIO_8	27	I2C_INT	43	VBIAS_4	59	VOL_UP
12	GPIO_9	28	USB_DP	44	AVDD	60	VOL_DN
13	GPIO_10	29	USB_DM	45	AVSS	61	MUTE_REC
14	GPIO_11	30	DVSS	46	AVDD	62	MUTE_PLAY
15	GPIO_12	31	REGV_3V3	47	AVSS	63	DVSS
16	LED_1	32	DVDD_5V	48	AVSS	64	PDSW

3.2 PIN-OUT DIAGRAM



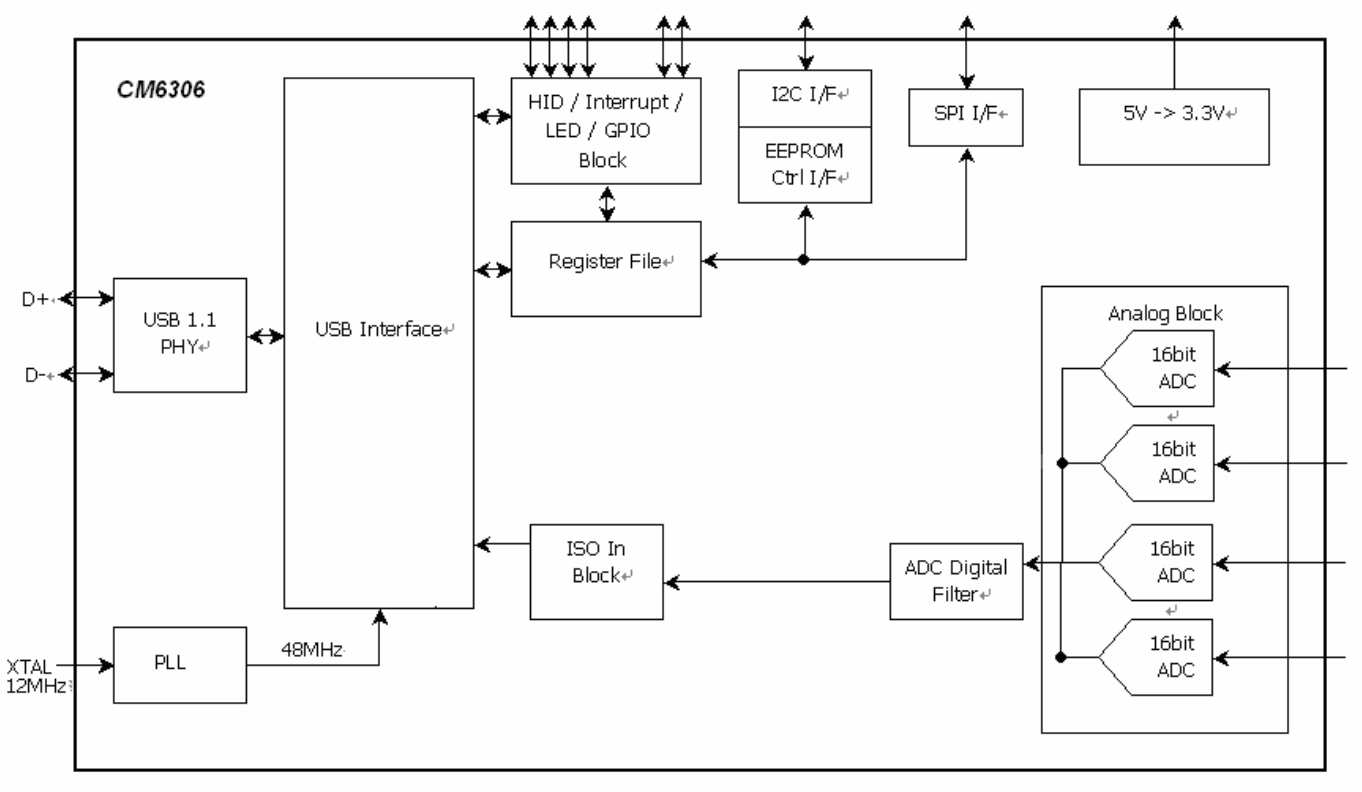
3.3 PIN SIGNAL DESCRIPTIONS

No.	Symbol	Type	Description
1	PWRSEL_1	DIO, PU	Bus/Self Power Selector (0: Self Power; 1: Bus Power)
2	PWRSEL_2	DIO, PU	Power Consumption Selector (0:500mA; 1:100mA)
3	TEST	DI, PD	Test Mode Select (0:Normal Mode; 1:Test Mode)
4	GPIO_1	DIO	General Purpose I/O Pin
5	GPIO_2	DIO	General Purpose I/O Pin
6	GPIO_3	DIO	General Purpose I/O Pin
7	GPIO_4	DIO	General Purpose I/O Pin
8	GPIO_5	DIO	General Purpose I/O Pin
9	GPIO_6	DIO	General Purpose I/O Pin
10	GPIO_7	DIO	General Purpose I/O Pin
11	GPIO_8	DIO	General Purpose I/O Pin
12	GPIO_9	DIO	General Purpose I/O Pin
13	GPIO_10	DIO	General Purpose I/O Pin
14	GPIO_11	DIO	General Purpose I/O Pin
15	GPIO_12	DIO	General Purpose I/O Pin
16	LED_1	DO	LED (Play or Record)
17	LED_3	DO	LED (Mute Record)
18	XTAL_I	DI	Input Pin for 12MHz Oscillator
19	XTAL_O	DO	Output Pin for 12MHz Oscillator
20	SPI_MOSI	DIO	SPI Master Data Output
21	SPI_MISO	DIO	SPI Master Data input
22	HID_EN	DI, PU	HID bottom function enable (0:Disable; 1:Enable)
23	SPI_SCK	DIO	SPI Clock
24	SPI_CS0	DIO	SPI Chip Selector
25	I2C_SCLK	OD, DIO	I2C Serial Clock / EEPROM 24c02 Serial Clock
26	I2C_SDAT	OD, DIO	I2C Serial Data / EEPROM 24c02 Serial Data
27	I2C_INT	DO	I2C Interrupt output
28	USB_DP	AIO	USB D+
29	USB_DM	AIO	USB D-
30	DVSS	P	Digital Ground
31	REGV_3V3	AO	5V->3.3V Regulator Output
32	DVDD_5V	P	5V Power Supply to Internal Regulator
33	AVSS	P	Analog Ground
34	MIC_1	AI	MIC0 in right channel
35	MIC_2	AI	MIC0 in left channel

36	N.C.	N.C.	N.C.
37	MIC_3	AI	MIC1 in left channel
38	MIC_4	AI	MIC1 in right channel
39	VREF	AO	2.25V reference Voltage output
40	VBIAS_1	AO	MIC bias Voltage
41	VBIAS_2	AO	MIC bias Voltage
42	VBIAS_3	AO	MIC bias Voltage
43	VBIAS_4	AO	MIC bias Voltage
44	AVDD	P	5V Analog Power for Analog Circuit
45	AVSS	P	Analog Ground
46	AVDD	P	5V Analog Power for Analog Circuit
47	AVSS	P	Analog Ground
48	AVSS	P	Analog Ground
49	N.C.	N.C.	N.C.
50	AVDD	P	5V Analog Power for Analog Circuit
51	AVDD	P	5V Analog Power for Analog Circuit
52	AVDD	P	5V Analog Power for Analog Circuit
53	REGV_4V5	AO	4.5V regulator output
54	AVSS	P	Analog Ground
55	DIGIMIC_ENB	DI, PU	External Digital Mic Enable (0: Enable; 1: Disable)
56	DM_CLK	DO	Digital Mic Clock Output
57	DM_DIN_1	DI, PD	Digital Mic Data Input 1
58	DM_DIN_2	DIO	Digital Mic Data Input 2
59	VOL_UP	DI, PU	HID Volume Up
60	VOL_DN	DI, PU	HID Volume Down
61	MUTE_REC	DI, PU	HID MIC Recording Mute
62	MUTE_PLAY	DI, PU	HID Master Volume Playback Mute
63	DVSS	P	Analog Ground
64	PDSW	OD, 5V	Power Down Switch Output (0:Normal Operation; 1:Suspend)

*Notes:
DI -> Digital Input
AI -> Analog Input
OD -> Open Drain
5V -> 5V Torrent
DO -> Digital Output
AO -> Analog Output
PU -> Internal Pull Up
P -> Power
DIO -> Digital I/O
AIO -> Analog I/O
PD -> Internal Pull Down

4. Block Diagram

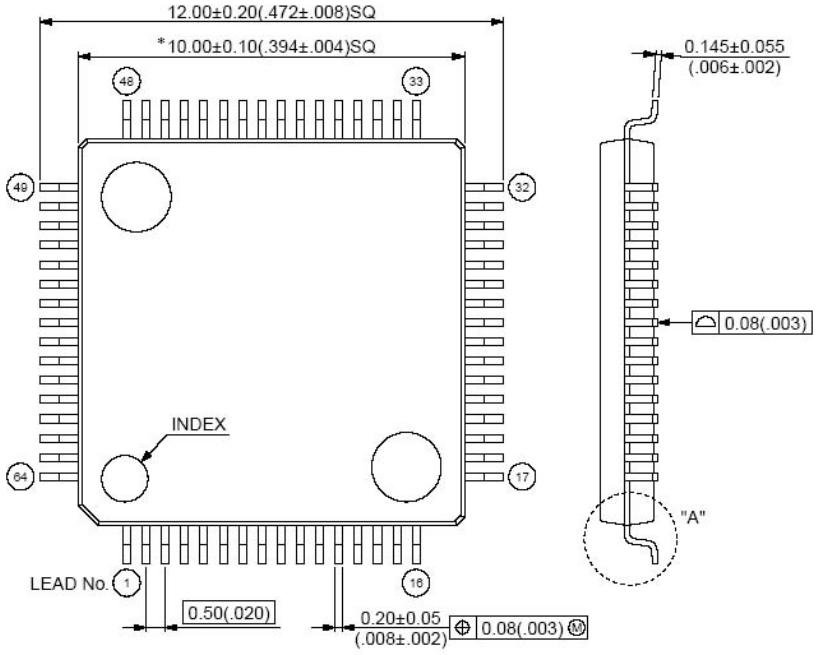


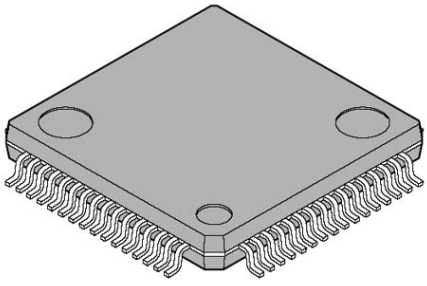
5. Ordering Information

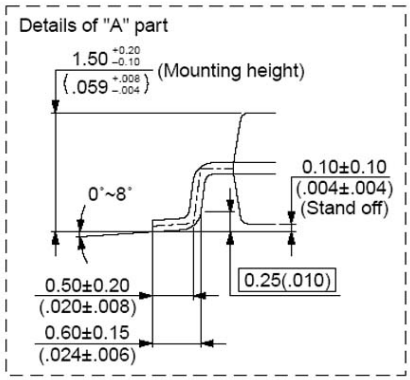
Model Number	Package	Operating Ambient Temperature	Supply Range
CM6306	64-Pin LQFP 10mm×10mm×1.4mm (Plastic)	0°C to +70°C	DVdd = 5V, AVdd = 5V

Outline Dimensions **Dimensions shown in inches and** （mm）

64-Lead Thin Plastic Quad Flatpack (LQFP)

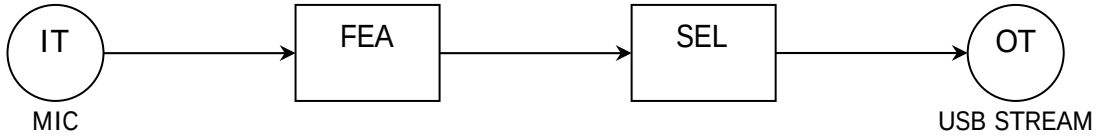






6. USB Audio Topology and Descriptors

6.1 USB Audio Topology



6.2 Device Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	12	Descriptor length
1	bDescriptorType	1	01	Device Descriptor
2	bcdUSB	2	0110	USB 1.1 compliant
4	bDeviceClass	1	00	Device class specified by interface
5	bDeviceSubClass	1	00	Device subclass specified by interface
6	bDeviceProtocol	1	00	Device protocol specified by interface
7	bMaxPacketSize0	1	40	Endpoint zero packet size
8	idVendor	2	0d8c	Vendor ID
10	idProduct	2	011D	Product ID
12	bcdDevice	2	0100	Device release number
14	iManufacturer	1	03	Index of string descriptor describing manufacturer
15	iProduct	1	01	Index of string descriptor describing product
16	iSerialNumber	1	00 or 02(*)	Index of string descriptor describing serial number
17	bNumConfigurations	1	01	Number of configuration

Note 1: When valid EEPROM is detected, Vendor ID and Product ID will be replaced by the content of EEPROM.
Note 2: iSerialNumber will be valid only if external EEPROM contain this info.

6.3 Configuration Descriptors

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	02	Configuration Descriptor
2	wTotalLength	2	0099	Total length of data returned for this configuration: 153 bytes
4	bNumInterfaces	1	03	Number of interfaces supported by this Configuration: 00: Control 02: ISO-In 03: INT-IN (HID)
5	bConfigurationValue	1	01	Configuration value
6	iConfiguration	1	00	Index of string descriptor describing this configuration
7	bmAttributes	1	a0 or 80 or e0 or c0	Bus Power and support Remote Wakeup: 8'ha0 (PWRSEL_1 = 1, HID_EN = 1) Bus Power and no Remote Wakeup: 8'h80 (PWRSEL_1 = 1, HID_EN = 0) Self Power and support Remote Wakeup: 8'he0 (PWRSEL_1 = 0, HID_EN = 1)) Self Power and no Remote Wakeup: 8'hc0 (PWRSEL_1 = 0, HID_EN = 0))
8	bMaxPower	1	32 or fa	Maximum power consumption from bus = 100mA: 8'h32 (50x2 mA) (PWRSEL_2 = 1) Maximum power consumption from bus = 500mA: 8'hfa (250x2 mA) (PWRSEL_2 = 0)

6.4 Standard HID Interface Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	04	Interface Descriptor
2	bInterfaceNumber	1	02	Interface number: 02
3	bAlternateSetting	1	00	Alternate interface
4	bNumEndpoints	1	01	Number of endpoint used by this interface
5	bInterfaceClass	1	03	HID Interface Class
6	bInterfaceSubClass	1	00	Subclass code
7	bInterfaceProtocol	1	00	Protocol code
8	iInterface	1	00	Index of string descriptor describing this interface

Class-specific HID Interface Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	09	Descriptor length
1	bDescriptorType	1	21	HID descriptor type
2	bcdHID	2	0100	HID class version
4	bCountryCode	1	00	No country code
5	bNumDescriptors	1	01	One HID class descriptor
6	bDescriptorType	1	22	Report Descriptor
7	wDescriptorLength	2	0032 / 001a	HID class descriptor length in byte: 50 / 26 bytes (Enable / Disable HID Button)

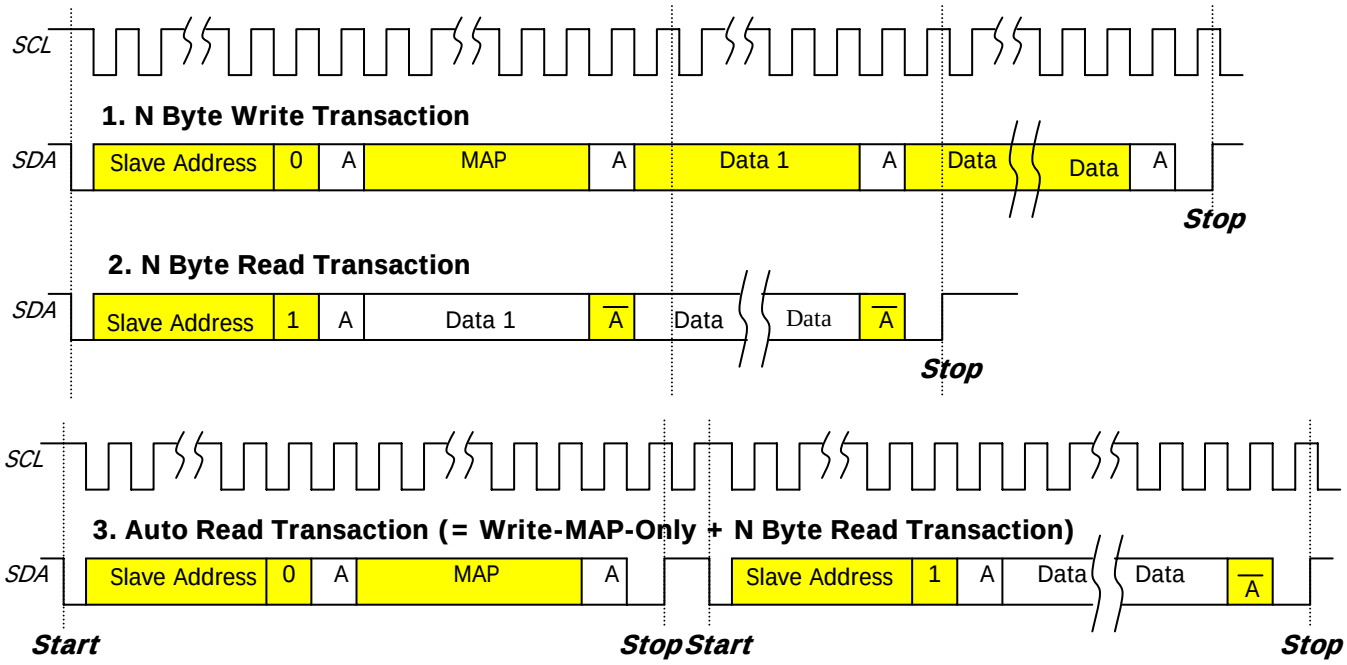
Standard HID Interrupt In Endpoint Descriptor

Offset	Field	Size	Value (Hex)	Description
0	bLength	1	07	Descriptor length
1	bDescriptorType	1	05	Endpoint Descriptor
2	bEndpointAddress	1	87	IN Endpoint, Endpoint number: 7
3	bmAttributes	1	03	Interrupt Endpoint
4	wMaxPacketSize	2	0010	Maximum packet size: 16 bytes
6	bInterval	1	01	1ms

7. Function Block Descriptions:

7.1 I Square C Interface (I2C)

7.1.1 Master Mode:



from master to slave

from slave to master

$A = acknowledg\ e\ (SDA\ Low)$

$\overline{A} = not\ acknowledg\ e\ (SDA\ High)$

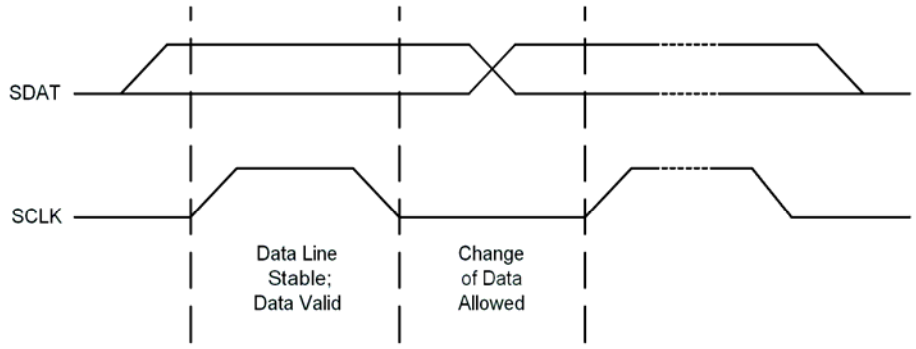
MAP: Memory Address Pointer
(The target register address in slave device)

7.1.2 Slave Mode:

"7-bit slave address = 7'b0111000"

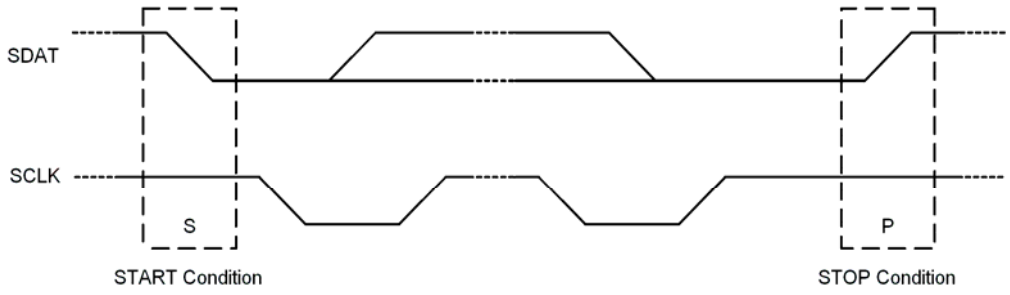
On the MCU serial interface, the CM6306 can serve as a slave device with bit rates up to 400Kbps (in fast mode). The MCU can write data to the CM6306 or read data from the CM6306 (No size limitations when using the I2C Interface). Since the host side and MCU can both access to the internal registers, access contention- when both host and MCU try to access the same register- should be avoided by the application. The 7-bit slave address of the CM6306 is assigned as 7'b0111000. When data is written by the MCU, the CM6306 will NOT transfer any interrupt to the PC until the INT bit of the I2C control Register has been set by the MCU.

The USB host will keep polling the upward HID report every 1ms. When any button is pressed or released, or MCU data is incoming, the CM6306 will transfer 16 bytes of HID report to the USB host. In I2C Slave Mode, the CM6306 has one open-drain input pin 'SCLK' where it receives the serial clock from the MCU, and one open-drain I/O pin 'SDAT' where it sends or receives serial signals to/from the MCU. As shown below, 'SDAT' should be stable when 'SCLK' is high, and can transition only when 'SCLK' is low.



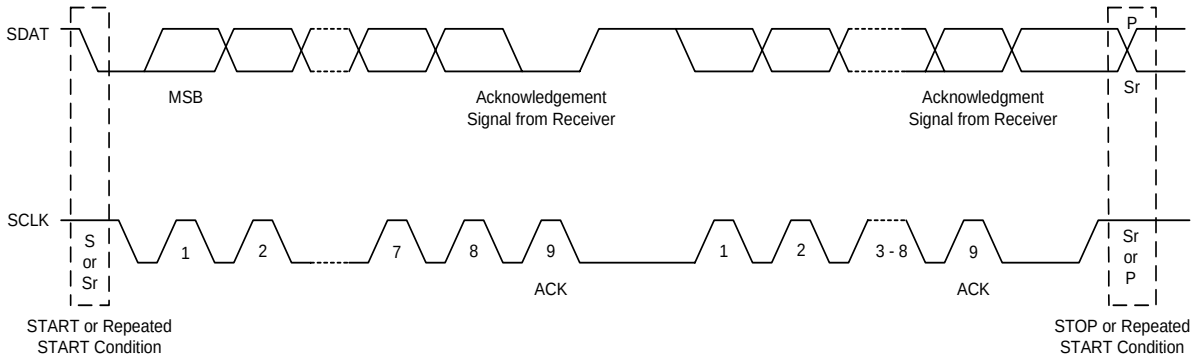
Bit Transfer on the MCU Interface

START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START).

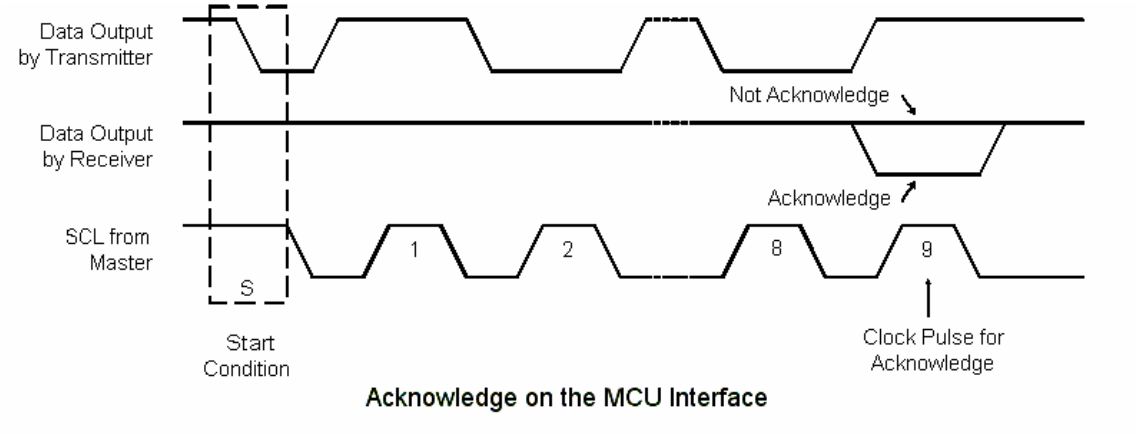


START and STOP Conditions

The figure below demonstrates a typical transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more details about the acknowledgement bit. Note that 'SCLK' is always driven by the master.

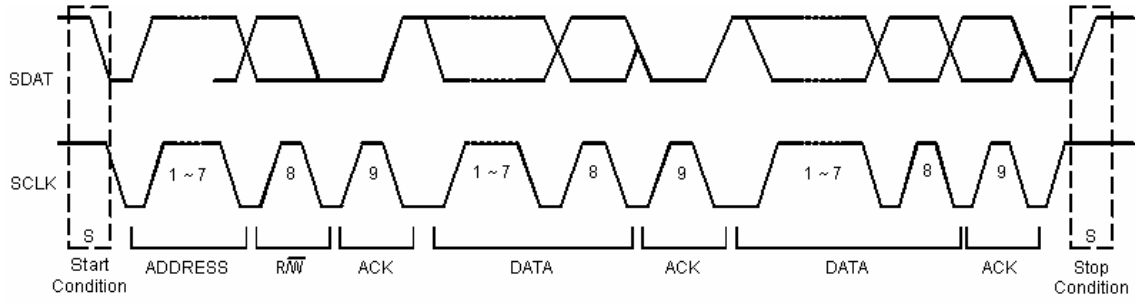


Data Transfer on the MCU Interface



Acknowledge on the MCU Interface

The figure below shows a complete data transfer. After a START, the MCU should send 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low. The first acknowledgement always comes from the CM6306.



A Complete Data Transfer

In the write transfer, the MCU continues to act as the master and the transfer direction is not changed. The following figure gives an example of a write transfer.

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	….	0	Byte N	0	P

	From CM6306 to MCU		From MCU to CM6306
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte data		

0x70 is the slave address of CM6306, and it also tells CM6306 that it's receiving a write command. CM6306 regards the first coming DATA byte as the register address. The second DATA byte is the DATA content that MCU writes at the register address. CM6306 will auto-increment the register address to the next register address for the following writes DATA. The figure below shows an example of read transfer. The MCU read command can not set the register address, so the MCU may use a write command to set the register address first and then start the read command. Because the CM6306 auto-increments the register address, the second DATA byte will be the register data on the next address.

MCU read:

S	0x70	0	addr	0								
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P	

	From CM6306 to MCU		From MCU to CM6306
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte n	One byte data		

The figure below gives a complete picture of a typical transaction between the MCU and CM6306. After a START, the MCU should send a 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low.

MCU write:

S	0x70	0	addr	0	Byte 0	0	Byte 1	0	…..	0	Byte N	0	P

MCU read:

S	0x70	0	addr	0							
S	0x71	0	Byte 0	0	Byte 1	0	…..	0	Byte N	1	P

	From CM6306 to MCU		From MCU to CM6306
S	START condition	P	STOP condition
0	Positive acknowledge	1	Negative acknowledge
Byte N	One byte data		

During a write transfer, the MCU continues acting as the transmitter. The CM6306 regards the first DATA byte as the start register address. The following DATA bytes are the content of the registers that the MCU requests. In a read transfer, two transactions are necessary. The MCU resets the start register address by the first transaction, then direction changes to get N of data.

7.2 Serial Peripheral Interface

The SPI interface is used to transfer control data between the CM6306 and external codecs. It is not a standard interface. Every vendor has its own slightly different implementation, but generally speaking, all of them comprise four signals, spi_cen, spi_clock, spi_data_o, spi_data_i. Their meanings are as follows.

- ***spi_cen***: the SPI chip enable signal that is used to inform a codec when it should latch onto the data.
- ***spi_clock***: the SPI clock signal.
- ***spi_data_o***: the SPI data output to codec.
- ***spi_data_i***: the SPI data input from codec.

7.2.1 The SPI Design Goal and SPI Transactions

Our goal is to design a robust SPI interface that can be suitable for all existing codecs. After analyzing the SPI interfaces of several codecs, we have written down the following differences among them.

1). An SPI interface that can read data from and write data to a codec has 4 wires, but some codecs only support input data. In other words, the data in the codec registers can not be retrieved by audio processor. This kind of codec only requires 3 wires.

2). An SPI transaction length is 2 or 3 bytes depending on the codec.

3). Some codecs latch control data on the SPI clock's high state, but others latch control data on the SPI clock's low state

4). The highest SPI clock frequencies are different for many codecs.

For difference 1 listed above, we have designed a 4-wire SPI interface, which is able to accommodate the 3-wire SPI interfaces as well. For difference 2 and 3, control bits in the SPI interface of the CM6306 are used to be initiated a 2-byte or 3-byte data transfer, and maintain SPI clock high or low at codec latching data. All of these can be observed in Figs. A ~ E.

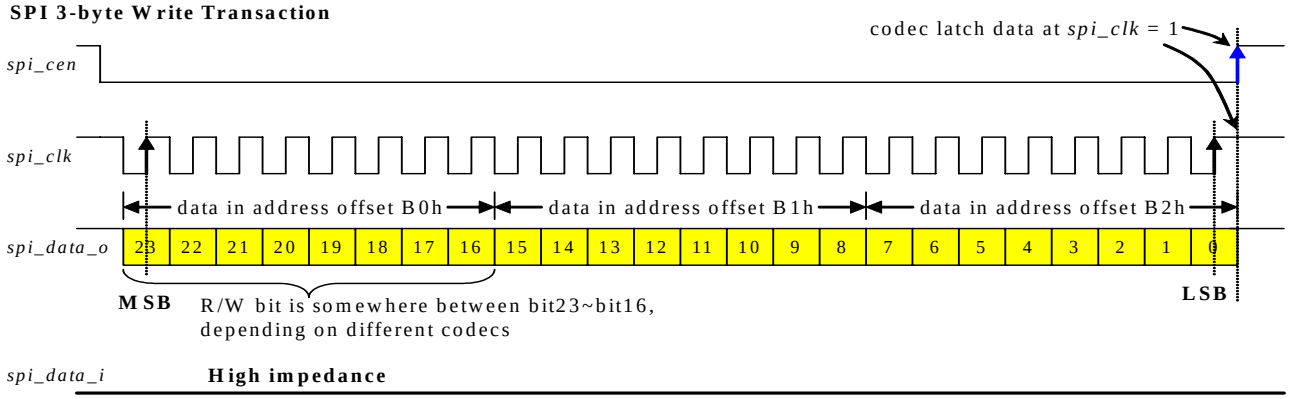


Fig. A. An SPI 3-byte write transaction with codec latching data at *spi_clk* high state.

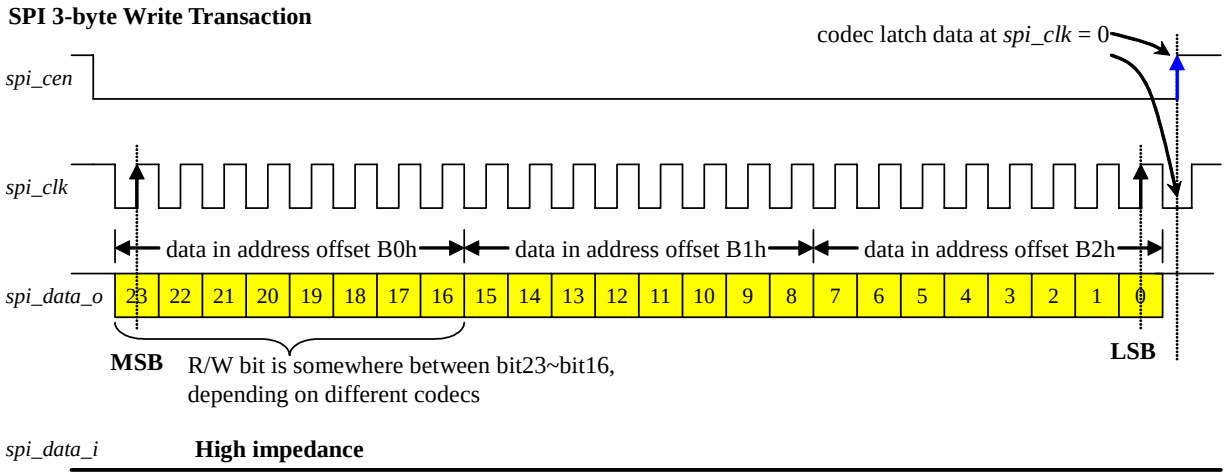


Fig. B. An SPI 3-byte write transaction with codec latching data at *spi_clk* low state.

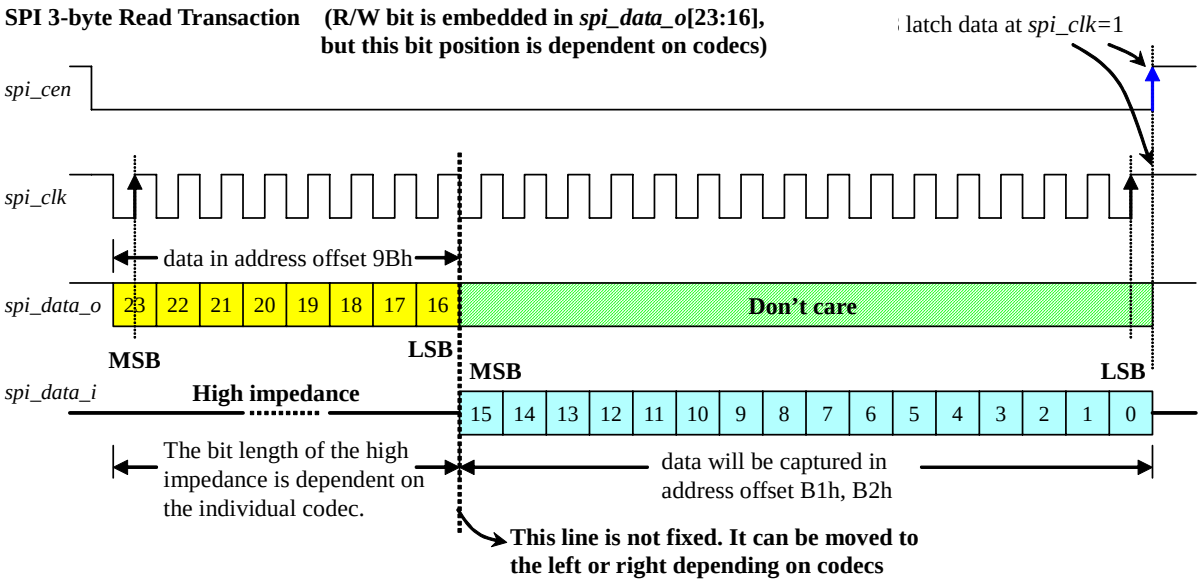


Fig. C. An SPI 3-byte read transaction with codec latching data at *spi_clk* high state.

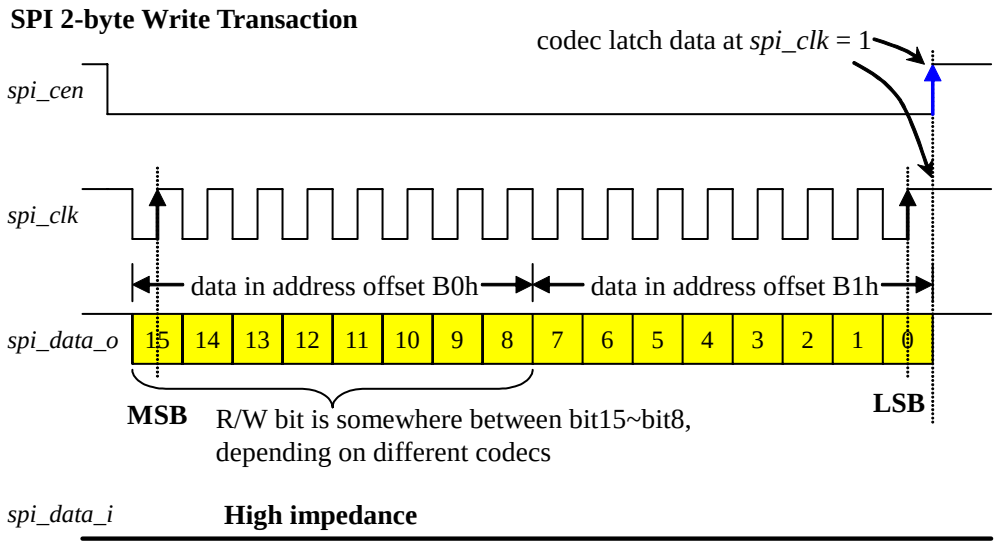


Fig. D. An SPI 2-byte write transaction with codec latching data at *spi_clk* high state.

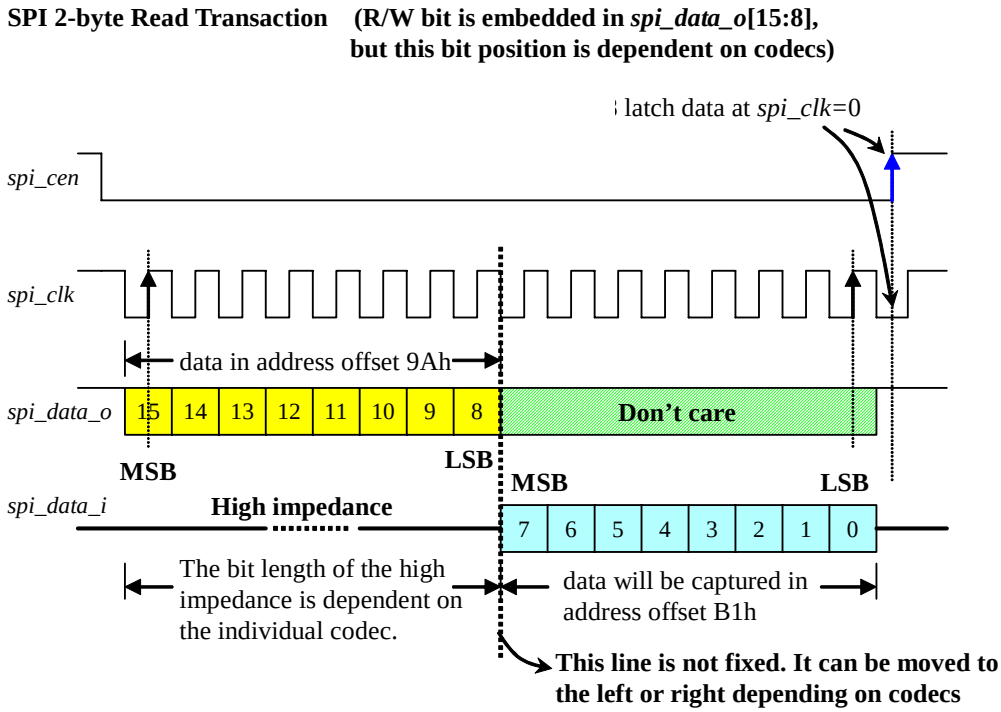


Fig. E. An SPI 2-byte read transaction with codecs latching data at *spi_clk* low state.

In order for our SPI interface to be capable of interfacing with all codecs, the content of the data registers (address offset 9Bh-99h, which includes address, r/w, and data bits) that are written to or read from the codec are not translated by the hardware SPI interface, but by the system driver. The meaning of the bits in this register should be interpreted according to the individual codec.

It is important to notice that the contents of this register, after a write transaction completes, have no meaning. However, after a read transaction completes, you should reference the codec's documentation to see how many bits in this register are valid. For example, if the codec is Analog Device AD1837, then SPI_Data_Reg[9:0] will be valid data.

As the highest SPI clock frequencies are different for many codecs, two control bits are used to adjust the spi_clk frequency to gain the maximum transfer speed. The CM6306 can control up to six codecs through the SPI interface, as shown in Fig. F below.

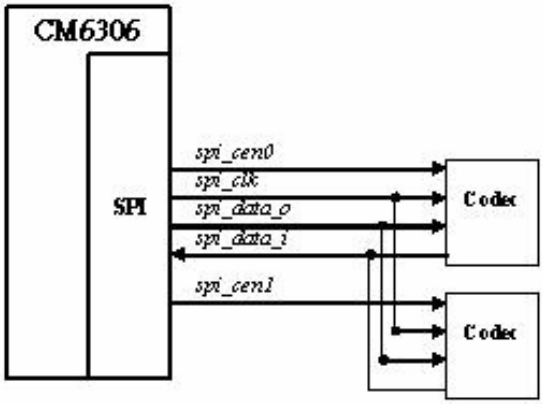
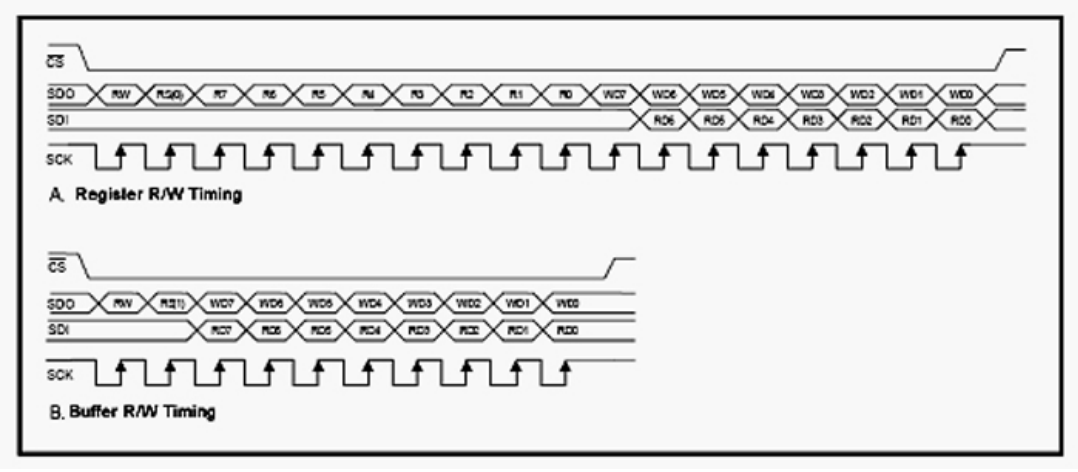


Fig. F. The SPI connection topology

7.2.2 2-bit leading mode

2-bit leading mode is designated for LCM controllers. Its waveform is almost the same as the general SPI except for two extra bits, RW and RS, in the beginning of each transaction. See the following figure.



7.2.3 The Serial Interface

The serial data is read from the serial data input pin on the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data on the rising edge of the eighth serial clock cycle for the processing. The A0 input is used to determine whether or not the serial data input is displaying data or command data; when A0 = “H”, the data is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip active. Figure 1 is a serial interface signal chart.

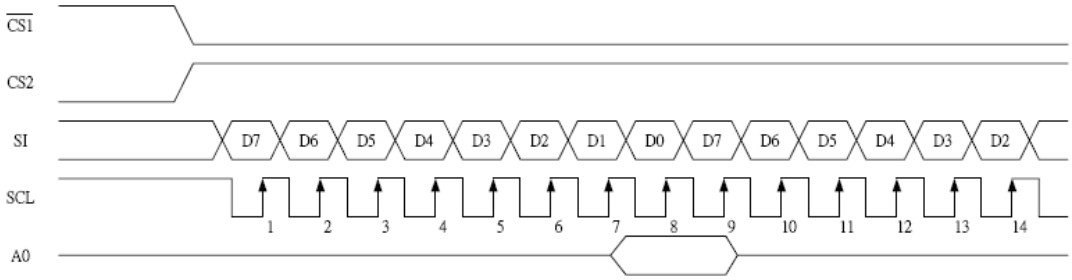
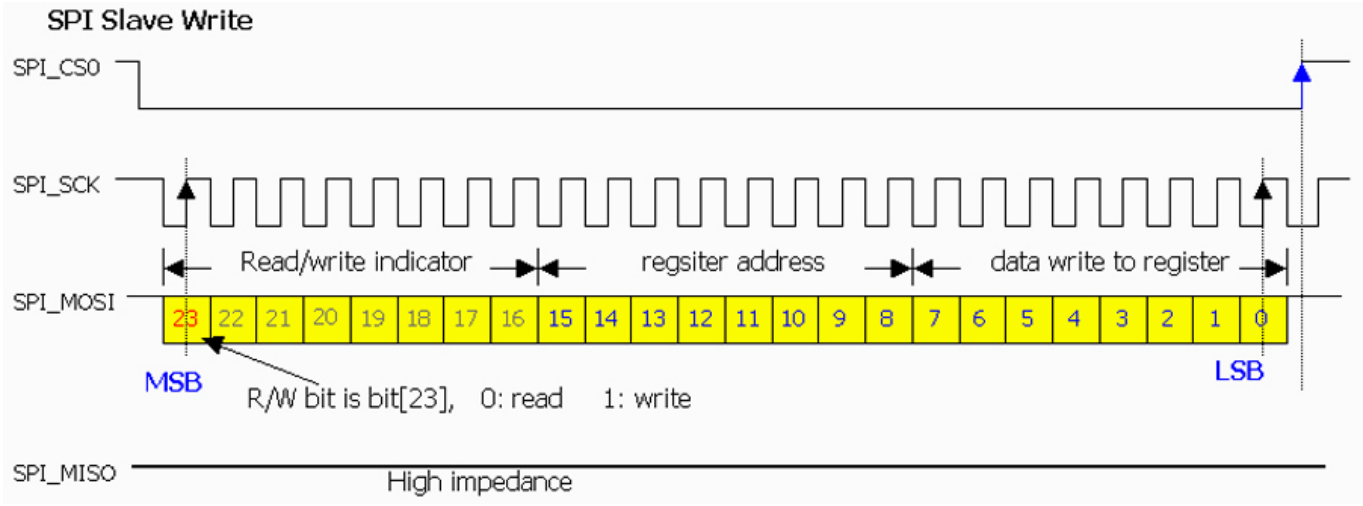
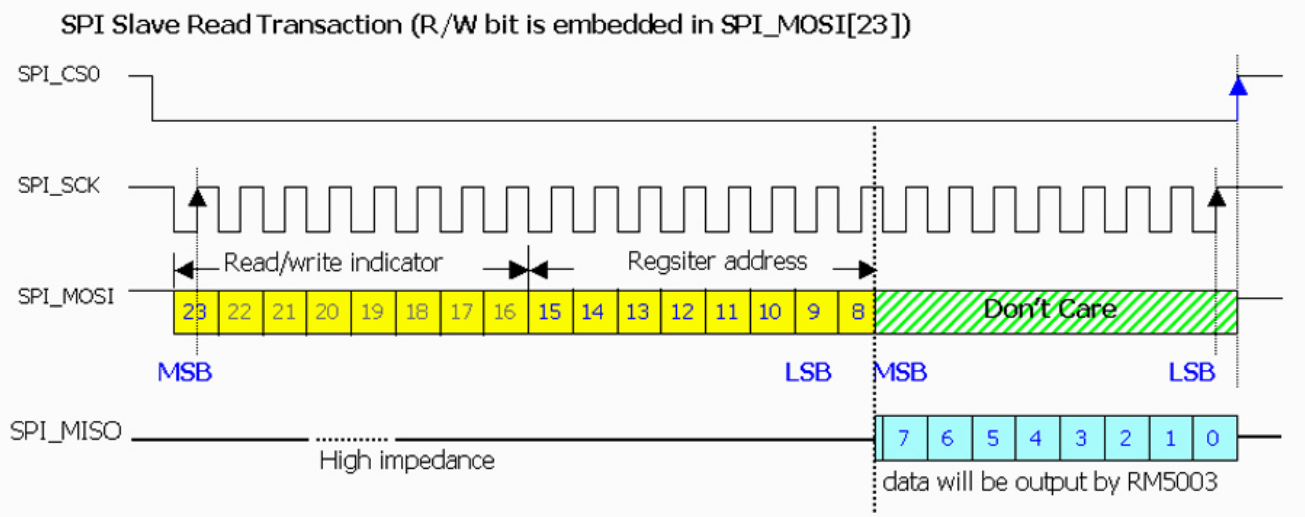


Figure 1

When the CM6306 acts as a SPI slave, the external MCU can read/write registers within the CM6306 through the SPI interface. Each transaction is 3-bytes long. The first byte is a read/write command indicator. Once the MSB of the first byte is low, it means a read transaction is occurring; otherwise it is a write transaction. The other bits of the first byte are meaningless. The second byte is the address of the desired register. The third byte, for a read transaction, is meaningless, and meanwhile the MISO would output the data of register. The third byte, for write transactions, is data.

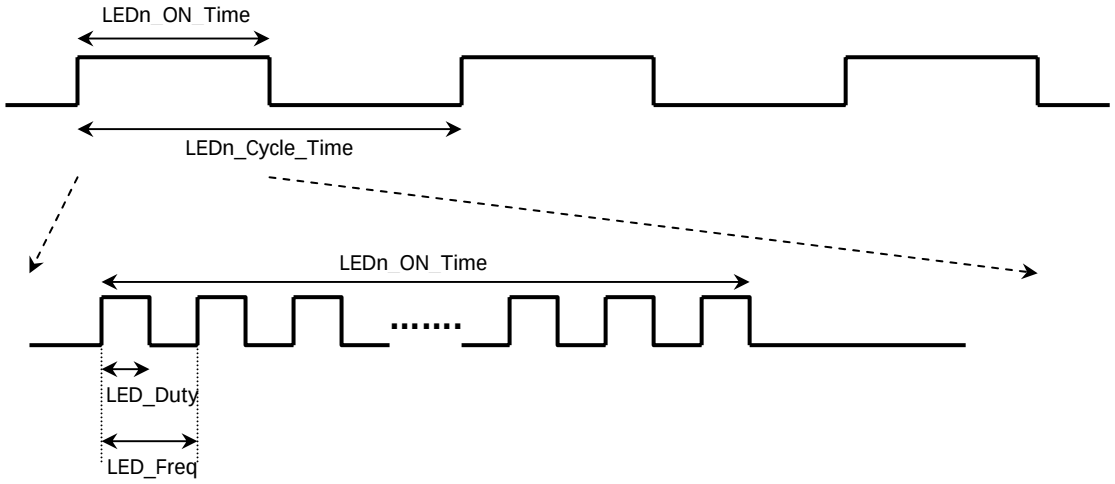



SPI Slave Read Transaction (R/W bit is embedded in SPI_MOSI[23])
SPI_CS0
SPI_SCK
SPI_MOSI
Read/write indicator
Regsiter address
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8
Don't Care
MSB
LSB
MSB
LSB
SPI_MISO
High impedance
7 6 5 4 3 2 1 0
data will be output by RM5003

7.3 LED Behavior and Software Control

LED1 (Config & Play/Rec)	3 times / sec
LED3 (Config & Rec Mute)	1 time / sec

LED Signal is like a PWM wave form:



* Notes: 1. Unit for LED_Duty / LED_Freq (Resolution) = 42.67 uS
2. Unit for LEDn_ON_Time / LEDn_Cycle_Time (Resolution) = 21.85 mS

7.4 EEPROM Content Data Format

24c02 (256 x 8 bit)

[ADDR]	[DATA]		
0x00,	Magic Word (“C”, 8’h43)		
0x01,	Magic Word (“M”, 8’h4D)		
0x02,	Total Data Length in EEPROM		
0x03,	EEPROM Content Setting		
	bit 0:	*Manufacture String Valid?*	*(0: No, 1: Yes)*
	bit 1:	*Product String Valid?*	*(0: No, 1: Yes)*
	bit 2:	*Serial Number Valid?*	*(0: No, 1: Yes)*
	bit 3:	*Get_Mem String Valid?*	*(0: No, 1: Yes)*
	bit 4:	*Reserved*	*(default set to 0)*
	bit 5:	*Recording (ADC) Control Valid?*	*(0: No, 1: Yes)*
	bit 6:	*Reserved*	*(default set to 0)*
	bit 7:	*Enable Remote Wakeup?*	*(0: Disable, 1: Enable)*
0x04,	Reserved		
0x05,	Reserved		
0x06,	Recording (ADC) Control		
	bit[4:0]:	*ADC (Unit fa / fb) initial Volume*	
		(5’h1f ~ 5’h04, +33 ~ -6dB/Mute, -1.5dB/step)	
	bit 5:	*Reserved*	*(default set to 1)*
	bit 6:	*Mute_fb (ADC Line) initial Value*	*(0: Un-Mute, 1: Mute)*
	bit 7:	*Mute_fa (ADC Mic) initial Value*	*(0: Un-Mute, 1: Mute)*
0x07,	Reserved		
0x08,	VID (Low Byte)		
0x09,	VID (High Byte)		
0x0A,	PID (Low Byte)		
0x0B,	PID (High Byte)		

[ADDR]	[DATA]	
0x0C ~ 0x29	Manufacture String (30 bytes)	
	0x0c	*[String1]*
	0x0d	*[String2]*
	…	…
	0x29	*[String30]*
0x2A ~ 0x65	Product String (60 bytes)	
	0x2A	*[String1]*
	0x2B	*[String2]*
	…	…
	0x65	*[String60]*
0x66 ~ 0x75	String of Serial Number (16 bytes)	
	0x66	*[String1]*
	0x67	*[String2]*
	…	…
	0x75	*[String16]*
0x76 ~ 0xC9	String of Get_Mem (84 bytes)	
	0x76	*[String1]*
	0x77	*[String2]*
	…	…
	0xC9	*[String84]*
0xCA ~ 0xFF	Reserved	(Default set to 8'h00)

8. Electrical Characteristics:

8.1 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
Dvmin	Min Digital Supply Voltage	– 0.3	V
Dvmax	Max Digital Supply Voltage	+ 6	V
Avmin	Min Analog Supply Voltage	– 0.3	V
Avmax	Max Analog Supply Voltage	+ 6	V
Dvinout	Voltage on any Digital Input or Output Pin	–0.3 to +5.5	V
Avinout	Voltage on any Analog Input or Output Pin	–0.3 to +5.5	V
T_{stg}	Storage Temperature Range	-40 to +125	^{0}C
ESD (HBM)	ESD Human Body Mode	3500	V
ESD (MM)	ESD Machine Mode	200	V

8.2 Operation Conditions

Operation conditions				
	Min	Typ	Max	Unit
Analog Supply Voltage	4.75	5.0	5.25	V
Digital Supply Voltage	4.75	5.0	5.25	V
Operation Power Consumption, (***Notes**)	-	TBD	TBD	mA
Standby Power Consumption	-	TBD	-	mA
Suspend Mode Power Consumption	-	380	-	uA
Operating ambient temperature	0	-	70	^{0}C

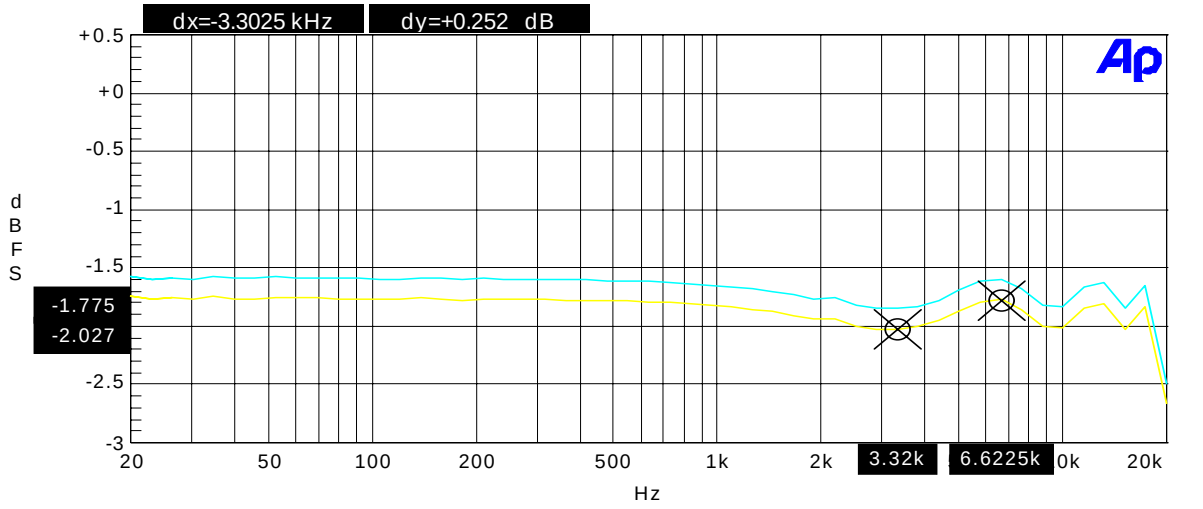
***Notes:** Test Environment Under 25^{o}C, 5.0V, 48K Sample Rate,
Max Output is Playing 1K Full Scale Sin Wave, Typical Output is Playing Music.

8.3 Electrical Parameters

	Min	Typ	Max	Unit
ADC				
Resolution	-	16	-	Bit
THD + N (20 ~ 20KHz)	-79	-	-84	dB
Dynamic Range	-	88	-	dB
Frequency Response 48KHz	20	-	20K	Hz
Frequency Response 44.1KHz	20	-	20K	Hz
Input Voltage (rms)	-	1	-	Vrms

9. FREQUENCY RESPONSE GRAPHS

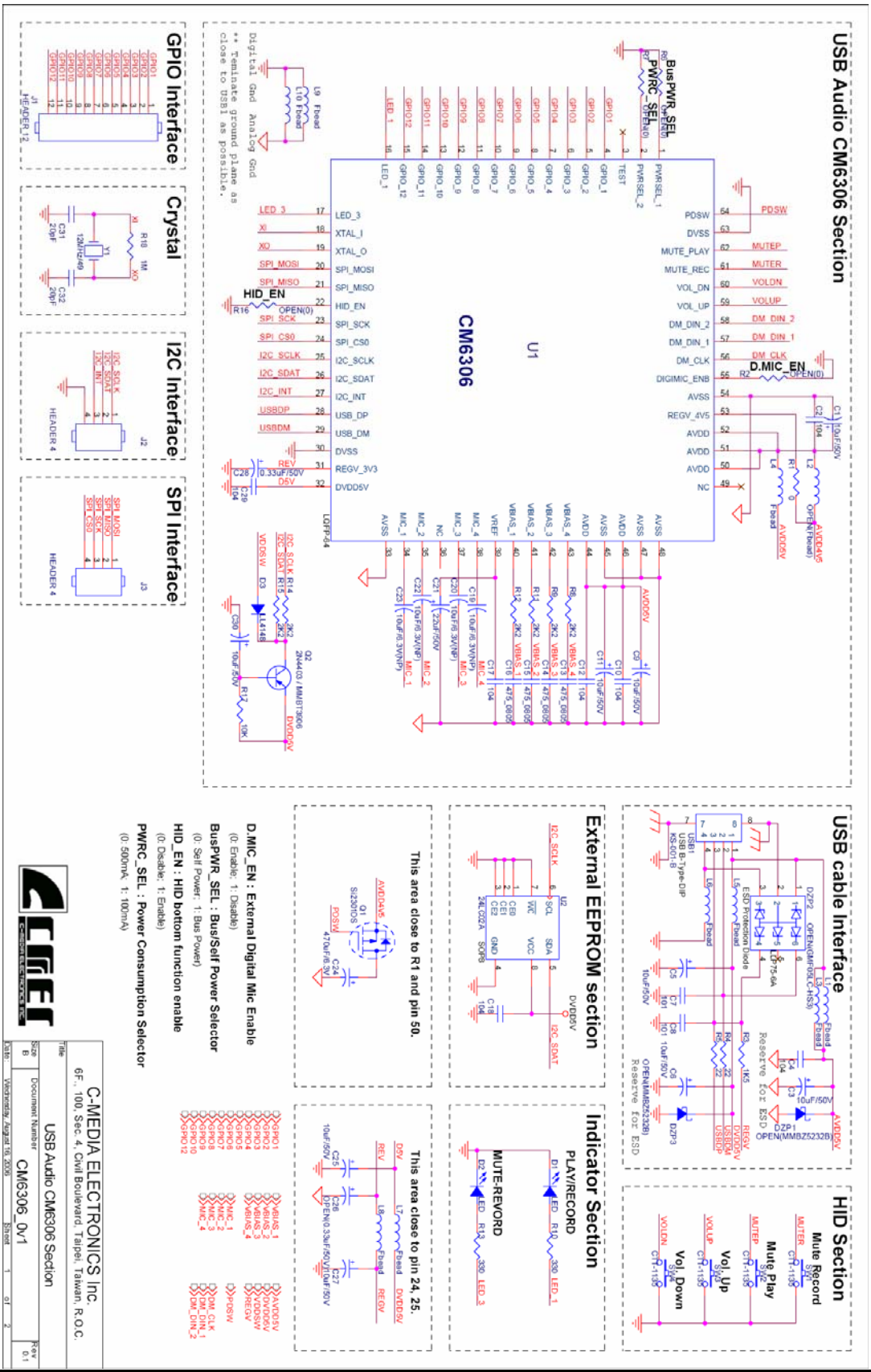
9.1 ADC (MIC IN) FREQUENCY RESPONSE

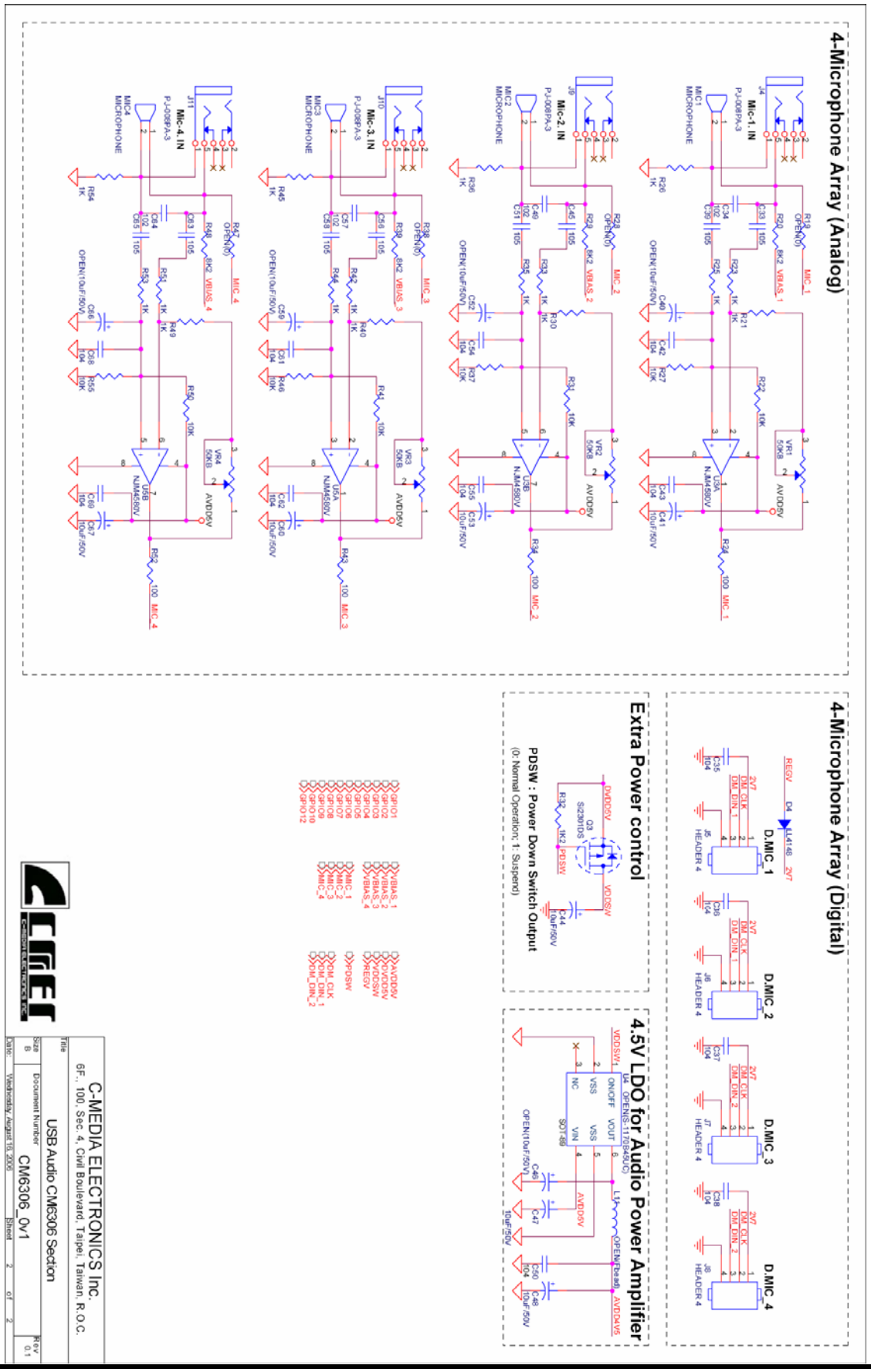


Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1
1	1	Yellow	Solid	1	DSP Anlr.Level A	Left		*-1.775 dBFS
1	2	Cyan	Solid	1	DSP Anlr.Level B	Left		-1.600 dBFS

Vista-A-D Frequency Response.at2c

10. APPLICATION CIRCUIT REFERENCE




4-Microphone Array (Analog)
4-Microphone Array (Digital)
Extra Power control
4.5V LDO for Audio Power Amplifier
PDSW : Power Down Switch Output
(0: Normal Operation; 1: Suspend)
C-MEDIA ELECTRONICS Inc.
6F., 100, Sec. 4, Civil Boulevard, Taipei, Taiwan, R.O.C.
USB Audio CM6306 Section
CM6306_0v1

REFERENCE

USB-IF, USB Specification, Revision 1.1 and 2.0, and USB Audio Device Class Specification, Revision 1.0,.

— End of Specification —

C-MEDIA ELECTRONICS INC.
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