# CM1643

*Advance Information*

# 4-Channel Low Capacitance Dual-Voltage ESD Protection Array

**ON Semiconductor®**

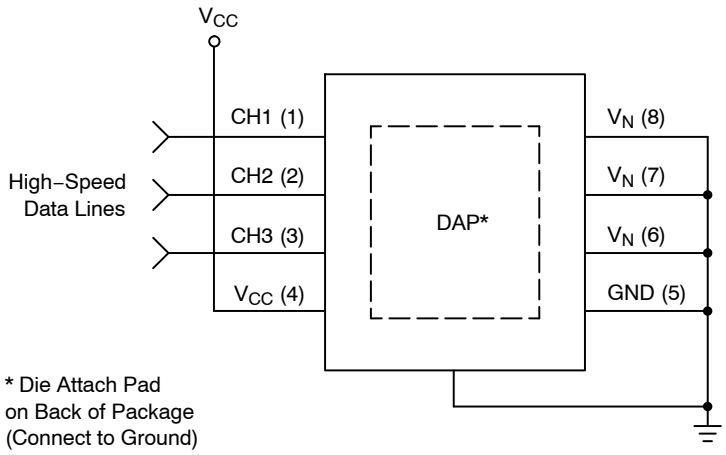
**http://onsemi.com**

**UDFN8**
**D4 SUFFIX**
**CASE 517BC**

### Features

- 3 Channels of Low Voltage ESD Protection
- 1 Channel of High Voltage ESD Protection
- Provides ESD Protection to IEC61000−4−2 Level 4:
  - ♦ ±8 kV Contact Discharge (Pins 1−3)
  - ♦ ±15 kV Contact Discharge (Pin 4)
- Low Channel Input Capacitance
- Minimal Capacitance Change with Temperature and Voltage
- High Voltage Zener Diode Protects Supply Rail
- No Need for External Bypass Capacitors
- Each I/O Pin can Withstand over 1000 ESD Strikes*
- These Devices are Pb−Free and are RoHS Compliant

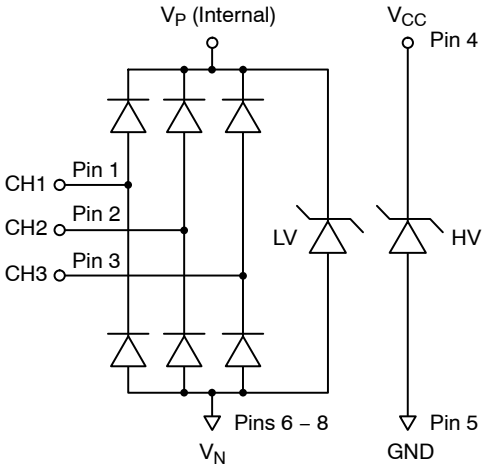
### TYPICAL APPLICATION




* Die Attach Pad on Back of Package (Connect to Ground)

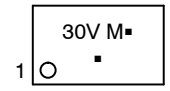
Note: All grounds must be connected.

### ELECTRICAL SCHEMATIC




Note: Pins 5 and 6 to 8 are connected to a common substrate.

### MARKING DIAGRAM




30V = CM1643−04D4
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| CM1643−04D4 | UDFN−8 0.4 mm (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

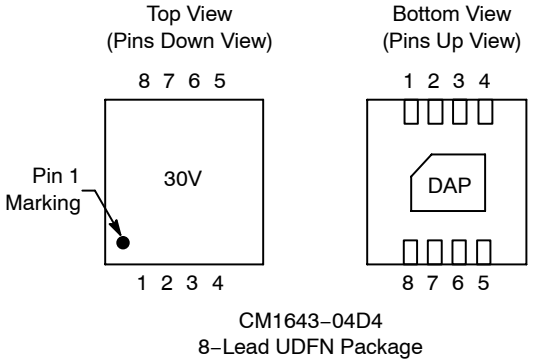
*Standard test condition is IEC61000−4−2 level 4 test circuit with each pin subjected to ±8 kV contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**Table 1. PIN DESCRIPTIONS**

| 4−Channel, 8−Lead, UDFN−8 Package | | | |
|---|---|---|---|
| **Pin** | **Name** | **Type** | **Description** |
| 1 | CH1 | I/O | LV Low−capacitance ESD Channel |
| 2 | CH2 | I/O | LV Low−capacitance ESD Channel |
| 3 | CH3 | I/O | LV Low−capacitance ESD Channel |
| 4 | $V_{CC}$ | HV $V_{DD}$ | HV ESD Channel |
| 5 | GND | − | Ground |
| 6 | $V_N$ | − | Negative Voltage Supply Rail |
| 7 | $V_N$ | − | Negative Voltage Supply Rail |
| 8 | $V_N$ | − | Negative Voltage Supply Rail |
| DAP | GND | − | Die Attach Pad (Ground) |

**PACKAGE / PINOUT DIAGRAMS**




CM1643−04D4
8−Lead UDFN Package

## SPECIFICATIONS

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Parameter | Rating | Units |
|---|---|---|
| DC Voltage on Low−Voltage Pins | 6 | V |
| DC Voltage on High−Voltage Pins ($V_{CC}$pin) | 29 | V |
| Storage Temperature Range | −65 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. STANDARD OPERATING CONDITIONS**

| Parameter | Rating | Units |
|---|---|---|
| Operating Temperature Range | −40 to +85 | °C |

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_F$ | LV Diode Reverse Voltage (Positive Voltage) | $I_F$ = 10 mA, $T_A$ = 25°C | 6.8 | 8.2 | 9.2 | V |
| | LV Diode Forward Voltage (Negative Voltage) | $I_F$ = 10 mA, $T_A$ = 25°C | −1.05 | −0.90 | −0.60 | |
| $I_{LEAK}$ | LV Channel Leakage Current (Pins 1 and 2) | $T_A$ = −30°C to 65°C, $V_{IN}$ = 3.3 V $V_N$ = 0 V | | | 100 | nA |
| | LV Channel Leakage Current (Pin 3 only) | $T_A$ = −30°C to 65°C, $V_{IN}$ = 3.3 V $V_N$ = 0 V | | | 100 | |
| $C_{IN}$ | LV Channel Input Capacitance | At 1 MHz, $V_N$ = 0 V, $V_{IN}$ = 1.65 V | | 1.2 | 1.5 | pF |
| $\Delta C_{IN}$ | LV Channel Input Capacitance Matching | At 1 MHz, $V_N$ = 0 V, VIN = 1.65 V | | 0.02 | | pF |
| $I_{LEAK\_HV}$ | HV Channel Leakage Current | $T_A$ = 25°C, $V_{CC}$ = 28 V, $V_N$ = 0 V | | 0.1 | 1.0 | μA |
| $C_{IN\_HV}$ | HV Channel Input Capacitance | At 1 MHz, $V_N$ = 0 V, $V_{IN}$ = 2.5 V | | 30 | | pF |
| $V_{F\_HV}$ | HV Diode Breakdown Voltage Positive Voltage | $I_F$ = 10 mA, $T_A$ = 25°C | 30 | | 35 | V |
| $V_{ESD}$ | ESD Protection Peak Discharge Voltage at any channel input, in system Contact Discharge per IEC 61000−4−2 Standard | $T_A$ = 25°C | ±8 (Pin 1−3) ±15 (Pin 4) | | | kV |

**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CL}$ | LV Channel Clamp Voltage (Pin 1−3)<br>Positive Transients<br>Negative Transients | <br>$T_A$ = 25°C, $I_{PP}$ = 1 A,<br>$t_P$ = 8/20 μS | | <br>+9.64<br>−1.75 | | V |
| $R_{DYN}$ | Dynamic Resistance<br>LV Channel Positive Transients<br>LV Channel Negative Transients<br>HV Channel Positive Transients<br>HV Channel Negative Transients | $I_{PP}$ = 1 A, $t_P$ = 8/20 μS<br>Any I/O Pin to Ground | | <br>0.72<br>0.59<br>4.00<br>0.20 | | Ω |

1. All parameters specified at $T_A$ = −40°C to +85°C unless otherwise noted.

## PERFORMANCE INFORMATION

### Input Channel Capacitance Performance Curves for Low Voltage Pins

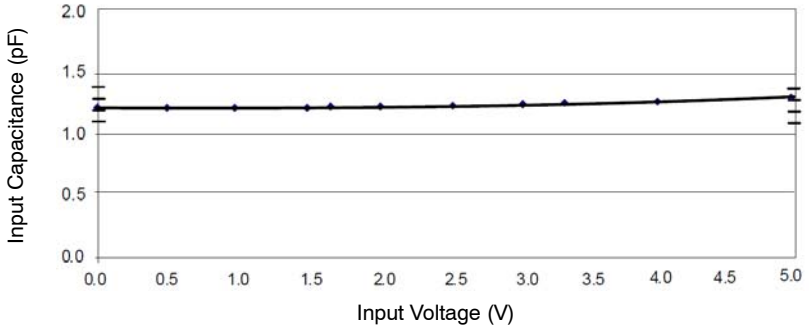



**Figure 1. Typical Variation of $C_{IN}$ vs. $V_{IN}$ (Low Voltage Inputs, f = 1 MHz, $V_N$ = 0 V )**

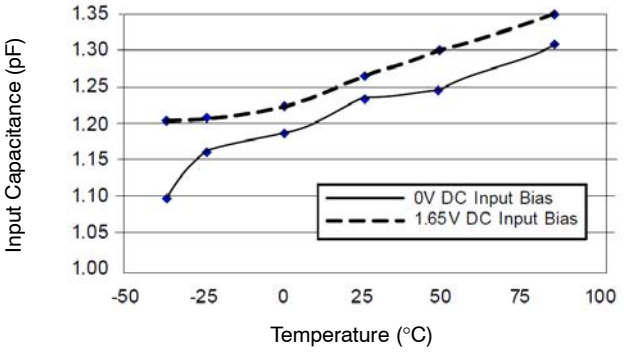



**Figure 2. Typical Variation of $C_{IN}$ vs. Temperature (Low Voltage Inputs, f = 1 MHz, $V_N$ = 0 V )**

## PERFORMANCE INFORMATION (Cont'd)

**Typical Filter Performance for Low Voltage Pins**

Nominal conditions unless specified otherwise, 50 Ω Environment.

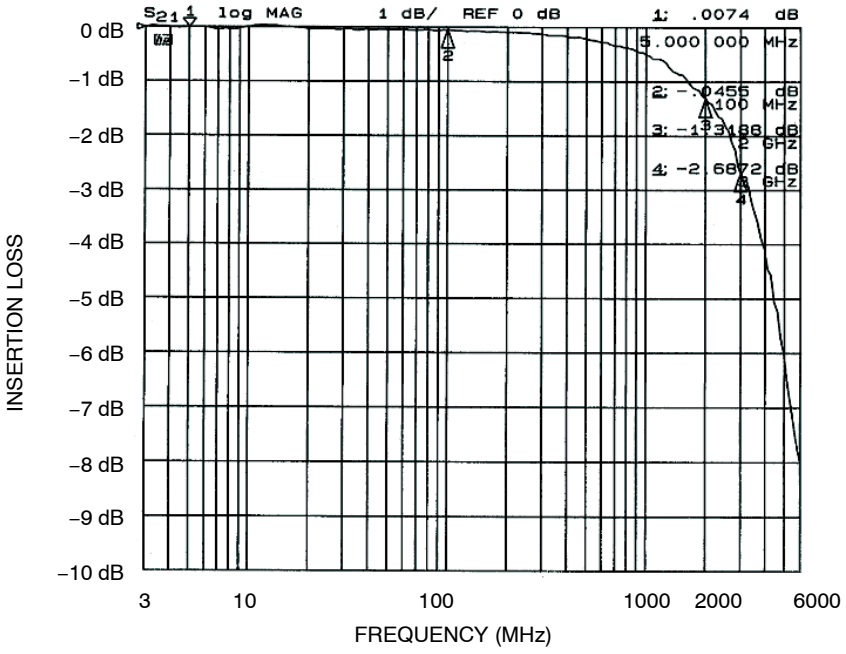



**Figure 3. Channel 1 vs. All GND Pins (0 V DC Bias)**

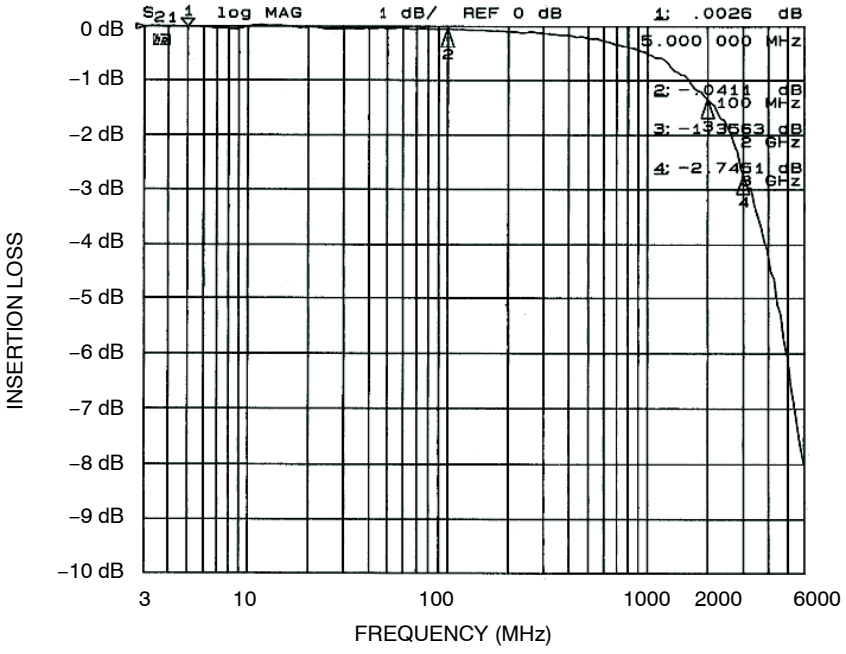



**Figure 4. Channel 2 vs. All GND Pins (0 V DC Bias)**

## PERFORMANCE INFORMATION (Cont'd)

**Typical Filter Performance for Low Voltage Pins**

Nominal conditions unless specified otherwise, 50 Ω Environment.

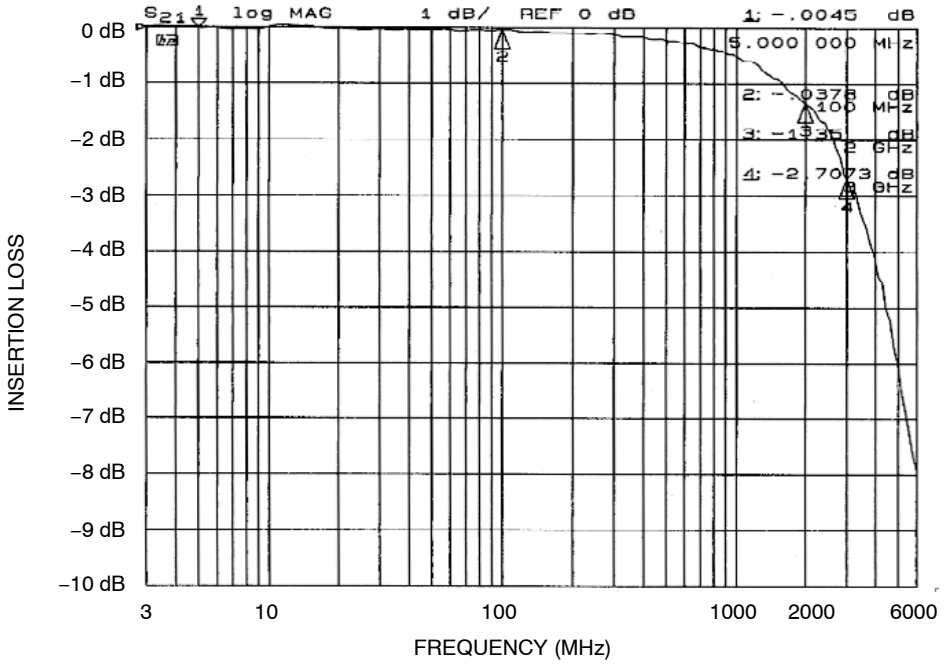
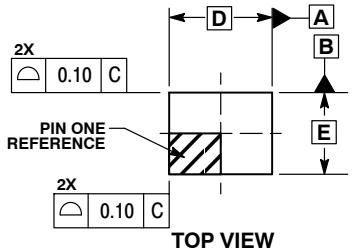
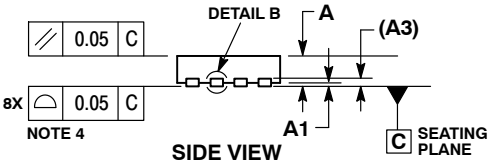


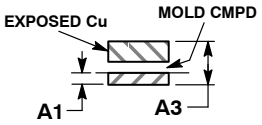

**Figure 5. Channel 3 vs. All GND Pins (0 V DC Bias)**

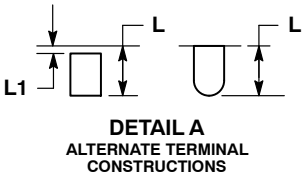
## PACKAGE DIMENSIONS

**UDFN8, 1.7x1.35, 0.4P**
CASE 517BC−01
ISSUE O



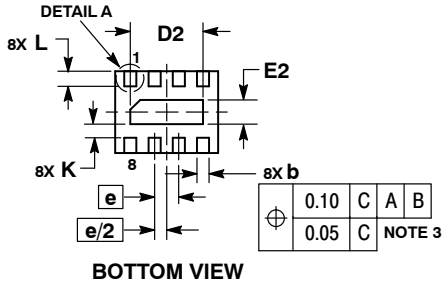



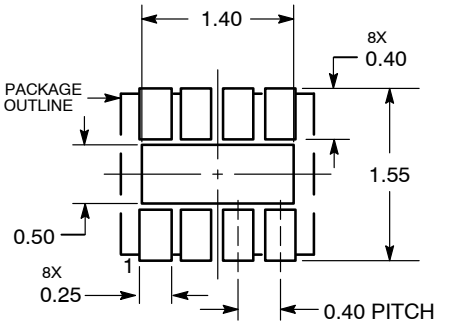




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.13 REF | |
| b | 0.15 | 0.25 |
| D | 1.70 BSC | |
| D2 | 1.10 | 1.30 |
| E | 1.35 BSC | |
| E2 | 0.30 | 0.50 |
| e | 0.40 BSC | |
| K | 0.15 | −−− |
| L | 0.20 | 0.30 |
| L1 | −−− | 0.05 |




### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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