Chunghwa Picture Tubes, Ltd.
Product Specification

To : **Plenteo**
Date : 110302

TFT LCD
CLAP101NC01CW

ACCEPTED BY : (V0.0)

APPROVED BY	CHECKED BY	PREPARED BY
張聖暉	李家銘	羅宇城

Prepared by :
Product Planning Management Division
Small & Medium TFT Product Business Unit
CHUNGHWA PICTURE TUBES, LTD.
1127 Hopin Rd., Padeh, Taoyuan, Taiwan 334, R.O.C.
TEL: +886-3-3675151 FAX: +886-3-377-3858

Doc.No:	SPEC_CLAP101NC01CW_V0.0_Plenteo_110302	Issue Date	20110117

REVISION STATUS

Revision Notice	Description	Page	Rev. Date
0.0	First revision (Tentative)	--	2011/01/17

CONTENTS

1. OVERVIEW

CLAP101NC01CW is 10.1" color TFT-LCD (Thin Film Transistor Liquid Crystal Display) OLB module (finish outer lead bonding) composed of LCD panel and driver ICs (the backlight is not included in this OLB module).

The 10.1" screen produces 1024(*3)X600 resolution image. By applying R.G.B. input signal, full color images are displayed.

General specifications are summarized in the following table:

ITEM	SPECIFICATION
Display Area (mm)	222.72(W) x 125.28(H)
Number of Pixels	1024(H) × 3 (RGB) × 600(V)
Pixel Pitch (mm)	0.2175(W) x 0.2088(H)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	Normally white
Number of color	16.2M
Response Time (Tr+Tf)	20ms(typ.)
Panel Transmittance (%)	5.9(typ)
Power Consumption(W)	480mW(typ.)
Surface Treatment	Anti-Glare

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VDD VDD_LVDS	-0.3	5	V	
Analog Supply Voltage	AVDD	-0.5	15	V	
Gate On Voltage	VGH	-0.3	40	V	
Gate Off Voltage	VGL	-20	0.3	V	
Gate On-Gate Off Voltage	VGH-VGL	-0.3	40	V	
Signal Input Voltage	NIND0 ~ NIND3 PIND0 ~ PIND3 NINC,PINC	-0.5	5	V	

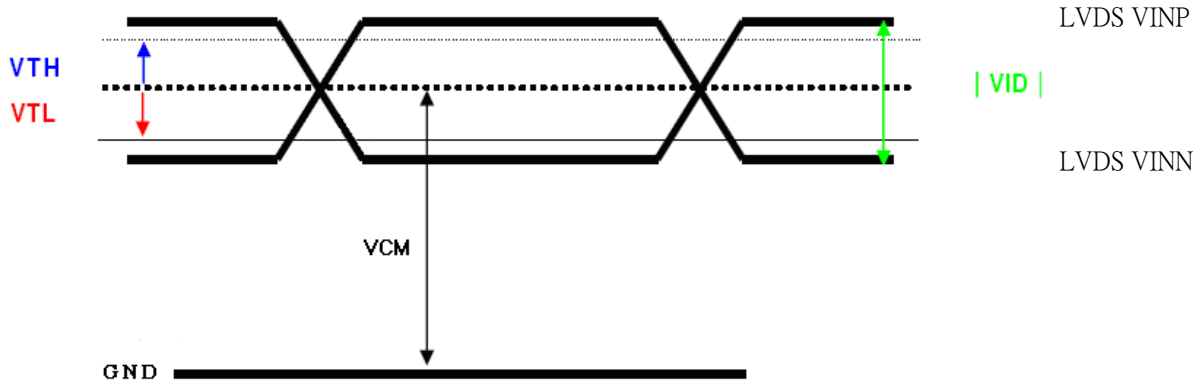
3. ELECTRICAL CHARACTERISTICS

3.1 Typical operation conditions

Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage For LCD	VDD VDD_LVDS	3	3.3	3.6	V	
Logic Input Voltage (LVDS:IN+,IN-)	VCM	$\frac{\lvert VID \rvert}{2}$	-	$2.4-\frac{\lvert VID \rvert}{2}$	V	Note1
	$\lvert VID \rvert$	200	-	600	mV	Note1
	VTH	-	-	100	mV	VCM=1.2V Note1
	VTL	-100	-	-	mV	
Analog Power Supply Voltage	AVDD	TBD	9.6	TBD	V	
Gate On Power Supply Voltage	VGH	17	18	19	V	
Gate Off Power Supply Voltage	VGL	-6.6	-6	-5.4	V	
Common Power Supply Voltage	VCOM	TBD	TBD	TBD	V	Note2

【Note1】
LVDS signal



【Note2】Please adjust VCOM to make the flicker level be minimum.

3.2 TFT-LCD Current consumption

ITEM	SYMBOL	Condition	MIN	TYPE	MAX	UNIT	NOTE
Gate on power current	IVGH	VGH =18V	-	0.5	1	mA	Note1
Gate off power current	IVGL	VGL= -6V	-	0.5	1	mA	Note1
Digital power current	IVDD	VDD = 3.3V	-	40	50	mA	Note1
Analog power current	IAVDD	AVDD = 9.6V	-	35	45	mA	Note1
Total Power Consumption	PC		-	480	621	mW	Note1

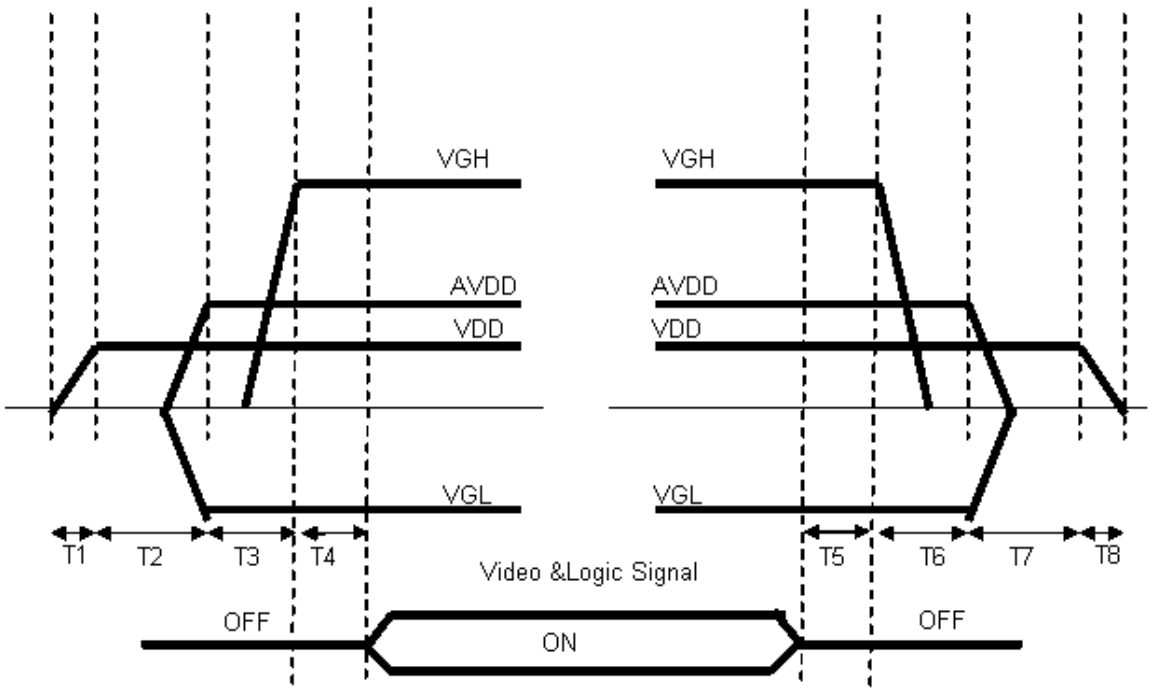
Note1: Typical: Under 256 gray pattern
Maximum: Under black pattern

256 gray pattern

Black Pattern

3.3 Power、Signal sequence

Power On：VDD→AVDD/VGL →VGH →Video &Logic Signal
Power Off：Video &Logic Signal→ VGH→AVDD/VGL→VDD



$0 < T1 \leqq 10ms$
$20ms < T2$
$10ms < T3$
$0 < T4 \leqq 10ms$

$0 < T5 \leqq 10ms$
$0 < T6$
$0 < T7$
$0 < T8$

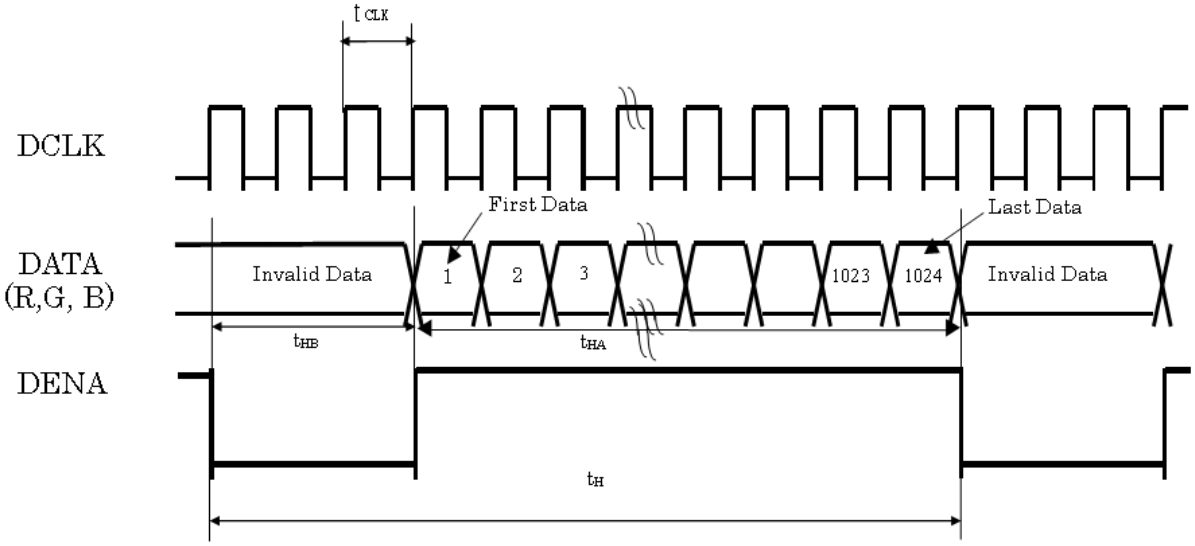
3.4 Timing characteristics of input signals

(1)Timing Specification

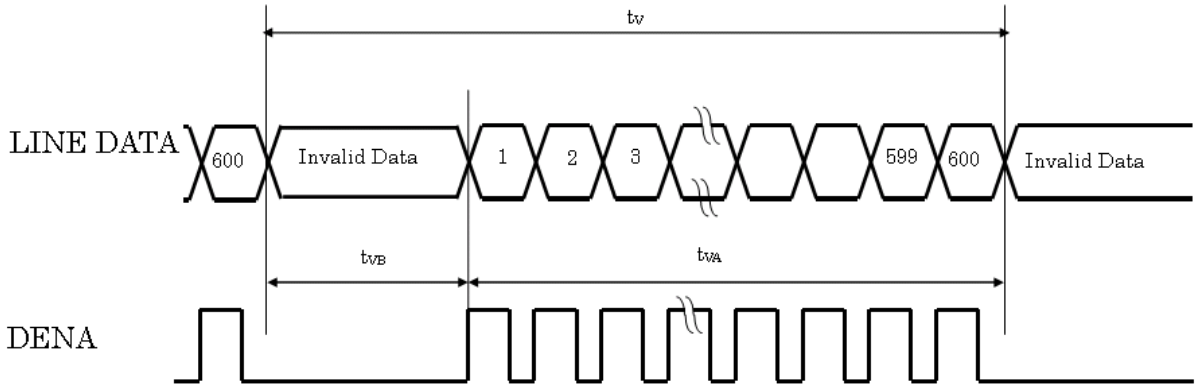
Item				Symbol	Min	Typ	Max	Unit
LVDS input signal sequence	CLK Frequency			tclk	45	51.2	57	MHz
LCD input signal sequence （Input LVDS Transmitter）	DENA	Horizontal	Horizontal total Time	t_H	1324	1344	1364	tCLK
			Horizontal effective Time	t_{HA}	1024			tCLK
			Horizontal Blank Time	t_{HB}	300	320	340	tCLK
		Vertical	Vertical total Time	t_V	625	635	645	t_H
			Vertical effective Time	t_{VA}	600			t_H
			Vertical Blank Time	t_{VB}	25	35	45	t_H

(2)Timing Chart

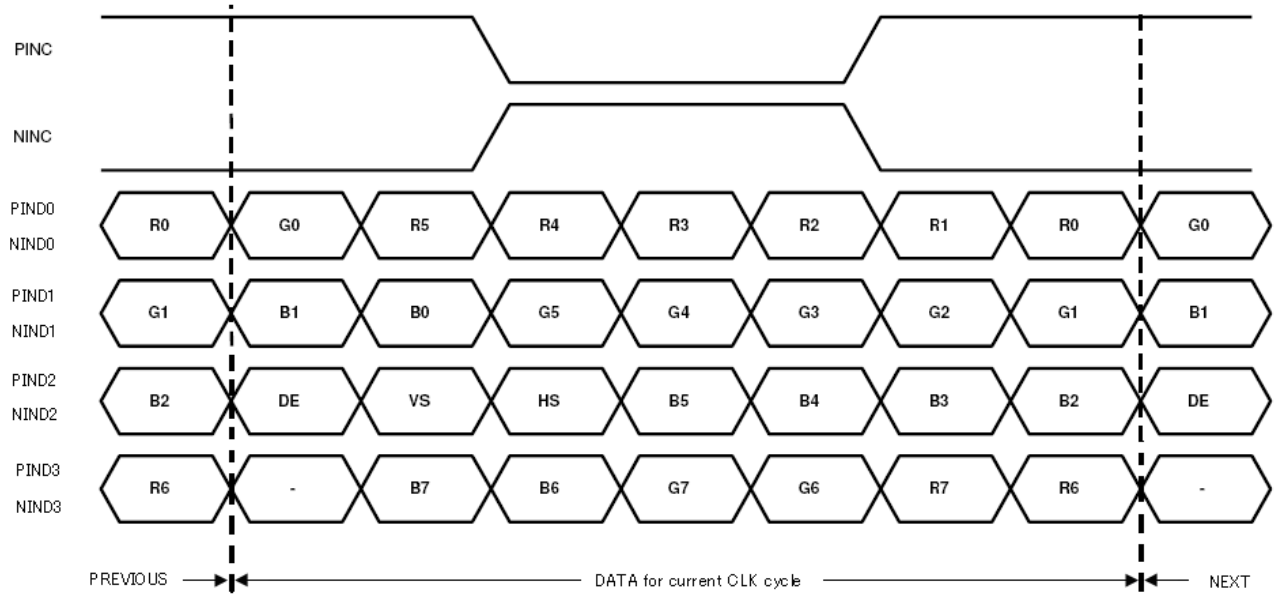
Horizontal Timing Sequence



Vertical Timing Sequence



LVDS Input Data mapping



4. INTERFACE CONNECTION:

4.1 CN1(Signal of interface)

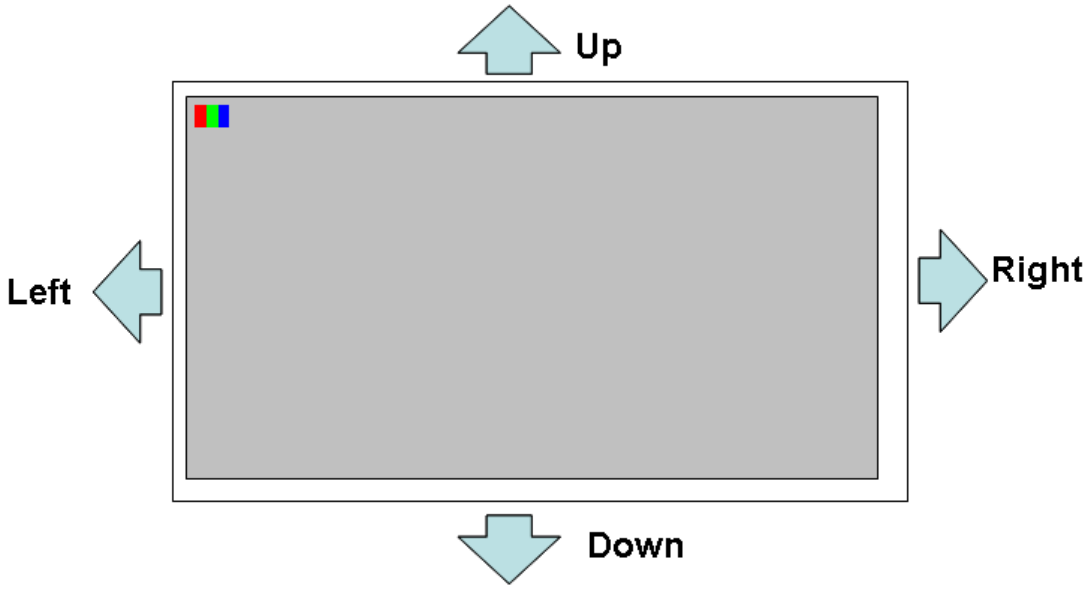
PIN NO	SYMBOL	DESCRIPTION
1	AGND	Analog ground
2	AVDD	Analog power
3	VDD	Digital power
4	GND	Digital ground
5	VCOM	Common voltage
6	VDD	Digital power
7	GND	Digital ground
8	V14	Gamma correction voltage reference
9	V13	Gamma correction voltage reference
10	V12	Gamma correction voltage reference
11	V11	Gamma correction voltage reference
12	V10	Gamma correction voltage reference
13	V9	Gamma correction voltage reference
14	V8	Gamma correction voltage reference
15	GND	Digital ground
16	VDD_LVDS	LVDS power
17	GND	Digital ground
18	PIND3	Positive LVDS differential data inputs
19	NIND3	Negative LVDS differential data inputs
20	GND	Digital ground
21	PINC	Positive LVDS differential clock inputs
22	NINC	Negative LVDS differential clock inputs
23	GND	Digital ground
24	PIND2	Positive LVDS differential data inputs
25	NIND2	Negative LVDS differential data inputs
26	GND	Digital ground
27	PIND1	Positive LVDS differential data inputs
28	NIND1	Negative LVDS differential data inputs
29	GND	Digital ground
30	PIND0	Positive LVDS differential data inputs
31	NIND0	Negative LVDS differential data inputs
32	GND	Digital ground
33	GND_LVDS	LVDS ground
34	GRB	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability. Normally pull high. (R=10KΩ，C=0.1μF)
35	STBYB	Standby mode, normally pull high STBYB=”1”, normal operation STBYB=”0”,timing control, source driver will turn off, all output are high-Z
36	SHLR	Left or right display control
37	VDD	Digital power
38	UPDN	Up / down display control
39	AGND	Analog ground
40	AVDD	Analog power
41	VCOM	Common voltage
42	DITH	Dithering function enable control. Normally pull low DITHER = “1”, Enable internal dithering function DITHER = “0”, Disable internal dithering function
43	GND	Digital ground
44	VDD	Digital Power
45	GND	Digital ground
46	V7	Gamma correction voltage reference
47	V6	Gamma correction voltage reference
48	V5	Gamma correction voltage reference
49	V4	Gamma correction voltage reference

50	V3	Gamma correction voltage reference
51	V2	Gamma correction voltage reference
52	V1	Gamma correction voltage reference
53	GND	Digital ground
54	VDD	Digital power
55	GND	Digital ground
56	VGH	Positive power for TFT
57	VDD	Digital power for Gate IC
58	VGL	Negative power for TFT
59	GND	Digital ground for Gate IC
60	NC	Not connect

Remarks：

1) Mating connector：089K60-000100-G2-R (STARCONN)
2) UPDN and SHLR control function

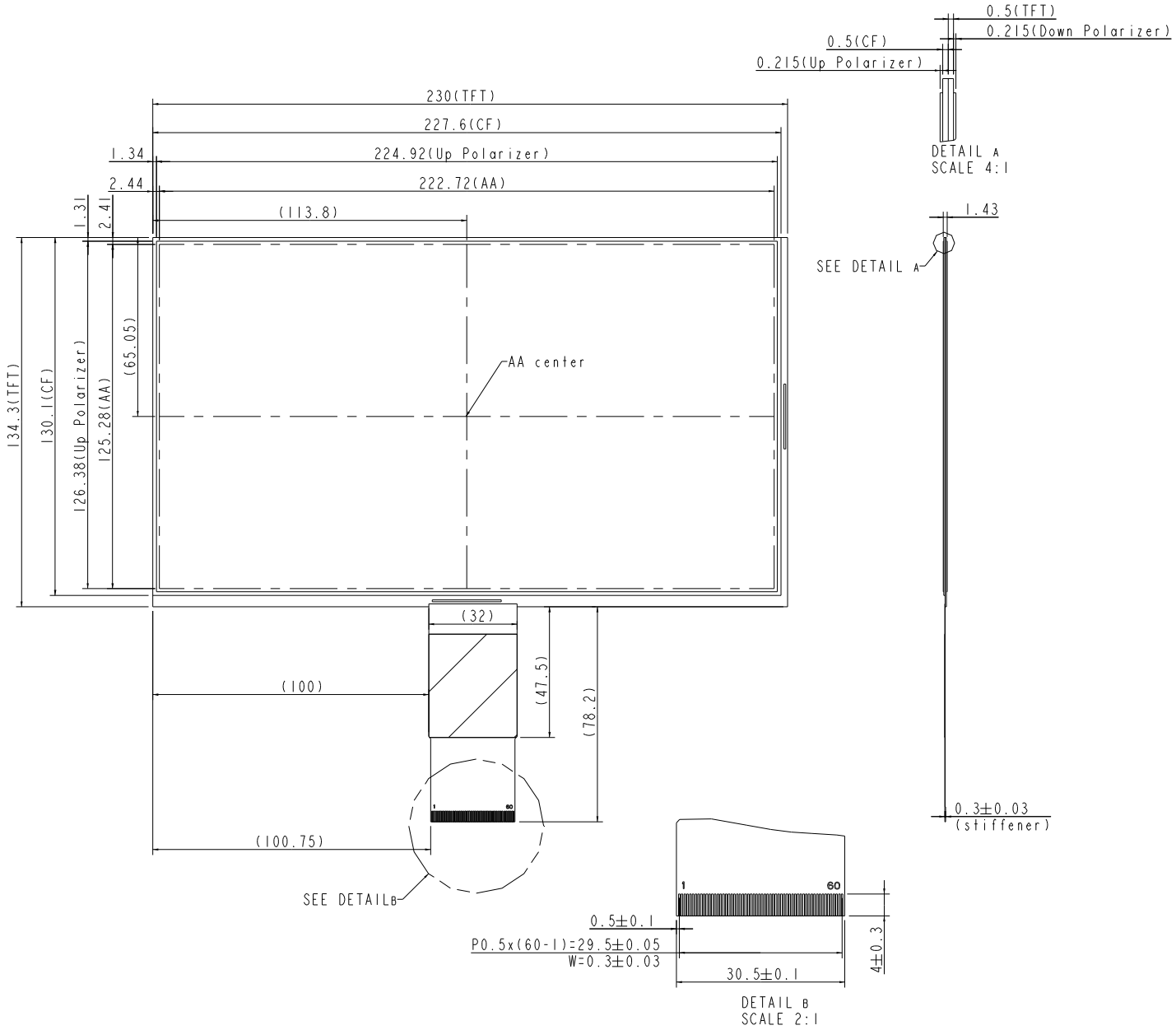
UPDN	SHLR	FUNCTION
0	1	Normal display
0	0	Inverse Left and Right
1	1	Inverse Up and Down
1	0	Inverse Left and Right Inverse Up and Down



5. MECHANICAL DIMENSION

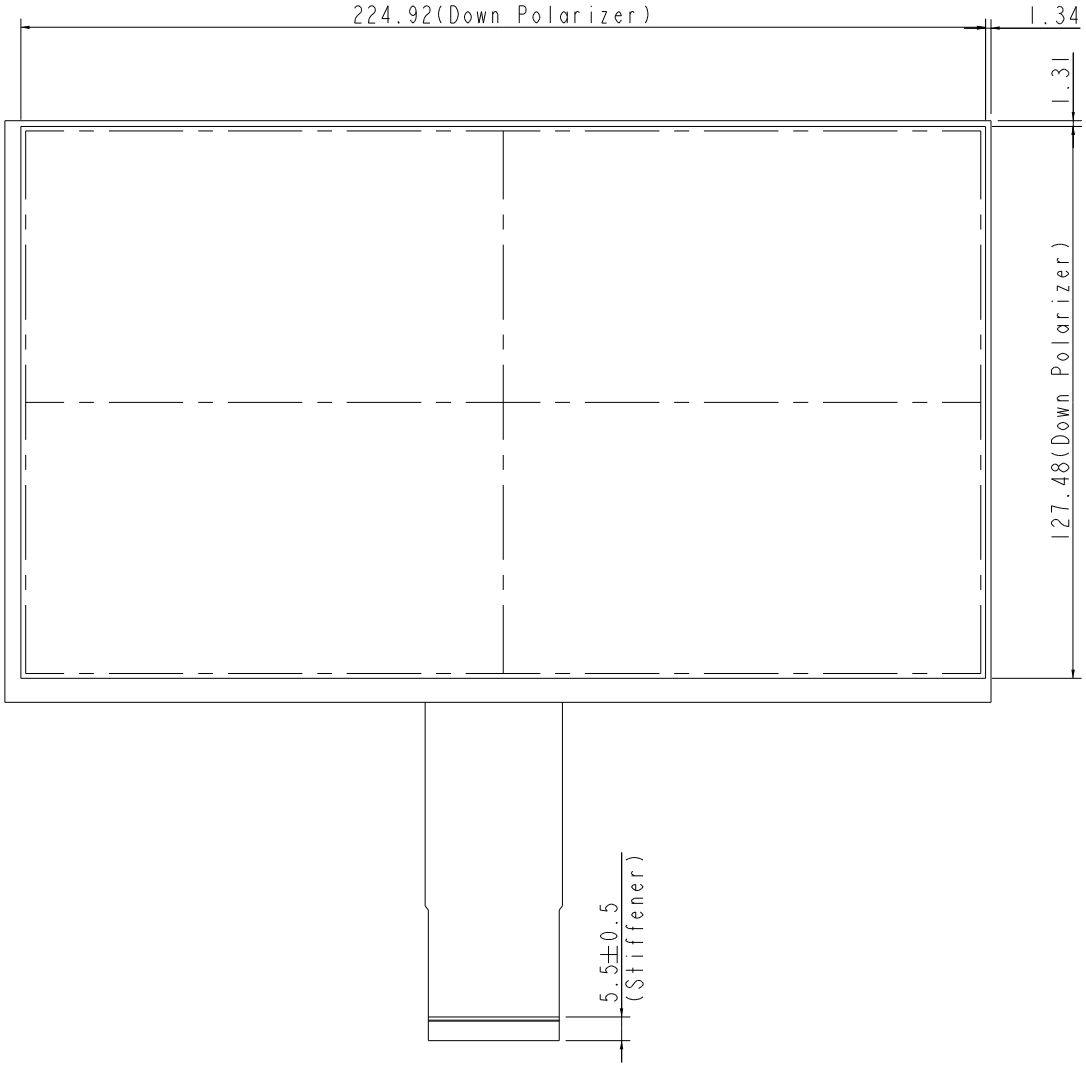
5.1 Front Side

(Unit： mm)



5.2 Rear Side

(Unit： mm)



NOTE: General tolerance=±0.3mm

6. OPTICAL CHARACTERISTICS

(Use CPT LED backlight) Ta=25℃

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
Panel Transmittance		T	~	5.5	5.9	--	%	
Response Time		Tr +Tf	Point-5	--	20	40	ms	. 1
Viewing Angle	Horizontal	ϕ	Point-5 CR≧10	120	140	--	°	2
	Vertical	θ		100	120	--	°	2
Color Filter Chromacicity	White	x	θ=ϕ= 0°	0.273	0.313	0.353		3
		y		0.289	0.329	0.369		3
	Red	x	θ=ϕ= 0°	(TBD)	(TBD)	(TBD)		3
		y		(TBD)	(TBD)	(TBD)		3
	Green	x	θ=ϕ= 0°	(TBD)	(TBD)	(TBD)		3
		y		(TBD)	(TBD)	(TBD)		3
	Blue	x	θ=ϕ= 0°	(TBD)	(TBD)	(TBD)		3
		y		(TBD)	(TBD)	(TBD)		3

Note 1: Definition of Response Time.(White-Black)
The response time is defined as the time interval between the 10% and 90% amplitudes.

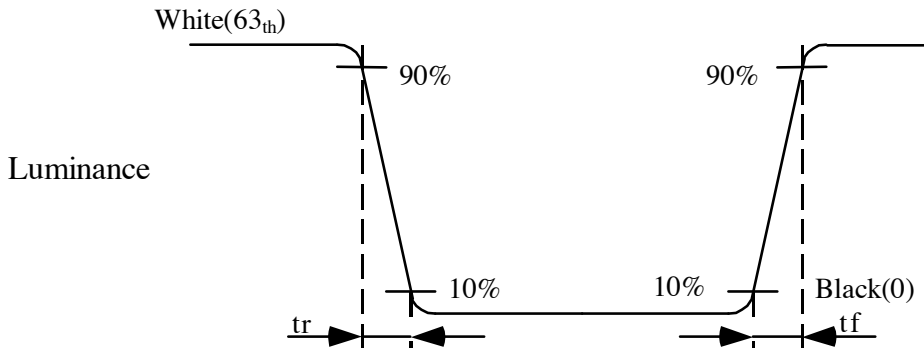


Fig. 6-1 Measuring point

Note 2: Definition of Viewing Angle(θ,ψ)

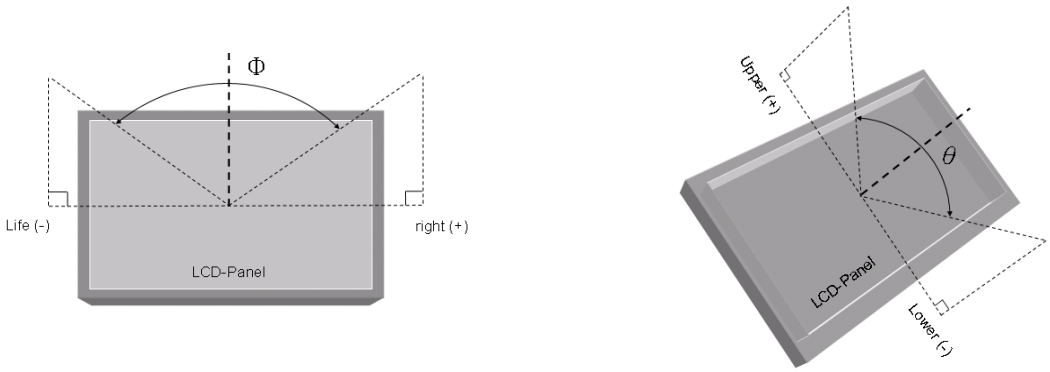


Fig.6-2 Definition of Viewing Angle

Note 3: Under C light

7. RELIABILITY TEST

(These tests are conducted with CPT backlight.)

7.1 Temperature and Humidity

TEST ITEMS	CONDITIONS	NOTE
High Temperature Operation	70℃ ;240hrs	
High Temperature Storage	80℃ ; 240hrs	
High Temperature High Humidity Operation	60℃ ; 90%RH ;240hrs	No condensation
Low Temperature Operation	-20℃ ; 240hrs	Backlight unit always turn on
Low Temperature Storage	-30℃ ; 240hrs	
Thermal Shock	–30℃(0.5hr) ~ 80℃(0.5hr) ; 200 Cycles	
Image Sticking	25 ℃± 2 ℃ ; 24hrs	Note 1.

Note 1.：

Condition of Image Sticking test：25 ℃± 2 ℃

Operation with test pattern sustained for 24 hrs, then change to gray pattern immediately.

After 5 mins, the mura must be disappeared completely .

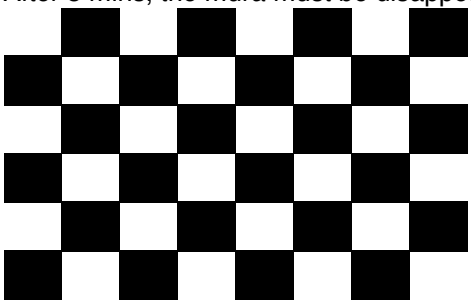


Image Sticking –pattern

Mid-Gray pattern

7.2 Shock and Vibration

TEST ITEMS	CONDITIONS
Shock (Non-operation)	● Shock level: 980m/s^2(equal to 100G). ● Waveform: half sinusoidal wave,6ms. ● Number of shocks: ±X,±Y,±Z axes for a total of six shock inputs.
Vibration (Non-operation)	● Frequency range:8~33.3Hz ● Stoke：1.3 mm ● Vibration: sinusoidal wave, perpendicular axis(both x, y axis: 2hrs ,z axis: 4hrs). ● Sweep: 2.9G,33.3 Hz -400 Hz ● Cycle time: 15 min

7.3 Electrostatic Discharge

TEST ITEM	CONDITIONS	NOTE
ESD	150pF，330Ω，±8kV&±15kV air& contact test	1
	200pF，0Ω，±200V contact test	2

Note: Measure point :

1. LCD glass and metal bezel
2. IF connector pins

7.4 Judgment Standard

The judgment of the above test should be made as follow:

Pass: Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

Fail: No display image, obvious non-uniformity, or line defects.