Chunghwa Picture Tubes, Ltd.
Product Specification

To :
Date :

TFT LCD

CLAN065WA41 3XB (OTM1283A-C35)

ACCEPTED BY : (V0.0)

Tentative

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REVISION STATUS

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1. OVERVIEW

CPT CLAN65WA41 3XB is a COG product which is a cell product with IC bonded. This is a 16：9 aspect ratio panel for the mobile application.

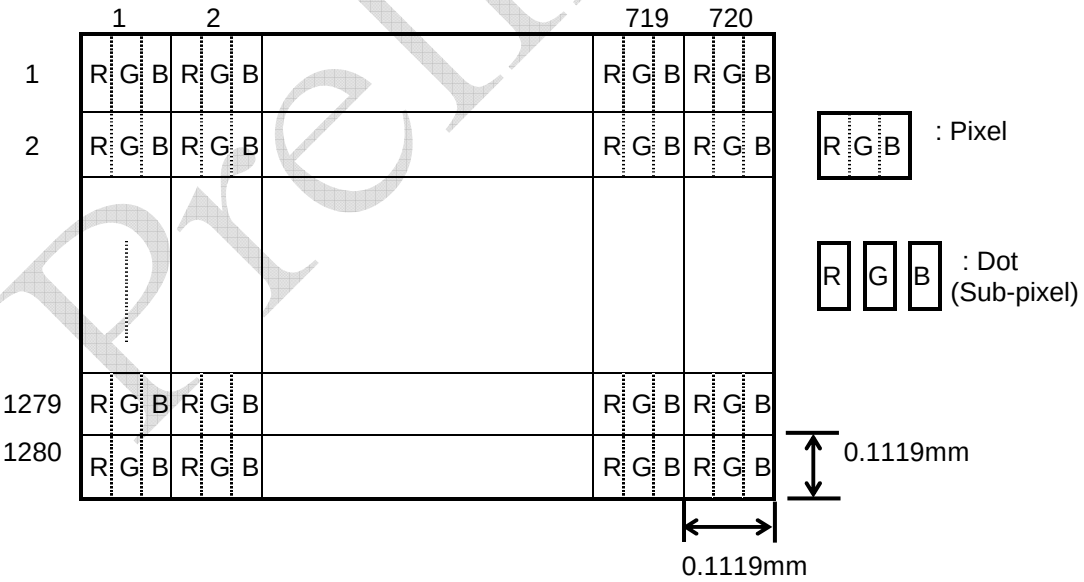
The 6.5” screen produces a high resolution image that is composed of 921,600 (720x1280) pixel elements in a stripe arrangement.

General specifications are summarized in the following table:

ITEM	SPECIFICATION
Panel Size	6.5 inch
Display Area (mm)	80.568 (H) x 143.232 (V)
CF glass dimension	83.368 (H) x 147.332 (V) x 0.2 (Thickness)
TFT glass dimension	83.368 (H) x 151.4 (V) x 0.2 (Thickness)
Number of Pixels	720 (H) x 3 x 1280 (V)
Pixel Pitch (mm)	0.1119 (H) x 0.1119 (V)
Color Pixel Arrangement	RGB Stripe
NTSC	70 % (TYP)
Display Mode	FFS (Normal Black)
Driving Method	TFT active matrix
Viewing Direction	85/85/85/85 (U/D/L/R)
Suggesting IC	OTM1283A-C35

Note: The FPC circuit design is possibly different according to the individual suggesting IC internal circuit definition and application. Please refer to the IC datasheet respectively.

LCD Cell Drawing
(Note 1)



The LCD products listed on this document are not suitable for use of aerospace equipment, submarine cables, nuclear reactor control system and life support systems. If customers intend to use these LCD products for above application or not listed in "Standard" as follows, please contact our sales people in advance.

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remark
Electrical Phase					
Power Supply Voltage for Analog	*VDD*	-0.3	4.4	V	
Power Supply Voltage for I/O	*VDDI*	-0.3	4.4	V	
TFT Gate High Voltage	*VGH*	--	18	V	
TFT Gate Low Voltage	*VGL*	-12	--	V	
Enviromental Phase					
Operating Ambient Temperature	T_{OP}	-20	+60	℃	
Operating Ambient Humidity	H_{OP}	10	90	%（RH）	
Storage Temperature	T_{STG}	-30	+80	℃	
Storage Humidity	H_{STG}	10	90	%（RH）	

Note 1. The absolute maximum ratings are the values that must not be exceeded at any time for this product. It is not allowed for any of these ratings to be exceeded. Should a product be used with any of the absolute maximum ratings exceeded, the characteristics of the product may not be recovered, or in an extreme case, the product may be permanently destroyed.

Therefore, when designing a system incorporating the product, make sure that adequate attentions be paid to the variations in the supply voltages, the characteristics of parts that are connected, surges in the input and output lines, and the ambient temperatures.

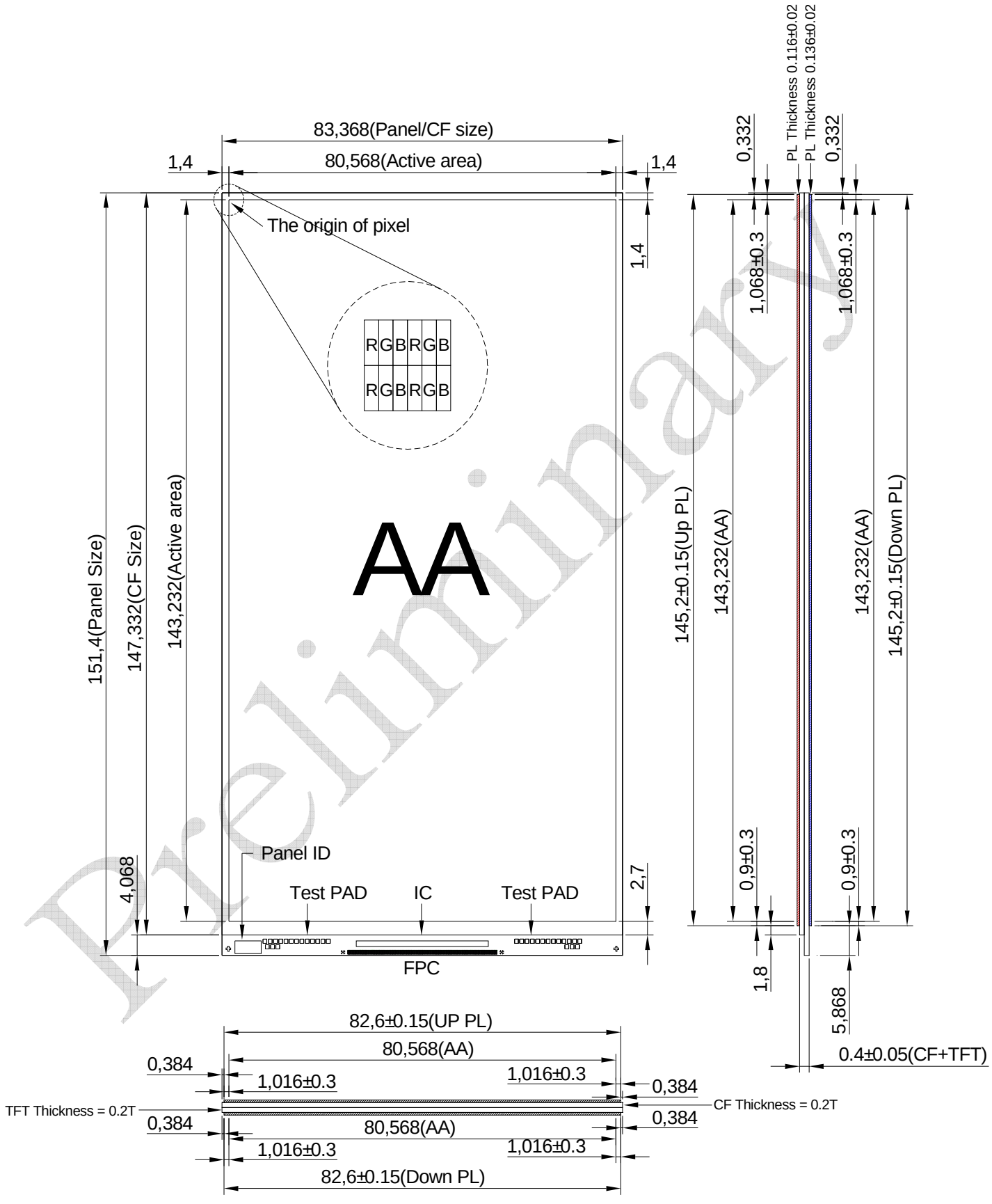
Note 2. This specification applys after the driver IC mounting and the FPC mounting. (This specification isn't applicable at time of driver IC un-mounting and FPC un-mounting.)

LCD should keep the condition that dew dosen't storage in case of driver IC un-mounting and FPC un-mounting. Dew may break the LCD. Especially part is very weak for dew.

3. MECHANICAL SPECIFICATIONS

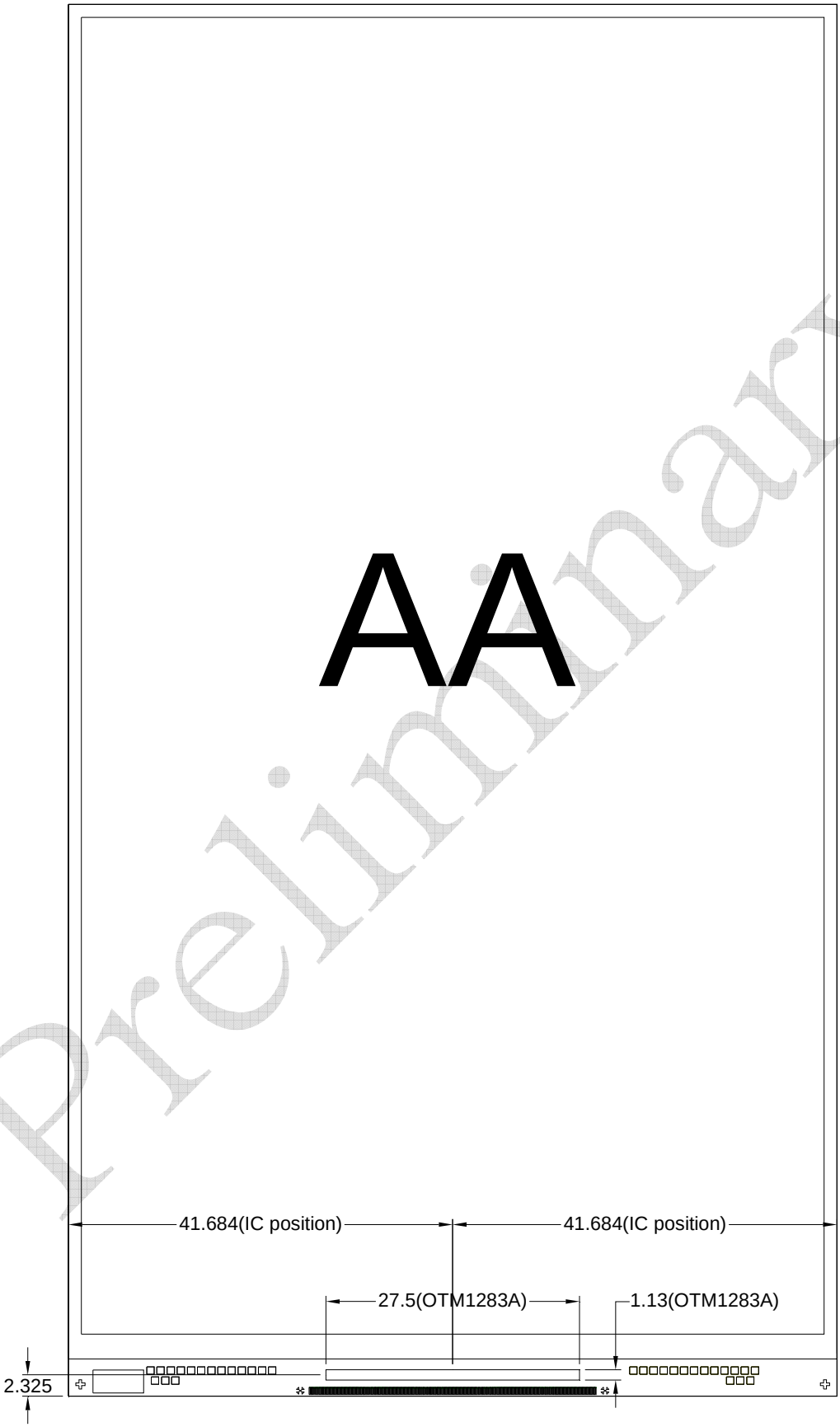
3.1. Outline Dimension

(unit: mm)



3.2. IC & FPC PAD

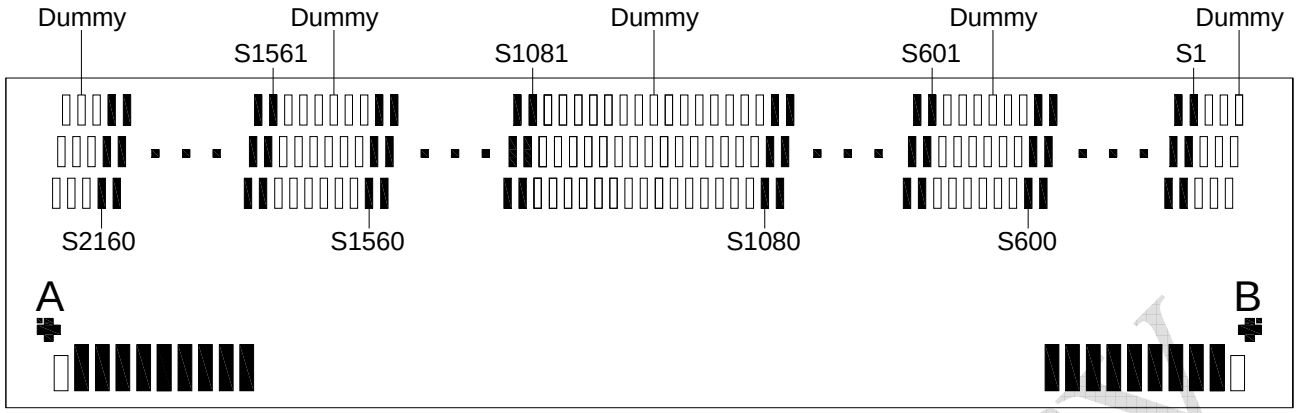
3.2.1. IC PAD



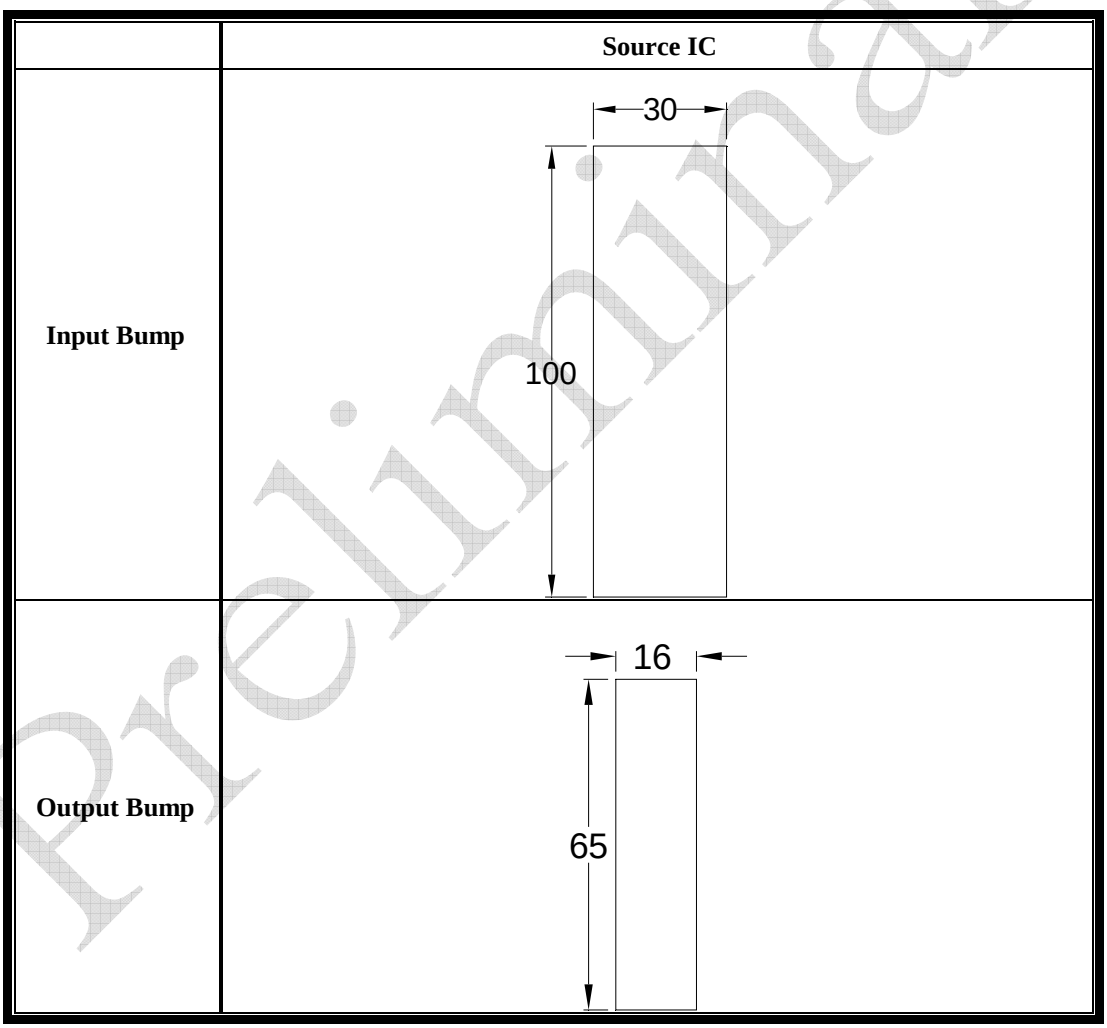
Note1. Color Filter is in the upper side , TFT is in the bottom side

3.2.2. COG Design (DOM)

- IC OTM1283A-C35



Gold Bump Size(unit：um)：

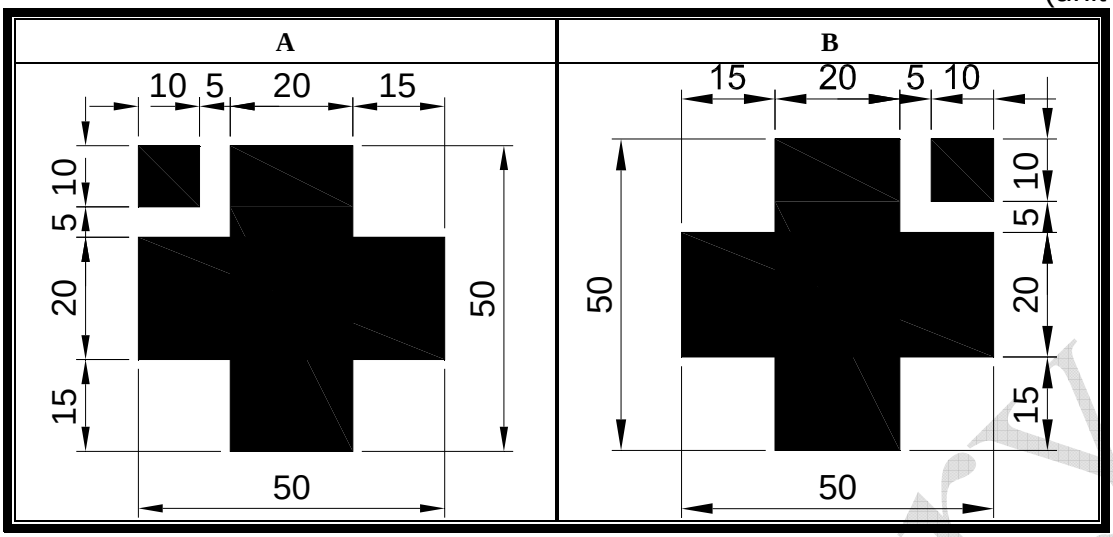


- Chip Size

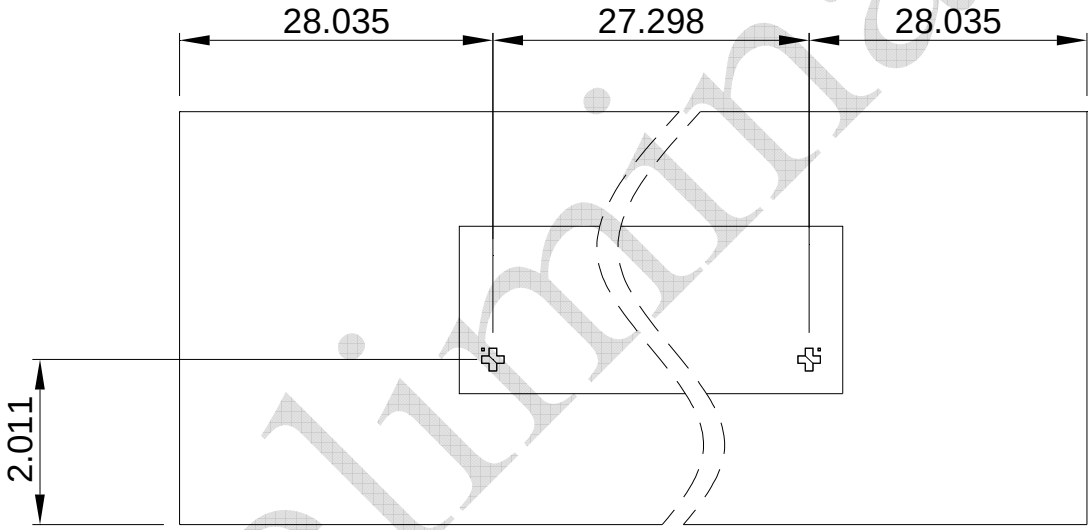
IC	Chip Size
OTM1283A-C35	27.5 mm x 1.13 mm

- Alignment Mark Size & Position

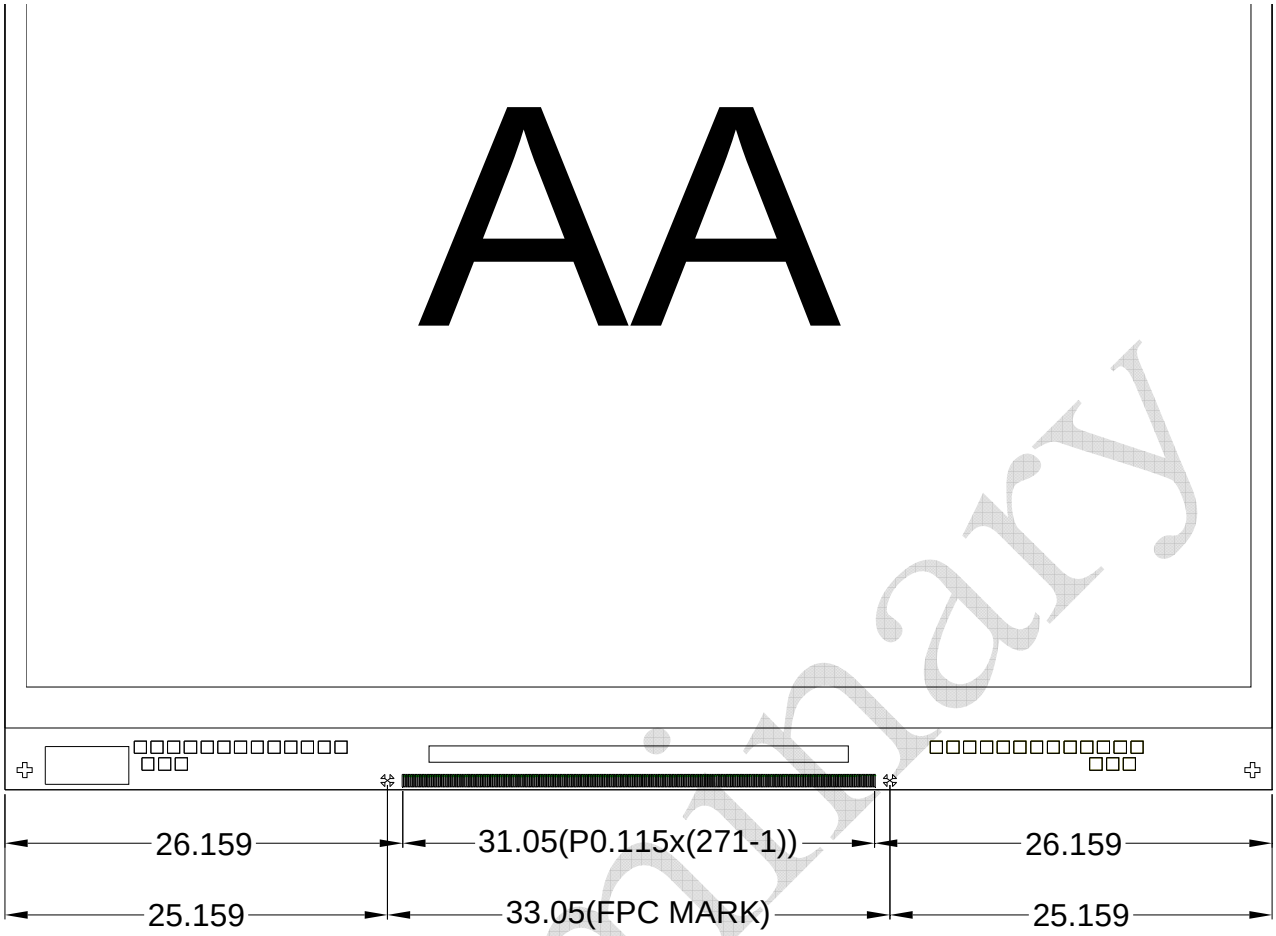
(unit = mm)



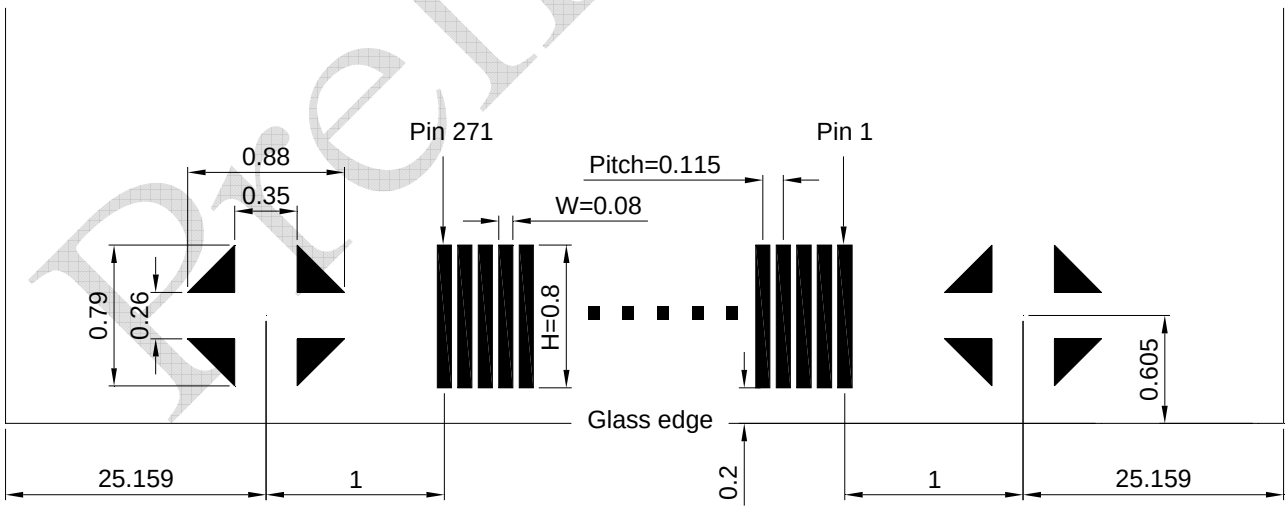
- Alignment Mark Position on the glass



3.2.3. FPC PAD



Detail FPC：



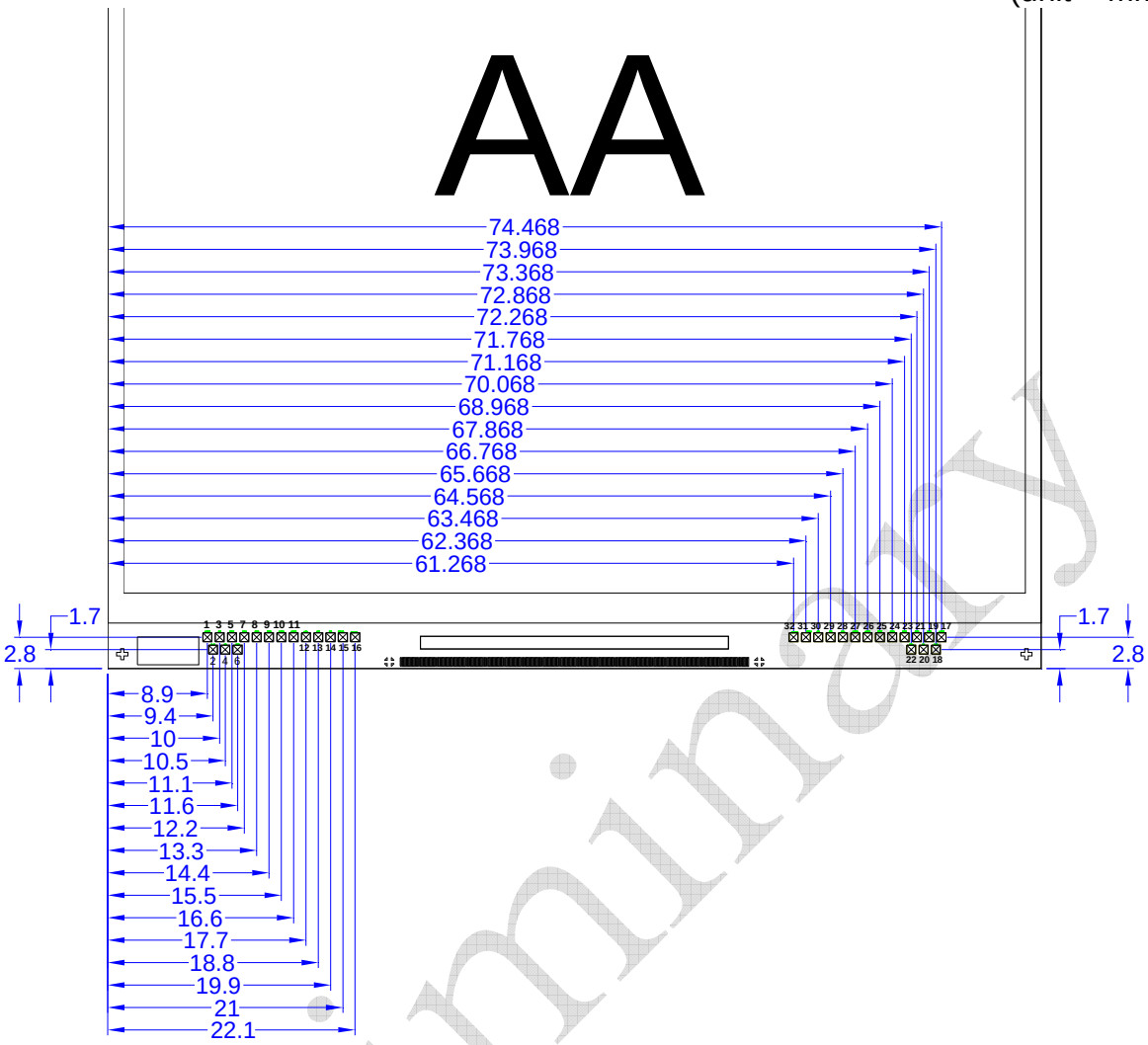
3.2.4. FPC Pin Assignment (OTM1283A-C35)

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	DUMMY	71	VCC	141	VSS	211	C21N
2	DUMMY	72	VCC	142	IM0	212	C21N
3	GND	73	VCC	143	VDDI	213	C22P
4	GND	74	VDD_18V	144	IM1	214	C22P
5	VCOM	75	VDD_18V	145	VSS	215	C22N
6	VCOM	76	VDD_18V	146	RS0	216	C22N
7	DUMMY	77	VDD_18V	147	VDDI	217	VGH
8	DUMMY	78	VDD_18V	148	RS1	218	VGH
9	DUMMY	79	VDD_18V	149	VSS	219	VCI
10	DUMMY	80	VDD_18V	150	LANSEL	220	VCI
11	DUMMY	81	VDD_18V	151	VDDI	221	DUMMY
12	DUMMY	82	VSS	152	BOOSTM0	222	VSS
13	DUMMY	83	VSS	153	VSS	223	VSS
14	DUMMY	84	VSS	154	BOOSTM1	224	VSS
15	VGLO_L	85	VSS	155	VCC	225	C23P
16	LVGL	86	TOUT0	156	VCC	226	C223P
17	DUMMY	87	VDDA	157	VCC	227	C23N
18	VGHO_L	88	VDDA	158	VCC	228	C23N
19	DUMMY	89	VDDA	159	VDD_18V	229	C24P
20	DUMMY	90	VDDA	160	VDD_18V	230	C24P
21	DUMMY	91	VDDA	161	VDD_18V	231	DUMMY
22	VCOM	92	VDDA	162	VDD_18V	232	C24N
23	VSSA	93	VDDA	163	VSS	233	C24N
24	VSSA	94	VDDA	164	VSS	234	C24N
25	VSSA	95	VSS	165	VSS	235	C24N
26	VSSA	96	VSS	166	VSS	236	VGL
27	LVDSVSS	97	VSS	167	EXTN	237	VGL
28	LVDSVSS	98	VSS	168	EXTN	238	VGL
29	D0N	99	VSS	169	EXTN	239	VGLC31P
30	D0N	100	C51P	170	EXTP	240	C31P
31	D0P	101	DUMMY	171	EXTP	241	C31P
32	D0P	102	C51P	172	EXTP	242	VGLO2
33	LVDSVSS	103	C51P	173	MTP_PWR	243	VGLO2
34	LVDSVSS	104	C51N	174	MTP_PWR	244	VGLO1
35	D1N	105	C51N	175	VCI	245	VGLO1
36	D1N	106	C51N	176	VCI	246	VCOMR
37	D1P	107	VSS	177	DUMMYN	247	VCOMR
38	D1P	108	C52P	178	DUMMYN	248	DUMMYR1
39	LVDSVSS	109	C52P	179	VSSA	249	VCOM
40	LVDSVSS	110	C52P	180	VSSA	250	DUMMY
41	CLKN	111	C52N	181	DUMMY	251	DUMMY

42	CLKN	112	C52N	182	VSSA	252	DUMMY
43	CLKP	113	C52N	183	VSSA	253	VGHO_R
44	CLKP	114	NVDDA	184	DUMMY	254	DUMMY
45	LVDSVSS	115	NVDDA	185	GVDD	255	LVGL
46	LVDSVSS	116	VSS	186	NGVDD	256	VGLO_R
47	D2N	117	D7	187	VREF	257	DUMMY
48	D2N	118	D6	188	VSS	258	DUMMY
49	D2P	119	D5	189	VSS	259	DUMMY
50	D2P	120	D4	190	VCI	260	DUMMY
51	LVDSVSS	121	D3	191	VCI	261	DUMMY
52	LVDSVSS	122	D2	192	VCL	262	DUMMY
53	LVDSVSS	123	D1	193	C41P	263	DUMMY
54	D3N	124	D0	194	C41P	264	DUMMY
55	D3N	125	HS	195	C41N	265	VGL
56	D3P	126	VS	196	C41N	266	VCOM
57	D3P	127	COUT_SEL	197	C42P	267	VCOM
58	LVDSVSS	128	PCLK	198	C42P	268	GND
59	LVDSVSS	129	DCX	199	C42N	269	GND
60	LVDSVSS	130	CSX	200	C42N	270	DUMMY
61	LVDSVSS	131	SCL	201	C42N	271	DUMMY
62	LVDSVDD	132	SDI	202	C42N		
63	LVDSVDD	133	SDO	203	CSP		
64	LVDSVDD	134	LEDPWM	204	VSP		
65	LVDSVDD	135	TE	205	VSP		
66	VDDAM	136	TE1	206	DUMMY		
67	VDDAM	137	RESX	207	VSN		
68	VDDAM	138	TEST2	208	CSN		
69	VDDAM	139	TEST1	209	C21P		
70	VCC	140	TEST0	210	C21P		

3.3. Panel Check Pad in Panel

(unit = mm)



Pad Size		800umx800um			
No.	Test Pad Name	Note	No.	Test Pad Name	Note
1	VCOM		17	VCOM	
2	D_R		18	D_G	
3	SW		19	D_B	
4	G2	不用測	20	G1	不用測
5	STV2	GIP Signal	21	STV1	GIP Signal
6	CK2		22	CK1	
7	CK4		23	CK3	
8	CK6		24	CK5	
9	CK8		25	CK7	
10	VDDO	不用測	26	VDDO	不用測
11	VDDE	不用測	27	VDDE	不用測
12	VGL	GIP Signal	28	VGL	GIP Signal
16	FW		29	FW	
14	BW		30	BW	
15	RST2		31	RST1	
16	G1280	不用測	32	G1280	不用測

3.3.1. CELL Test Light Waveform

Frame	D_GB	D_RG	D_BR	SW	Vcom
White (W)	L	L	L	H	DC/GND
Black (BK)	H	H	H	H	DC/GND
Gray (GY)	Gray	Gray	Gray	H	DC/GND
Zebra Stripe (Z)	H	H	H	H	DC/GND

Display Mode: TN, Normally White

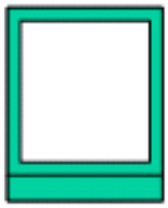
Every Frame stay > 2sec.

Ex. LC=5V, Vcom=0V

Data H=+/-5V, Data L=0V, Data Gray=+/-2.5V

SW_H=10V above (on duty), SW_L=-6V (not on duty)

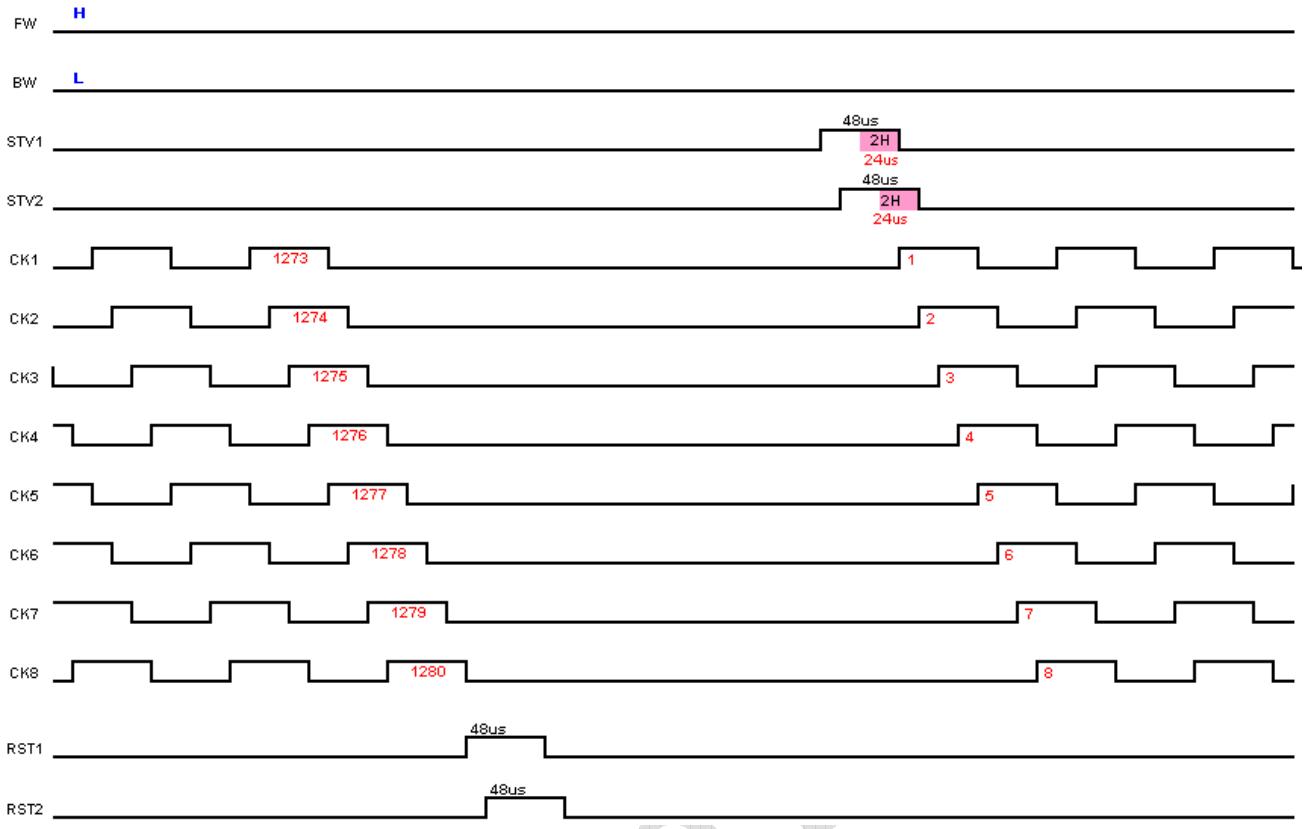
Just suggestion!



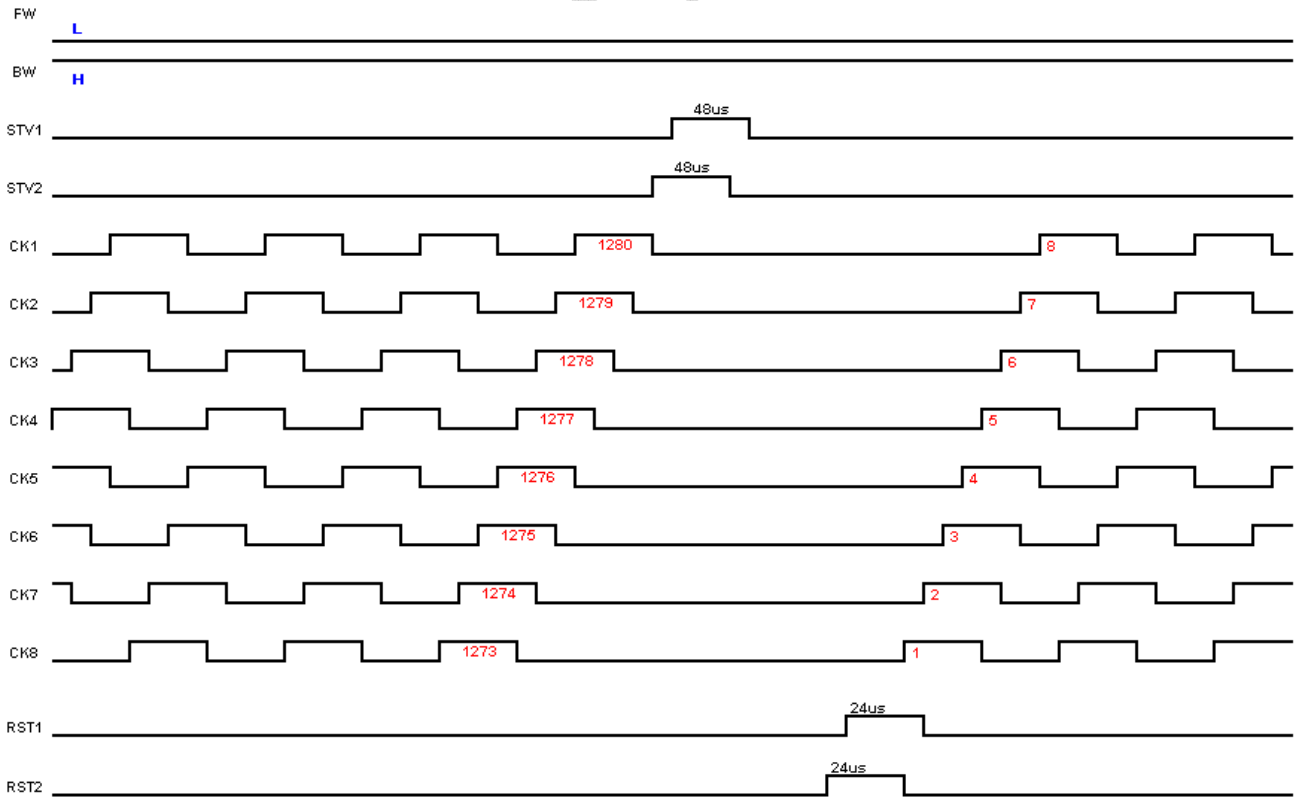
VGL, CK1~CK8, STV1,STV2,RST1,RST2…etc, please follow the timing char below.

3.3.2. GIP Timing Char

< Forward scan >

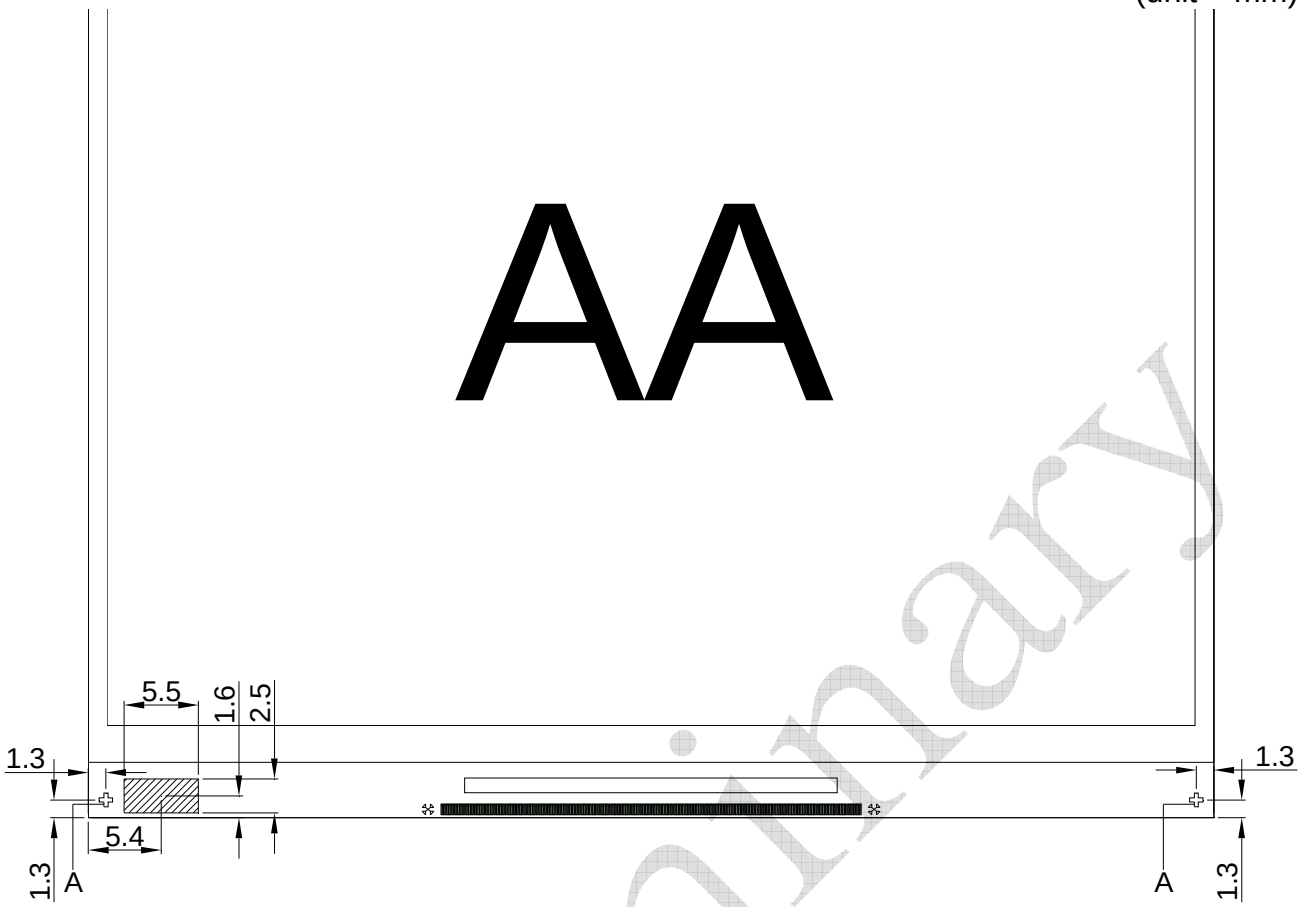


< Backward scan >

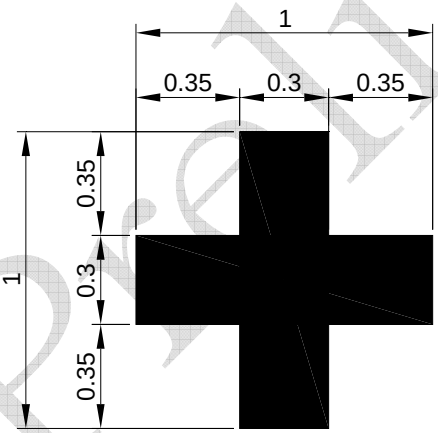


3.4. Panel ID PAD

(unit = mm)



Detail A :



4. ELECTRICAL CHARACTERISTICS

4.1. TFT LCD Power Supply Voltage

(GND=VSSA=VSSD=0V) Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Analog Supply Voltage	*VDD*	2.6	2.8	3.6	V	
I/O Operating Voltage	*VDDI*	1.65	1.8	3.3	V	
TFT Gate High Voltage	*VGH*	14	--	18	V	Note 1
TFT Gate Low Voltage	*VGL*	-12	--	-9	V	
TFT Common Electrode Voltage	*VCOMDC*	-2.5	--	0	V	Note 2
TFT Feed-Through Voltage	*ΔVp*	1.37	--	1.40	V	
Input Signal Voltage	*VIH*	0.7*VDDI	--	VDDI	V	
	VIL	GND	--	0.3*VDDI	V	
Output Signal Voltage	*VOH*	0.8*VDDI	--	VDDI	V	
	VOL	GND	--	0.2*VDDI	V	

Note 1. VGH/VGL must be adjusted by software to optimize display quality.

Note 2. VCOM DC must be adjusted to optimize display quality.

4.2. TFT LCD Consumption Current

(GND=VSSA=0V) Ta = 25℃

MODE	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Total Power Consumption	PC		-	TBD	TBD	mW	Note1

Note1: Typ. specification：Gray-level test Pattern
Max. specification：White test Pattern

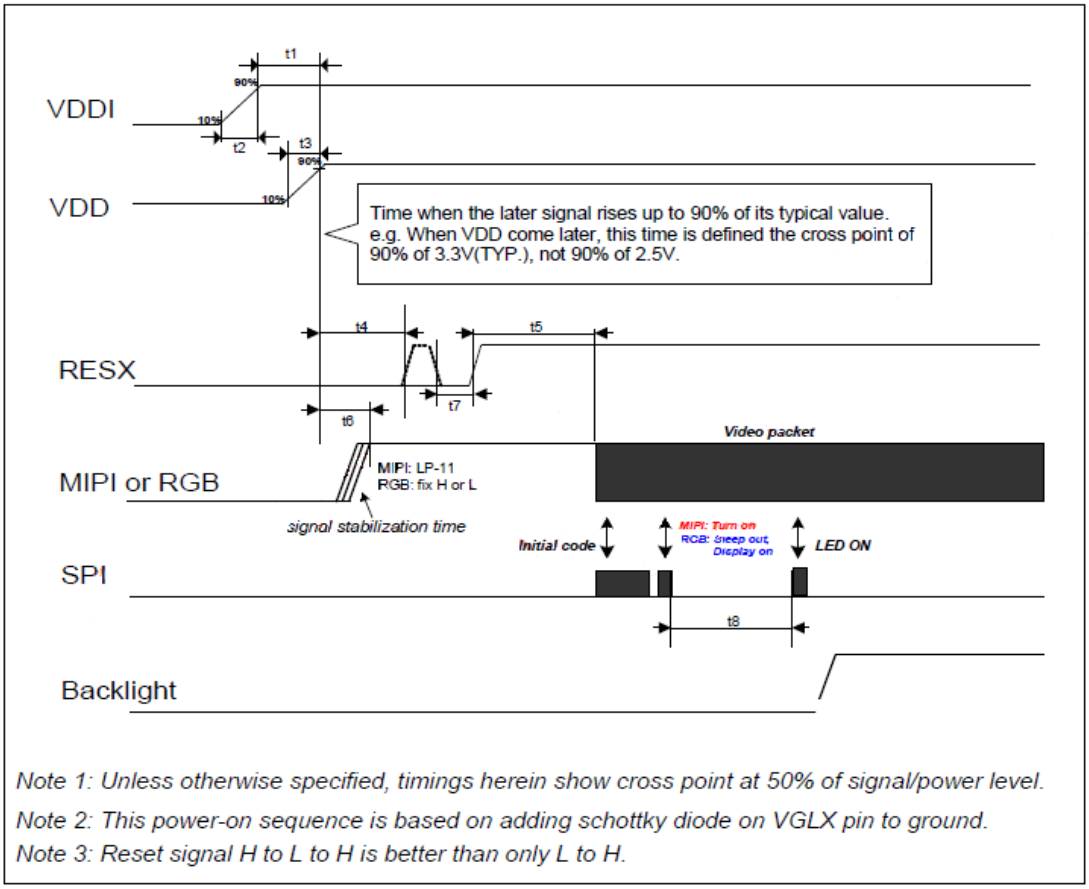
(a)Gray-level Pattern

(b)White Pattern

4.3. Power ON / OFF Sequence

4.3.1. Case 1 - Power On Sequence

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD (VDDA) and VDDIO have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

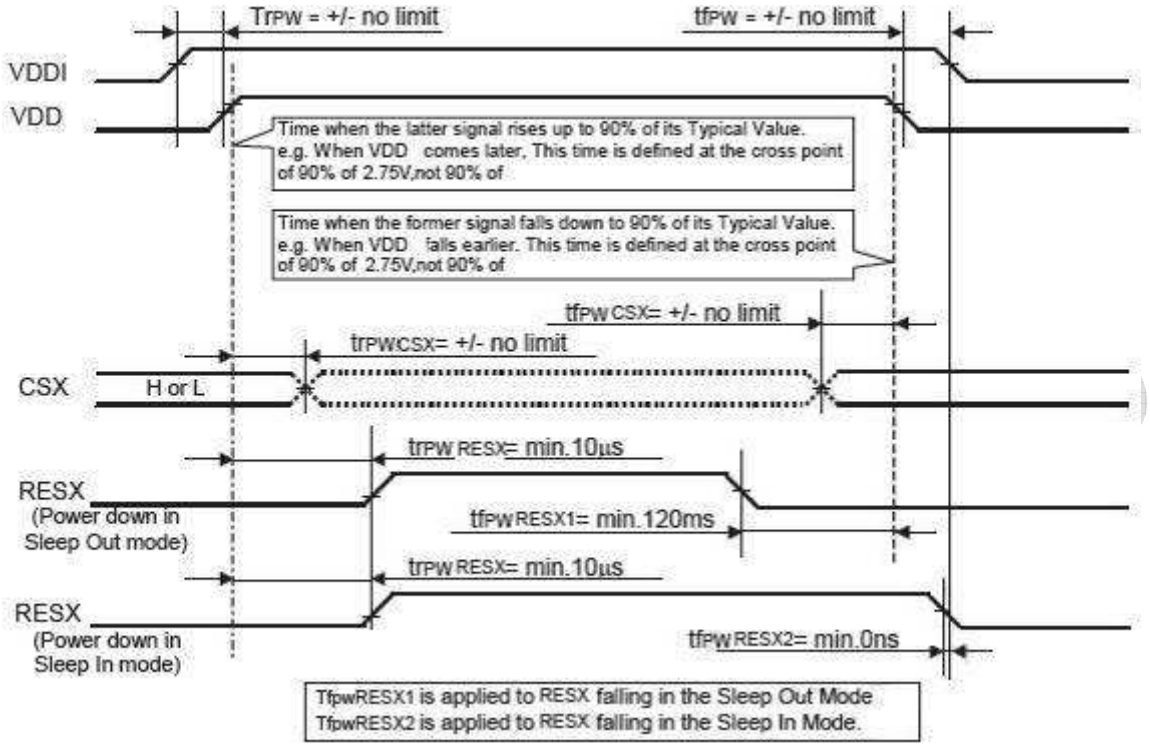
Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground.

Note 3: Reset signal H to L to H is better than only L to H.

Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
t1		No limit		ms	Schettky diode should added on VGLX
t2			150	us	
t3			150	us	
t4	40			ms	
t5	20			ms	
t6	0		<t4	ms	
t7	10			us	
t8	7			VS	Keep data more than 7 frame (VS)

4.3.2. Case 2 – Power Off Sequence

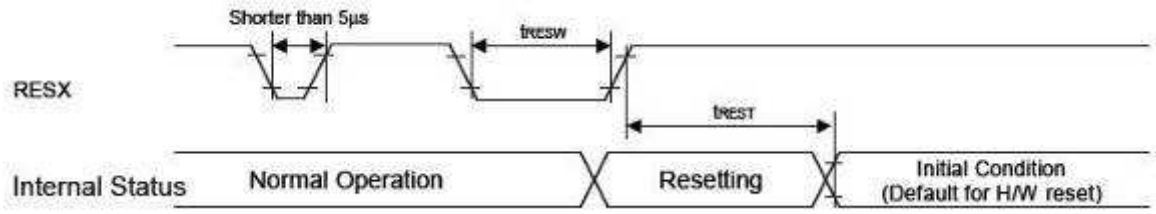
If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10usec after both VDD and VDDIO have been applied.



4.4. Timing Characteristics of Input Signals

4.4.1. MIPI DSI characteristics

4.4.1.1. Reset Timing Characteristics



VSS=0V, VDDIO=1.6V to 3.6V, VCI=2.5V to 5.5V, Ta=-30 to 70℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	us
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

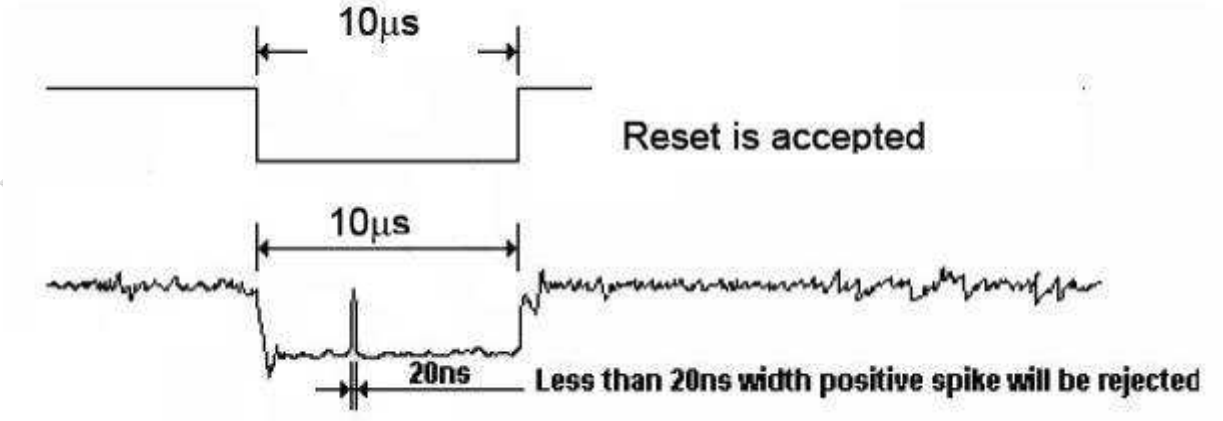
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according t the table below.

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts (It depends on voltage and teperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, ID1/ID2/ID3/ID4 and VCOM Value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

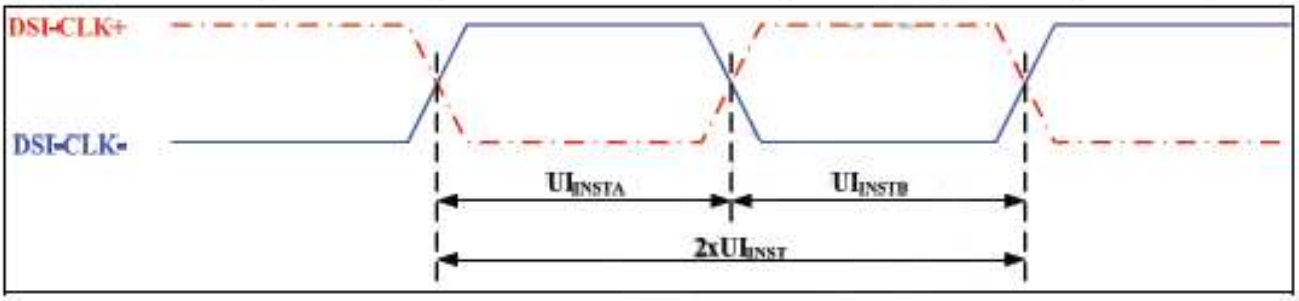
Note 4. Spike Rejection also applies during a valid reset as shown below.

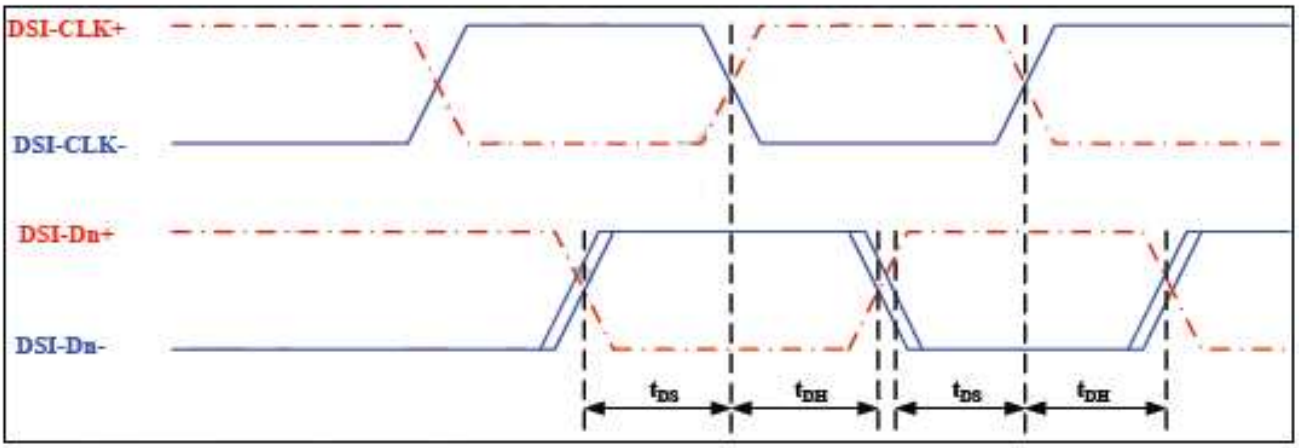


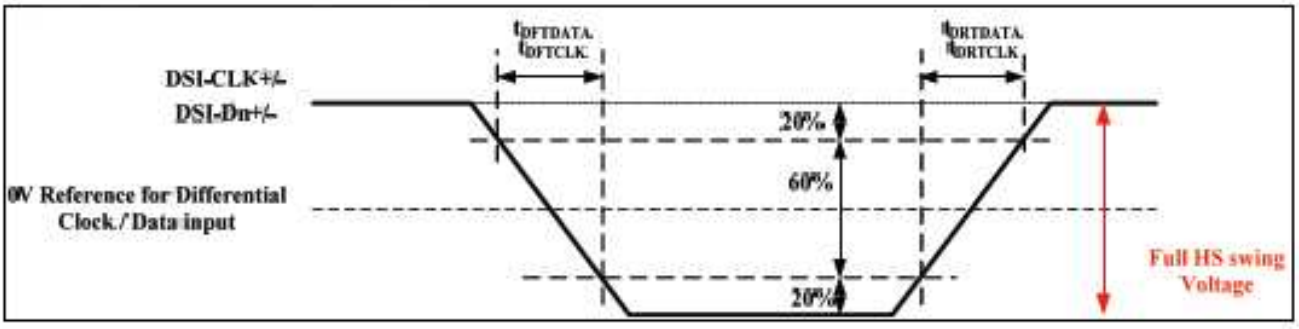
Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Alsp Sleep Out command cannot be sent for 120msec.

4.4.1.2. High Speed Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	2	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps







4.4.1.3. Low Power Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5XT_{LPXD}$	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4XT_{LPXD}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

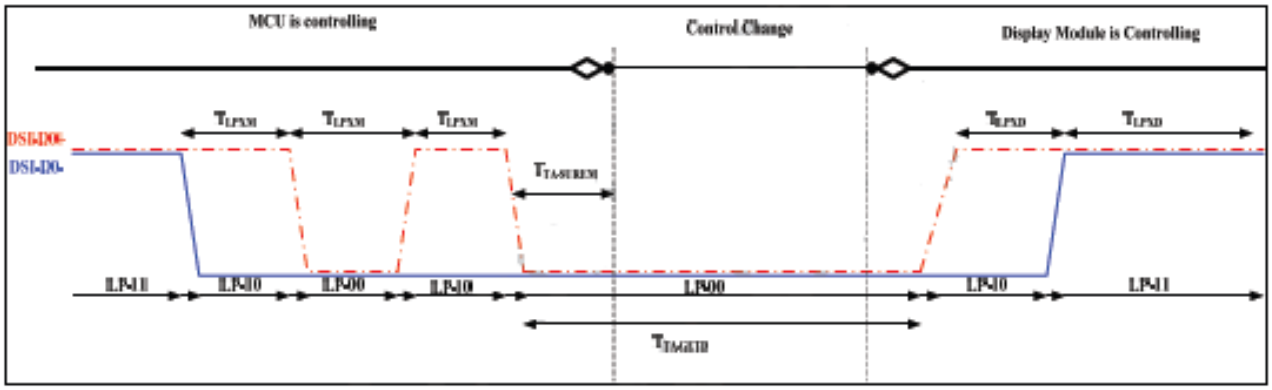
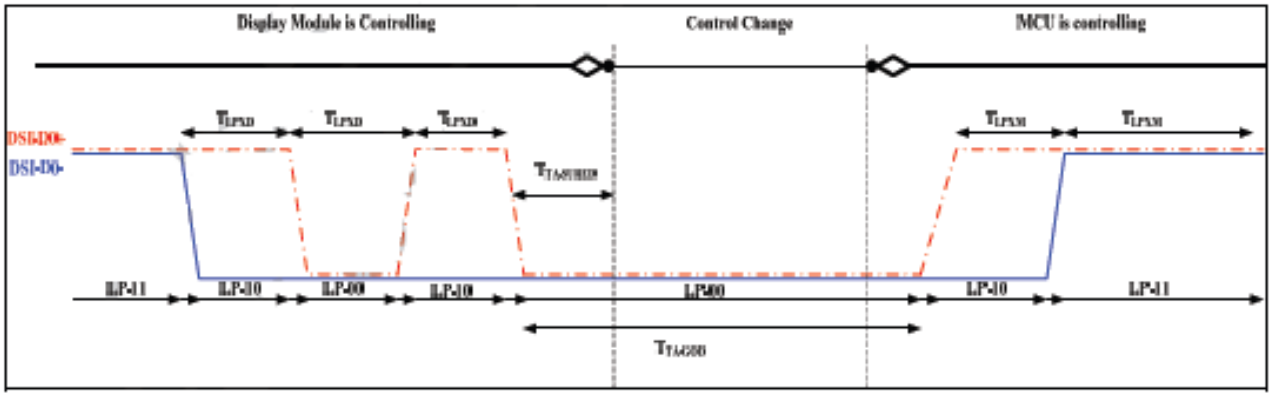
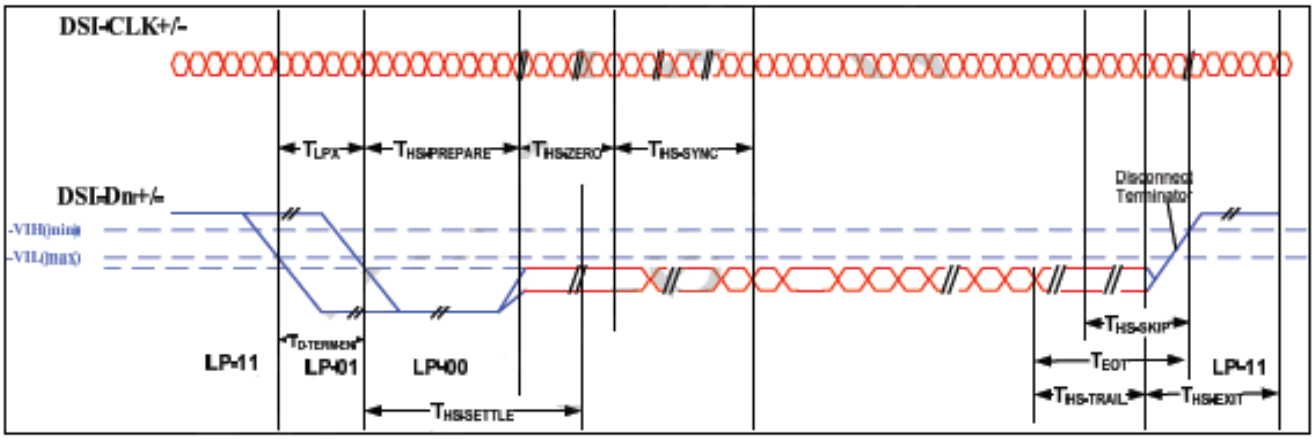


Fig. 7.3.1.2: BTA from the MCU to the Display Module

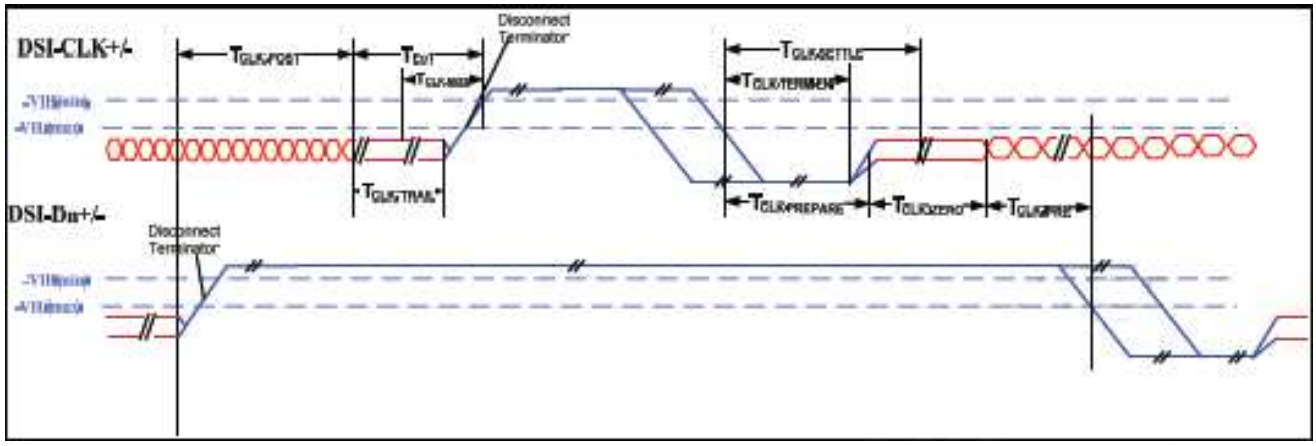


4.4.1.4. DSI Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns



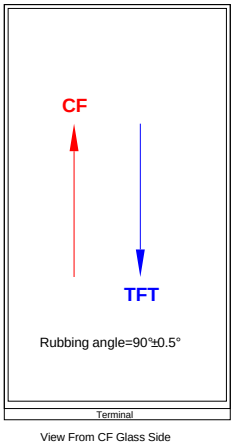
Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns



5. CELL PROCESS RULES

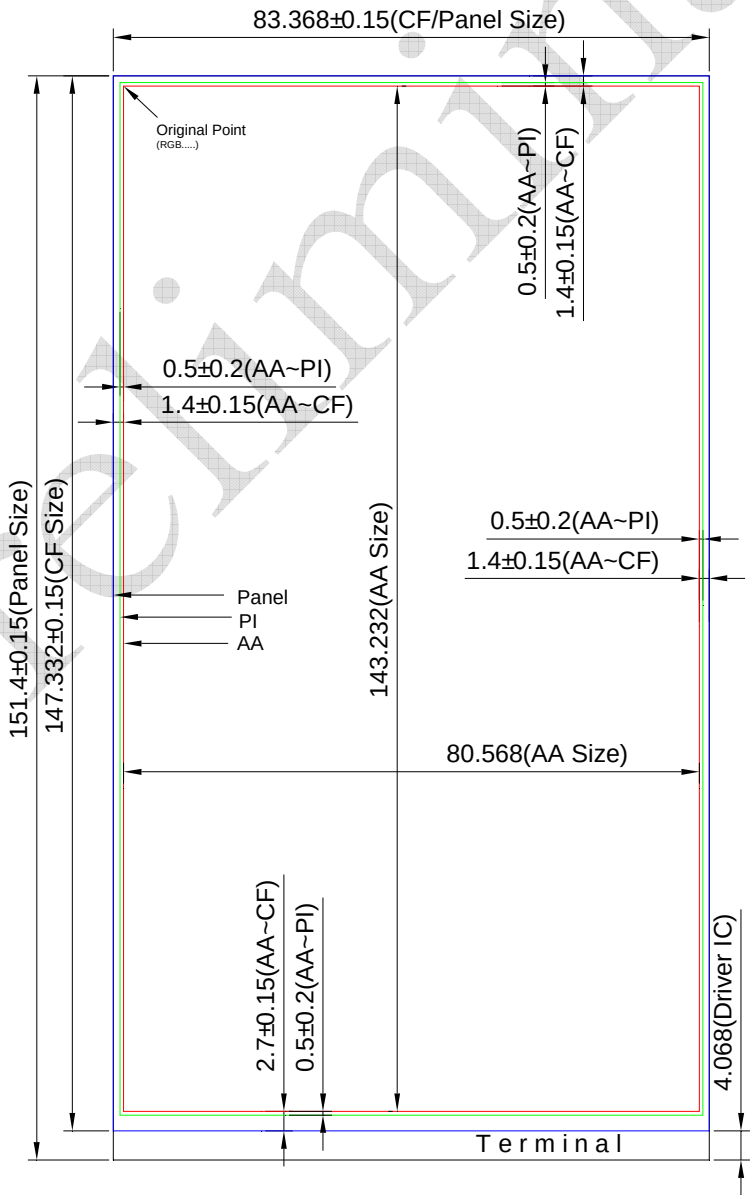
Item	Specification
Cell gap	3.6±0.2um
Assembly precision	±4.0um

5.1. Rubbing Direction



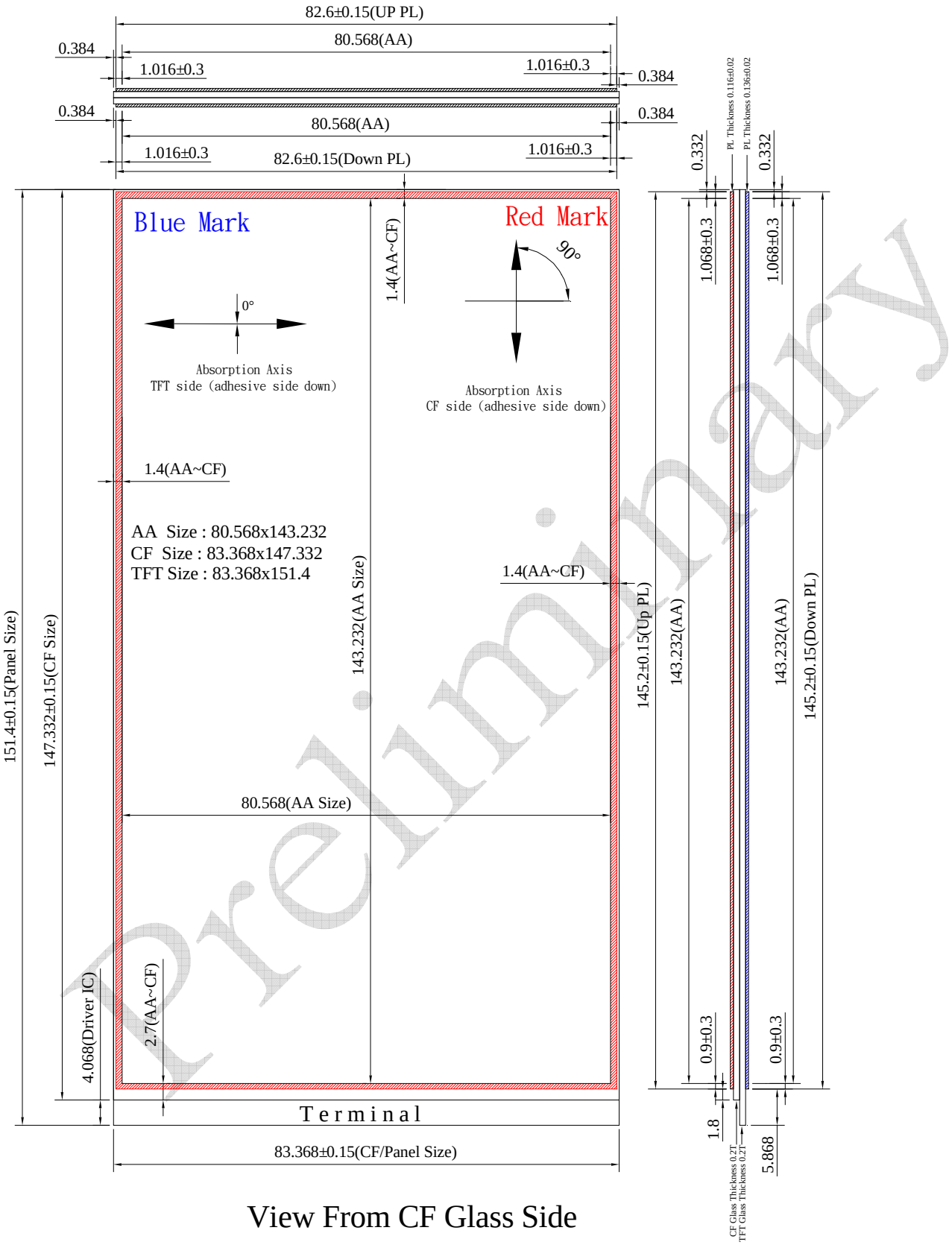
5.2. PI Pattern

(unit = mm)



5.3. Polarizer Information

(unit = mm)

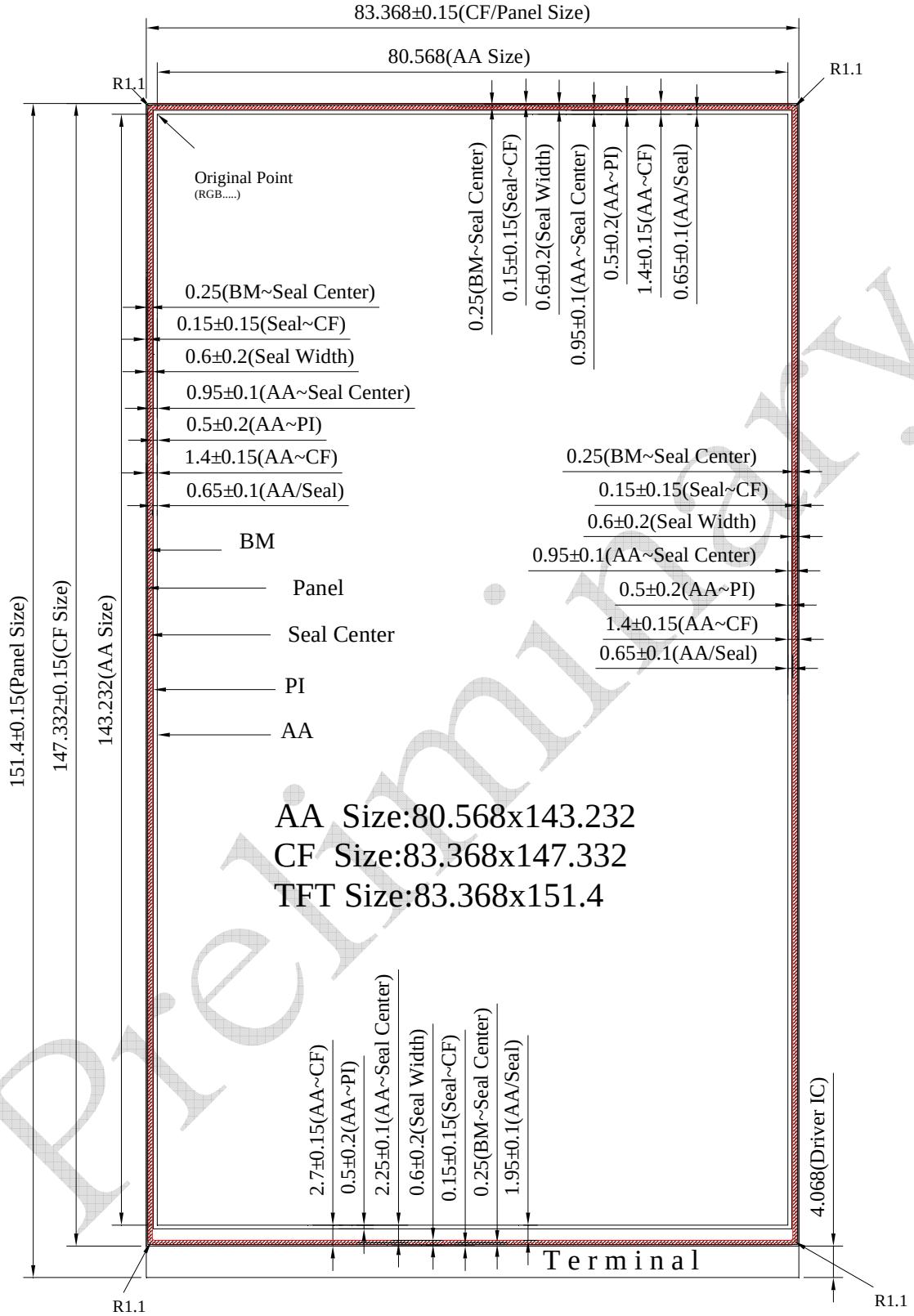


View From CF Glass Side

Up PL Size : 82.6 x 145.2 mm
Down PL Size : 82.6 x 145.2 mm
PL Thickness : 0.116 ± 0.02mm(U)/ 0.136 ± 0.02mm (D) ;
Surface treatment : Up: HC / Down:APCF (Zero Tac Type)

5.4. Seal Pattern

(unit = mm)

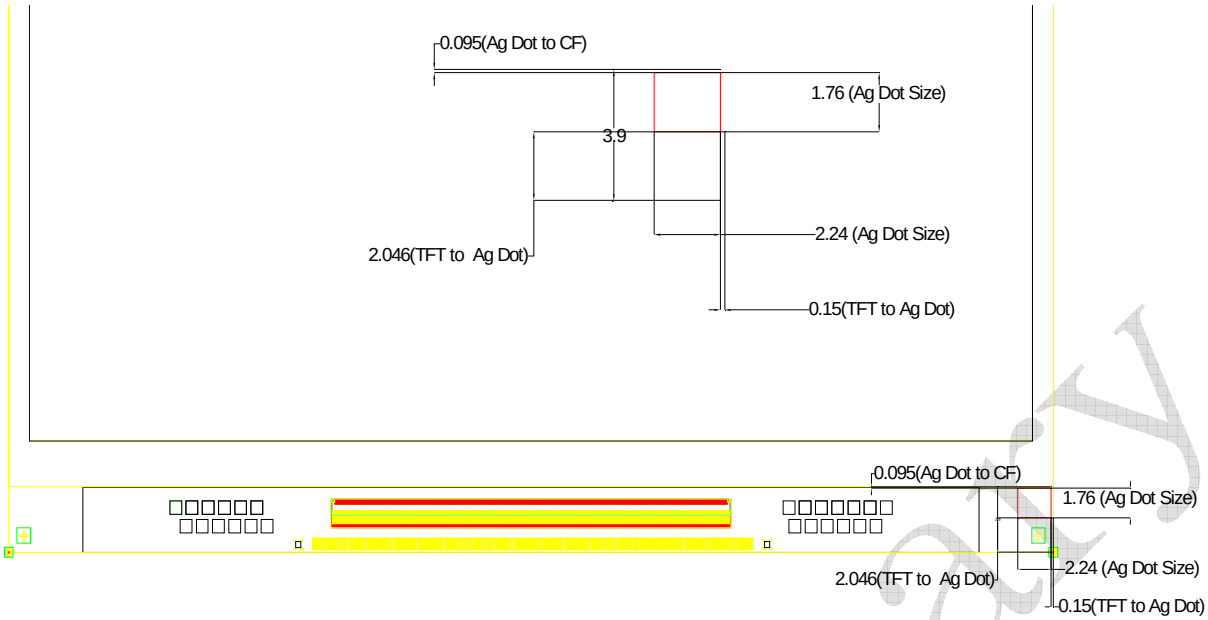


Notes:

1. Seal width (Typ.) = 0.6±0.2mm
2. With ODF process，Seal junction length = 15mm (max.) and width = (0.6+0.4)mm
3. Seal center to CF edge = 0.45±0.2mm

5.5. Sliver Pasre Size & Position

(unit = mm)



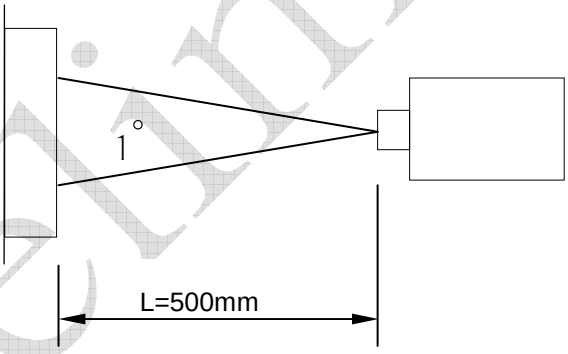
6. OPTICAL SPECIFICATION

(Taransmittance, contrast ratio, response time, viewing angle results are using CPT LC + Zero tac Polarizer + Corresponding Backlight, reference only)

Ambient condition：25 ± 2℃ ，60 ± 10% RH，under 10 Lunx in the darkroom.

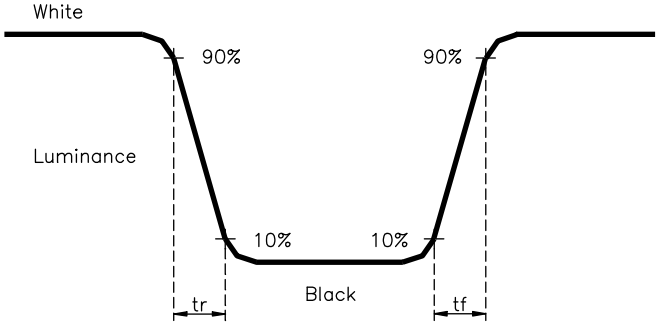
ITEM		SYMBOL		CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Transmittance (Without APCF)		T_{PL}		$\theta = \phi = 0°$	3.8	4		%	Note 2
Transmittance (With APCF)		T_{PL}		$\theta = \phi = 0°$	5	5.3		%	Note 2
Contrast Ratio		CR			---	700	---	--	Note 3
Response Time		Tr+Tf		$\theta = \phi = 0°$	---	30	40	ms	Note 4
Viewing Angle	Vertical	U	θ*2	CR≧10	---	85	---	degree	Note 5
		D			---	85	---	degree	
	Horizontal	L	ϕ*2		---	85	---	degree	
		R			---	85	---	degree	
Color Filter Chromacicity (W/ B-ITO) (CIE 1931)	W	x		$\theta = \phi = 0°$	(0.286)	(0.306)	(0.326)	--	Note 6
		y			(0.314)	(0.334)	(0.354)	--	
	R	x			(0.640)	(0.660)	(0.680)	--	
		y			(0.310)	(0.330)	(0.350)	--	
	G	x			(0.274)	(0.294)	(0.314)	--	
		y			(0.572)	(0.592)	(0.612)	--	
	B	x			(0.117)	(0.137)	(0.157)	--	
		y			(0.088)	(0.108)	(0.128)	--	
	NTSC				---	70	---		

Note 2. Measure device：BM-5A (TOPCON)，viewing cone = 1°，I_L= 20mA。

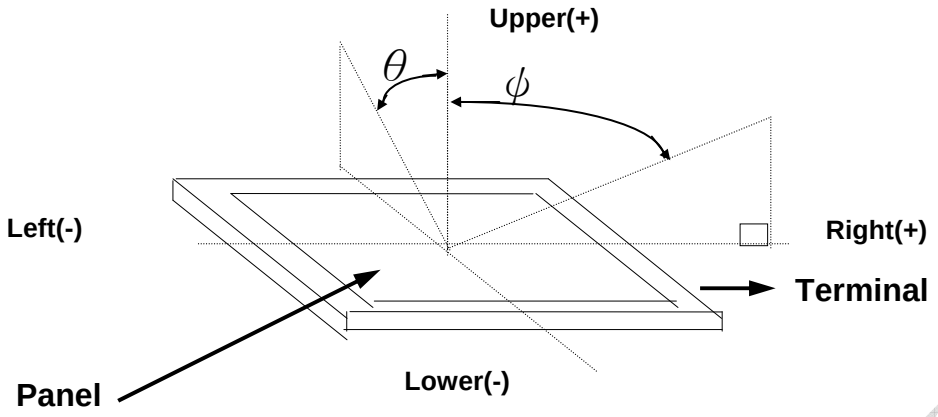


Note 3. Definition of Contrast Ratio：
CR = White Luminance (ON) / Black Luminance (OFF)

Note 4. Definition of response time：The response time is defined as the time interval between the 10% and 90% amplitudes.



Note 5. Definition of view angle(θ，ϕ)：



Note 6. Light source: C light.

7. RELIABILITY TEST ITEM

NO.	TEST ITEM	CONDITIONS
1	HighTemperature Operation	70℃, 240 hrs
2	Low Temperature Operation	-20℃, 240 hrs
3	High Temperature and High Humidity Operation	60℃ , 90% RH, 240 hrs

NOTE

1. All judgement of display are performed after temperature of panel return to room temperature.
2. Display function should be no change under normal operating condition.
3. Under no condensation of dew.
4. CPT only guarantee the above 3 test items, and without guarantee the others.