



Chunghwa Picture Tubes, Ltd. Technology Specification

TFT LCD

CLAN060LB41 2XC (COG)

APPROVED BY	CHECKED BY	PREPARED BY

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REVISION STATUS

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1. OVERVIEW

CPT CLAN060LB41 2XC is a cell product after LC ODF. This is 4:3 aspect ratio panels for the mobile application.

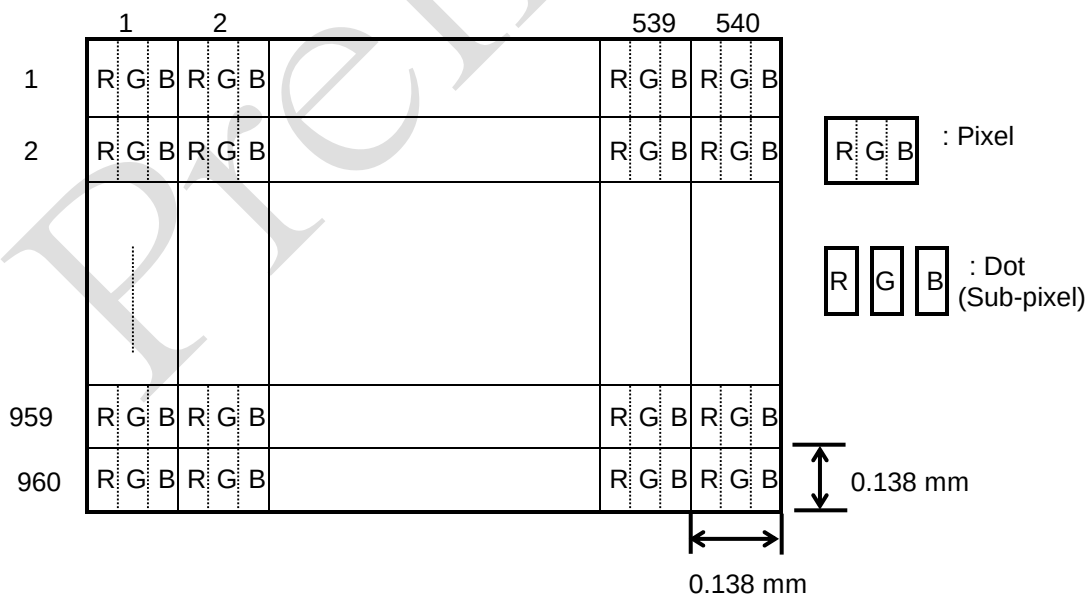
The 4.0" screen produces a high resolution image that is composed of 1,152,000 pixel elements in a stripe arrangement.

General specifications are summarized in the following table:

ITEM	SPECIFICATION
Panel Size	5.98 inch
Display Area (mm)	74.52 (W) x 132.48 (H)
CF glass dimension	77.32 (W) x 136.53 (H) x 0.2 (Thickness)
TFT glass dimension	77.32 (W) x 140.2 (H) x 0.2 (Thickness)
Number of Pixels	540RGB (W) x 960 (H)
Pixel Pitch (mm)	0.138 (W) x 0.138 (H)
Color Pixel Arrangement	RGB Stripe
NTSC	70 %
Display Mode	Normally Black
Driving Method	TFT active matrix
Viewing Direction	Up/down/left/right 80/80/80/80
Suggesting IC	OTM9605

Note: The FPC circuit design is possibly different according to the individual suggesting IC internal circuit definition and application. Please refer to the IC datasheet respectively.

LCD Cell Drawing (Note 1)



The LCD Products listed on this document are not suitable for use of aerospace equipment, submarine cables, nuclear reactor control system and life support systems. If customers intend to use these LCD products for above application or not listed in "Standard" as follows, please contact our sales people in advance.

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remark
Enviromental Phase					
Operating Ambient Temperature	T_{OP}	-20	+70	°C	
Operating Ambient Humidity	H_{OP}	10	90	% (RH)	
Storage Temperature	T_{STG}	-30	+80	°C	
Storage Humidity	H_{STG}	10	90	% (RH)	
Electrical Phase					
TFT Gate High Voltage	V_{GH}	14	18	V	
TFT Gate Low Voltage	V_{GL}	-12	-9	V	
TFT Common Electrode Voltage	$V_{COM DC}$	-3	0	V	NOTE3
TFT Feed-Through Voltage	ΔV_p	TBD	TBD	V	

Note 1. The absolute maximum ratings are the values that must not be exceeded at any time for this product. It is not allowed for any of these ratings to be exceeded. Should a product be used with any of the absolute maximum ratings exceeded, the characteristics of the product may not be recovered, or in an extreme case, the product may be permanently destroyed.

Therefore, when designing a system incorporating the product, make sure that adequate attentions be paid to the variations in the supply voltages, the characteristics of parts that are connected, surges in the input and output lines, and the ambient temperatures.

Note 2. This specification applies after the driver IC mounting and the FPC mounting. (This specification isn't applicable at time of driver IC un-mounting and FPC un-mounting.)

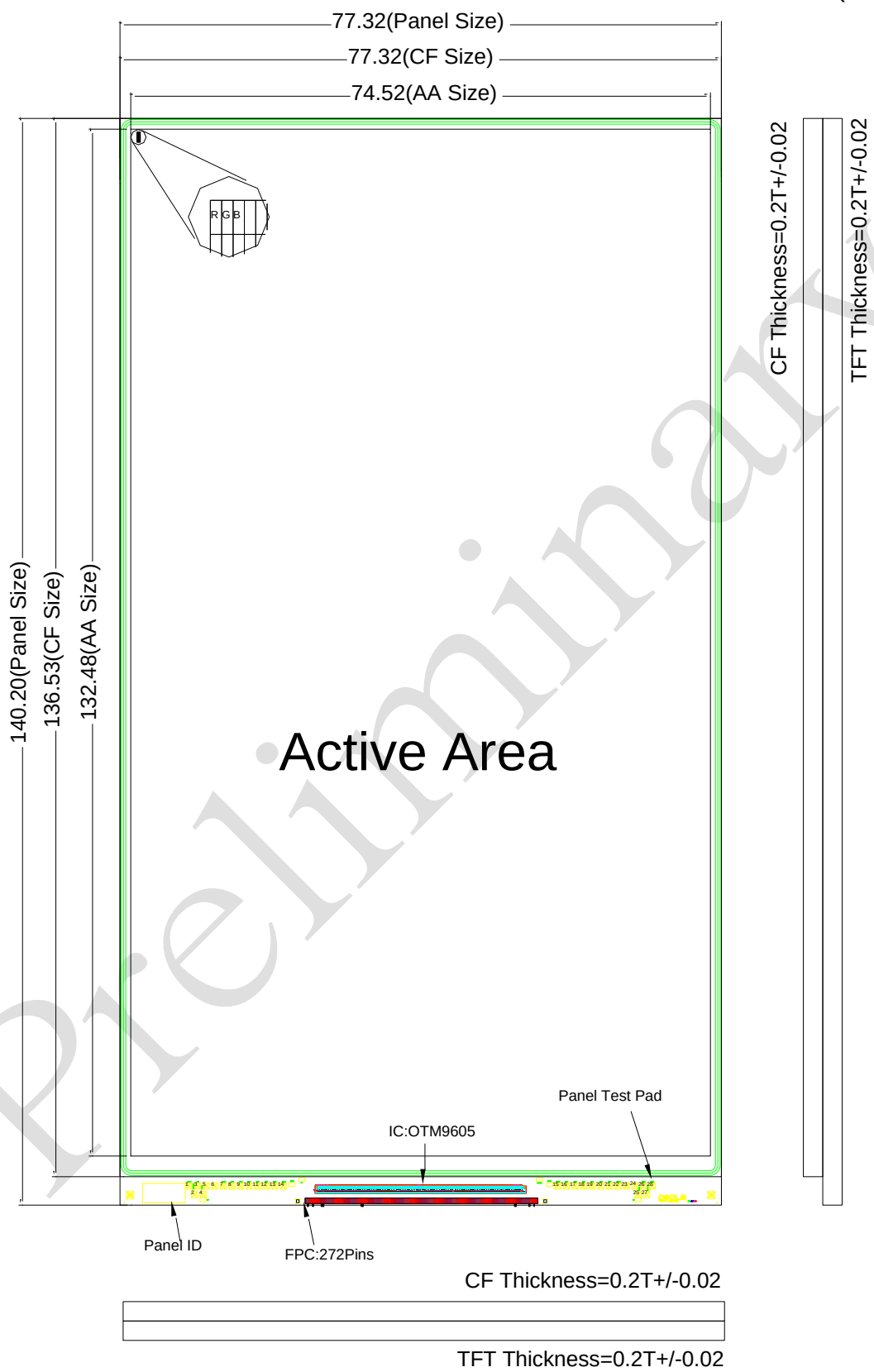
LCD should keep the condition that dew doesn't storage in case of driver IC un-mounting and FPC un-mounting. Dew may break the LCD. Especially part is very weak for dew.

Note 3. Vcom must be adjusted to optimize display quality, as Crosstalk and Contrast Ratio etc.,

3. MECHANICAL SPECIFICATIONS

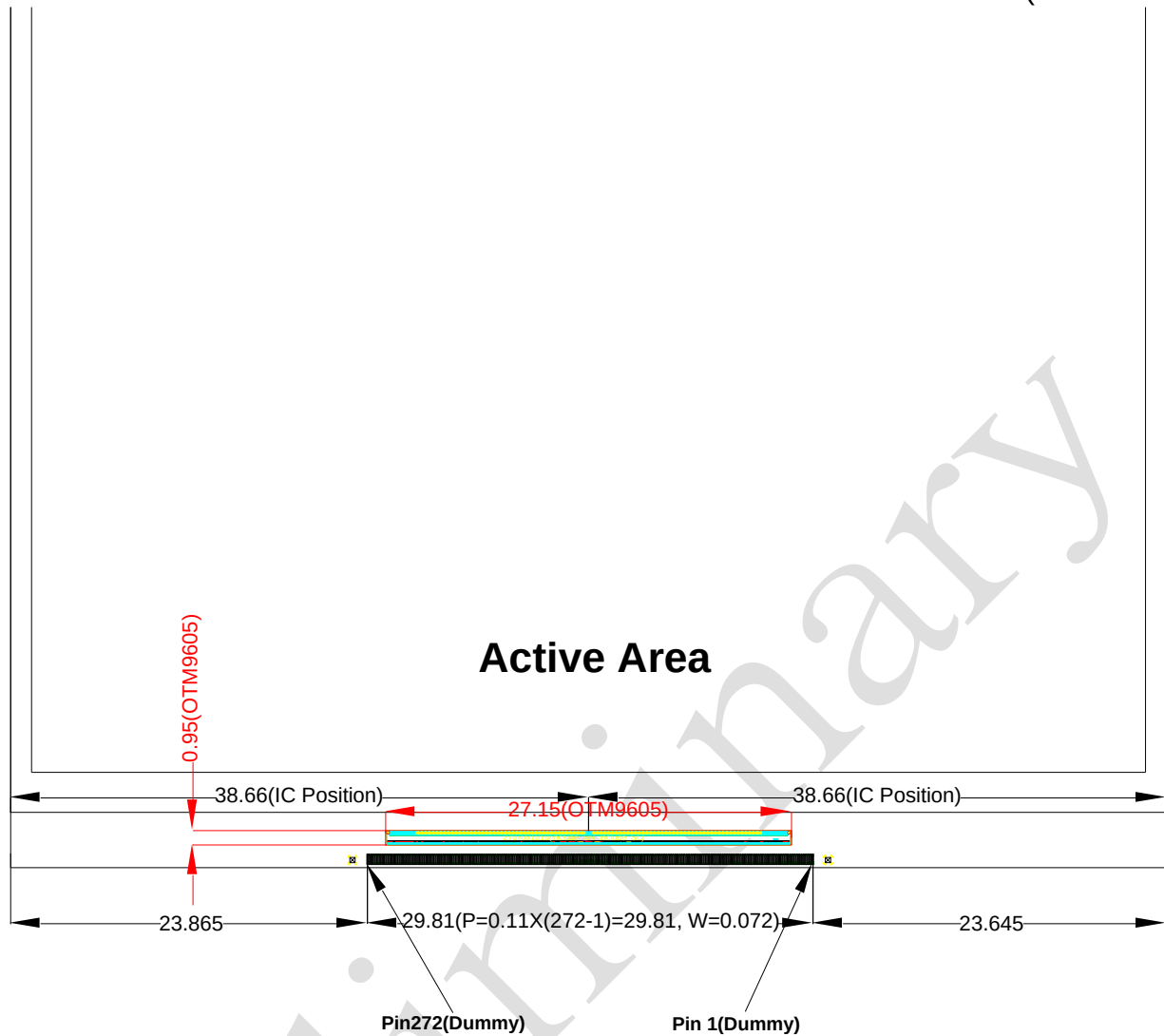
3.1 Outline Dimension

(unit: mm)



3.2 IC & FPC Pad

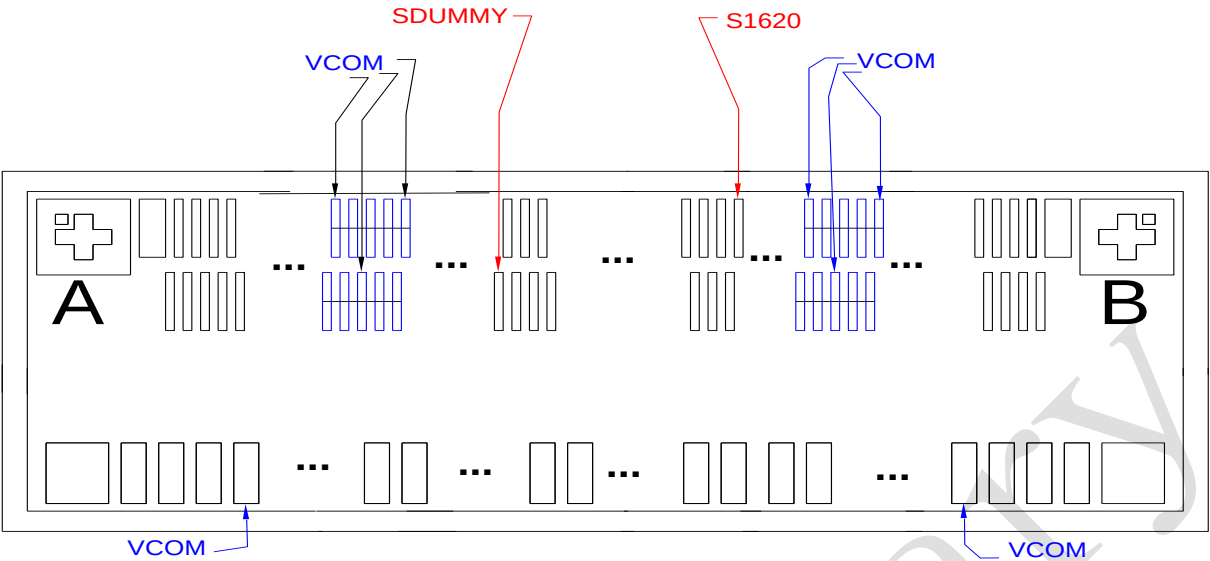
(unit = mm)



Note1. Color Filter is in the upper side , TFT is in the bottom side
Note2. This IC size is For OTM9605

3.2.1 COG Design (DOM)

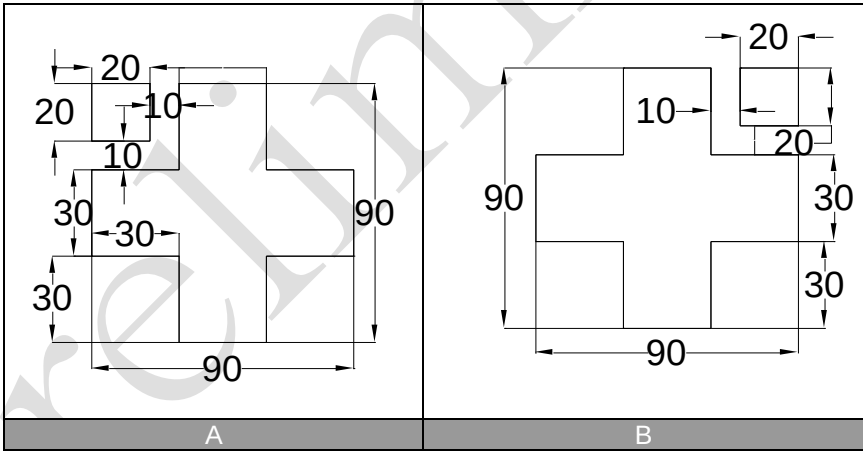
- IC OTM9605 :



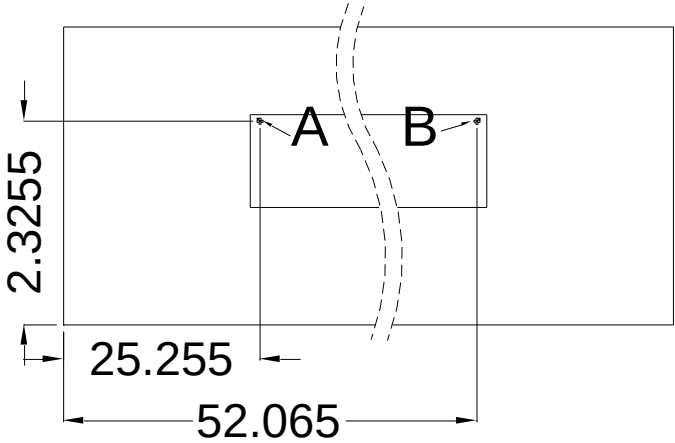
1. Chip Size

IC	Chip Size
OTM9605	27.15mm x 0.95mm

2. Alignment Mark Size & Position :

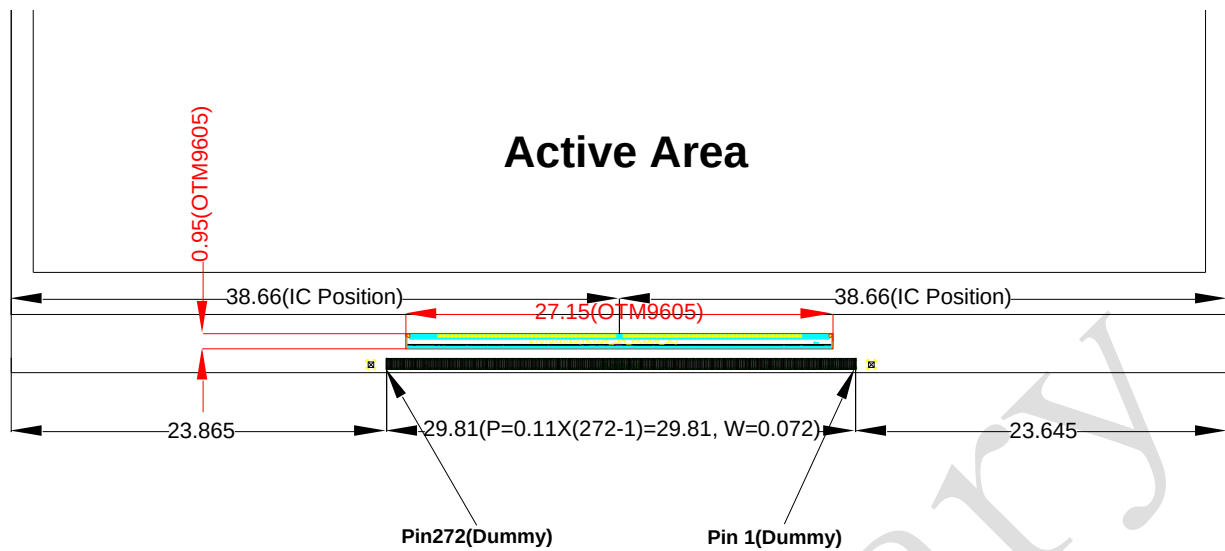


Unit : um

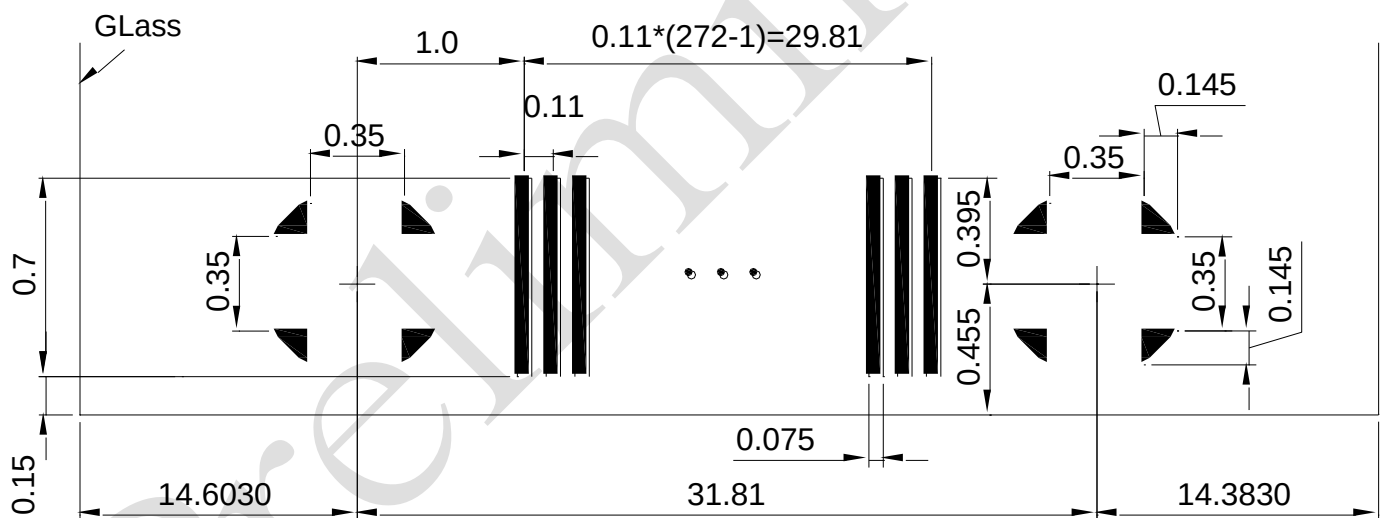


3.2.2 FPC Pad

(unit = mm)



Detail FPC :



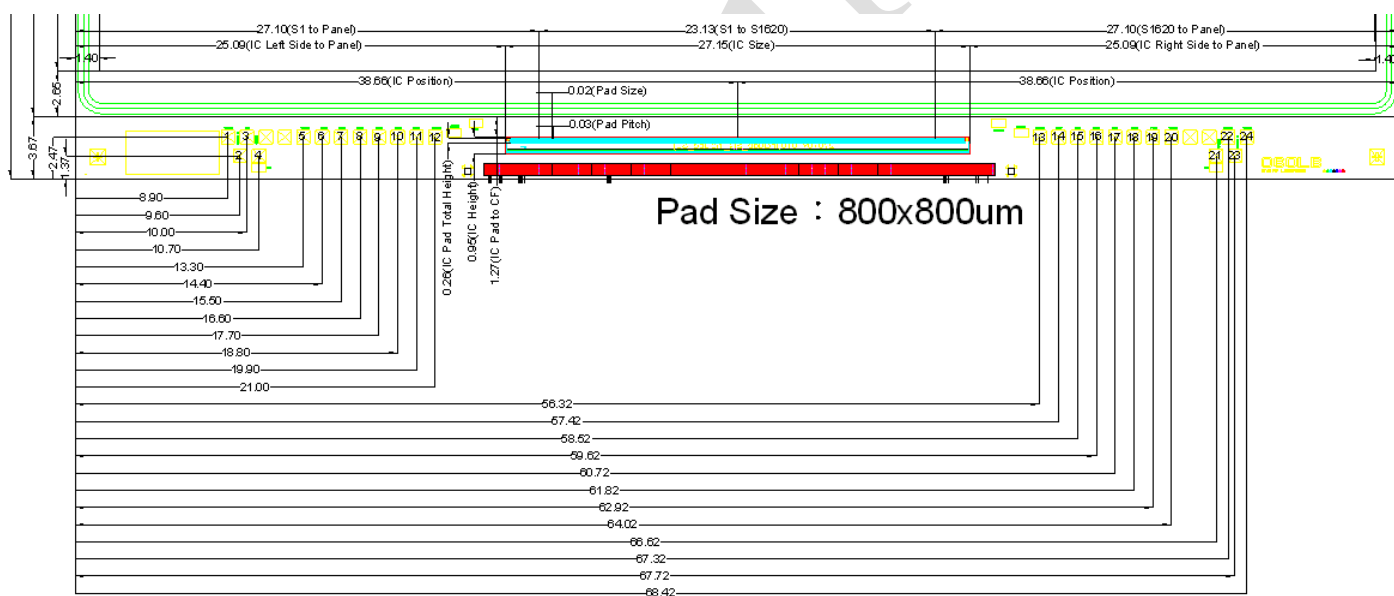
3.2.3 FPC Pin Assignment (OTM9605A)

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	DUMMY	71	CSX	141	D0P	211	C21N
2	DUMMY	72	RESX	142	D0N	212	C21N
3	Ground	73	VSSI	143	D0N	213	C21N
4	Ground	74	VDDIO	144	LVDSVSS	214	C22P
5	VCOM	75	NBWSSEL	145	D2P	215	C22P
6	DUMMY	76	D23	146	D2P	216	C22P
7	DUMMY	77	D22	147	D2N	217	C22N
8	DUMMY	78	D21	148	D2N	218	C22N
9	DUMMY	79	D20	149	LVDSVSS	219	C22N
10	VCOM	80	D19	150	VDD	220	C23N
11	VCOM	81	D18	151	TE_R	221	C23N
12	3D_CLK_0	82	D17	152	VSS	222	C23N
13	3D_CLK_0	83	D16	153	VREFCP	223	C23P
14	3D_CLK_1	84	D15	154	VRGH	224	C23P
15	3D_CLK_1	85	D14	155	EXTP	225	C23P
16	3D_CLK_2	86	D13	156	CSP	226	NVDDA
17	3D_CLK_2	87	D12	157	EXTN	227	NVDDA
18	3D_CLK_3	88	D11	158	CSN	228	NVDDA
19	3D_CLK_3	89	D10	159	VSSA	229	VDD
20	BVP3D	90	D9	160	VSSA	230	VDD
21	BNV3D	91	D8	161	VSSA	231	VDD
22	MTP_PWR	92	D7	162	C11P	232	VSS
23	VGL	93	D6	163	C11P	233	VSS
24	VGL_REG	94	D5	164	C11P	234	VSS
25	VRGH	95	D4	165	C11N	235	C41P
26	VCL	96	D3	166	C11N	236	C41P
27	VCL	97	D2	167	C11N	237	C41N
28	VCL	98	D1	168	C12P	238	C41N
29	VREF	99	D0	169	C12P	239	C51N
30	VSSA	100	DE	170	C12P	240	C51N
31	VSSA	101	PCLK	171	C12N	241	C51P
32	VDD	102	HS	172	C12N	242	C51P
33	VDD	103	VS	173	C12N	243	VGH
34	VDD	104	LEDPWM	174	C13N	244	VGH
35	VSS	105	LEDON	175	C13N	245	VGH
36	VDD	106	ERR	176	C13N	246	VGH
37	DIOPWR	107	VDDIO	177	C13P	247	VRGH
38	VGSN	108	VSS	178	C13P	248	VRGH
39	VGSP	109	VCC	179	C13P	249	VGL_REG
40	VGMN	110	VCC	180	VDDA	250	VGL_REG
41	VGMP	111	VCC	181	VDDA	251	VGL
42	VSS	112	VDDA	182	VDDA	252	VGL
43	VSS	113	VDDA	183	VDD	253	VGL
44	VDD_1.8V	114	NVDDA	184	VDD	254	VGL
45	VDD_1.8V	115	NVDDA	185	VDD	255	VSSA
46	VSSA	116	VSS	186	VDD	256	VSSA
47	VSSA	117	VSS	187	VDD	257	VDD
48	LANSEL	118	VDD_1.8V	188	VSS	258	VDD
49	DSWAP0	119	VDD_1.8V	189	VSS	259	VDD_1.8V
50	DSWAP1	120	LVDSVDD	190	VSS	260	VDD_1.8V
51	PSWAP	121	VDDAM	191	VSS	261	VSS
52	DSTB_SEL	122	VDDP	192	VSS	262	VSS
53	RGBBP	123	LVDSVSS	193	C31P	263	VCOM
54	I2C_SA0	124	LVDSVSS	194	C31P	264	VCOM
55	IM3	125	D22P	195	C31P	265	DUMMY
56	IM2	126	D22P	196	C31N	266	DUMMY
57	IM1	127	D22N	197	C31N	267	DUMMY
58	IM0	128	D22N	198	C31N	268	DUMMY
59	GPO3	129	LVDSVSS	199	C32P	269	VGL
60	GPO2	130	D1P	200	C32P	270	VCOM
61	GPO1	131	D1P	201	C32P	271	DUMMY
62	GPO0	132	D1N	202	C32N	272	DUMMY
63	EXB1T	133	D1N	203	C32N		
64	TE_L	134	LVDSVSS	204	C32N		
65	VSEL	135	CLKP	205	VCL		
66	SDO	136	CLKP	206	VCL		
67	SDI	137	CLKN	207	VCL		
68	DCX	138	CLKN	208	C21P		
69	WRX	139	LVDSVSS	209	C21P		
70	RDX	140	D0P	210	C21P		

3.3 Panel Check Pad in Panel

(unit = mm)

Panel Check Pad				
Pad Size		800 μm $\times$ 800 μm		
Pad Pitch		1100 μm		
Pad Name	01	VCOM	13	RSTO
	02	D_R	14	CK7
	03	SW	15	CK5
	04	STVE	16	CK3
	05	VGLE	17	CK1
	06	FWE	18	BWO
	07	BWE	19	FWO
	08	CK2	20	VGLO
	09	CK4	21	STVO
	10	CK6	22	D_B
	11	CK8	23	D_G
	12	RSTE	24	VCOM



3.3.1 CELL Test Light Waveform

Frame	D_GB	D_RG	D_BR	SW	Vcom
White (W)	L	L	L	H	DC/GND
Black (BK)	H	H	H	H	DC/GND
Gray (GY)	Gray	Gray	Gray	H	DC/GND
Zebra Stripe (Z)	H	H	H	H	DC/GND

Display Mode: TN, Normally White

Every Frame stay > 2sec.

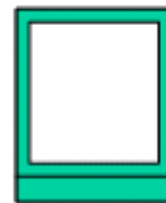
Ex. LC=5V, Vcom=0V

Data H=+/-5V, Data L=0V, Data Gray=+/-2.5V

SW_H=10V above (on duty), SW_L=-6V(not on duty)

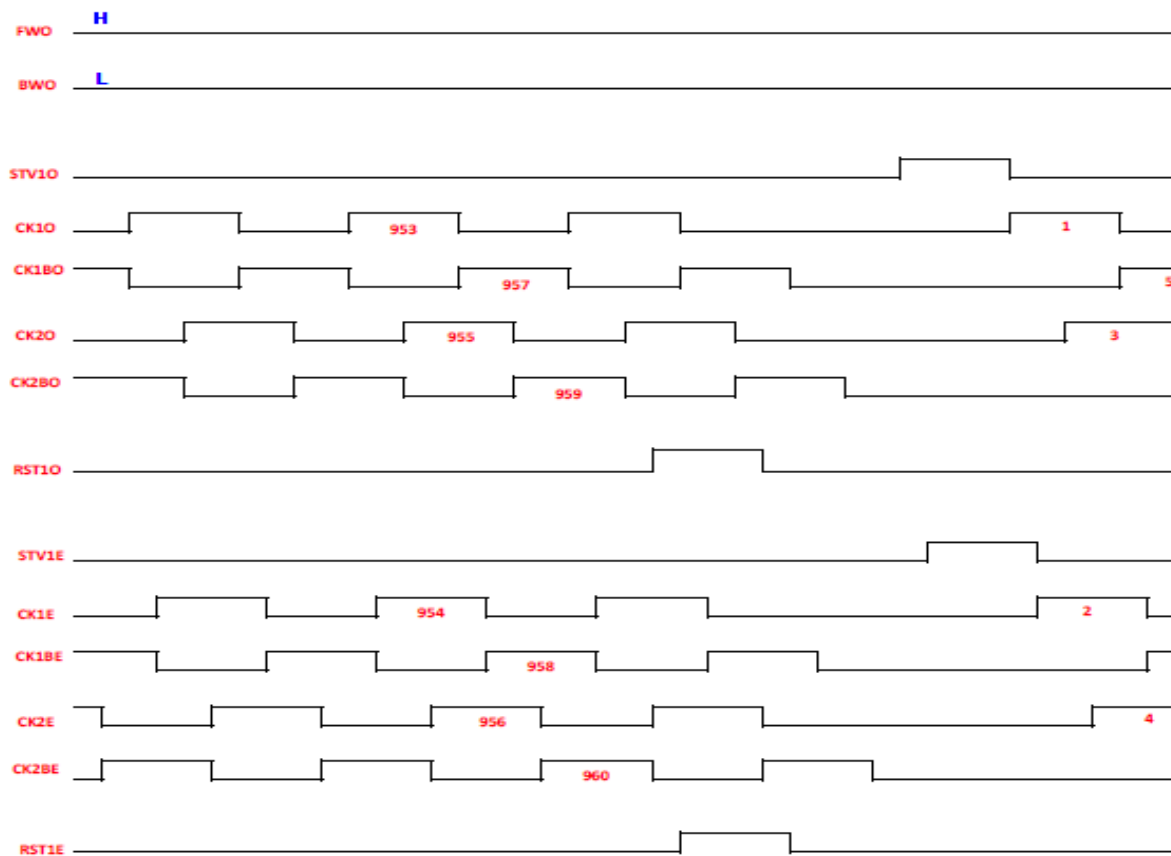
Just suggestion!

VGL, CK1~CK8, STV1,STV2,RST1,RST2...etc, please follow the timing char below.

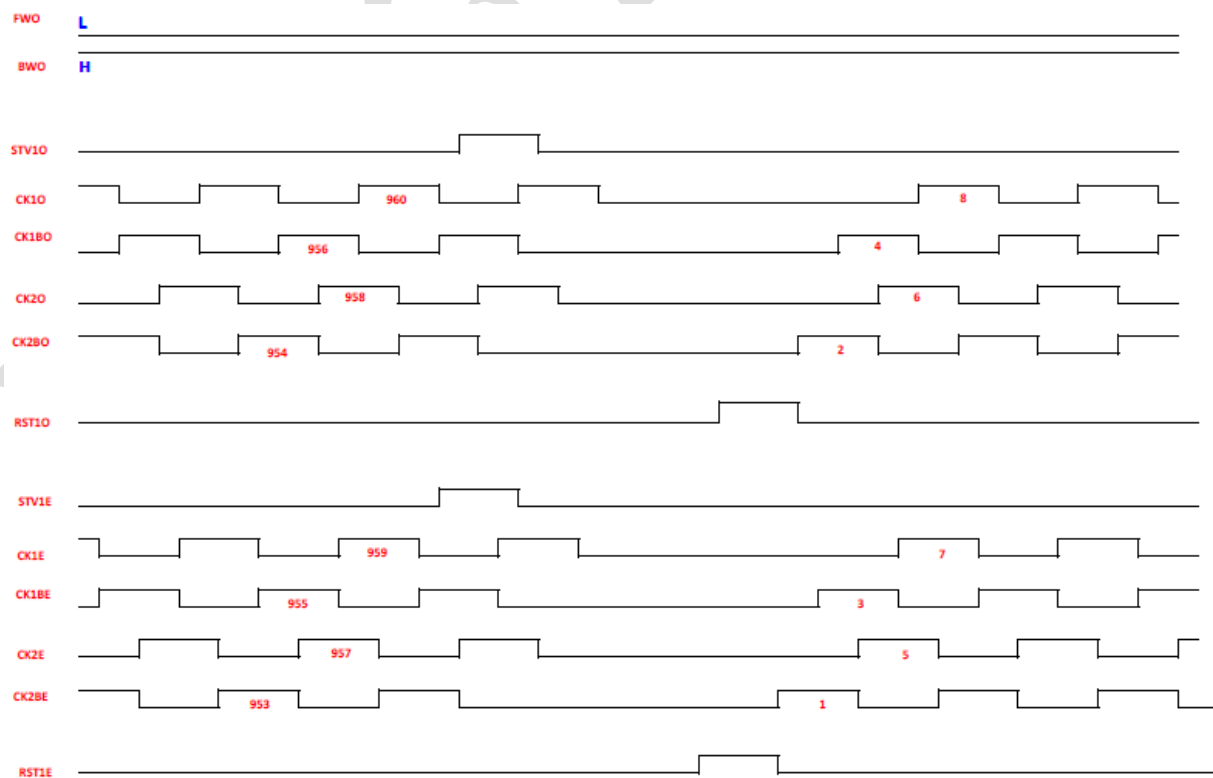


3.3.2 GIP Timing Char

< Forward scan >



< Backward scan >



4. INPUT SIGNAL TIMING

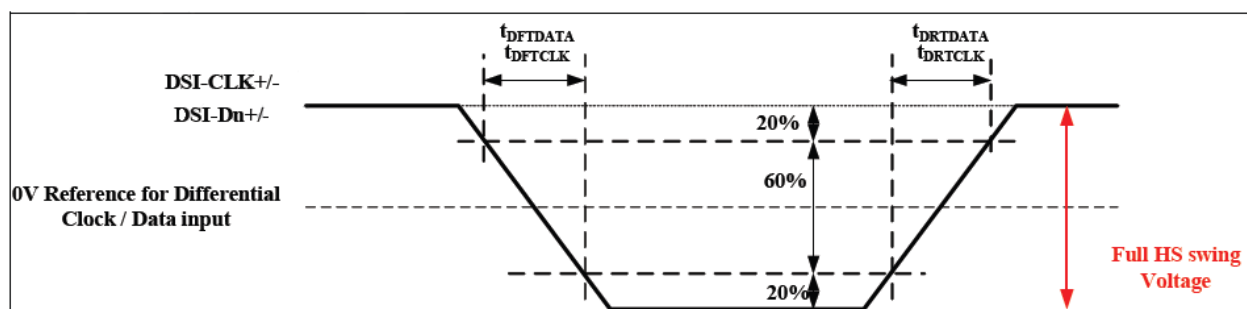
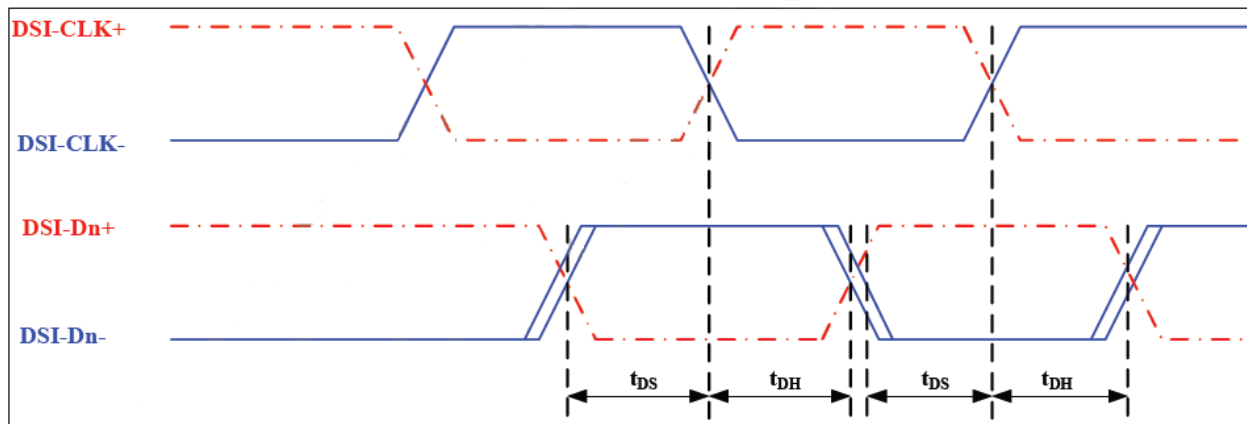
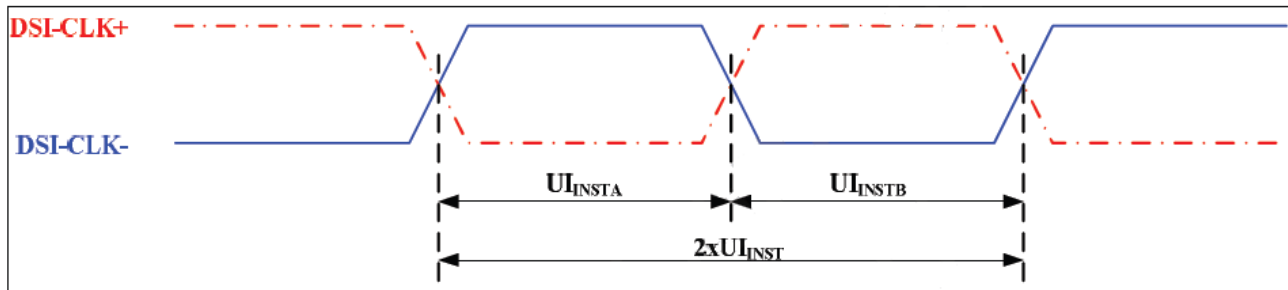
4.1 MIPI Timing DC Characteristics

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	VDDAM	-	2.3	2.8	4.8	V
	VDDP	For LPDT	1.1	1.2	1.3	V
	LVDSVDD	-	1.5	1.55	1.6	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	VGND SH	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	VDDAM	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VILCD,MIN	-	450	-	VDDAM	mV
Logic 0 contention threshold	VIHCD,MAX	-	0	-	200	mV
Output impedance of LPDT	ZOLP	-	80	100	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedance	ZID	-	80	100	125	ohm

4.2 MIPI Timing AC Characteristics

4.2.1. High Speed Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed mode						
DSI-CLK+/-	2xUI _{INST}	Double UI instantaneous	4	-	25	ns
DSI-CLK+/-	UI _{INSTA} , UI _{INSTB}	UI instantaneous Halfs	2	-	12.5	ns
DSI-Dn+/-	t _{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t _{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t _{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	t _{DRTDATA}	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t _{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	t _{DFTDATA}	Differential fall time for data	150	-	0.3UI	ps



4.2.2. Low Power Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T _{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	-	ns
DSI-D0+/-	T _{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	58	-	-	ns
DSI-D0+/-	T _{TA-SURED}	Time-out before the MPU start driving	T _{LPXD}	-	2XT _{LPXD}	ns
DSI-D0+/-	T _{TA-GETD}	Time to drive LP-00 by display module	5XT _{LPXD}	-	-	ns
DSI-D0+/-	T _{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	4XT _{LPXD}	-	-	ns
DSI-D0+/-	Ratio T _{LPX}	Ratio of T _{LPXM} / T _{LPXD} between MCU and display module	2/3	-	3/2	

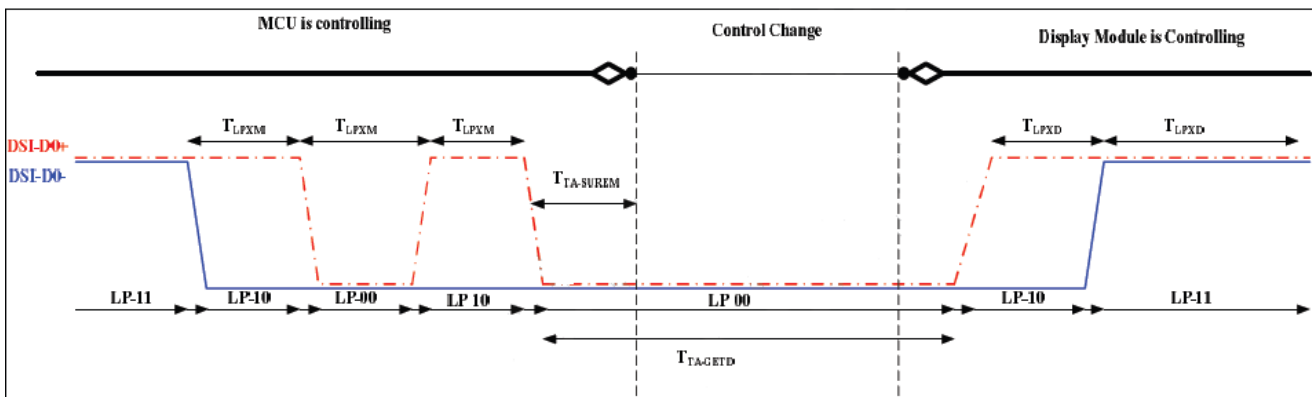
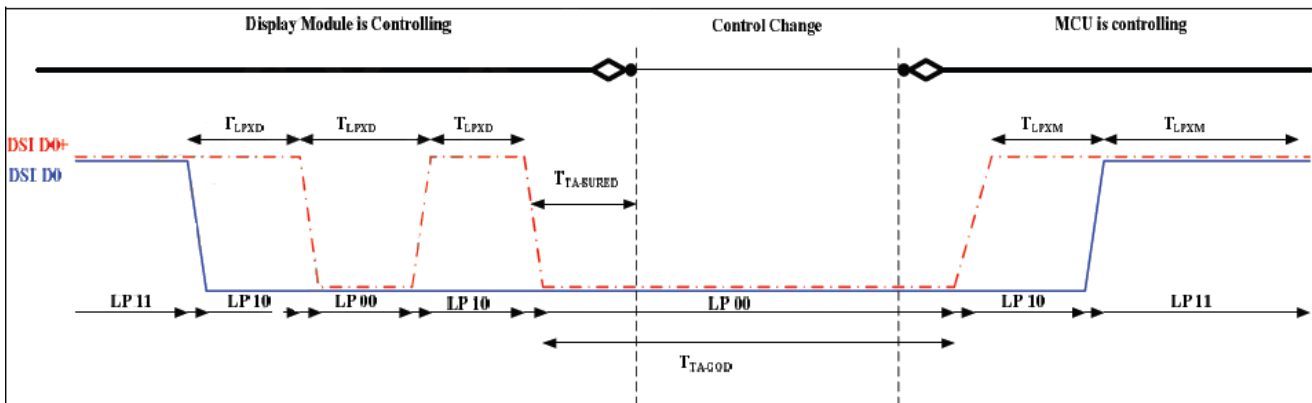


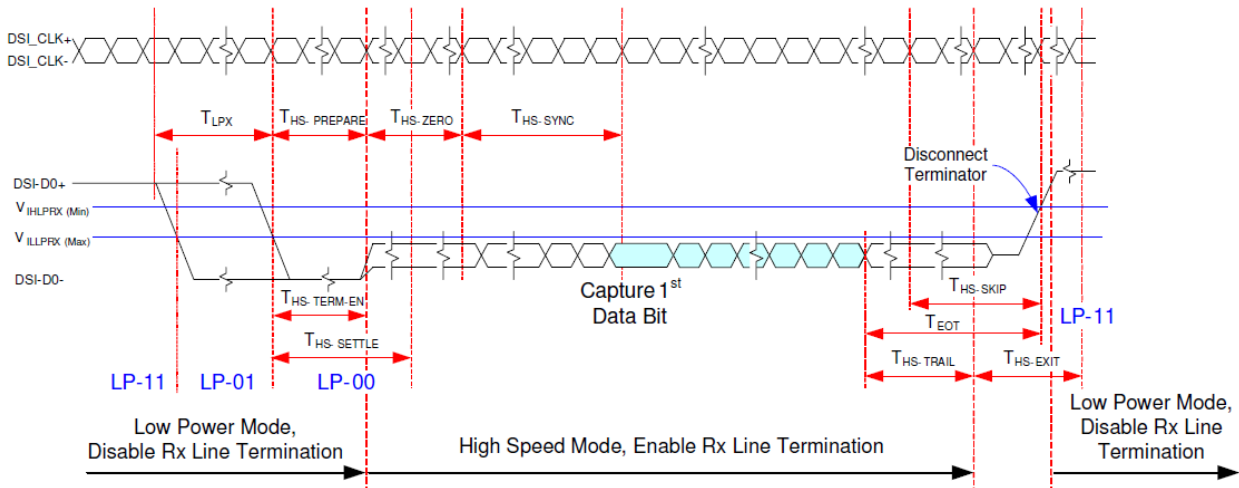
Fig. 7.3.6.2.1: BTA from the MCU to the Display Module



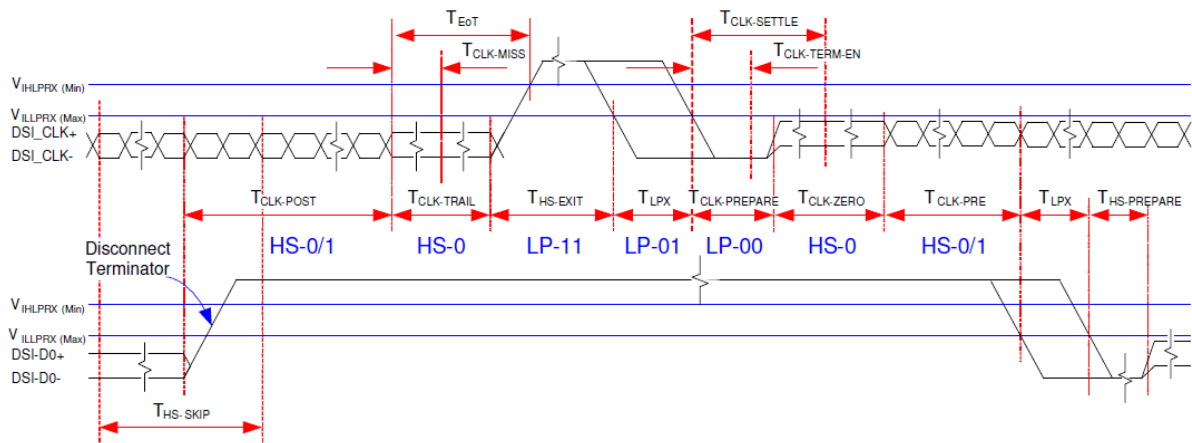
4.2.3. DSI Bursts

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T _{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	T _{HS-TERM-EN}	Time to enable data receiver line termination measured from when Dn crosses V _{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	T _{HS-SKIP}	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	T _{HS-TRAIL}	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	T _{CLK-POS}	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	T _{CLK-TERM-EN}	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	T _{CLK-PREPARE} + T _{CLK-ZERO}	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note) Dn = D0 and D1.

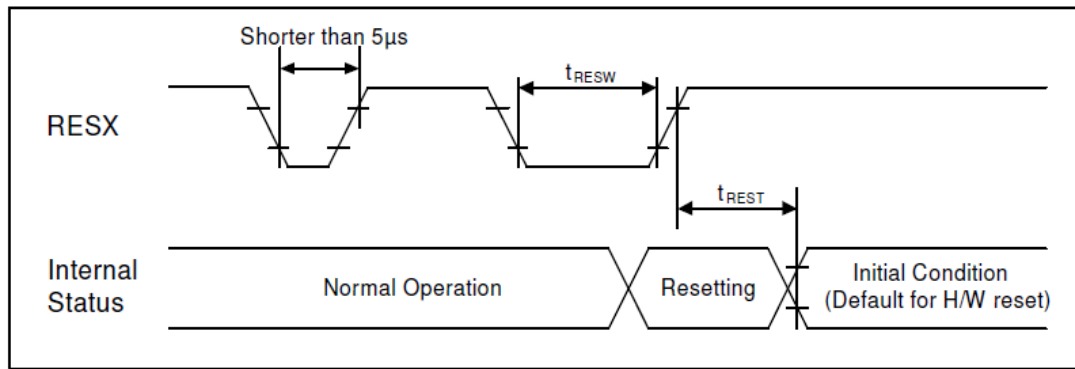


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

4.2.4. Reset Input Timing

**Reset input timing**

(GND=VSS=0V, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, Ta=25°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t _{RESW}	Reset "L" pulse width (Note 1)	10	-	-	µs	
	t _{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

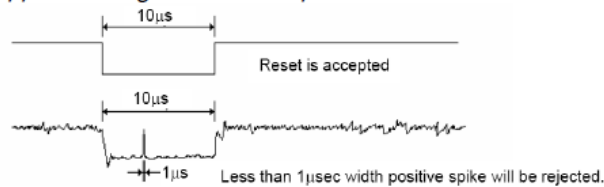
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:

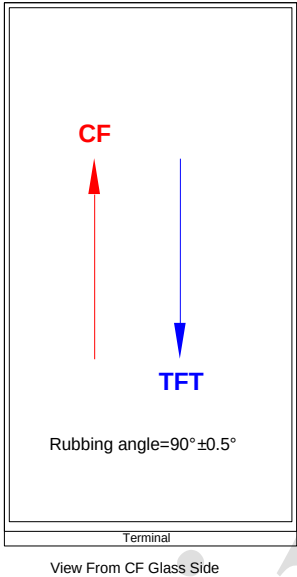


Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

5. CELL PROCESS RULES

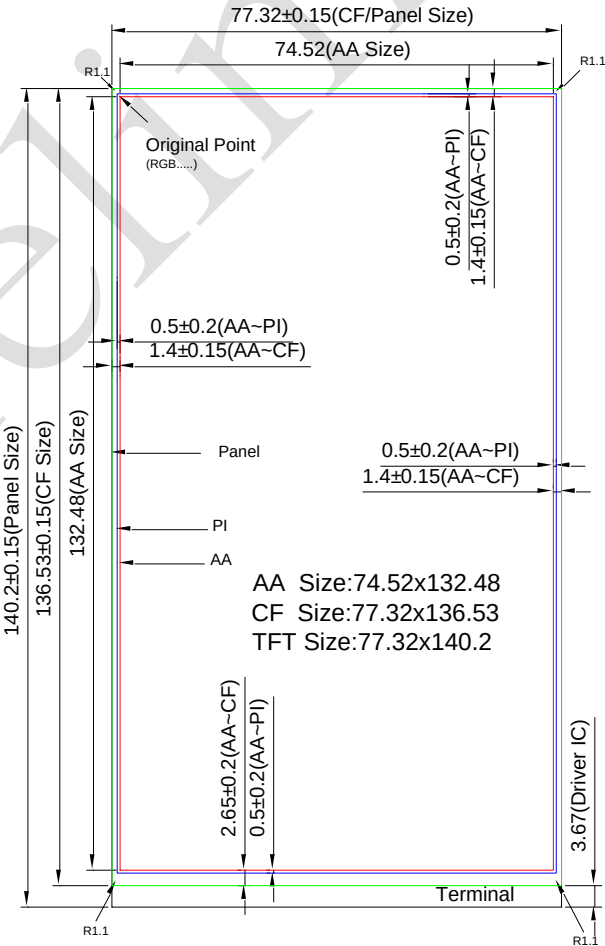
Item	Specification
Cell gap	3.6±0.2um
Assembly precision	±4.0um

5.1 Rubbing Direction

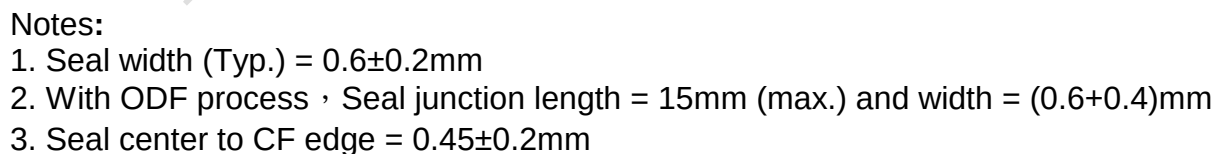


5.2 PI Pattern

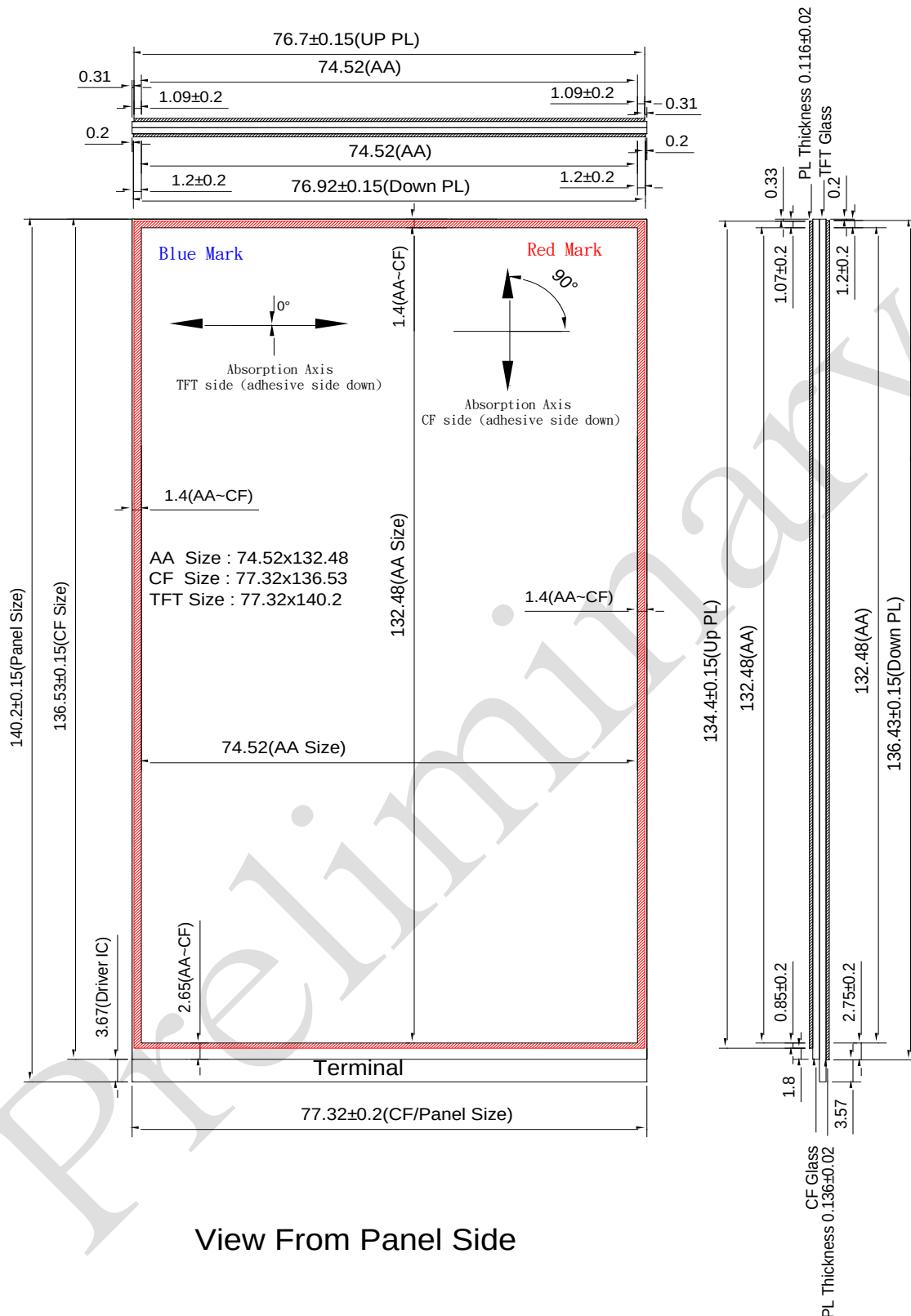
(unit = mm)



(unit = mm)



5.4 Polarizer Information



Up PL Size : 76.7 x 134.4 mm

Down PL Size : 76.92 x 136.43 mm

PL Thickness : 0.116 ± 0.02mm(U) / 0.136 ± 0.02mm (D) ;

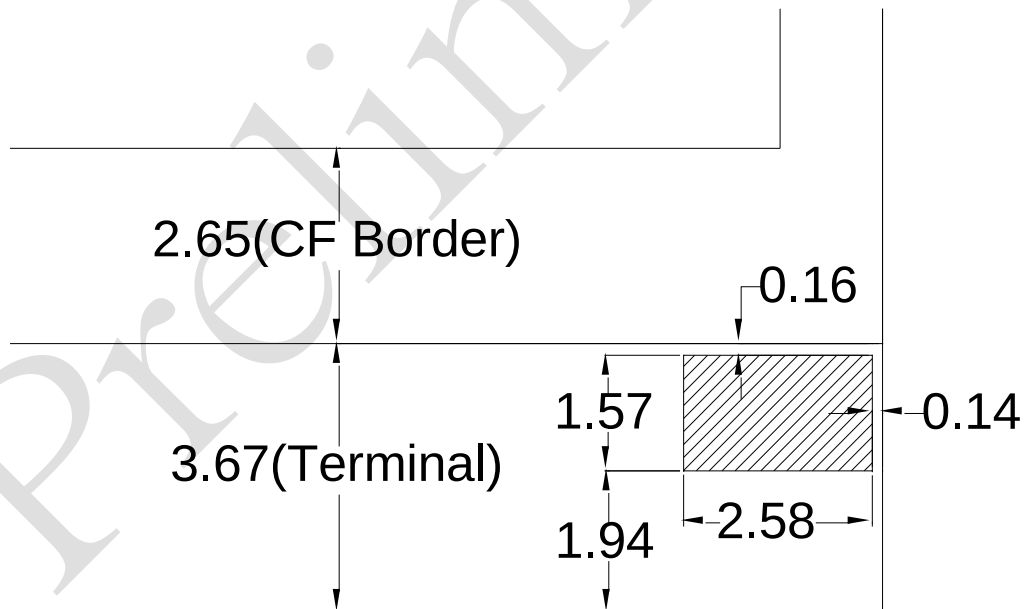
Surface treatment : Up: AG42% / Down:APCF (Zero Tac Type)

5.5 Sliver Pad Size & Position

(unit = mm)



Detail of Silver Pad :



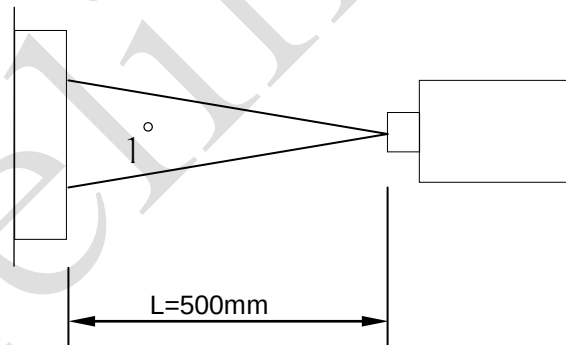
6. OPTICAL SPECIFICATION

(Transmittance, contrast ratio, response time, viewing angle results are using CPT LC + Zero tac Polarizer + Corresponding Backlight, reference only)

Ambient condition : $25 \pm 2^{\circ}\text{C}$, $60 \pm 10\% \text{ RH}$, under 10 Lux in the darkroom.

ITEM		SYMBOL		CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Transmittance (With APCF)		T _{PL}		$\theta = \phi = 0^{\circ}$	4.7	5.0	---	%	Note 2
Contrast Ratio		CR			700	900	---	--	Note 3
Response Time		Tr+Tf		$\theta = \phi = 0^{\circ}$	---	25	35	ms	Note 4
Viewing Angle	Vertical	U	$\theta * 2$	$CR \geq 10$	---	80	---	degree	Note 5
		D			---	80	---	degree	
	Horizontal	L	$\phi * 2$		---	80	---	degree	
		R			---	80	---	degree	
Color Filter Chromaticity (W/ B-ITO) (CIE 1931)	W	x		$\theta = \phi = 0^{\circ}$	(0.306)	(0.316)	(0.336)	--	Note 6
		y			(0.324)	(0.344)	(0.364)	--	
	R	x			(0.636)	(0.656)	(0.676)	--	
		y			(0.299)	(0.319)	(0.339)	--	
	G	x			(0.242)	(0.262)	(0.282)	--	
		y			(0.563)	(0.583)	(0.603)	--	
	B	x			(0.120)	(0.140)	(0.160)	--	
		y			(0.073)	(0.093)	(0.113)	--	
	NTSC				---	70	---		

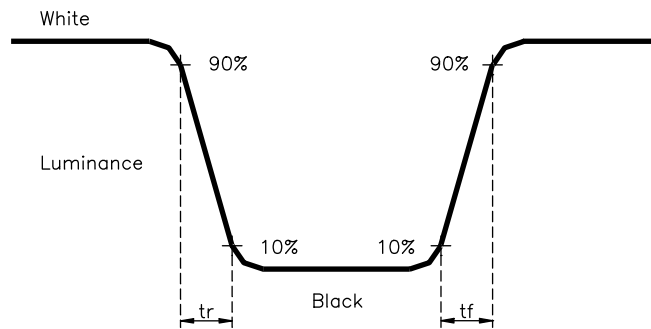
Note 2.Measure device : BM-5A (TOPCON) , viewing cone= 1° , $I_L=20\text{mA}$.



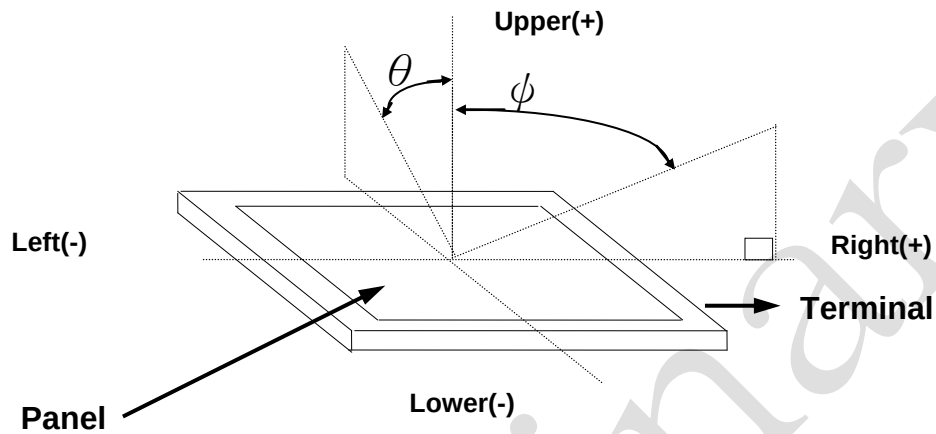
Note 3. Definition of Contrast Ratio :

$CR = \text{White Luminance (ON)} / \text{Black Luminance (OFF)}$

Note 4. Definition of response time : The response time is defined as the time interval between the 10% and 90% amplitudes.



Note 5. Definition of view angle(θ , ϕ) :



Note 6. Light source: C light.

7. RELIABILITY TEST ITEM

N0.	TEST ITEM	CONDITIONS
1	HighTemperature Operation	70° C , 240 hrs
2	Low Temperature Operation	-20° C , 240 hrs
3	High Temperature and High Humidity Operation	60 ° C , 90% RH, 240 hrs

NOTE

1. All judgement of display are performed after temperature of panel return to room temperature.
2. Display function should be no change under normal operating condition.
3. Under no condensation of dew.
4. CPT only guarantee the above 3 test items, and without guarantee the others.