# Chunghwa Picture Tubes, Ltd.
# Product Tentative Specification

To ：華耀/華奕

Date ：201410109

*TFT LCD*

## CLAN050LG41 1XB (COG)-MIPI

**ACCEPTED BY :**

**Tentative V0.0**

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| Doc.No: | SPEC_CLAN050LG41_1XB _V0.2_CPT_20130628 | Issue Date: | 2013.06.28 |
|---|---|---|---|

# REVISION STATUS

| Revision Notice | Description | Page | Rev. Date |
|---|---|---|---|
| 0.0 | First revision (Tentative) | --- | 2013.05.30 |
| 0.1 | Modify Optical specification | 28 | 2013.06.28 |
| 0.2 | Modify Optical specification | 28 | 2013.06.28 |
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**CONTENTS**

# 1. OVERVIEW

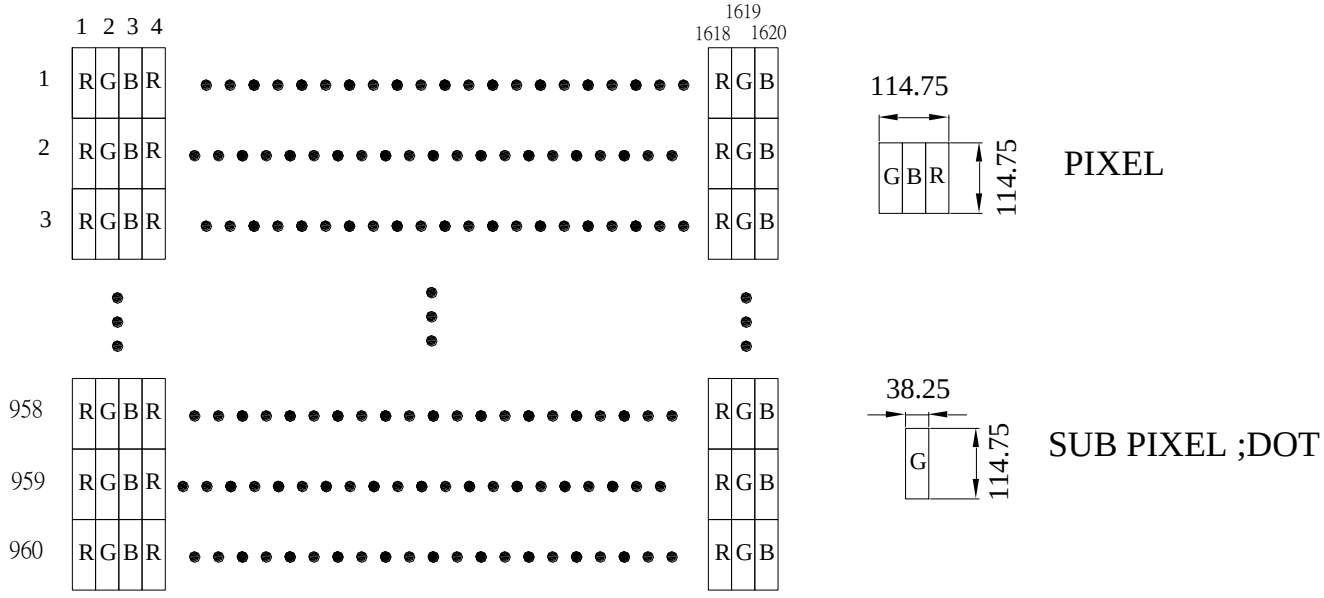
CPT CLAN050LG41 is a full cell (or ODF Full cell) product of TFT-LCD substrate with optimum arrangement provides up to 312 pieces of 9:16 aspect ratio panels for the high end PND or PDVD application.

The 5” screen produces a high resolution image that is composed of 518,400 (540×960) pixel elements in a delta arrangement.

General specifications are summarized in the following table:

| ITEM | SPECIFICATION |
|---|---|
| Panel Size | 5" inch |
| Display Area (mm) | 61.965 (H) x 110.16 (V) |
| CF glass dimension | 64.87 (H) x 114.31 (V) x 0.2(Thickness) |
| TFT glass dimension | 64.87 (H) x 118.31 (V) x 0.2(Thickness) |
| Number of Pixels | 540x3(H) x 960(V) |
| Pixel Pitch (mm) | 0.11475(H) x 0.11475(V) |
| Color Pixel Arrangement | RGB stripe type |
| Display Mode | normally black |
| NTSC | **70%** |
| Up Polarizer(mm) | **64.47 x 113.31 x 0.116( HC)** |
| Down Polarizer(mm) | **64.47 x 113.31 x 0.136 (APCF)** |
| Driving Method | TFT active matrix |
| Viewing Direction | 85/85/85/85 |
| Suggesting IC | OTM9605 |

LCD Cell Drawing
(Note 1)




The LCD products listed on this document are not suitable for use of aerospace equipment, submarine cables, nuclear reactor control system and life support systems. If customers intend to use these LCD products for above application or not listed in "Standard" as follows, please contact our sales people in advance.

## 2. ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|
| **Enviromental Phase** | | | | | |
| Operating Ambient Temperature | $T_{OP}$ | -20 | +70 | ˚C | |
| Operating Ambient Humidity | $H_{OP}$ | 10 | 90 | % (RH) | |
| Storage Temperature | $T_{STG}$ | -30 | +80 | ˚C | |
| Storage Humidity | $H_{STG}$ | 10 | 90 | % (RH) | |
| **Electrical Phase** | | | | | |
| Power supply for Analog | VDD | -0.3 | 6.0 | V | |
| Power supply for Logic | VCC | -0.3 | 6.0 | V | |
| Power supply for I/O and Digital | VDDIO | -0.3 | 4.5 | V | |
| Power supply for highspeed | VDDAM | -0.3 | 6.0 | V | |
| TFT Gate On Voltage | *VGH* | 13 | 19 | V | |
| TFT Gate Off Voltage | *VGL* | -13 | -8 | V | |
| TFT Common Voltage | *VCOM* | -2 | 0 | V | Note 3 |

Note 1. The absolute maximum ratings are the values that must not be exceeded at any time for this product. It is not allowed for any of these ratings to be exceeded. Should a product be used with any of the absolute maximum ratings exceeded, the characteristics of the product may not be recovered, or in an extreme case, the product may be permanently destroyed.

Therefore, when desigining a system incorporating the product, make sure that adequate attentions be paid to the variations in the supply voltages, the characteristics of parts that are connected, surges in the input and output lines, and the ambient temperatures.

Note 2. This specification applys after the driver IC mounting and the FPC mounting. (This specification isn't applicable at time of driver IC un-mounting and FPC un-mounting.)

LCD should keep the condition that dew dosen't storage in case of driver IC un-mounting and FPC un-mounting. Dew may break the LCD. Especially part is very weak for dew.

Note 3. Vcom must be adjusted to optimize display quality, as crosstalk and contrast ratio etc.

# 3. ELECTRICAL CHARACTERISTICS

## 3.1 TFT LCD Power Supply Voltage

(GND=AVSS=0V)

Ta = 25℃

| Parameter | SYMBOL | Min | Typ | Max | Unit | Remarks |
|---|---|---|---|---|---|---|
| Analog Power Voltage1 | VCCA | 2.5 | 2.8 | 3.6 | V | |
| Analog Power Voltage2 | VCC | 2.5 | 2.8 | 3.6 | V | |
| **I/Oand Digital Power Voltage** | VCCIO | 1.65 | 1.8 | 3.6 | V | |
| Highspeed Power Voltage | HS_VCC | 1.65 | 2.8 | 3.3 | V | |
| Current For Driving | IDD | | TBD | TBD | mA | Note 1 |
| Input Signal Voltage | VIH | 0.7*VDDIO | - | VDDIO | V | Note 2 |
| | VIL | 0 | - | 0.3*VDDIO | V | |

Note 1：Typ. specification：Gray-256 test Pattern

Max. specification：White test Pattern

Note 2：VDDIO = 1.8V

## 3.2 TFT-LCD consumption Current

(GND=AVSS=0V)

Ta = 25℃

| MODE | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT | REMARK |
|---|---|---|---|---|---|---|---|
| Total Power Consumption | Pc | | - | TBD | TBD | mW | Note1 |

Note1：Typ. specification：Gray-256 test Pattern

Max. specification：White test Pattern

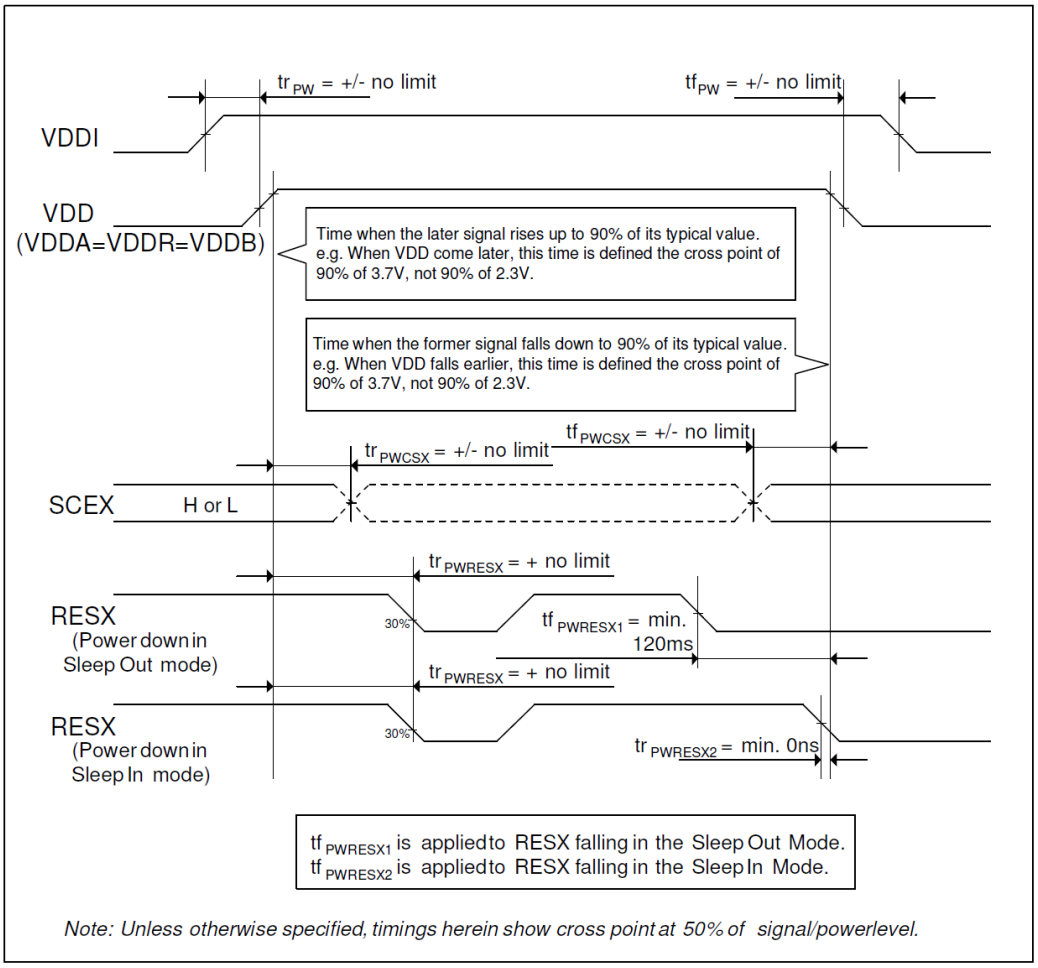
(a)Gray-256 Pattern

(b)White Pattern

## 3.3 Power on/off sequence

**Case 1 – RESX line is held High or Unstable by Host at Power On**

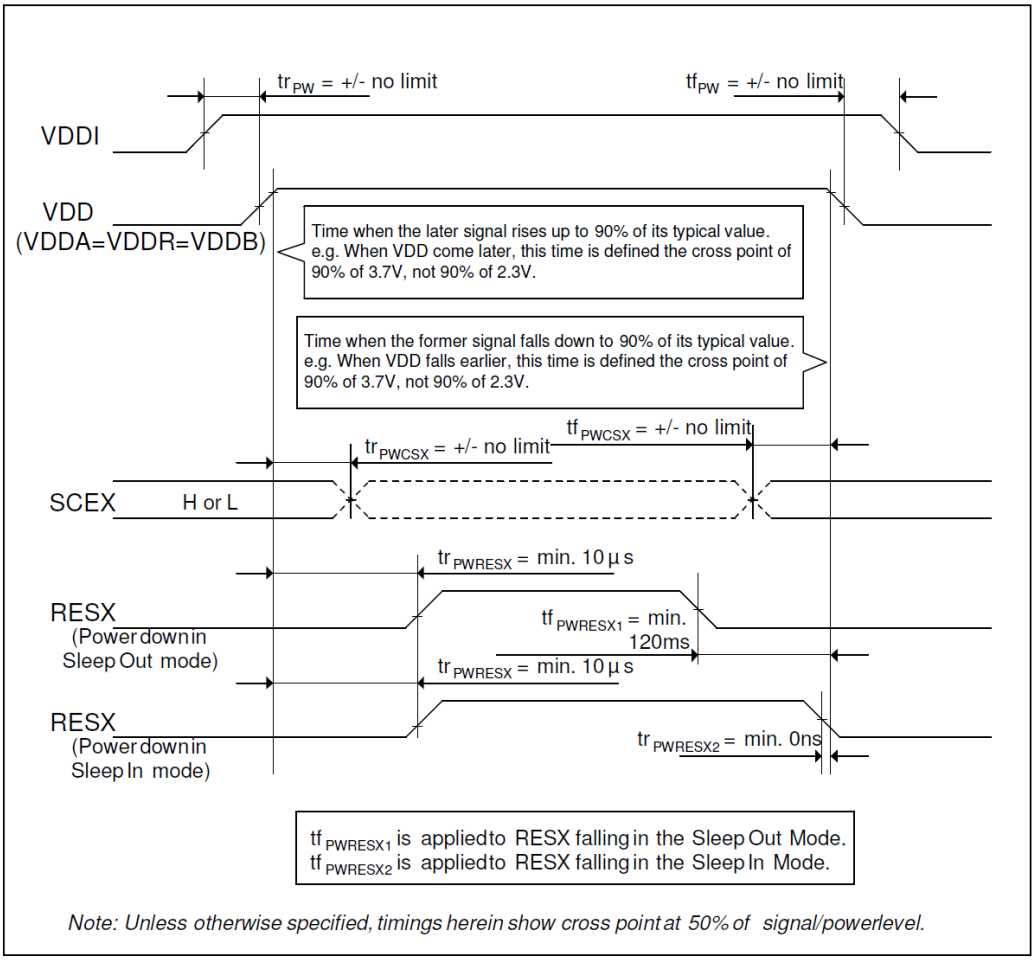
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD (VDDA) and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.




*Note: Unless otherwise specified, timings herein show cross point at 50% of signal/powerlevel.*

**Case 2 – RESX line is held Low by host at Power On**

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD (VDDA) and VDDI have been applied.




*Note: Unless otherwise specified, timings herein show cross point at 50% of signal/powerlevel.*

# 4. INPUT SIGNAL TIMING

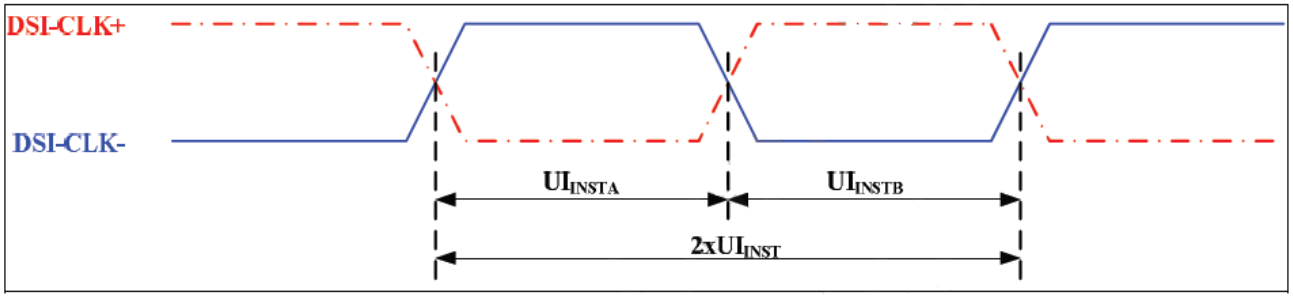
## 4.1 MIPI Timing DC Characteristics

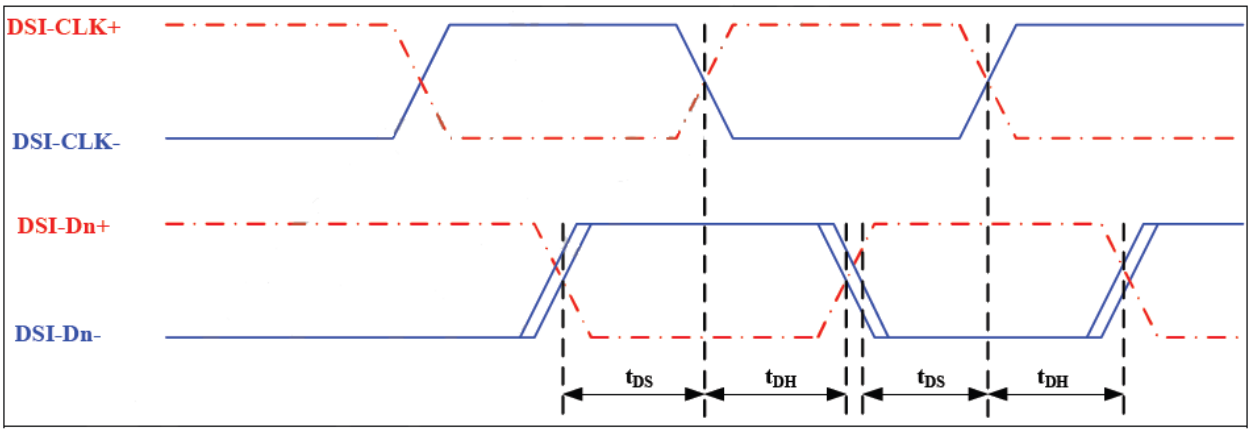
| Parameter | Symbol | Conditions | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Power supply voltage for MIPI Interface** | | | | | | |
| Power supply voltage for MIPI interface | VDDAM | - | 2.3 | 2.8 | 4.8 | V |
| | VDDP | For LPDT | 1.1 | 1.2 | 1.3 | V |
| | LVDSVDD | - | 1.5 | 1.55 | 1.6 | V |
| **LPDT Input Characteristics** | | | | | | |
| Pad signal voltage range | VI | - | -50 | - | 1350 | mV |
| Ground Shift | VGNDSH | - | -50 | - | 50 | mV |
| Logic 0 input threshold | VIL | - | 0 | - | 550 | mV |
| Logic 1 input threshold | VIH | - | 880 | - | VDDAM | mV |
| Input hysteresis | VHYST | - | 25 | - | - | mV |
| **LPDT Output Characteristics** | | | | | | |
| Output low level | VOL | - | -50 | - | 50 | mV |
| Output high level | VOH | - | 1.1 | 1.2 | 1.3 | V |
| Logic 1 contention threshold | VILCD,MIN | - | 450 | - | VDDAM | mV |
| Logic 0 contention threshold | VIHCD,MAX | - | 0 | - | 200 | mV |
| Output impedence of LPDT | ZOLP | - | 80 | 100 | 125 | ohm |
| **Hi-speed Input/Output Characteristics** | | | | | | |
| Single-end input low voltage | VILHS | - | -40 | - | - | mV |
| Single-end input high voltage | VIHHS | - | - | - | 460 | mV |
| Common mode voltage | VCMRXDC | - | 70 | - | 330 | mV |
| Hi-speed transmit voltage | VOD | - | 140 | 200 | 250 | mV |
| Differential input impedence | ZID | - | 80 | 100 | 125 | ohm |

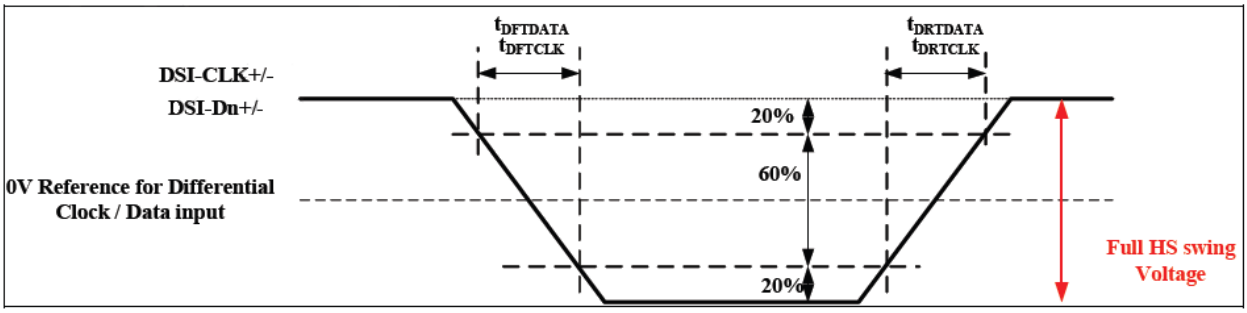
## 4.2 MIPI Timing AC Characteristics

### 4.2.1. High Speed Mode

| Parameter | Symbol | Parameter | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **High Speed mode** | | | | | | |
| **DSI-CLK+/-** | **$2xUI_{INST}$** | **Double UI instantaneous** | 4 | - | 25 | **ns** |
| **DSI-CLK+/-** | **$UI_{INSTA}$ , $UI_{INSTB}$** | **UI instantaneous Halfs** | 2 | - | 12.5 | **ns** |
| **DSI-Dn+/-** | **$t_{DS}$** | **Data to clock setup time** | 0.15 | - | - | **UI** |
| **DSI-Dn+/-** | **$t_{DH}$** | **Data to clock hold time** | 0.15 | - | - | **UI** |
| **DSI-CLK+/-** | **$t_{DRTCLK}$** | **Differential rise time for clock** | 150 | - | 0.3UI | **ps** |
| **DSI-Dn+/-** | **$t_{DRTDATA}$** | **Differential rise time for data** | 150 | - | 0.3UI | **ps** |
| **DSI-CLK+/-** | **$t_{DFTCLK}$** | **Differential fall time for clock** | 150 | - | 0.3UI | **ps** |
| **DSI-Dn+/-** | **$t_{DFTDATA}$** | **Differential fall time for data** | 150 | - | 0.3UI | **ps** |




DSI-CLK+
DSI-CLK-
DSI-Dn+
DSI-Dn-
tDS
tDH
tDS
tDH


tDFTDATA
tDFTCLK
tDRTDATA
tDRTCLK
DSI-CLK+/-
DSI-Dn+/-
20%
60%
20%
0V Reference for Differential
Clock / Data input
Full HS swing
Voltage

4.2.2. Low Power Mode

| Parameter | Symbol | Parameter | Specification | | | Unit |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **Low Power mode** | | | | | | |
| DSI-D0+/- | $T_{LPXM}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module | 50 | - | - | ns |
| DSI-D0+/- | $T_{LPXD}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU | 58 | - | - | ns |
| DSI-D0+/- | $T_{TA-SURED}$ | Time-out before the MPU start driving | $T_{LPXD}$ | - | $2XT_{LPXD}$ | ns |
| DSI-D0+/- | $T_{TA-GETD}$ | Time to drive LP-00 by display module | $5XT_{LPXD}$ | - | - | ns |
| DSI-D0+/- | $T_{TA-GOD}$ | Time to drive LP-00 after turnaround request - MPU | $4XT_{LPXD}$ | - | - | ns |
| DSI-D0+/- | Ratio $T_{LPX}$ | Ratio of $T_{LPXM}$ / $T_{LPXD}$ between MCU and display module | 2/3 | - | 3/2 | |

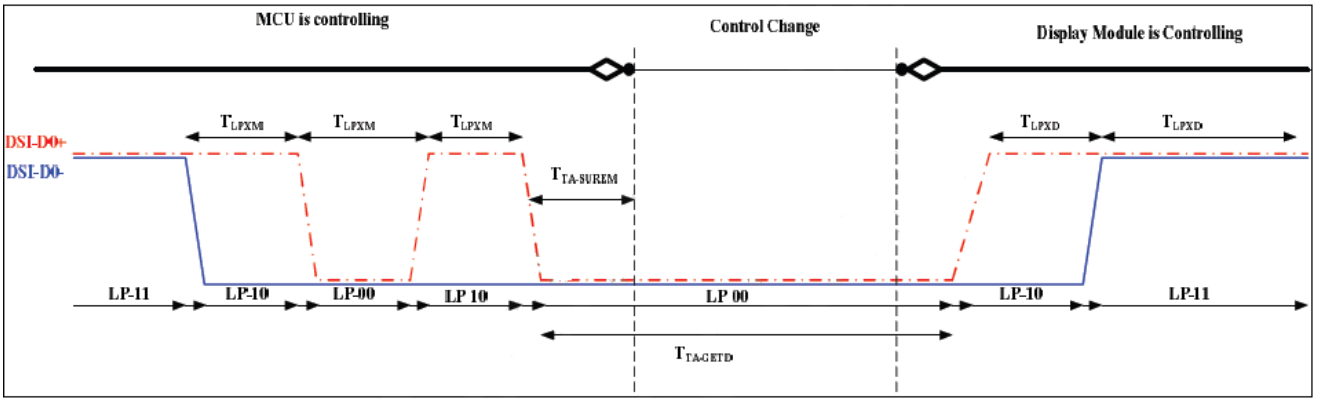
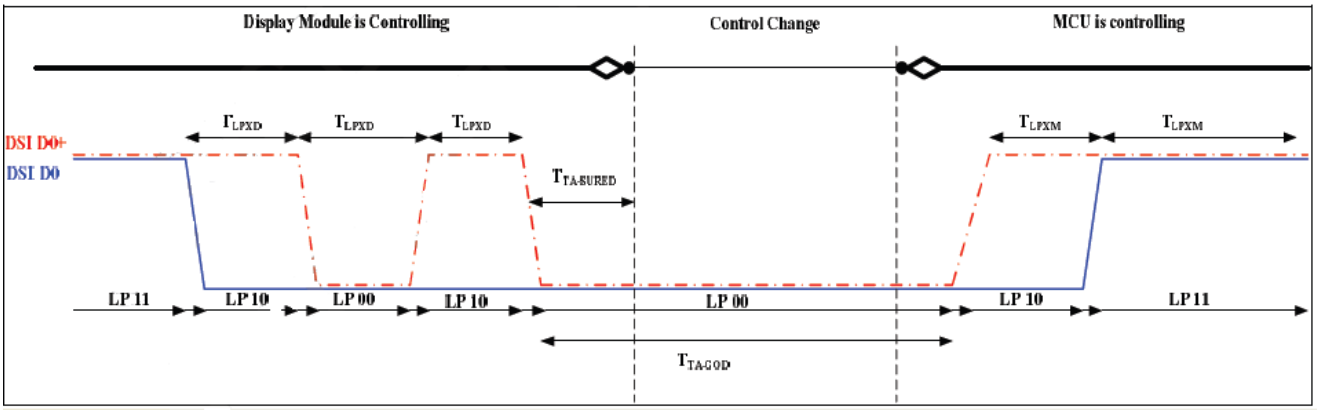


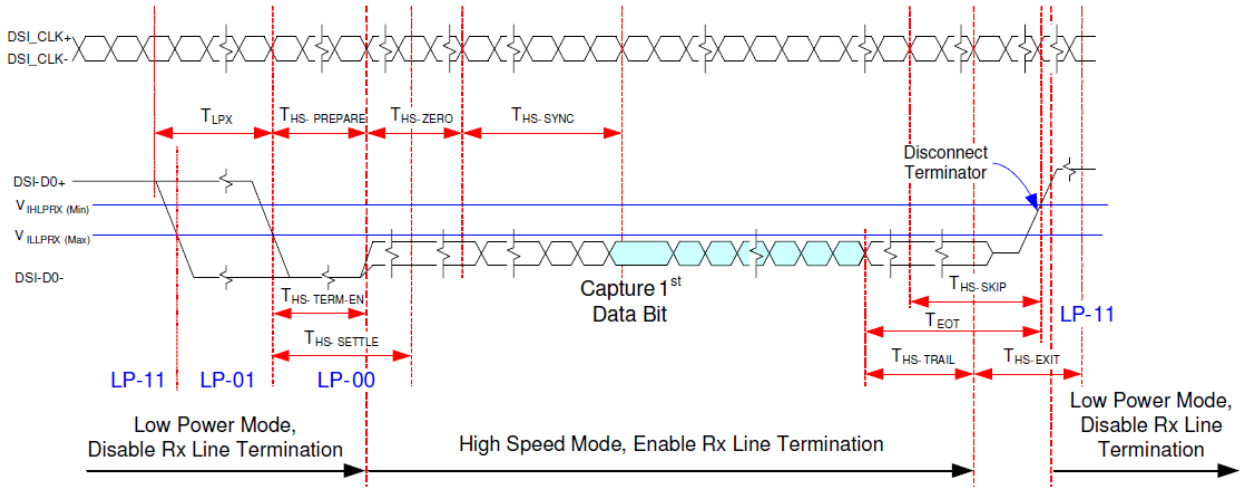

Fig. 7.3.6.2.1: BTA from the MCU to the Display Module



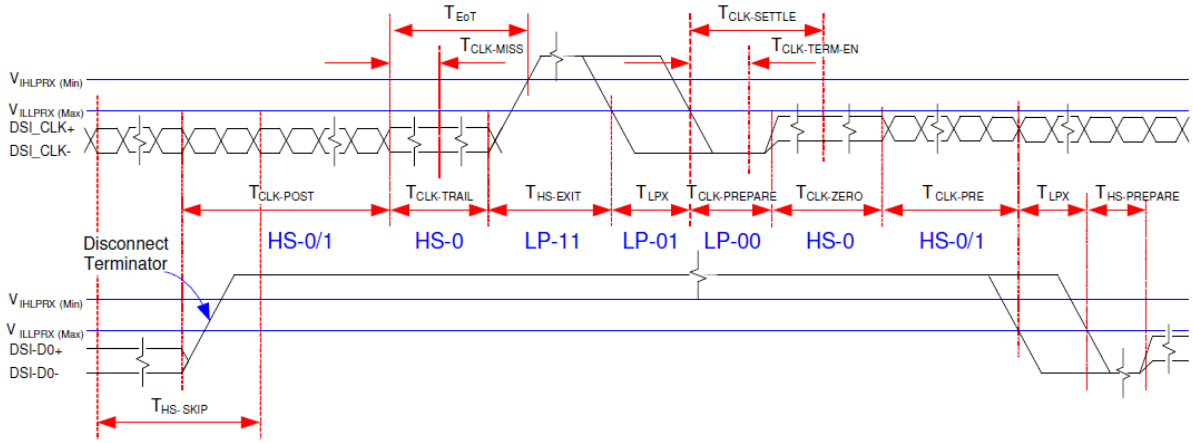
4.2.3. DSI Bursts

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| Low Power Mode to High Speed Mode Timing | | | | | | | |
| DSI-Dn+/- | $T_{LPX}$ | Length of any low power state period | 50 | - | - | ns | Input |
| DSI-Dn+/- | $T_{HS-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 40+4xUI | - | 85+6xUI | ns | Input |
| DSI-Dn+/- | $T_{HS-TERM-EN}$ | Time to enable data receiver line termination measured from when Dn crosses $V_{ILMAX}$ | - | - | 35+4xUI | ns | Input |
| High Speed Mode to Low Power Mode Timing | | | | | | | |
| DSI-Dn+/- | $T_{HS-SKIP}$ | Time-out at display module to ignore transition period of EoT | 40 | - | 55+4xUI | ns | Input |
| DSI-Dn+/- | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | - | ns | Input |
| DSI-Dn+/- | $T_{HS-TRAIL}$ | Time to drive flipped differential state after last payload data bit of a HS transmission burst | 60+4xUI | - | - | ns | Input |
| High Speed Mode to/from Low Power Mode Timing | | | | | | | |
| DSI-CLK+/- | $T_{CLK-POS}$ | Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode | 60+52xUI | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-TRAIL}$ | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | - | ns | Input |
| DSI-CLK+/- | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 38 | - | 95 | ns | Input |
| DSI-CLK+/- | $T_{CLK-TERM-EN}$ | Time-out at clock lane display module to enable HS transmission | - | - | 38 | ns | Input |
| DSI-CLK+/- | $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | Minimum lead HS-0 drive period before starting clock | 300 | - | - | ns | Input |
| DSI-CLK+/- | $T_{CLK-PRE}$ | Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode | 8xUI | - | - | ns | Input |

*Note) Dn = D0 and D1.*

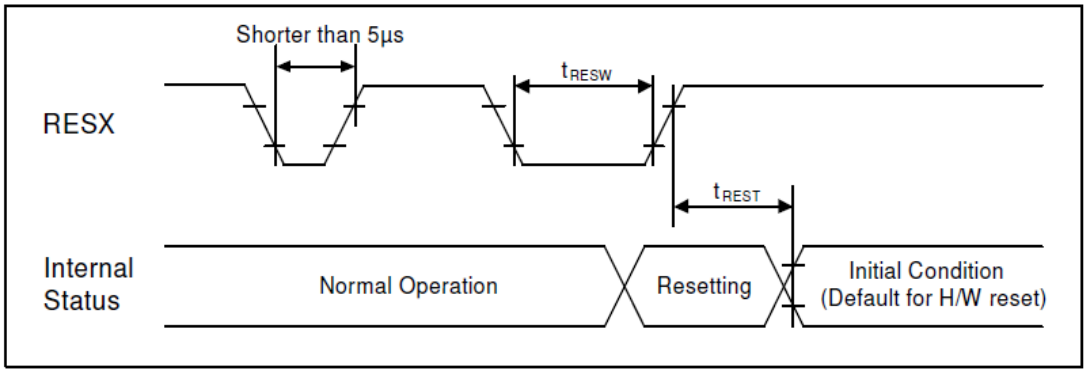



***Data lanes-Low Power Mode to/from High Speed Mode Timing***




***Clock lanes- High Speed Mode to/from Low Power Mode Timing***

4.2.4. Reset Input Timing




***Reset input timing***

(GND=VSS=0V, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, Ta=25°C)

| Signal | Symbol | Parameter | MIN | TYP | MAX | Unit | Description |
|---|---|---|---|---|---|---|---|
| RESX | tRESW | Reset "L" pulse width (Note 1) | 10 | - | - | µs | |
| | tREST | Reset complete time (Note 2) | - | - | 5 | ms | When reset applied during Sleep In Mode |
| | | | - | - | 120 | ms | When reset applied during Sleep Out Mode |

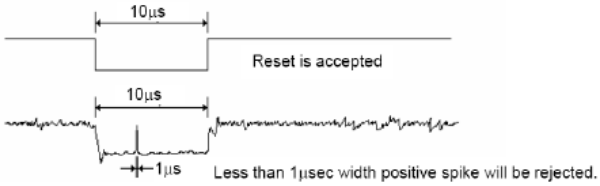
*Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.*

| *RESX Pulse* | *Action* |
|---|---|
| *Shorter than 5µs* | *Reset Rejected* |
| *Longer than 10µs* | *Reset* |
| *Between 5µs and 10µs* | *Reset Start* |

*Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.*

*Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time ($t_{REST}$) within 5ms after a rising edge of RESX.*

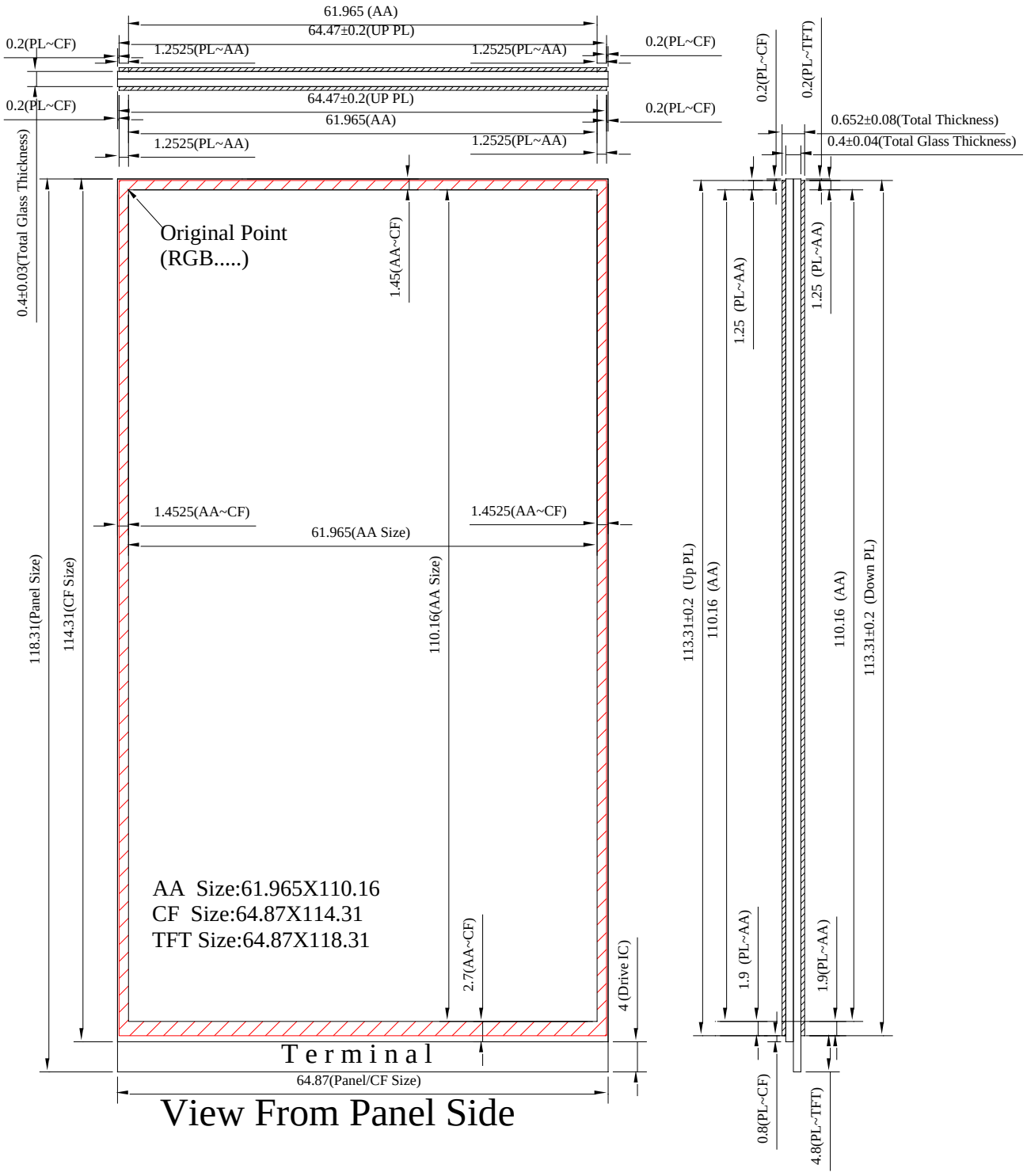
*Note 4) Spike Rejection also applies during a valid reset pulse as shown below:*




*Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec*

# 5. MECHANICAL SPECIFICATIONS

## 5.1 Outline Dimension

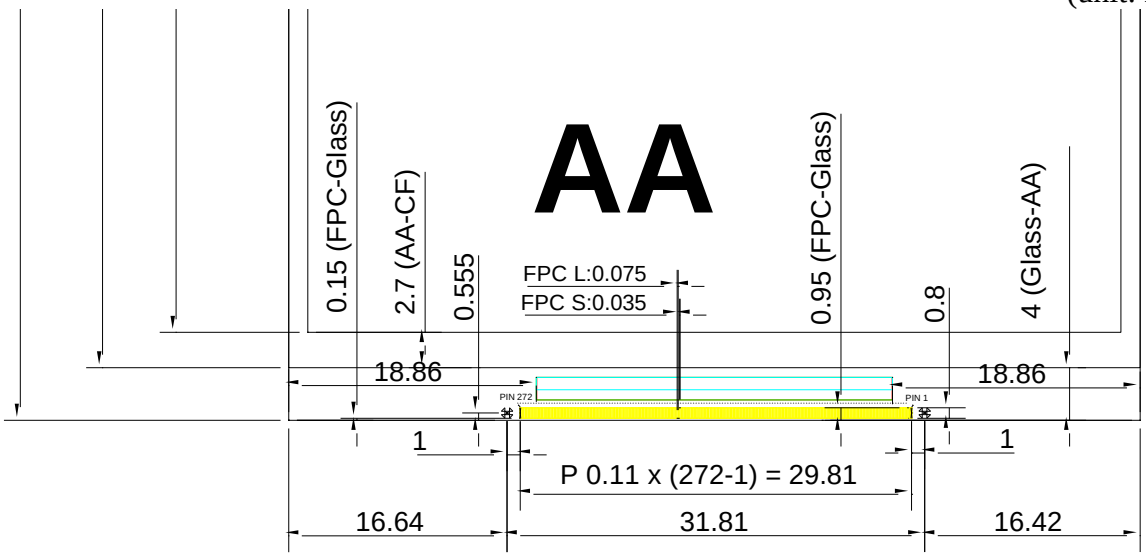



Up PL : HC **64.47 x 113.31 x 0.116**
Down PL : APCF **64.47 x 113.31x 0.136**
Up PL Thickness& Surface Treatment : 116um±20um HC
Down PL Thickness& Surface Treatment : 136um±20um APCF

(unit: mm)

## 5.2 IC & FPC Pads

(unit: mm)

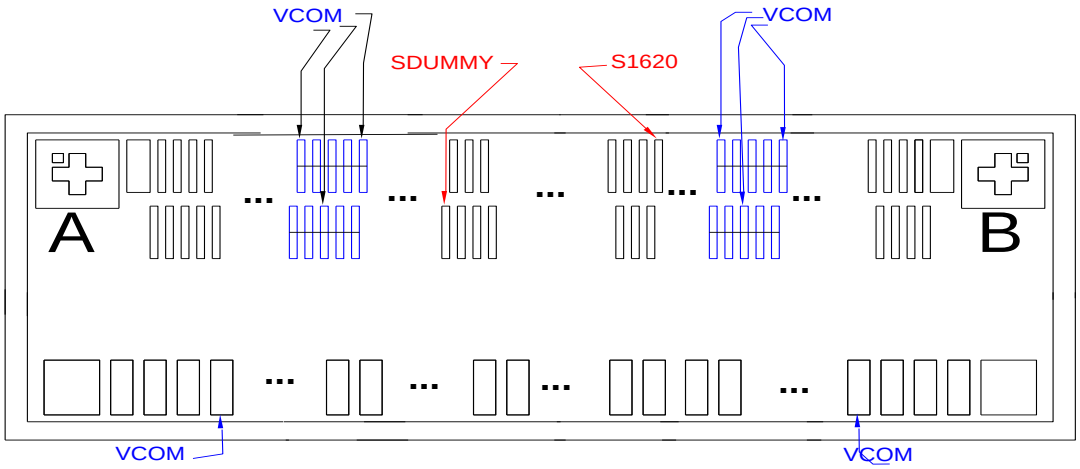



Note1. Color Filter is at the side , TFT is at bottom side

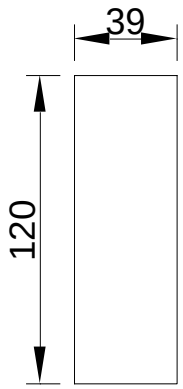
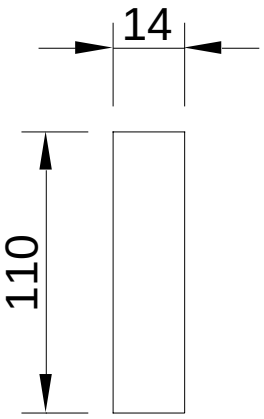
Note2. This Source IC size is of OTM9605

5.2.1 IC Pads

Source IC （OTM9605）



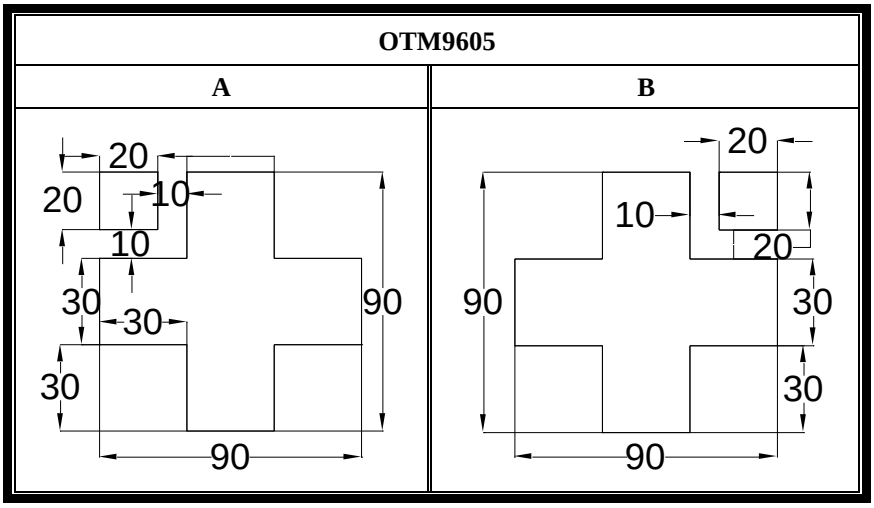

**1. Gold Bump Size(unit：um)：**

| | **Source IC (OTM9605)** |
|---|---|
| **Input Bump** |   |
| **Output Bump** |   |

2. Chip Size：

| IC | Chip Size |
|---|---|
| OTM9605 | 27.15 mm x 0.95 mm |

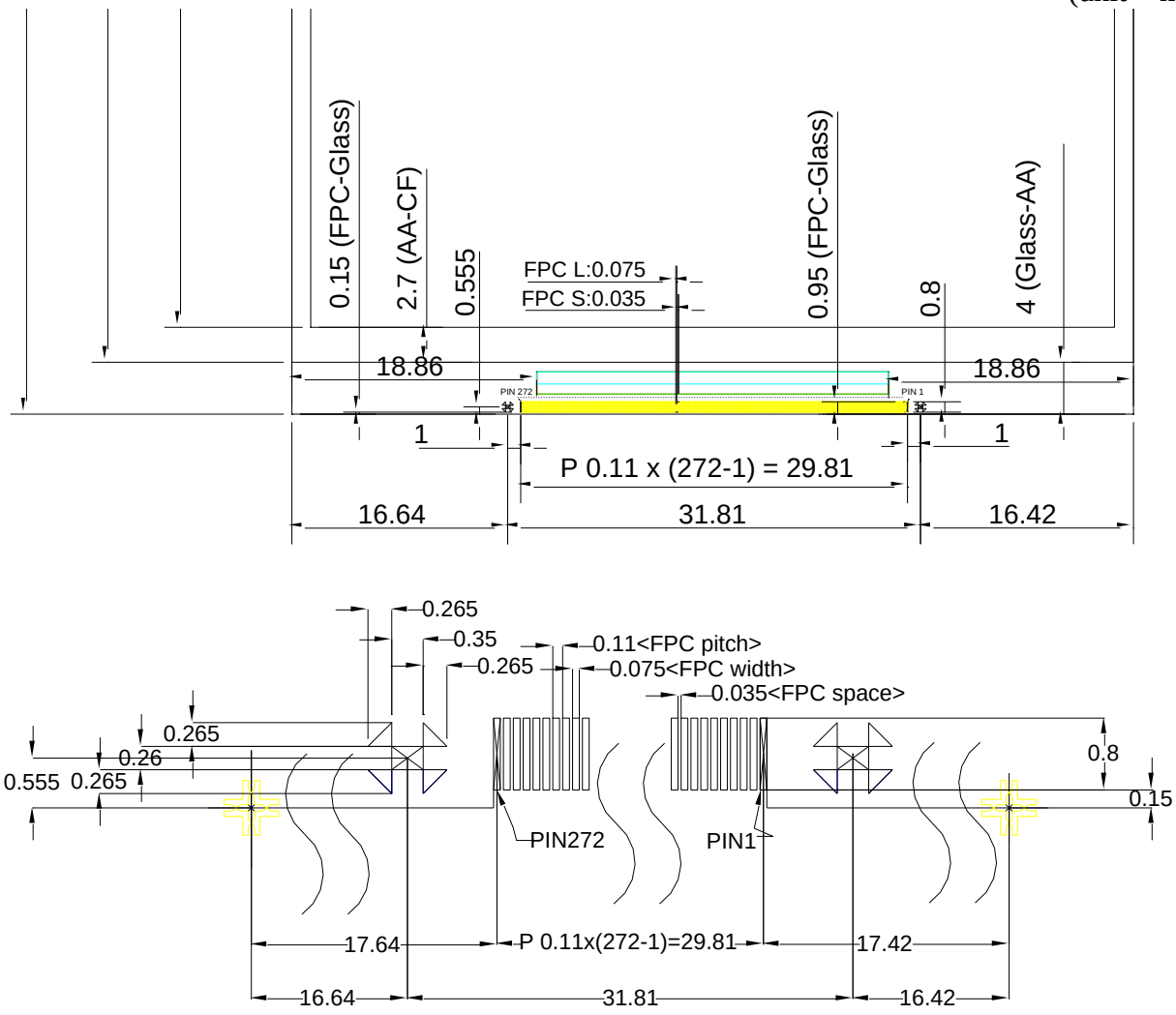
3. Alignment Mark Size (unit：um)：




(unit = mm)

5.2.2 FPC Pads

(unit = mm)

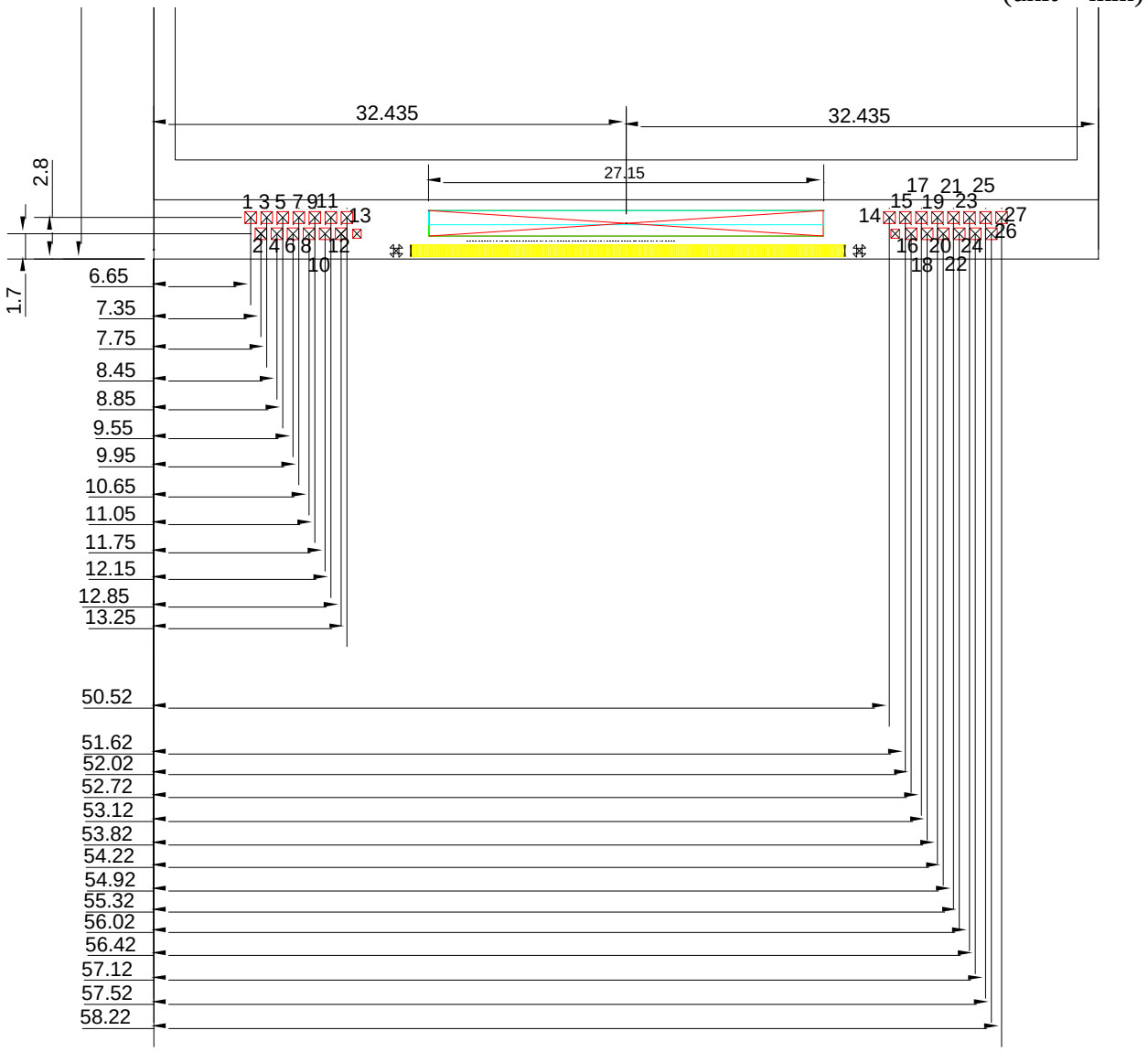


## 5.2.3 FPC Pin Assignment (OTM9605A)

| Pin No. | Symbol | Pin No. | Symbol | Pin No. | Symbol | Pin No. | Symbol |
|---|---|---|---|---|---|---|---|
| 1 | DUMMY | 71 | CSX | 141 | D0P | 211 | C21N |
| 2 | DUMMY | 72 | RESX | 142 | D0N | 212 | C21N |
| 3 | Ground | 73 | VSSI | 143 | D0N | 213 | C21N |
| 4 | Ground | 74 | VDDIO | 144 | LVDSVSS | 214 | C22P |
| 5 | VCOM | 75 | NBWSEL | 145 | D2P | 215 | C22P |
| 6 | DUMMY | 76 | D23 | 146 | D2P | 216 | C22P |
| 7 | DUMMY | 77 | D22 | 147 | D2N | 217 | C22N |
| 8 | DUMMY | 78 | D21 | 148 | D2N | 218 | C22N |
| 9 | DUMMY | 79 | D20 | 149 | LVDSVSS | 219 | C22N |
| 10 | VCOM | 80 | D19 | 150 | VDD | 220 | C23N |
| 11 | VCOM | 81 | D18 | 151 | TE_R | 221 | C23N |
| 12 | 3D_CLK_0 | 82 | D17 | 152 | VSS | 222 | C23N |
| 13 | 3D_CLK_0 | 83 | D16 | 153 | VREFCP | 223 | C23P |
| 14 | 3D_CLK_1 | 84 | D15 | 154 | VRGH | 224 | C23P |
| 15 | 3D_CLK_1 | 85 | D14 | 155 | EXTP | 225 | C23P |
| 16 | 3D_CLK_2 | 86 | D13 | 156 | CSP | 226 | NVDDA |
| 17 | 3D_CLK_2 | 87 | D12 | 157 | EXTN | 227 | NVDDA |
| 18 | 3D_CLK_3 | 88 | D11 | 158 | CSN | 228 | NVDDA |
| 19 | 3D_CLK_3 | 89 | D10 | 159 | VSSA | 229 | VDD |
| 20 | BVP3D | 90 | D9 | 160 | VSSA | 230 | VDD |
| 21 | BVN3D | 91 | D8 | 161 | VSSA | 231 | VDD |
| 22 | MTP_PWR | 92 | D7 | 162 | C11P | 232 | VSS |
| 23 | VGL | 93 | D6 | 163 | C11P | 233 | VSS |
| 24 | VGL_REG | 94 | D5 | 164 | C11P | 234 | VSS |
| 25 | VRGH | 95 | D4 | 165 | C11N | 235 | C41P |
| 26 | VCL | 96 | D3 | 166 | C11N | 236 | C41P |
| 27 | VCL | 97 | D2 | 167 | C11N | 237 | C41N |
| 28 | VCL | 98 | D1 | 168 | C12P | 238 | C41N |
| 29 | VREF | 99 | D0 | 169 | C12P | 239 | C51N |
| 30 | VSSA | 100 | DE | 170 | C12P | 240 | C51N |
| 31 | VSSA | 101 | PCLK | 171 | C12N | 241 | C51P |
| 32 | VDD | 102 | HS | 172 | C12N | 242 | C51P |
| 33 | VDD | 103 | VS | 173 | C12N | 243 | VGH |
| 34 | VDD | 104 | LEDPWM | 174 | C13N | 244 | VGH |
| 35 | VSS | 105 | LEDON | 175 | C13N | 245 | VGH |
| 36 | VDD | 106 | ERR | 176 | C13N | 246 | VGH |
| 37 | DIOPWR | 107 | VDDIO | 177 | C13P | 247 | VRGH |
| 38 | VGSN | 108 | VSS | 178 | C13P | 248 | VRGH |
| 39 | VGSP | 109 | VCC | 179 | C13P | 249 | VGL_REG |
| 40 | VGMN | 110 | VCC | 180 | VDDA | 250 | VGL_REG |
| 41 | VGMP | 111 | VCC | 181 | VDDA | 251 | VGL |
| 42 | VSS | 112 | VDDA | 182 | VDDA | 252 | VGL |
| 43 | VSS | 113 | VDDA | 183 | VDD | 253 | VGL |
| 44 | VDD_1.8V | 114 | NVDDA | 184 | VDD | 254 | VGL |
| 45 | VDD_1.8V | 115 | NVDDA | 185 | VDD | 255 | VSSA |
| 46 | VSSA | 116 | VSS | 186 | VDD | 256 | VSSA |
| 47 | VSSA | 117 | VSS | 187 | VDD | 257 | VDD |
| 48 | LANSEL | 118 | VDD_1.8V | 188 | VSS | 258 | VDD |
| 49 | DSWAP0 | 119 | VDD_1.8V | 189 | VSS | 259 | VDD_1.8V |
| 50 | DSWAP1 | 120 | LVDSVDD | 190 | VSS | 260 | VDD_1.8V |
| 51 | PSWAP | 121 | VDDAM | 191 | VSS | 261 | VSS |
| 52 | DSTB_SEL | 122 | VDDP | 192 | VSS | 262 | VSS |
| 53 | RGBBP | 123 | LVDSVSS | 193 | C31P | 263 | VCOM |
| 54 | I2C_SA0 | 124 | LVDSVSS | 194 | C31P | 264 | VCOM |
| 55 | IM3 | 125 | D22P | 195 | C31P | 265 | DUMMY |
| 56 | IM2 | 126 | D22P | 196 | C31N | 266 | DUMMY |
| 57 | IM1 | 127 | D22N | 197 | C31N | 267 | DUMMY |
| 58 | IM0 | 128 | D22N | 198 | C31N | 268 | DUMMY |
| 59 | GPO3 | 129 | LVDSVSS | 199 | C32P | 269 | VGL |
| 60 | GPO2 | 130 | D1P | 200 | C32P | 270 | VCOM |
| 61 | GPO1 | 131 | D1P | 201 | C32P | 271 | DUMMY |
| 62 | GPO0 | 132 | D1N | 202 | C32N | 272 | DUMMY |
| 63 | EXB1T | 133 | D1N | 203 | C32N | | |
| 64 | TE_L | 134 | LVDSVSS | 204 | C32N | | |
| 65 | VSEL | 135 | CLKP | 205 | VCL | | |
| 66 | SDO | 136 | CLKP | 206 | VCL | | |
| 67 | SDI | 137 | CLKN | 207 | VCL | | |
| 68 | DCX | 138 | CLKN | 208 | C21P | | |
| 69 | WRX | 139 | LVDSVSS | 209 | C21P | | |
| 70 | RDX | 140 | D0P | 210 | C21P | | |

## 5.3 Panel Testing pads in panel

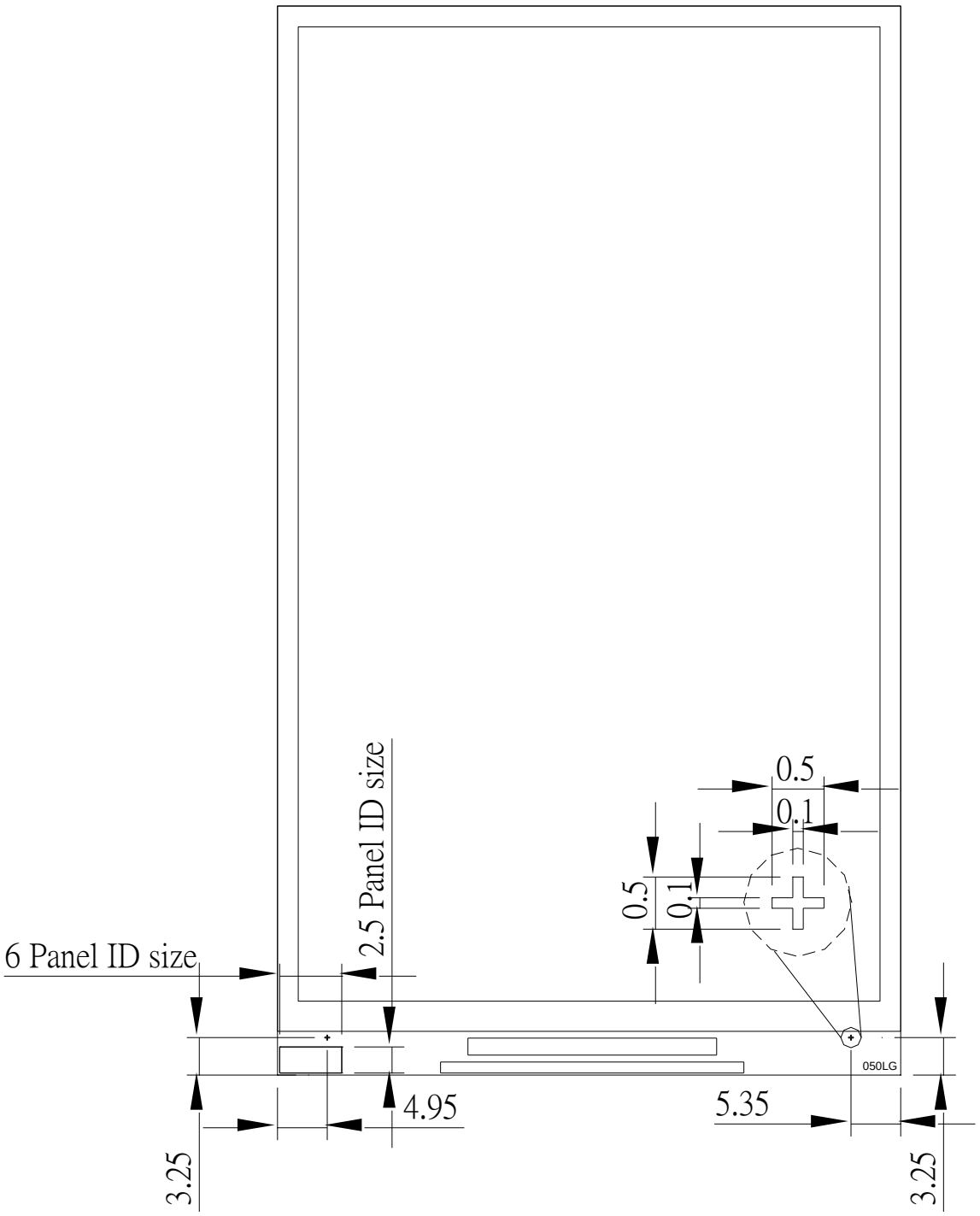
(unit = mm)




| No. | TEST PAD NAME | Note | No. | TEST PAD NAME | Note |
|---|---|---|---|---|---|
| 1 | VCOM | - | 14 | VCOM | - |
| 2 | D_R | P TEST | 15 | VGLTEST | GIP signal |
| 3 | SW | P TEST | 16 | RSTO | GIP signal |
| 4 | STVE | GIP signal | 17 | CK2BO | GIP signal |
| 5 | VGLE | GIP signal | 18 | CK2O | GIP signal |
| 6 | DIR1E | GIP signal | 19 | CK1BO | GIP signal |
| 7 | DIR2E | GIP signal | 20 | CK1O | GIP signal |
| 8 | CK1E | GIP signal | 21 | DIR2O | GIP signal |
| 9 | CK1BE | GIP signal | 22 | DIR1O | GIP signal |
| 10 | CK2E | GIP signal | 23 | VGLE | GIP signal |
| 11 | CK2BE | GIP signal | 24 | STVO | GIP signal |
| 12 | RSTE | GIP signal | 25 | D_B | P TEST |
| 13 | VCOM | - | 26 | D_G | P TEST |
| | | | 27 | VCOM | - |

5.4 Panel ID pad

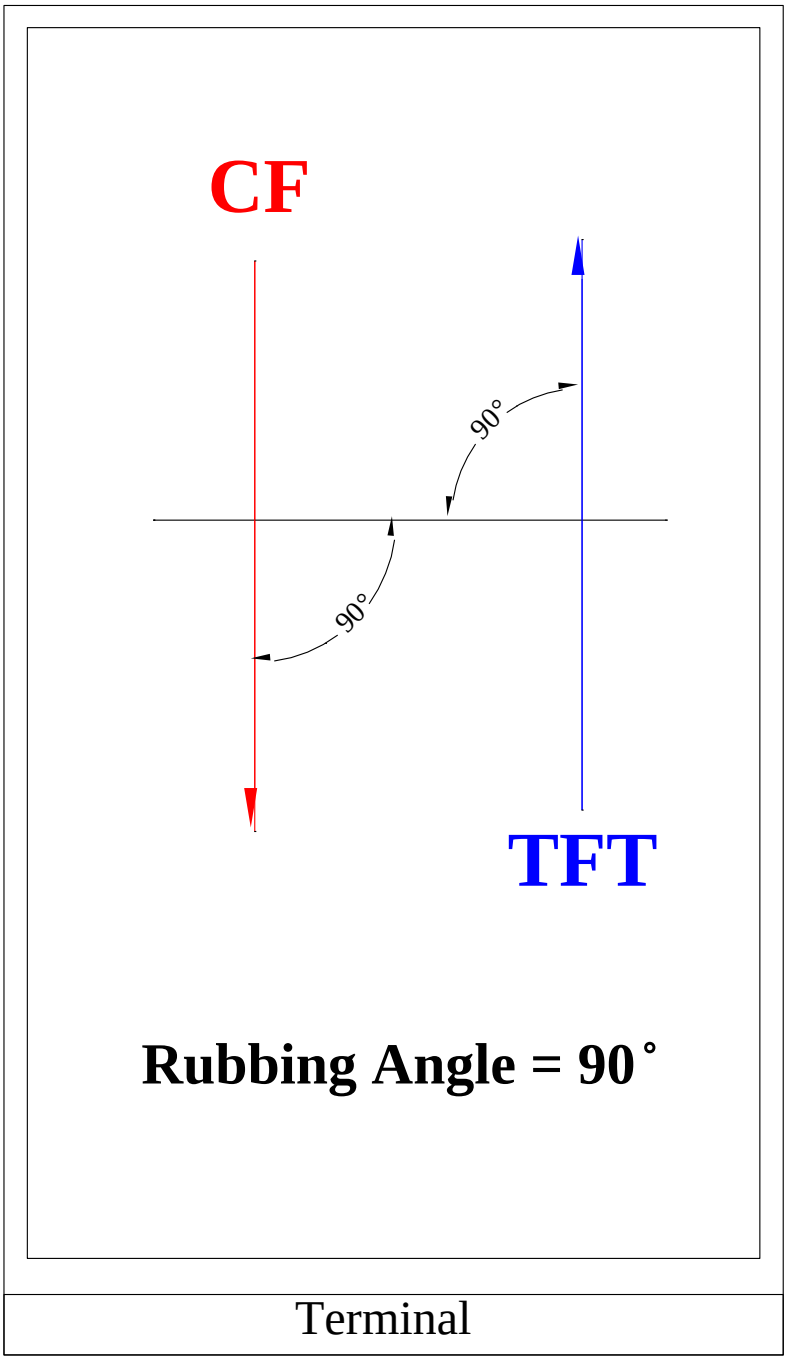
(unit = mm)



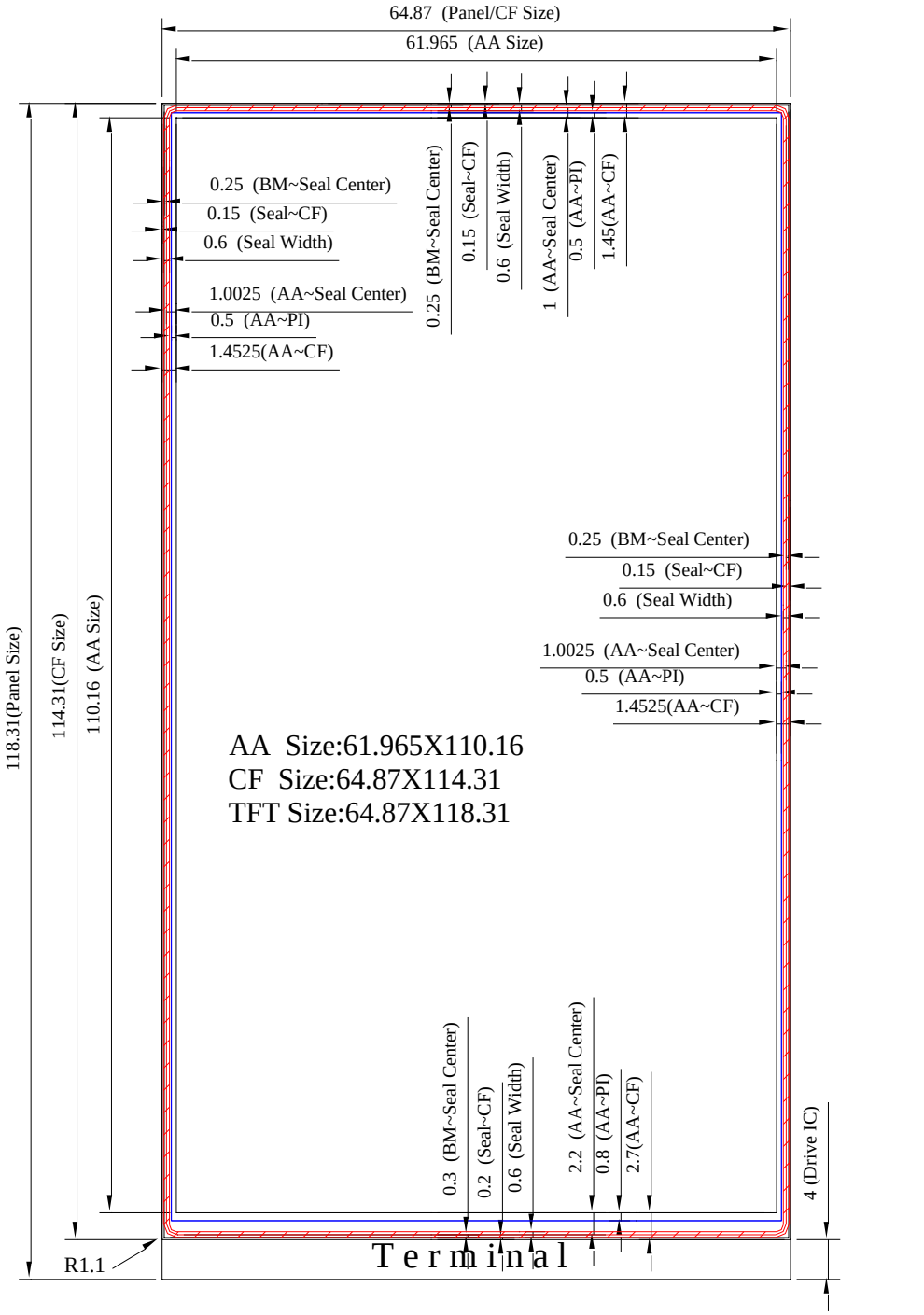
## 6. CELL PROCESS RULES

| Item | Specification |
|---|---|
| Cell gap | 3.6±0.2um |
| Assembly precision | ±4um |

6.1 Rubbing Direction



## 6.2 Seal & PI Pattern

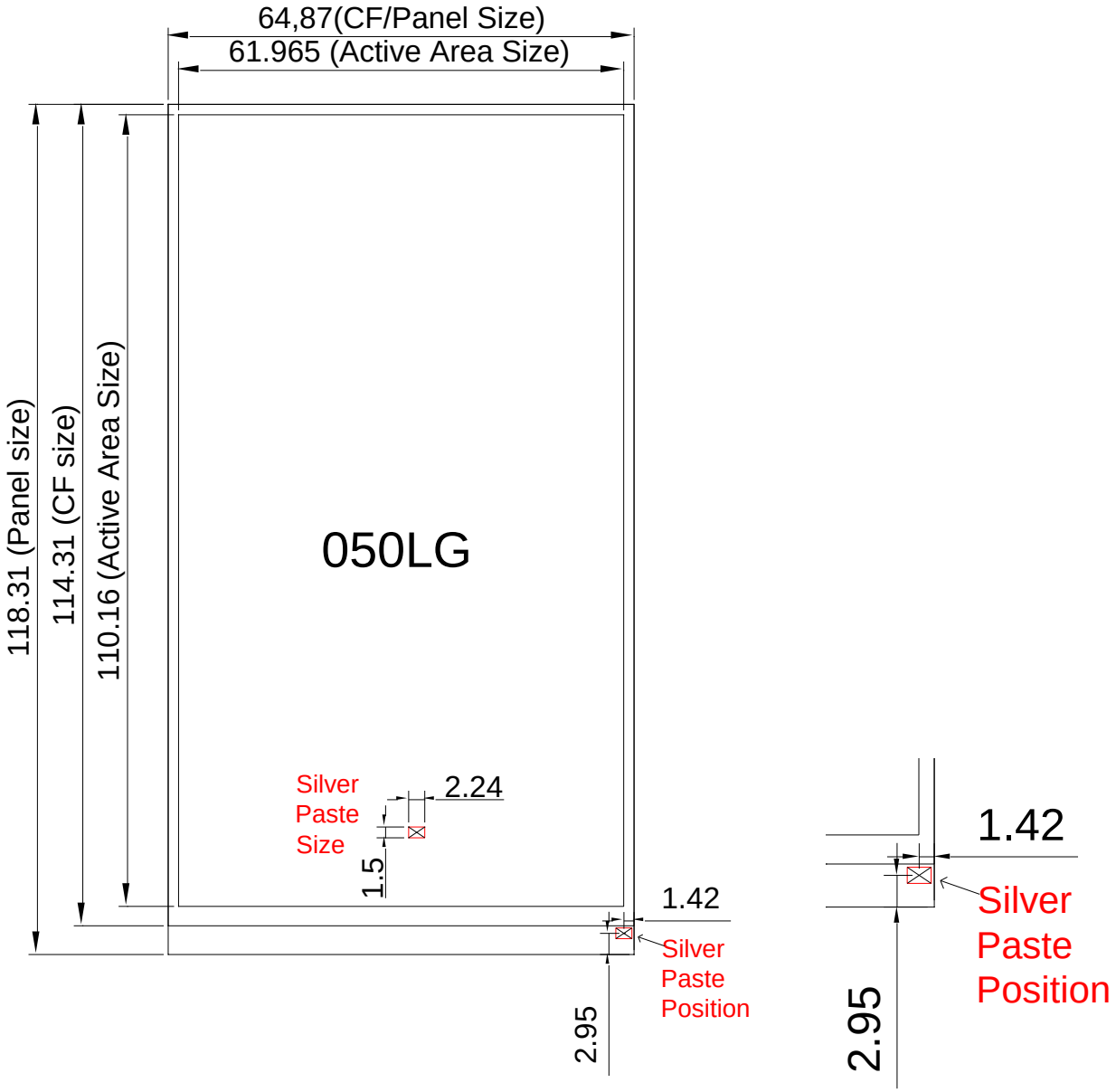



(unit = mm)

**Notes:**

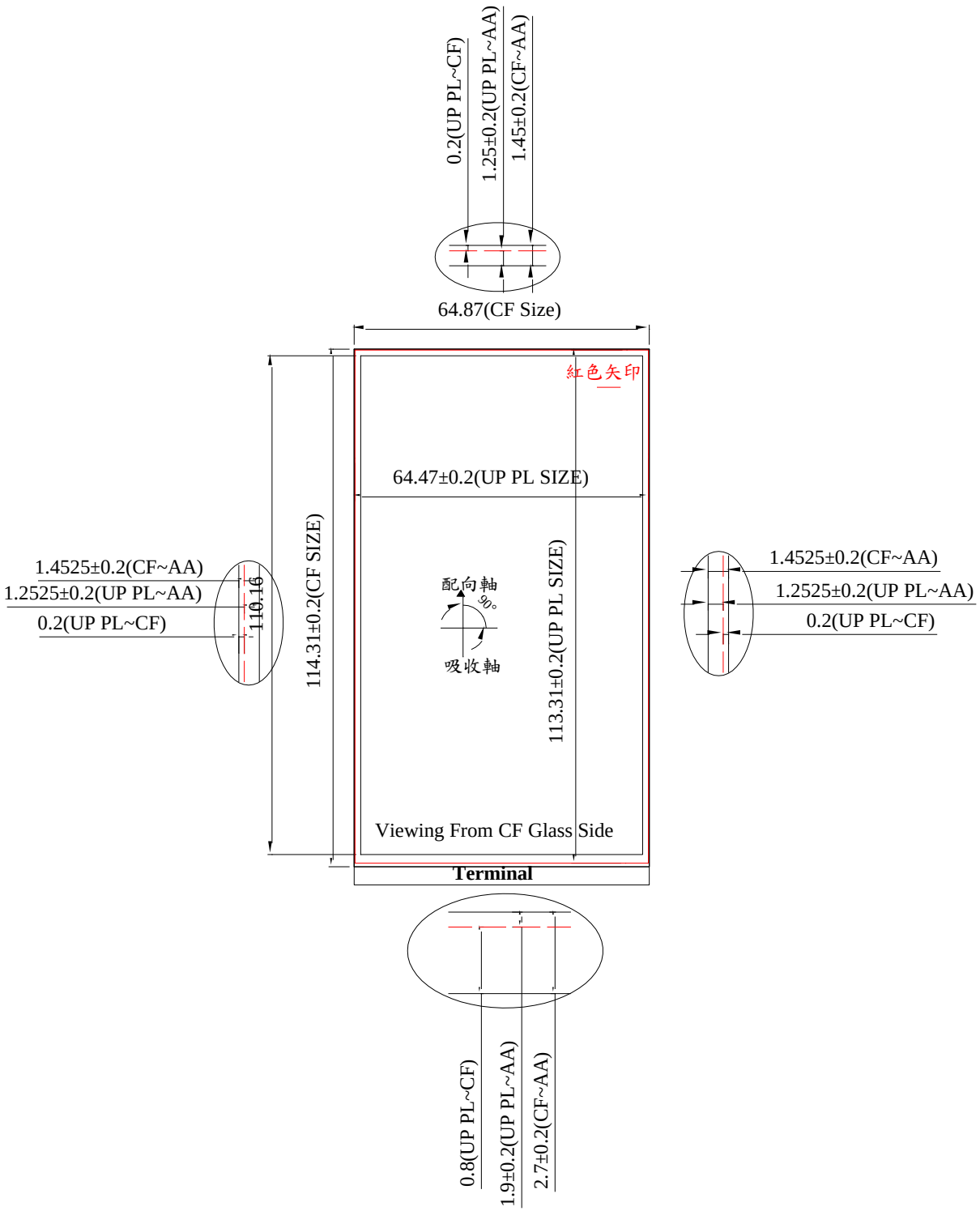
1. Seal width (Typ.) = 0.6±0.2mm
2. Seal center to CF edge = 0.45±0.2mm (面板左、右側)
   Seal center to CF edge = 0.45±0.2mm (面板上側)
   Seal center to CF edge = 0.5±0.2mm (面板下側)

6.3 Silver Paste Position

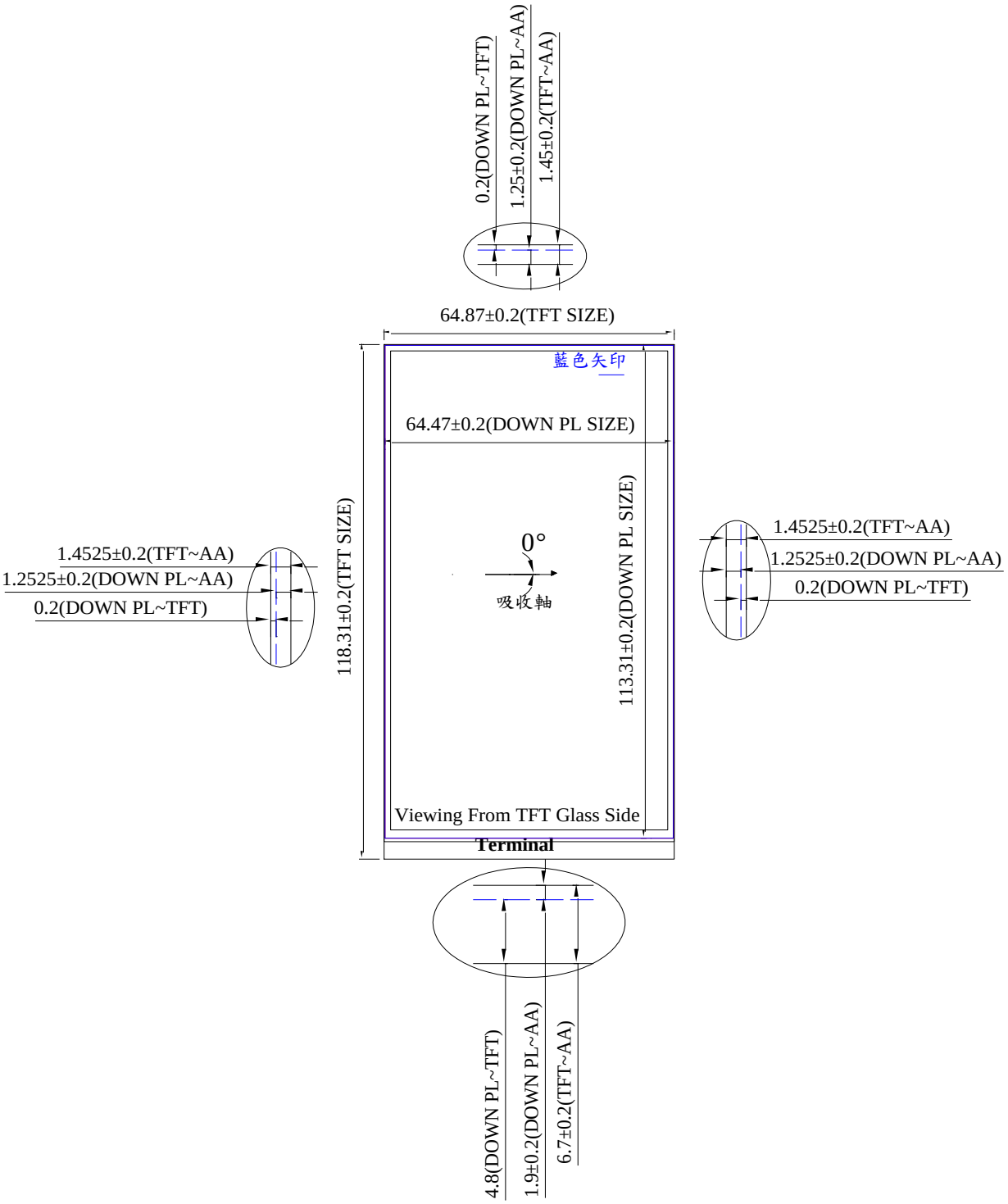


## 6.4 Polarizer Information

a. CF Side



b. TFT Side

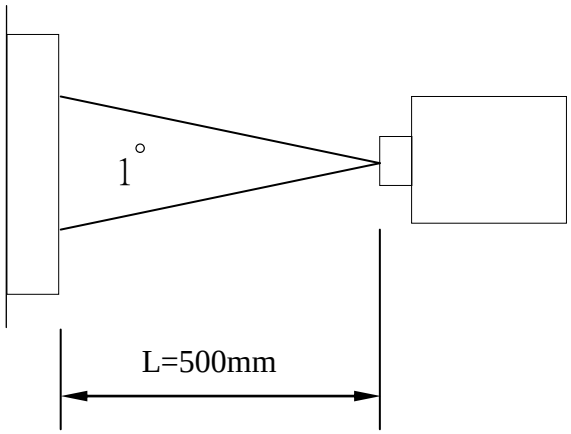



Up PL : HC **64.47 x 113.31 x 0.116mm**
Down PL : APCF **64.47 x 113.31x 0.136mm**
Up PL Thickness& Surface Treatment : 116um±20um HC
Down PL Thickness& Surface Treatment : 136um±20um APCF

# 7. OPTICAL SPECIFICATION

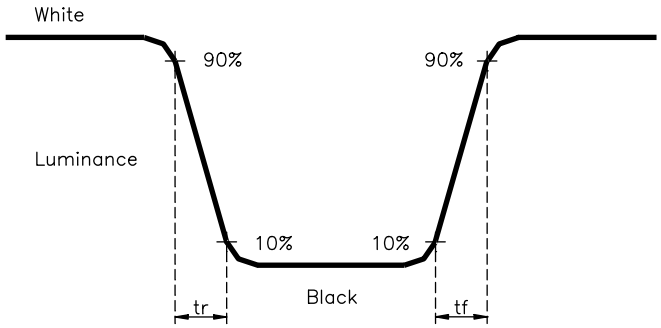
| ITEM | | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT | REMARK |
|---|---|---|---|---|---|---|---|---|
| Transmittance | | T | | 4.6 (W/ APCF) | 4.97 (W/ APCF) | | % | |
| Contrast Ratio | | CR | *1) | 500 | 800 | | - | Note 3 |
| Response Time | | Tr+ Tf | *3) | | - | 30ms | 40ms | Note 4 |
| Viewing Angle | U | θ*2) | - - - - | - | 85 | - | | Note 5 |
| | D | | | - | 85 | - | | |
| | L | ψ*2) | | - | 85 | - | | |
| | R | | | - | 85 | - | | |
| Color Filter Chromacicity | White | x<br>y<br>Y | θ = ϕ = 0° | 0.281 | 0.301 | 0.321 | | Note 6 |
| | | | | 0.299 | 0.319 | 0.339 | | |
| | | | | 28.98 | 29 | 29.02 | | |
| | Red | x<br>y<br>Y | θ = ϕ = 0° | 0.63 | 0.65 | 0.67 | | |
| | | | | 0.32 | 0.34 | 0.36 | | |
| | | | | 21.38 | 21.4 | 21.42 | | |
| | Green | x<br>y<br>Y | θ = ϕ = 0° | 0.258 | 0.278 | 0.298 | | |
| | | | | 0.582 | 0.602 | 0.622 | | |
| | | | | 52.78 | 52.8 | 52.82 | | |
| | Blue | x<br>y<br>Y | θ = ϕ = 0° | 0.119 | 0.139 | 0.159 | | |
| | | | | 0.084 | 0.104 | 0.124 | | |
| | | | | 12.68 | 12.7 | 12.72 | | |
| | NTSC | | | -- | 70% | - | | |

Note 1.Ambient condition：25℃±2℃，60±10%RH，under 10 Lunx in the darkroom。
Note 2.Measure device：BM-5A (TOPCON)，viewing cone=1°，$I_L$=20mA。

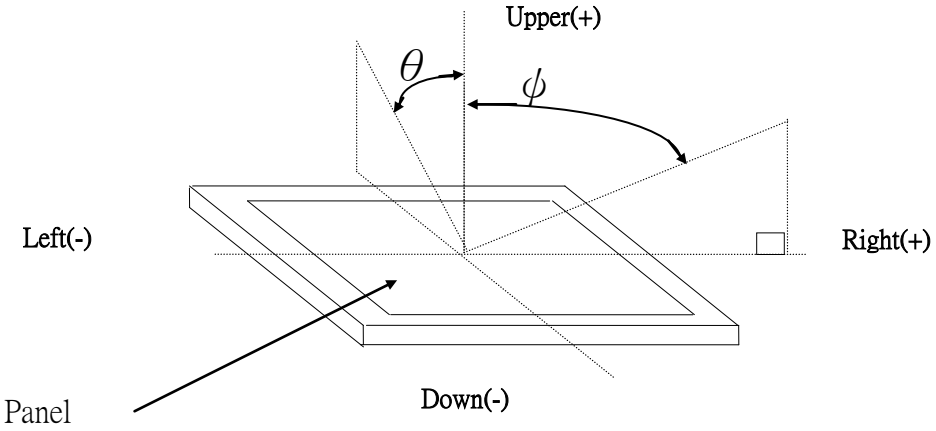



Note 3. Definition of Contrast Ratio：
CR = White Luminance (ON) / Black Luminance (OFF)

Note 4. Definition of response time：The response time is defined as the time interval between the 10% and 90% amplitudes.




Note 5. Definition of view angle(θ，ψ)：




Note 6. Light source: C light.

# 8. RELIABILITY TEST ITEM

| N0. | TEST ITEM | CONDITIONS |
|---|---|---|
| 1 | High Temperature and High Humidity Operation | 65°C, 90% RH, 240 hrs |
| 2 | High Temperature Operation | 70°C, 240 hrs |
| 3 | Low Temperature Operation | -20°C, 240 hrs |
| 4 | High Temperature Storage | 80°C, 240 hrs |
| 5 | Low Temperature Storage | -30°C, 240 hrs |
| 6 | Thermal Shock | -30℃(30min) ⇔ 80℃(30min)<br>200Cycles |

**NOTE**
1. All judgement of display are performed after temperature of panel return to room temperature.
2. Display function should be no change under normal operating condition.
3. Under no condensation of dew.
4. CPT only guarantee the above 8 test items, and without guarantee the others.

# 9. HANDLING PRECAUTIONS FOR EMPTY CELL

| Item | Min. | Max. | Unit | Remark |
|---|---|---|---|---|
| Storage Temperature | -26 | 20 | ˚C | |
| Storage Humidity | 50 | 58 | % (RH) | |
| Storage Time | — | 1 | month | |