CL-GD7548

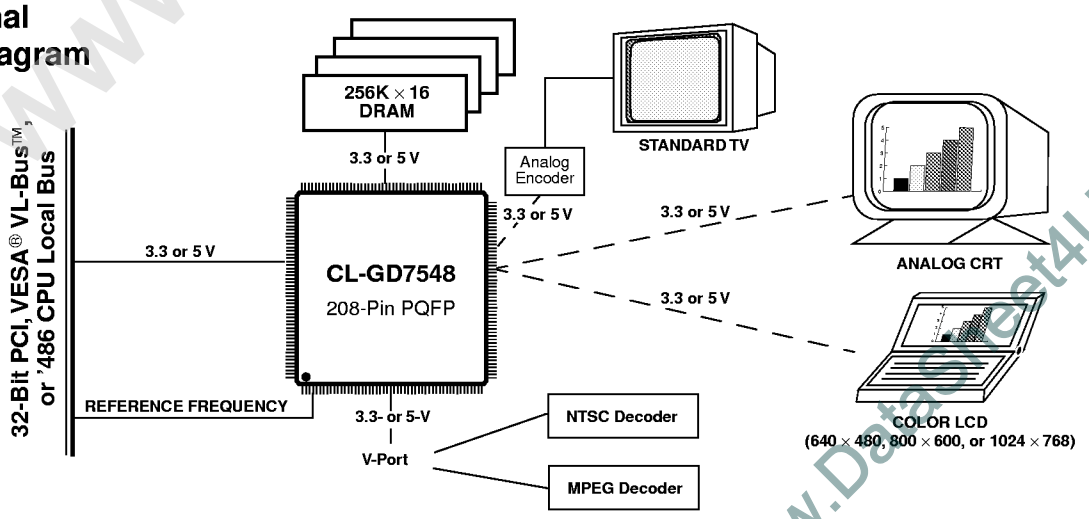
Advance Hardware Reference Manual

FEATURES

GUI-Accelerated XGA/SVGA LCD Controller with Low-Cost Multimedia Options from Enhanced MVA™

- **Single-chip XGA/Super VGA LCD controller**
  - — Pin-compatible superset of CL-GD7541/7543 SVGA LCD controllers
  - — IBM® VGA hardware-compatible
- **GUI acceleration**
  - — BitBLT engine (double-buffering, auto-start, memory-mapped I/O, and transparent BitBLT)
  - — Color expansion for 8- or 16-bit pixels
  - — True packed-pixel addressing for 4, 8, 16, and 24 bits per pixel
  - — Programmable linear memory addressing
  - — 32 × 32 or 64 × 64 hardware cursor
- **Cost-effective multimedia enhancements with 1-MByte DRAM**
  - — Enhanced MVA™ (Motion Video Acceleration™)
    - True-color, full-motion video playback
    - Mixed graphics/video color depths (multi-format frame accelerator)
    - Supports 4:2:2 YCrCb, RGB 5-5-5, and AccuPak (8-bit) color space formats
    - Integrated 4:2:2 YCrCb -to-RGB 8-8-8 color space converter
    - Up to 4X continuous horizontal/vertical upscaling
    - Full MVA™ support with TFT and STN color LCDs
  - — Dual apertures (video/graphics) with VESA® VL-Bus™ and PCI bus
  - — Interface to analog NTSC/PAL encoders for TV OUT
- **Cost-effective multimedia enhancements with 1-MByte DRAM** *(cont.)*
  - — Flexible V-Port™
    - 8-/16-bit V-Port™ connected to display memory
    - Single-chip live video solution with popular decoders (such as the Philips® SAA7110 or the CL-PX4072)
    - Two-chip MPEG solution (MPEG decoder and 256K × 16 DRAM)
    - 1024 × 768 video using AccuPak (live video and playback)
    - On-chip AccuPak: compression through V-Port™, decompression at display time
    - Low-cost multimedia solution through PCMCIA multimedia cards
    - Supports serial programming interface to popular decoders (video, audio, MPEG) through DDC-2b
    - Zoomed Video compliance with DCI 1.x and Windows® 95 DirectDraw™

Functional Block Diagram



FEATURES (cont.)

- **32-bit direct-connect CPU host bus interfaces**
  - — '486 CPU local bus (up to 50 MHz)
  - — VESA® VL-Bus™ @ 50-MHz bus clock
  - — PCI bus @ 33-MHz bus clock with burst support: big-endian byte-order hardware support for PowerPC™
- **64 × 64 pixel size hardware pop-up icons**
  - — Displays up to four independently controlled, 4-color icons
- **Scalable 1- and 2-Mbyte display memory**
  - — 32-bit-wide interface to display memory
  - — Two/four 256K × 16 DRAMs
  - — Four 512K × 8 DRAMs
  - — Optimized support for Extended Data-Out (Hyper-Page-Mode) DRAMs
- **Integrated programmable frequency synthesizer**
  - — VCLK up to 80 MHz at 5 V; 75 MHz at 3.3 V
  - — MCLK up to 66 MHz at 5 V; 54 MHz at 3.3 V
- **Integrated 24-bit true-color RAMDAC**
  - — Non-interlaced CRTs: 640 × 480 with 16M colors, 800 × 600 with 64K colors, or 1024 × 768 non-interlaced with 256 colors
  - — Interlaced CRTs: 1280 × 1024 with 256 colors
- **640 × 480 (VGA), 800 × 600 (SVGA), and 1024 × 768 (XGA) LCDs**
  - — Color TFT LCDs
    - 1-pixel/shift clock (9-, 12-, 18-, and 24-bit interfaces)
    - 2-pixel/shift clock with external multiplexor (18- and 24-bit interfaces)
  - — Dual-scan color STN LCDs (640 × 480 and 800 × 600)
  - — Dithering algorithm automatically adds up to 6 bits per primary color without decreasing spatial resolution
  - — Enhanced frame-rate modulation algorithm improves display quality with fast-response STN LCDs
  - — Hardware expansion to 800 × 600 with lower-resolution VGA modes
  - — SimulSCAN™ (simultaneous CRT and LCD)
- **Power-management capabilities**
  - — 3.3-V, 5.0-V, and mixed-voltage operation
  - — VESA® DPMS (Display Power Management Signaling)
  - — DDC-1 and DDC-2b (Display Data Channel) support
- **EIAJ standard 208-pin plastic quad flat package**

OVERVIEW

The CL-GD7548 GUI-accelerated SVGA LCD controller with MVA (Motion Video Acceleration) provides an extremely flexible, high-quality, cost-effective multimedia option for the next generation of mid-range to premium portable computers.

With its enhanced BitBLT GUI acceleration, continuous upscaling for 1024 × 768 and 800 × 600 LCDs, true-color capability, and mixed-voltage operation for low power consumption, the CL-GD7548 delivers exceptional graphics/video performance.

The CL-GD7548 V-Port enables high-quality, low-cost multimedia options such as a single-chip NTSC/PAL video decoder or MPEG decoder by eliminating the need for an additional video frame buffer and providing a dedicated path to a PCMCIA card. The CL-GD7548 V-Port is fully Zoomed Video compliant. A complete graphics subsystem can be built with only three active components: the CL-GD7548 and two 256K × 16 DRAMs

The CL-GD7548 fully supports all features of the CL-GD7543, including MVA™ for playback of MPEG or Video for Windows .AVI (audio-video interleaved) files.

UNIQUE FEATURES

BENEFITS

High Performance

- BitBLT engine, color expansion, hardware cursor, linear addressing, and 32-bit memory interface
  - ❒ Accelerates GUIs such as Microsoft® Windows®; provides high resolution and color-depth capabilities.
- BitBLT double-buffering, auto-start, and memory-mapped I/O
  - ❒ Reduced BLT setup, overlapped execution, more efficient Windows® GDI (graphical device interface) software.
- BitBLT with transparency
  - ❒ Accelerates games.
- 32-bit local bus interfaces operating up to 50 MHz
  - ❒ Increases system throughput; PCI interface allows use in 'X86, PowerPC™, or other platforms.
- Hardware 'pop-up' icons
  - ❒ Provides hot-key display for on-screen symbols such as battery 'fuel gauge' and contrast/brightness controls.

Multimedia and MVA™

- MVA™ (Motion Video Acceleration™)
  - ❒ Hardware enhancement for playback of files that are compatible with the DCI (Display Control Interface) and DirectDraw™ standard.
- Multi-format frame buffer
  - ❒ Displays separate graphics and video windows at independent color depths. Maintains high rate of video playback without degrading performance.
- Dual independent apertures: one for graphics and one for video
  - ❒ A BitBLT operation in Microsoft® Windows® can be in progress while live video data is being simultaneously shown through the secondary aperture.
- Interface to CL-PX4072 video pixel decoder requires no external logic
  - ❒ Allows capability for live 'TV in a window' at real-time speeds.
- 8 or 16-bit V-Port to display memory
  - ❒ Eliminates external video frame buffer and additional hardware; enables low-cost multimedia add-in PCMCIA cards.
  - ❒ V-Port clock rate decoupled from display clock rate.
- 8-bit Overlay Port; video data overlay for display
  - ❒ Enables external hardware to support occlusion.
  - ❒ Overlay regions defined with internal window registers and/or color keys.
- Interface to NTSC/PAL analog encoders
  - ❒ Integrated design can be developed to display computer-generated data on a TV or to record to a VCR.
- AccuPak™ compression and decompression logic on-chip
  - ❒ 2:1 reduction in storage and data rate requirements over 16-bpp formats.

Enhanced LCD Support

- 1024 × 768 LCD support (TFT)
  - ❒ 2-pixel/shift clock external multiplexor.
  - ❒ Up to 800 × 600 hardware expansion for lower-resolution modes.
- 800 × 600 LCD support (both TFT and dual-scan STN) with comprehensive hardware resolution-compensation support
  - ❒ Enables full use of the display area whether in graphics or text mode.
- Enhanced frame-rate modulation
  - ❒ Improves display quality; increases stability of shades for dual-scan STNs.
- Intelligent dithering algorithm expands the number of input bits per primary color (RGB) on TFT or STN LCDs
  - ❒ Displays high- and true-color modes with smooth shading (no contouring) on all supported LCD types.

Power Management

- 3.3-V, 5.0-V, or mixed-voltage support
  - ❒ Minimizes operating power consumption; provides manufacturing flexibility.
- Hardware-initiated Standby and Suspend modes and VESA® DPMS support for CRTs
  - ❒ Reduces power consumption; supports Energy Star monitors for 'green PC' compliance.

Software

- Complete suite of drivers for multiple operating systems
  - ❒ Supports all popular application environments.
- User-friendly utilities
  - ❒ Enables fast and on-the-fly changes.

SOFTWARE SUPPORT

Operating System and Application Software Drivers

Software Drivers[a]	Resolution Supported	Number of Colors
Microsoft®/Intel® DCI™ v1.x	640 × 480, 800 × 600, 1024 × 768	256
Microsoft® Windows® v3.1 Microsoft® Windows® 95™ Microsoft® Windows® 95™ with DirectDraw™ Cirrus Logic VPM (Video Port Manager)	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024 640 × 480, 800 × 600 640 × 480	256 65,536 16 million
Microsoft® Windows NT™ v3.5	640 × 480, 800 × 600, 1024 × 768	16 and 256
OS/2® v2.0, WARP 3.0	640 × 480, 800 × 600, 1024 × 768 640 × 480, 800 × 600 640 × 480	16 and 256 65,536 16 million
AutoCAD® v11, v12	640 × 480, 800 × 600, 1024 × 768 640 × 480, 800 × 600 640 × 480	16 and 256 65,536 16 million
Autoshade® v2.0 3D Studio® v1, v2	640 × 480, 800 × 600, 1024 × 768 640 × 480, 800 × 600 640 × 480	256 65,536 16 million

[a] Driver support for additional applications is provided by independent software vendors, either with specific drivers or through VESA mode support. For more information concerning driver support, contact the software manufacturer.

BIOS

Feature	*Benefit*
■ 48-Kbyte BIOS	❒ Provides optimum performance with VGA and VESA® extended mode support ❒ Provides system design options for the best combination of performance and functionality.
■ Fully IBM® VGA-compatible BIOS	❒ Compatible with the existing base of PC applications.
■ VESA® VBE (VGA BIOS extensions) 1.2 and PM (power management) support	❒ Compatible with industry standards for extended mode support beyond VGA and power-management control.

Software Utilities

Utility	Function
AutoResolution Switching	Windows® application for automatically switching display resolutions (for example, from a 1024 × 768 CRT to lower-resolution 640 × 480 or 800 × 600 LCDs) without relaunching Windows
CLMode	Video mode and video display configuration utility suitable for end-use distribution (includes foreign language translations)
OEMSI	BIOS-customization utility for OEM development use
PCLRegs	VGA controller register viewer/editor for OEM development use
V-Port Regs	Windows®-based register viewer/editor and V-Port/Video Window display configuration utility for OEM development use
WinMode	Windows® application for graphics mode and display type configuration (includes foreign language translations, selectable from within the utility)

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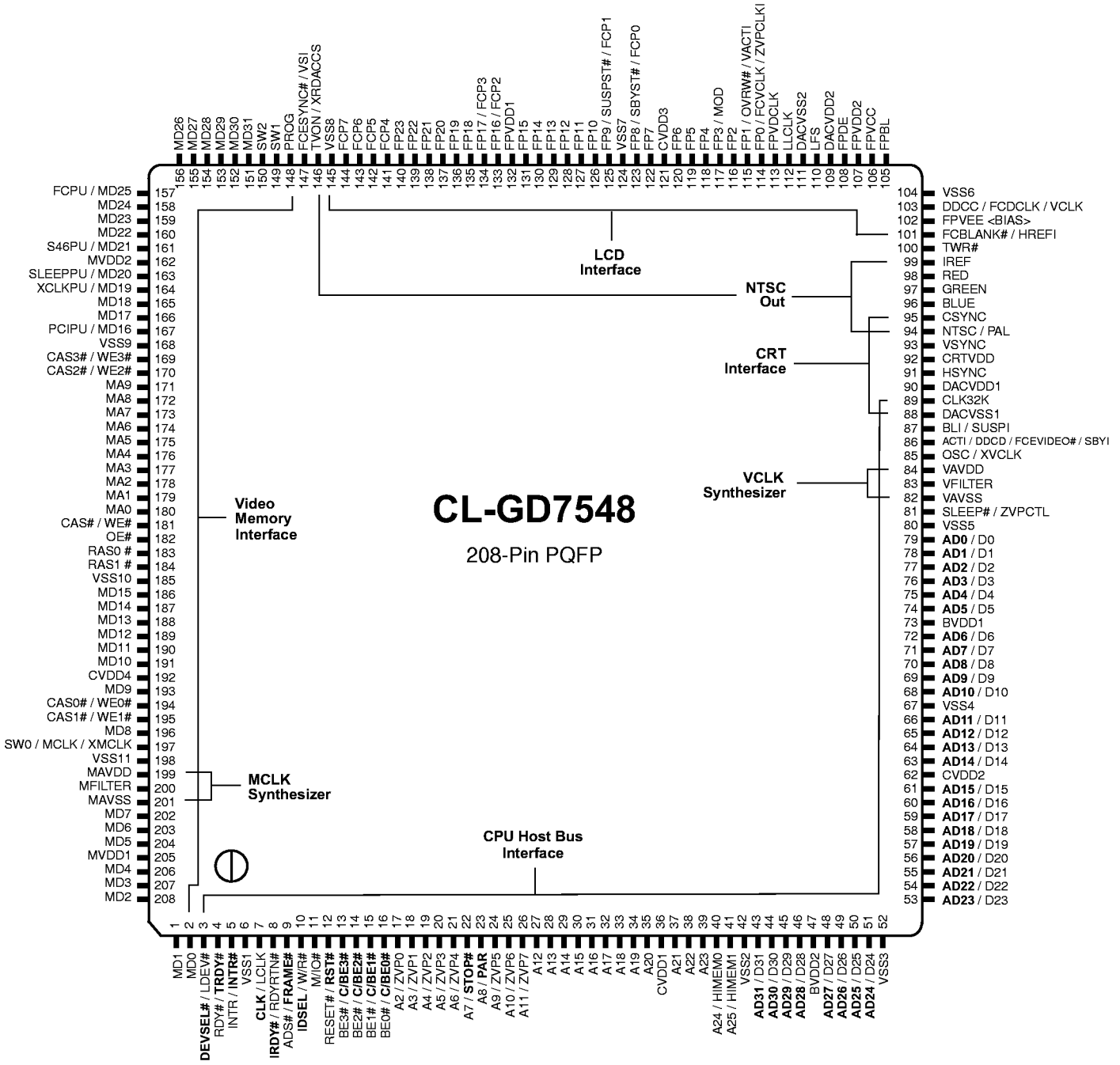
Appendices

1. PIN INFORMATION

1.1 Pin Diagram



NOTE: Pin names that are in bold print indicate pins that are used for PCI bus configuration.

Figure 1-1. Pin Diagram

1.2 Pin Tables

In the table that follows:

- Pin names that are in bold print indicate pins that are used for PCI bus configuration.
- Pin numbers with an asterisk (*) have pull-up options, discussed in Section 2.7, "Configuration Input Pins".

Table 1-1. CL-GD7548 Pins in Numerical Order

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	MD1	37	A21	73	BVDD1
2	MD0	38	A22	74	**AD5** / D5
3	**DEVSEL#** / LDEV#	39	A23	75	**AD4** / D4
4	RDY# / **TRDY#**	40	A24 / HIMEM0	76	**AD3** / D3
5	INTR / **INTR#**	41	A25 / HIMEM1	77	**AD2** / D2
6	VSS1	42	VSS2	78	**AD1** / D1
7	**CLK** / LCLK	43	**AD31** / D31	79	**AD0** / D0
8	**IRDY#** / RDYRTN#	44	**AD30** / D30	80	VSS5
9	ADS# / **FRAME#**	45	**AD29** / D29	81	SLEEP# / ZVPCTL
10	**IDSEL** / W/R#	46	**AD28** / D28	82	VAVSS
11	M/IO#	47	BVDD2	83	VFILTER
12	RESET# / **RST#**	48	**AD27** / D27	84	VAVDD
13	BE3# / **C/BE3#**	49	**AD26** / D26	85	OSC / XVCLK
14	BE2# / **C/BE2#**	50	**AD25** / D25	86	ACTI / DDCD / FCEVIDEO# / SBYI
15	BE1# / **C/BE1#**	51	**AD24** / D24	87	BLI / SUSPI
16	BE0# / **C/BE0#**	52	VSS3	88	DACVSS1
17	A2 / ZVP0	53	**AD23** / D23	89	CLK32K
18	A3 / ZVP1	54	**AD22** / D22	90	DACVDD1
19	A4 / ZVP2	55	**AD21** / D21	91	HSYNC
20	A5 / ZVP3	56	**AD20** / D20	92	CRTVDD
21	A6 / ZVP4	57	**AD19** / D19	93	VSYNC
22	A7 / **STOP#**	58	**AD18** / D18	94	NTSC / PAL
23	A8 / **PAR**	59	**AD17** / D17	95	CSYNC
24	A9 / ZVP5	60	**AD16** / D16	96	BLUE
25	A10 / ZVP6	61	**AD15** / D15	97	GREEN
26	A11 / ZVP7	62	CVDD2	98	RED
27	A12	63	**AD14** / D14	99	IREF
28	A13	64	**AD13** / D13	100	TWR#
29	A14	65	**AD12** / D12	101	FCBLANK# / HREFI
30	A15	66	**AD11** / D11	102	FPVEE <BIAS>
31	A16	67	VSS4	103	DDCC / FCDCLK / VCLK
32	A17	68	**AD10** / D10	104	VSS6
33	A18	69	**AD9** / D9	105	FPBL
34	A19	70	**AD8** / D8	106	FPVCC
35	A20	71	**AD7** / D7	107	FPVDD2
36	CVDD1	72	**AD6** / D6	108	FPDE

Table 1-1. CL-GD7548 Pins in Numerical Order *(cont.)*

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
109	DACVDD2	143	FCP6	177	MA3
110	LFS	144	FCP7	178	MA2
111	DACVSS2	145	VSS8	179	MA1
112	LLCLK	146	TVON / XRDACCS	180	MA0
113	FPVDCLK	147	FCESYNC# / VSI	181	CAS# / WE#
114	FP0 / FCVCLK / ZVPCLKI	148	PROG	182	OE#
115	FP1 / OVRW# / VACTI	149	SW1	183	RAS0 #
116	FP2	150	SW2	184	RAS1#
117	FP3 / MOD	151	MD31	185	VSS10
118	FP4	152	MD30	186	MD15
119	FP5	153	MD29	187	MD14
120	FP6	154	MD28	188	MD13
121	CVDD3	155	MD27	189	MD12
122	FP7	156	MD26	190	MD11
123	FP8 / SBYST# / FCP0	157*	MD25 / FCPU	191	MD10
124	VSS7	158	MD24	192	CVDD4
125	FP9 / SUSPST# / FCP1	159	MD23	193	MD9
126	FP10	160	MD22	194	CAS0# / WE0#
127	FP11	161*	MD21 / S46PU	195	CAS1# / WE1#
128	FP12	162	MVDD2	196	MD8
129	FP13	163*	MD20 / SLEEPPU	197	SW0 / MCLK / XMCLK
130	FP14	164*	MD19 / XCLKPU	198	VSS11
131	FP15	165	MD18	199	MAVDD
132	FPVDD1	166*	MD17	200	MFILTER
133	FP16 / FCP2	167*	MD16 / PCIPU	201	MAVSS
134	FP17 / FCP3	168	VSS9	202	MD7
135	FP18	169	CAS3# / WE3#	203	MD6
136	FP19	170	CAS2# / WE2#	204	MD5
137	FP20	171	MA9	205	MVDD1
138	FP21	172	MA8	206	MD4
139	FP22	173	MA7	207	MD3
140	FP23	174	MA6	208	MD2
141	FCP4	175	MA5		
142	FCP5	176	MA4		

Table 1-2 lists the CL-GD7548 pins that connect through a DB-44 connector to corresponding pins of LCD flat panels. In Table 1-2, the following abbreviations are used:

- (O) indicates pin type is an output function

Table 1-2. CL-GD7548 Interface Pins to LCD Flat Panels

CL-GD7548			DB-44 Connector	LCD Flat Panel Type – Corresponding Pins					
Pin No.	Pin Name (Only Flat Panel Function Names)	Pin Type	Pin No.	TFT LCD Types				STN LCD Types Color	
				24-Bit	18-Bit	12-Bit	9-Bit	16-Bit	8-Bit
140	FP23	O	13	R7	R5	R3	R2	SUD3	—
139	FP22	O	14	R6	R4	R2	R1	SUD2	—
138	FP21	O	15	R5	R3	R1	R0	SUD1	—
137	FP20	O	16	R4	R2	R0	—	SUD0	—
136	FP19	O	9	R3	R1	—	—	SUD7	—
135	FP18	O	10	R2	R0	—	—	SUD6	—
134	FP17	O	44	R1	—	—	—	—	—
133	FP16	O	42	R0	—	—	—	—	—
131	FP15	O	8	G7	G5	G3	G2	SLD7	SUD3
130	FP14	O	7	G6	G4	G2	G1	SLD6	SUD2
129	FP13	O	6	G5	G3	G1	G0	SLD5	SUD1
128	FP12	O	5	G4	G2	G0	—	SLD4	SUD0
127	FP11	O	11	G3	G1	—	—	SUD5	—
126	FP10	O	12	G2	G0	—	—	SUD4	—
125	FP9	O	20	G1	—	—	—	—	—
123	FP8	O	29	G0	—	—	—	—	—
122	FP7	O	4	B7	B5	B3	B2	SLD3	SLD3
120	FP6	O	3	B6	B4	B2	B1	SLD2	SLD2
119	FP5	O	2	B5	B3	B1	B0	SLD1	SLD1
118	FP4	O	1	B4	B2	B0	—	SLD0	SLD0
117	FP3 / MOD	O	23	B3	B1	—	—	MOD	MOD
116	FP2	O	39	B2	B0	—	—	—	—
115	FP1	O	43	B1	—	—	—	—	—
114	FP0	O	24	B0	—	—	—	—	—
113	FPVDCLK	O	18	FPVDCLK				SCLK	SCLK
112	LLCLK	O	35	LLCLK				LP	LP
110	LFS	O	22	LFS				FLM	FLM
108	FPDE	O	26	DE				—	—

NOTE: Pin numbers and names for specific LCDs are given in the "Panel Interface Guide" in the *CL-GD754X Application Book*.

Table 1-3 lists the power connections for the CL-GD7548 interface pin groups. For design flexibility and to minimize overall power consumption, each of the CL-GD7548 interface pin groups listed below may receive either +3.3 or 5 V from independent sources.

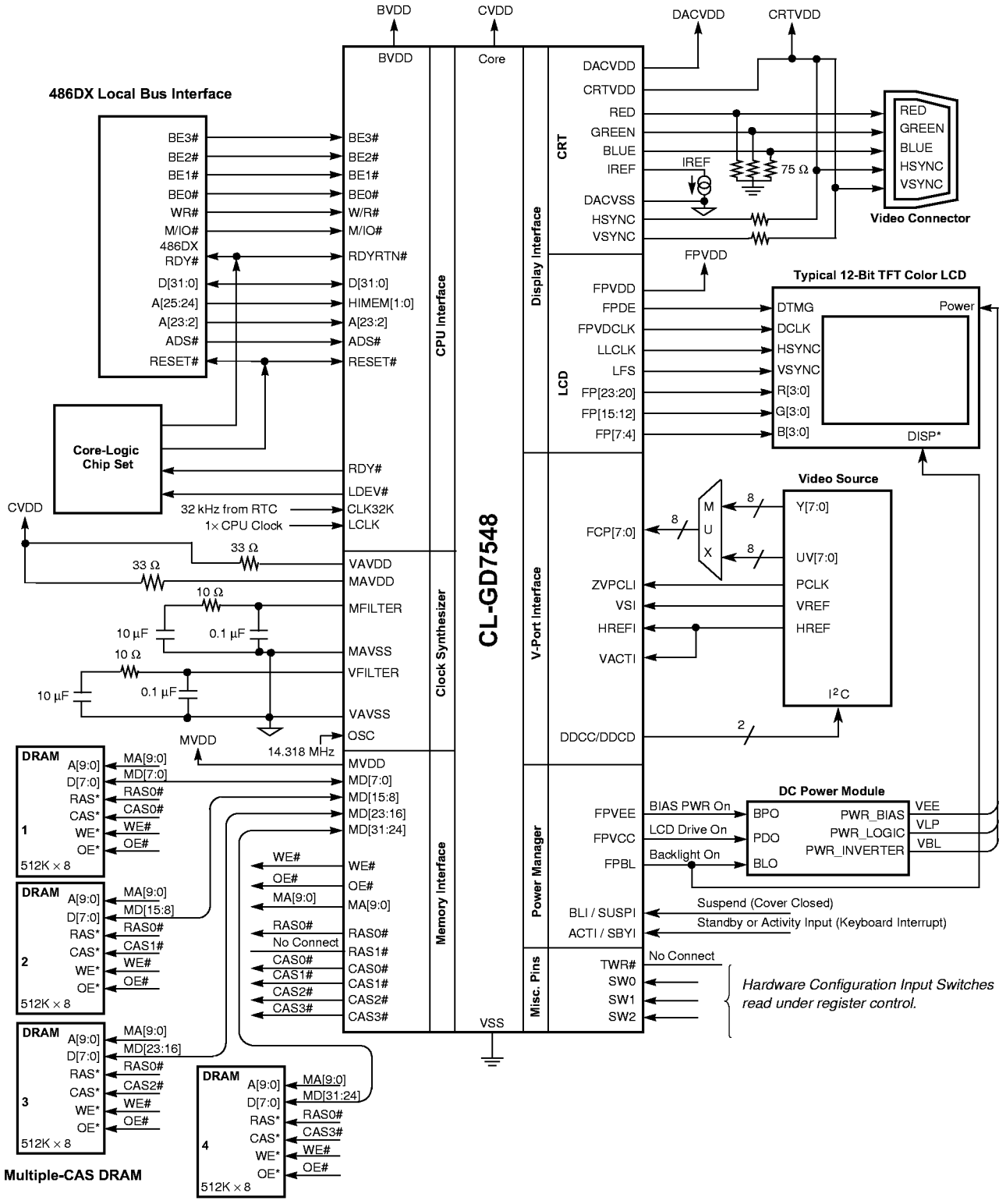
Table 1-3. Power Connections for Interface Pin Groups

Name of Interface Pin Group	Power Pin to Interface Pin Group		CL-GD7548 Pins in Interface Pin Group
	Power Pin Name	Power Pin Number	
Clock Frequency Synthesizer:			
MCLK (Memory Clock) Frequency Synthesizer	MAVDD*	199	197, 199–201
VCLK (Video Clock) Frequency Synthesizer	VAVDD*	84	82–85, 89
Core Logic	CVDD1*	36	6, 36, 42, 52, 62, 67, 80, 100, 104, 121, 145, 149, 150, 168, 185, 192, 198
	CVDD2*	62	
	CVDD3*	121	
	CVDD4*	192	
CPU Host Bus	BVDD1	73	3–5, 7–35, 37–41, 43–51, 53–61, 63–66, 68–79, 81
	BVDD2	47	
CRT	CRTVDD	92	88, 91–99, 111, 146
CRT: NTSC (and PAL)	CRTVDD	92	94–98, 146
Digital-to-Analog (RAMDAC)	DACVDD1*	90	90, 109
	DACVDD2*	109	
LCD	FPVDD1	132	86, 87, 101–103, 105–108, 110, 112–120, 122–123, 125–144, 147, 148
	FPVDD2	107	
Video Memory	MVDD1	205	1, 2, 151–167, 169–184, 186–191, 193–196, 202–208
	MVDD2	162	

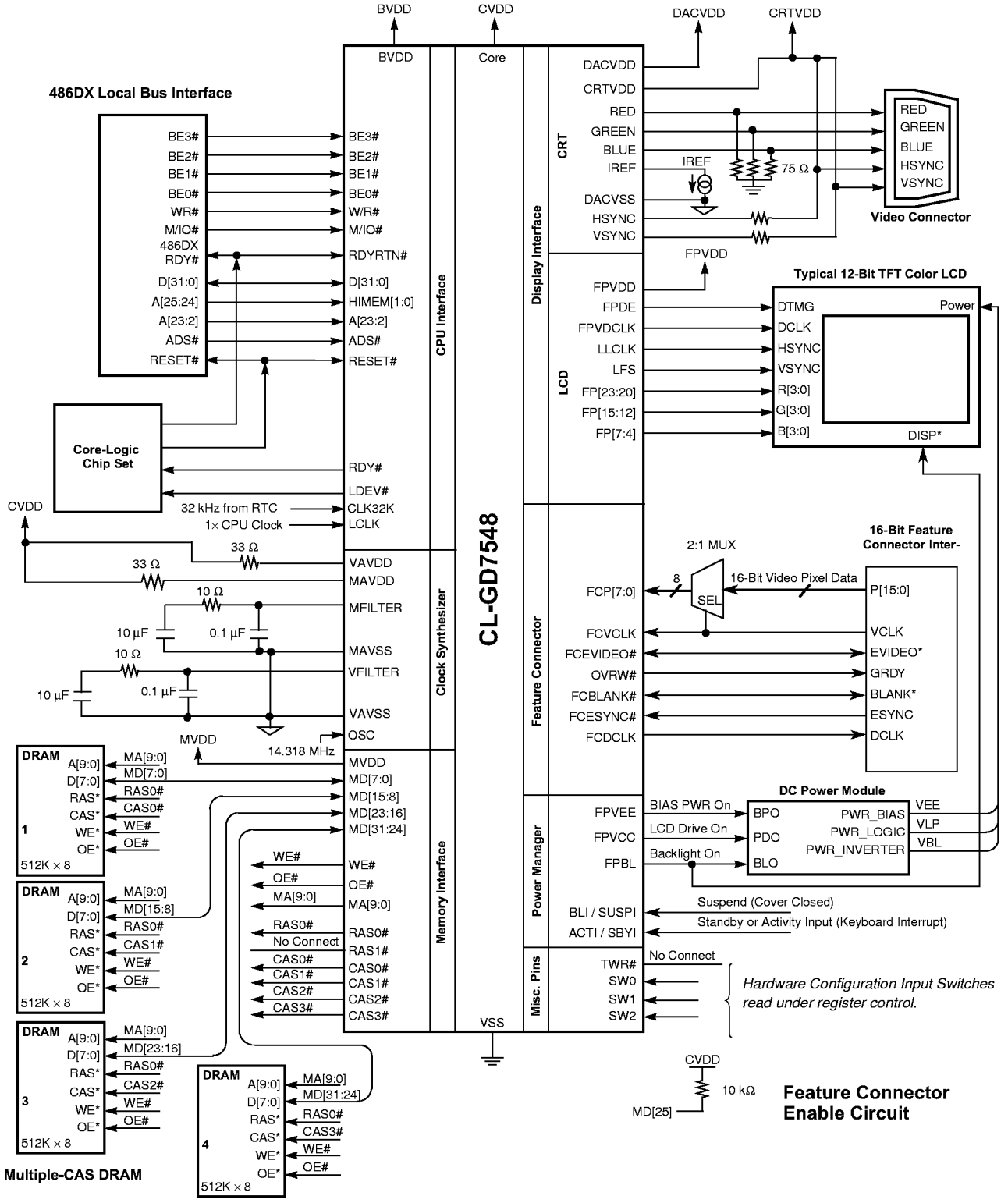
* Pin names that have asterisks indicate pins that must all be set to the same voltage level.

1.3 Block Diagrams: CL-GD7548 Interfaces

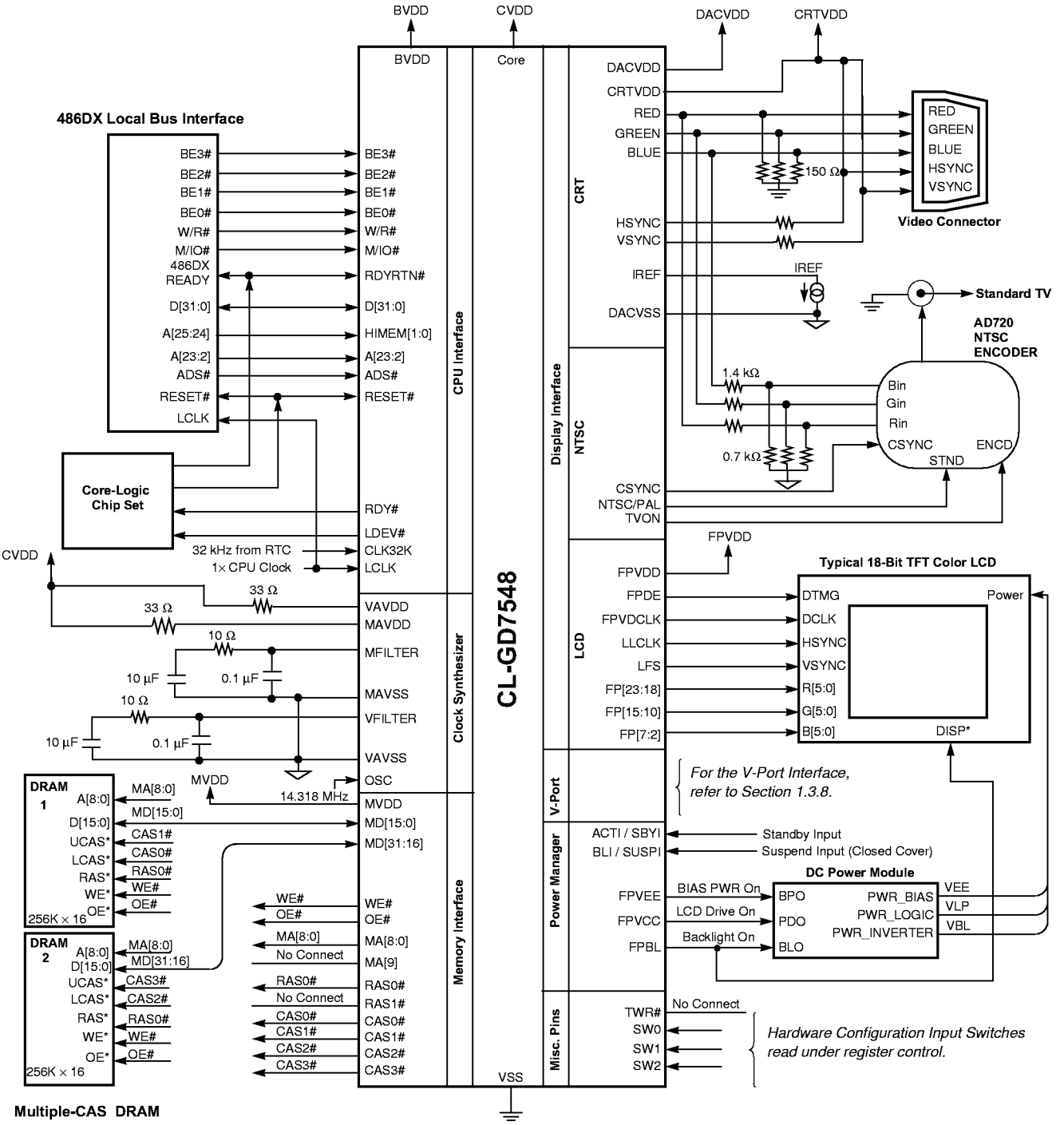
1.3.1 Local Bus (32-Bit '486DX or VESA® VL-Bus™), 2-Mbyte 512K × 8 DRAM, 12-Bit TFT Color, V-Port™ Interface



1.3.2 Local Bus (32-Bit '486DX or VESA® VL-Bus™), 2-Mbyte 512K × 8 DRAM, 12-Bit TFT Color, Feature Connector Interface



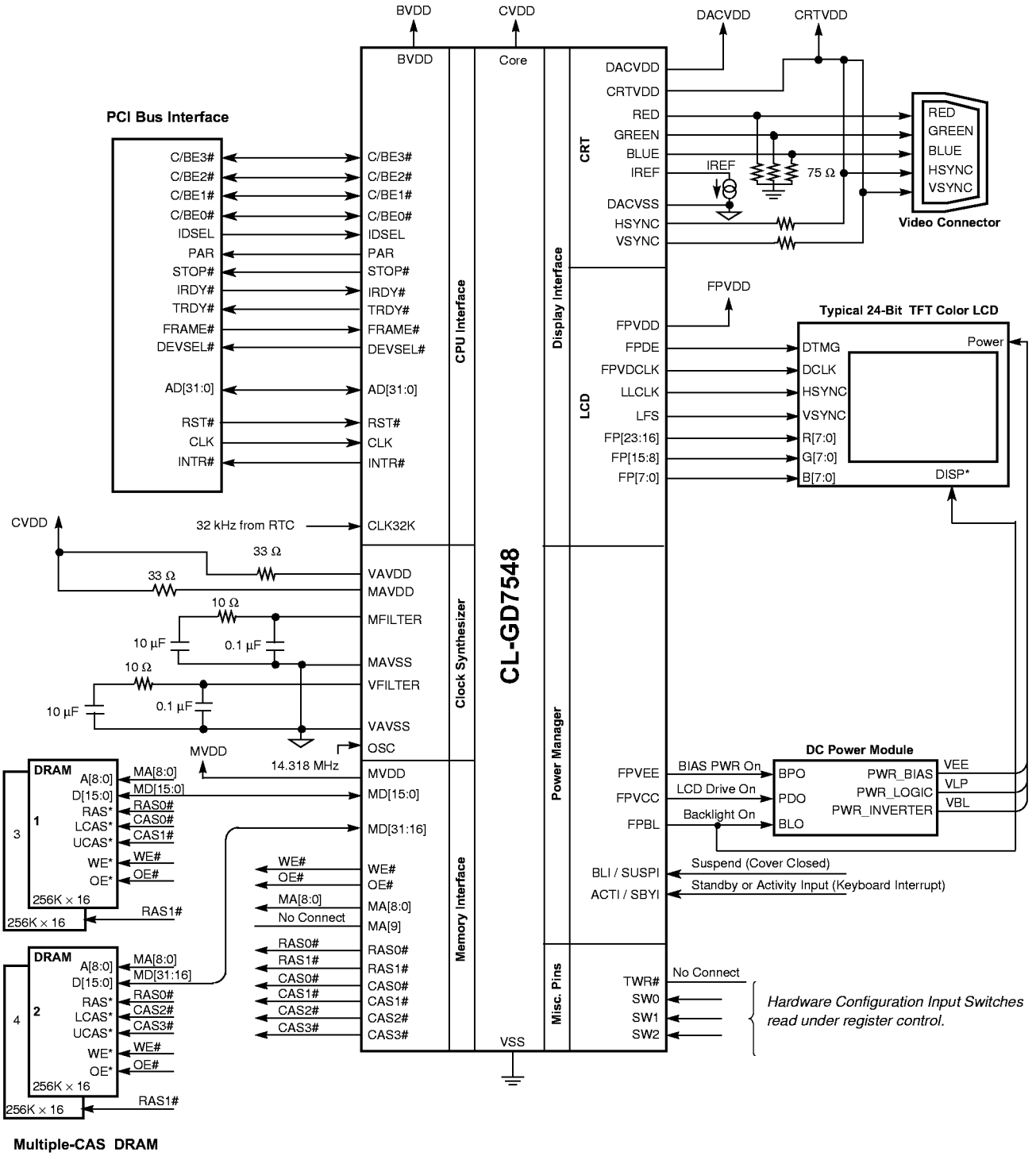
1.3.3 Local Bus (32-Bit '486DX or VESA® VL-Bus™), 1-Mbyte 256K × 16 DRAM, 18-Bit TFT Color, NTSC Output, V-Port™ Interface



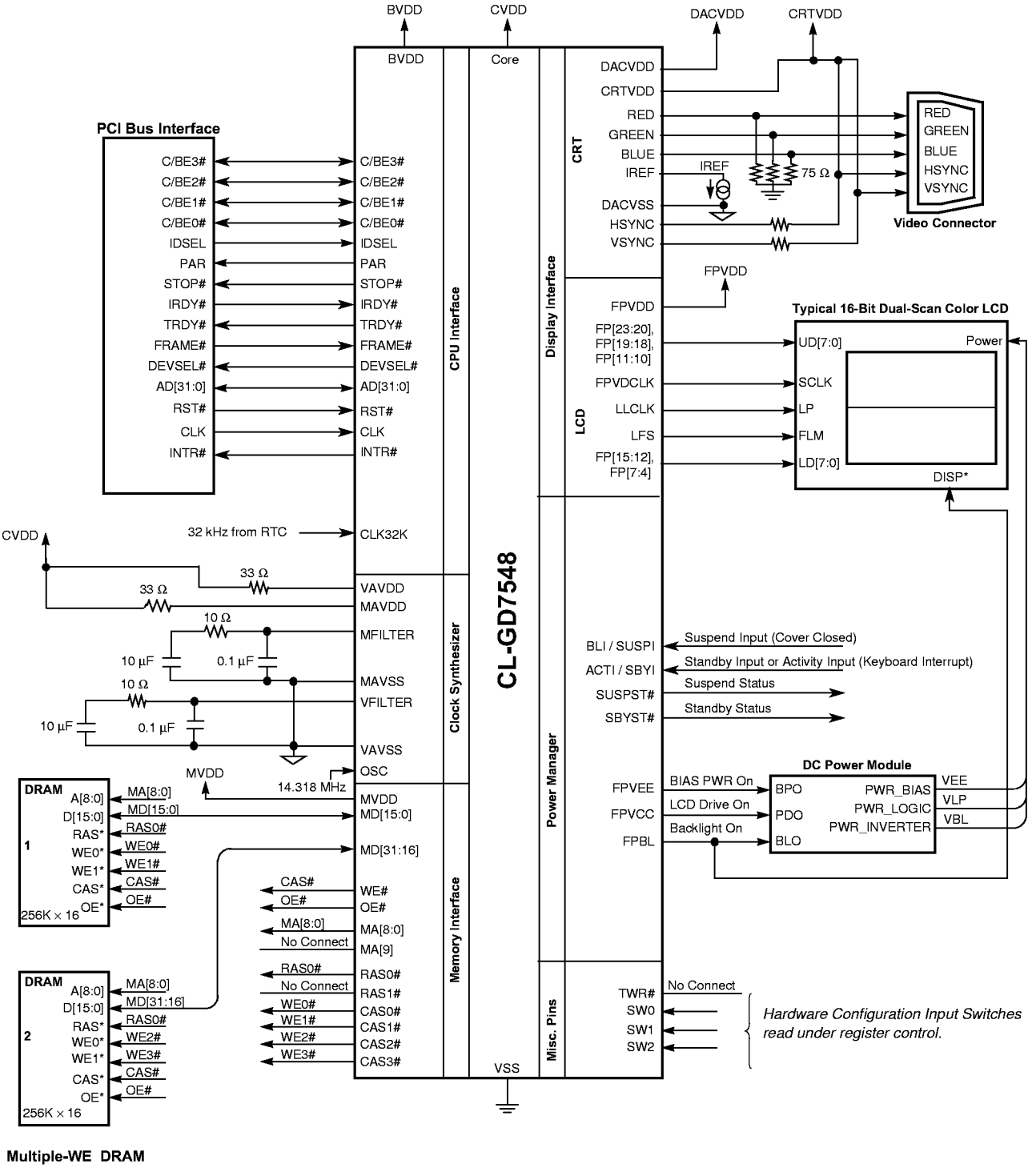
NOTES:

1) When using the design featured in this diagram, the CRT must be disconnected when using the NTSC output.
2) This diagram illustrates general signal connections. All information is preliminary and subject to change. For detailed design examples, refer to the *CL-GD754X Application Book*.

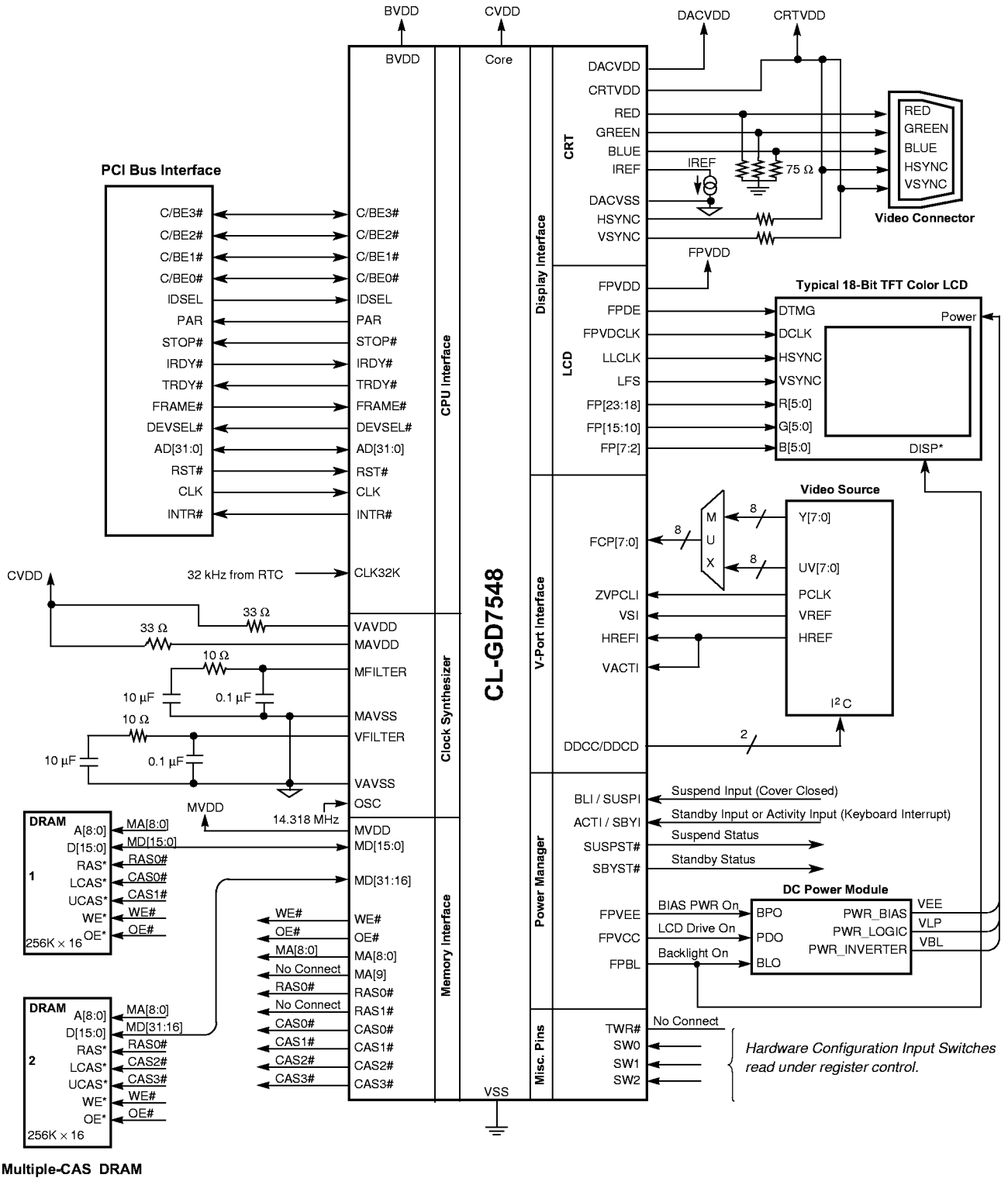
1.3.4 PCI Bus, 2-Mbyte 256K × 16 DRAM, 24-Bit TFT Color



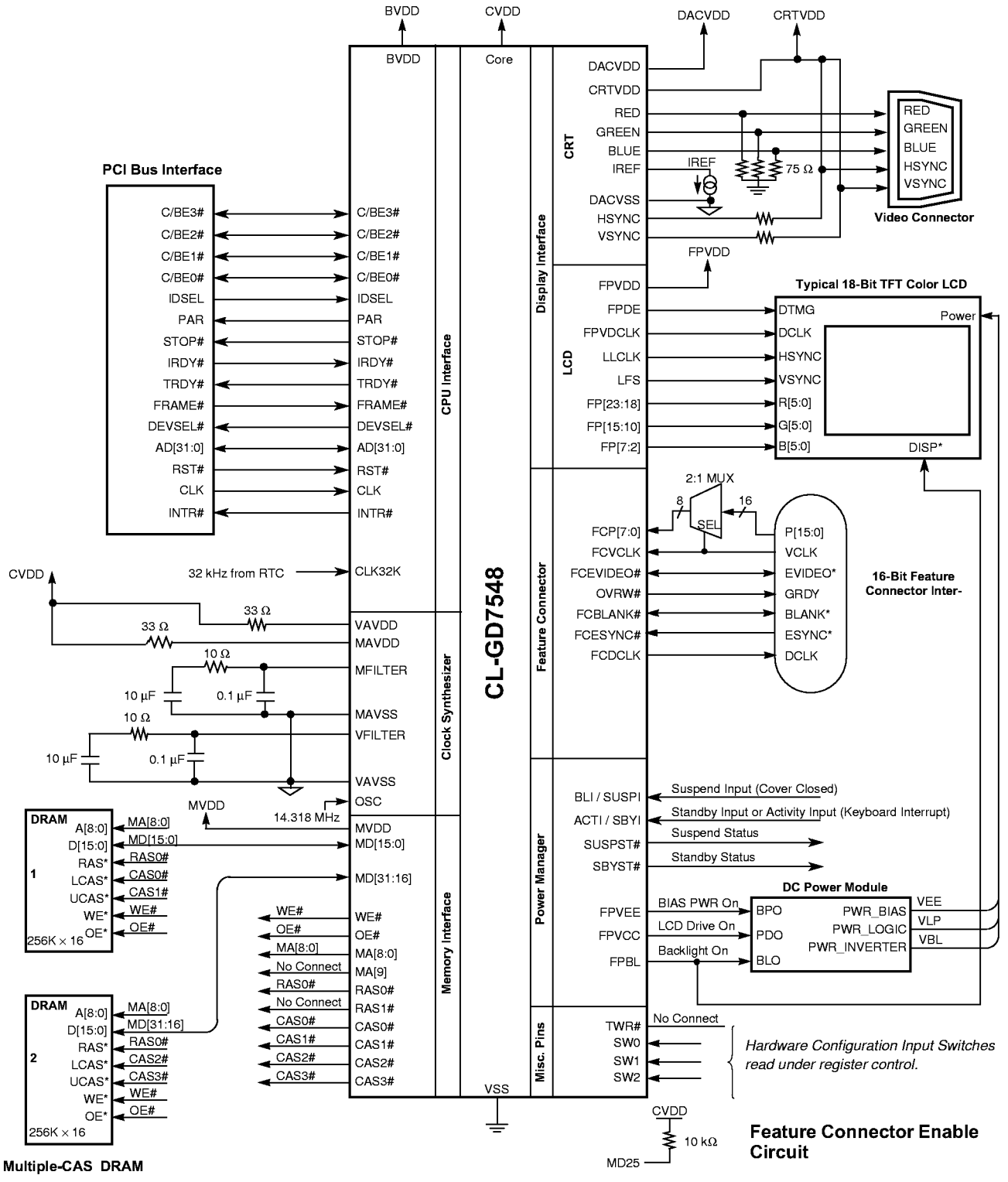
1.3.5 PCI Bus, 1-Mbyte 256K × 16 DRAM, 16-Bit Dual-Scan Color



1.3.6 PCI Bus, 1-Mbyte 256K × 16 DRAM, 18-Bit TFT Color, V-Port™ Interface

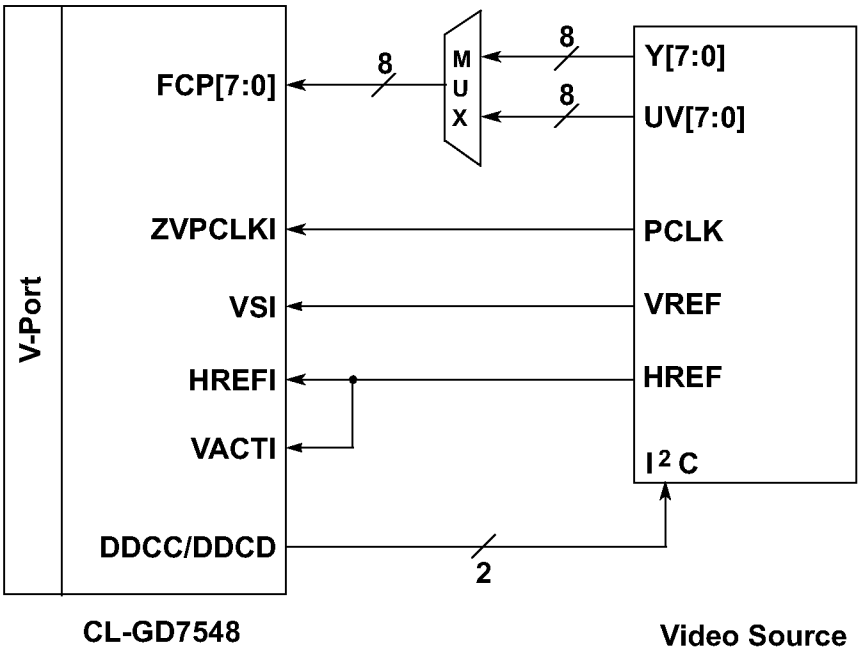


1.3.7 PCI Bus, 1-Mbyte 256K × 16 DRAM, 18-Bit TFT Color, Feature Connector Interface

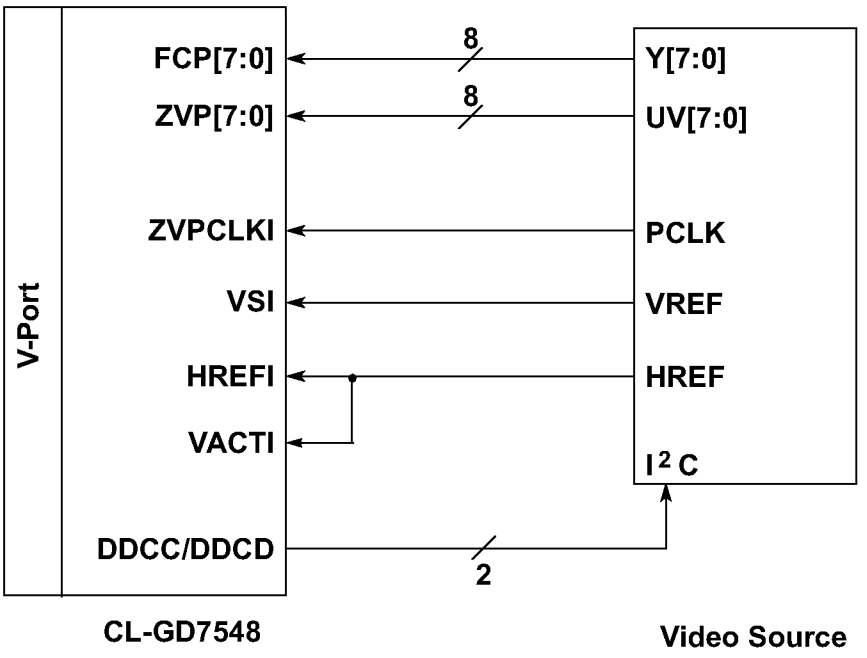


1.3.8 V-Port™ Interfaces for VESA VL-Bus and PCI Bus Systems

VESA VL-Bus V-Port Configuration



PCI Bus V-Port Configuration



2. PIN DESCRIPTIONS

The following abbreviations are used for pin types in the following sections:

- (I) indicates input function
- (O) indicates output function
- (I/O) indicates a bidirectional function
- (I or O) indicates either an input or output function, depending on the mode that is being used
- (O-OD) indicates open-drain output (electrically equivalent to open-collector)
- (O-TS) indicates tristate output
- (S-TS) indicates sustained tristate output (that is, one that is driven inactive before it is forced off)
- (#) indicates active-low function

2.1 Host CPU Bus Interface Pins

As explained in this section, a number of CL-GD7548 pins that interface to the CPU host bus pins are defined according to the type of CPU host to which the CL-GD7548 is connected.

2.1.1 CL-GD7548 CPU Host Bus Interface Pins to '486 or VESA® VL-Bus™ Local Bus

Pin Name	Pin No.	Type	Pin Description
A[25:24]	41:40	I	**ADDRESS [25:24]:** For the description of how pins 41:40 are used for an address function, within this table refer to pin name HIMEM[1:0].
A[23:21], A[20:2]	39:37, 35:17	I	**ADDRESS [23:2]:** These inputs are used to select the resource to be accessed during local bus memory or I/O operations.
ADS#	9	I	**ADDRESS DATA STROBE#:** This active-low input indicates that a new local bus cycle has begun. The ADS# signal is generated from a decode of the CPU output signals, A[23:2] and M/IO#. This output goes low before the middle of the first timing (T2) cycle after ADS# goes low. When connecting the CL-GD7548 to a '486 local bus, this pin must be connected directly to the '486 local bus ADS# pin.
BE[3:0]#	13–16	I	**BYTE ENABLE [3:0]#:** These active-low inputs are connected directly to corresponding CPU byte-enable outputs.
D[31:28], D[27:24], D[23:15], D[14:11], D[10:6], D[5:0]	43–46, 48–51, 53–61, 63–66, 68–72, 74–79	I/O	**DATA [31:0]:** These bidirectional pins are used to transfer data during any memory or I/O operation. When connecting the CL-GD7548 to a local bus (either a '486 local bus or a VESA VL-Bus), these pins must be connected directly to the local bus D[31:0] pins.
HIMEM[1:0] / A[25:24]	41:40	I	**HIGH MEMORY [1:0] / ADDRESS [25:24]:** These inputs are a decode of the upper CPU Address bits. Normally, these inputs are used as CPU Address bits A[25:24]. However, in combination with Extension registers SR7 and SR2D, they can be used as CPU Address bits A[31:30] in order to leave 2 Gbytes of upper system memory address space for boards that are based on the MPEG (Moving Picture Experts Group) and JPEG (Joint Picture Expert Group) standards.
INTR	5	O	**INTERRUPT REQUEST:** This output indicates that the CL-GD7548 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border. For a description of controls for this pin, refer to CRT Controller register CR11[3:0].

2.1.1 CL-GD7548 CPU Host Bus Interface Pins to '486 or VESA® VL-Bus™ Local Bus *(cont.)*

Pin Name	Pin No.	Type	Pin Description
LCLK	7	I	**LOCAL BUS CLOCK:** This input is the timing reference when the CL-GD7548 is connected to a local bus. When connecting the CL-GD7548 to: • *A '486 local bus*, this pin must be connected directly to the '486 local bus CLK1X# pin. If no CLK1X is available from the '486, CLK2 must be divided by two and connected to the CL-GD7548 LCLK pin, and clock skew must be less than 2.0 ns. • *A VESA VL-Bus*, this pin must be connected directly to the VESA VL-Bus LCLK pin.
LDEV#	3	O	**LOCAL BUS DEVICE#:** This active-low output is driven low to indicate the CL-GD7548 is responding to the current cycle. This pin is active when the CL-GD7548 I/O and memory address space is decoded. When connecting the CL-GD7548 to: • *A '486 local bus,* to select a local bus, this pin must be connected to the equivalent pin of a core-logic chip or chip set. • *A VESA VL-Bus*, this pin is connected to the VESA VL-Bus LDEV# pin.
M/IO#	11	I	**MEMORY I/O#:** This active-low input indicates whether a memory or I/O operation is to occur. When M/IO# is: • *Low*, an I/O operation is selected. • *High,* a memory operation is selected. This pin *must* be connected directly to the CPU M/IO# pin.
RDY#	4	S-TS	**READY#:** This active-low sustained tristate output is used to terminate a CL-GD7548 bus cycle. When connecting the CL-GD7548 to: • *A '486 local bus*, this pin must be connected to the '486 local bus RDY# pin. • *A VESA VL-Bus*, this pin must be connected to the VESA VL-Bus LRDY# pin.

2.1.1 CL-GD7548 CPU Host Bus Interface Pins to '486 or VESA® VL-Bus™ Local Bus *(cont.)*

Pin Name	Pin No.	Type	Pin Description
RDYRTN#	8	I	**READY RETURN#:** This active-low input establishes a handshake between the CL-GD7548 and a local bus so that the CL-GD7548 is informed when the cycle has ended. RDYRTN# typically goes low in the same LCLK cycle that LRDY# goes low. When LCLK is higher than 33 MHz, RDYRTN# can trail LRDY# by one LCLK cycle. During DMA or system I/O bus master operations, RDYRTN# goes low for one LCLK cycle when commands end for either the DMA or the system I/O bus masters. When connecting the CL-GD7548 to: • *A '486 local bus*, this pin must be connected to the '486 local bus RDY# pin. • *A VESA VL-Bus*, this pin must be connected to the VESA VL-Bus RDYRTN# pin.
RESET#	12	I	**RESET#:** When this active-low input is low, it initializes the CL-GD7548 to a known state. The trailing (rising) edge of this input loads the configuration Extension registers SR22[7:0] and SR24[7] with the data on MD[25:16] pins. The data on the MD[25:16] pins is determined either by internal pull-down resistors or optional external pull-up resistors. When RESET# is low, it also forces all outputs to a high-impedance state, and it initializes all registers to their system reset state.
SLEEP#	81	I	**SLEEP#:** This active-low input is used by the external hardware to put the CL-GD7548 into bus Sleep mode. When this input is low, the memory and I/O interfaces are disabled. Once this pin is low, no other chip access is possible until this pin goes high.
ZVPCTL	81	o	**V-Port CONTROL:** This output allows the V-Port to synchronize with a new video source when the external source is changed. If Extension register SR22[4] is 0, (that is, a pull-up is not connected to pin 163, the SLEEPPU pin) the value programmed into Extension register CR5C[7] takes effect. In this case, when Extension register CR5C[7] is: • 0, a low occurs on this pin at the falling (trailing) edge of the V-Port VSYNC signal. • 1, a high occurs on this pin at the falling (trailing) edge of the V-Port VSYNC signal.

2.1.1 CL-GD7548 CPU Host Bus Interface Pins to '486 or VESA® VL-Bus™ Local Bus *(cont.)*

Pin Name	Pin No.	Type	Pin Description
W/R#	10	I	**WRITE/READ#:** This active-low input indicates whether a write or read operation is selected by the CPU. When W/R# is: • *Low*, a read occurs. • *High*, a write occurs. This pin *must* be connected directly to the CPU W/R# pin.
ZVPCTL	81	O	**V-Port CONTROL:** For the description of how pin 81 is used for the ZVPCTL function, within this table refer to pin name SLEEP#.

2.1.2 CL-GD7548 CPU Host Bus Interface Pins to PCI Bus

Pin Name	Pin No.	Type	Pin Description
AD[31:28], AD[27:24], AD[23:15], AD[14:11], AD[10:6], AD[5:0]	43–46, 48–51, 53–61, 63–66, 68–72, 74–79	I/O	**ADDRESS AND DATA [31:0]:** These multiplexed, bidirectional pins are used to transfer system address and data during any memory or I/O operation on the PCI bus. During the first clock of a transaction, these pins act as inputs that contain a 32-bit physical byte address. During subsequent clocks, these pins act as bidirectional pins that are used to transfer data during any memory or I/O operation. These pins directly connect to the PCI bus AD[31:0] pins.
C/BE[3:0]#	13–16	I or O	**COMMAND AND BYTE ENABLE [3:0]#:** These active-low multiplexed pins are used to transfer Bus Command and Byte Enables during any memory or I/O operation on the PCI bus. During the address phase of the operation, these pins act as inputs that define the bus command. (Refer to Table 2-1.) During the data phase, these pins are used as Byte Enable outputs. C/BE0# applies to byte 0. C/BE3# applies to byte 3. These pins directly connect to the PCI bus C/BE[3:0]# pins.

Table 2-1. Command and Byte Enable#

C/BE#				Command Type	Supported by CL-GD7548?
[3]	[2]	[1]	[0]		
0	0	0	0	Interrupt Acknowledge	–
0	0	0	1	Special Cycle	–
0	0	1	0	I/O Read	Yes
0	0	1	1	I/O Write	Yes
0	1	0	0	Reserved	–
0	1	0	1	Reserved	–
0	1	1	0	Memory Read	Yes
0	1	1	1	Memory Write	Yes
1	0	0	0	Reserved	–
1	0	0	1	Reserved	–
1	0	1	0	Configuration Read	Yes
1	0	1	1	Configuration Write	Yes
1	1	0	0	Memory Read Multiple	–
1	1	0	1	Dual Address Cycle	–
1	1	1	0	Memory Read Line	–
1	1	1	1	Memory Write and Invalidate	–

2.1.2 CL-GD7548 CPU Host Bus Interface Pins to PCI Bus *(cont.)*

Pin Name	Pin No.	Type	Pin Description
CLK	7	I	**CLOCK:** This input is the timing reference for the CL-GD7548, when it is connected to a PCI bus. This pin must be connected directly to the PCI bus CLK pin.
DEVSEL#	3	S-TS	**DEVICE SELECT#:** This active-low sustained tristate output is driven low to indicate that the CL-GD7548 is responding to the current PCI bus cycle.
FRAME#	9	I	**FRAME#:** This active-low input indicates the beginning and duration of a PCI bus transaction. When FRAME# goes: • *Low*, it indicates the beginning of a PCI bus transaction. While FRAME# is low, data transfers continue. • *High*, the PCI bus transaction is in its final data phase.
IDSEL	10	I	**INITIALIZATION DEVICE SELECT:** This input, during configuration PCI bus read and write cycles, is used as a chip select in lieu of the upper 24 address lines.
INTR#	5	O-TS	**INTERRUPT REQUEST#:** This active-low tristate output, controlled by CRT Controller register CR11[3:0], when low, indicates the CL-GD7548 has reached the end of an active field. Specifically, the transition occurs at the beginning of the bottom border.
IRDY#	8	I	**INITIATOR READY#:** This active-low input establishes a handshake between the CL-GD7548 and PCI bus so that the CL-GD7548 can detect the end of a cycle. The CL-GD7548 inserts wait states until both IRDY# and TRDY# are low.
PAR	23	I/O	**PARITY:** This bidirectional pin provides even parity across AD[31:0] and C/BE[3:0]#. The CL-GD7548 samples this signal during PCI bus write cycles and transmits the correct parity for PCI bus read cycles.
RST#	12	I	**RESET#:** This active-low input, when low, initializes the CL-GD7548 to a known state. The trailing (rising) edge of this input loads Extension registers SR22[7:0] and SR24[7] with the data on MD[25:16], which is determined by internal pull-down resistors or optional external pull-up resistors.
STOP#	22	S-TS	**STOP#:** This active-low sustained tristate output, when low indicates a request to the PCI bus master to stop the current transaction.
TRDY#	4	S-TS	**TARGET READY#:** This active-low sustained tristate output is used to terminate a CL-GD7548 PCI bus cycle.

2.2 LCD Interface Pins

The LCD interface is determined by the type of LCD used. For specific connection information, refer to the Cirrus Logic "Panel Interface Guide" in the *CL-GD754X Application Book*.

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP0	114	O	B0	**24-BIT TFT BLUE BIT [0]:** This output is BLUE Color Data bit 0 (LSB) for 24-bit TFT color LCDs.
FP1	115	O	B1	**24-BIT TFT BLUE BIT [1]:** This output is BLUE Color Data bit 1 for 24-bit TFT color LCDs.
FP2	116	O	B2	**24-BIT TFT BLUE BIT [2]:** This output is BLUE Color Data bit 2 for 24-bit TFT color LCDs.
			B0	**18-BIT TFT BLUE BIT [0]:** This output is BLUE Color Data bit 0 (LSB) for 18-bit TFT color LCDs.
FP3	117	O	B3	**24-BIT TFT BLUE BIT [3]:** This output is BLUE Color Data bit 3 for 24-bit TFT color LCDs.
			B1	**18-BIT TFT BLUE BIT [1]:** This output is BLUE Color Data bit 1 for 18-bit TFT color LCDs. **NOTE:** For the description of how pin 117 is used for the MOD function, within this table refer to pin name MOD.
FP4	118	O	B4	**24-BIT TFT BLUE BIT [4]:** This output is BLUE Color Data bit 4 for 24-bit TFT color LCDs.
			B2	**18-BIT TFT BLUE BIT [2]:** This output is BLUE Color Data bit 2 for 18-bit TFT color LCDs.
			B0	**12-BIT TFT BLUE BIT [0]:** This output is BLUE Color Data bit 0 (LSB) for 12-bit TFT color LCDs.
			SLD0	**16-BIT STN COLOR LOWER BIT [0]:** This output is Lower Data bit 0 (LSB) for 16-bit dual- and single-scan STN color LCDs.
			SLD0	**8-BIT STN COLOR LOWER BIT [0]:** This output is Lower Data bit 0 (LSB) for 8-bit dual- and single-scan STN color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP5	119	O	B5	**24-BIT TFT BLUE BIT [5]:** This output is BLUE Color Data bit 5 for 24-bit TFT color LCDs.
			B3	**18-BIT TFT BLUE BIT [3]:** This output is BLUE Color Data bit 3 for 18-bit TFT color LCDs.
			B1	**12-BIT TFT BLUE BIT [1]:** This output is BLUE Color Data bit 1 for 12-bit TFT color LCDs.
			B0	**9-BIT TFT BLUE BIT [0]:** This output is BLUE Color Data bit 0 (LSB) for 9-bit TFT color LCDs.
			SLD1	**16-BIT STN COLOR LOWER BIT [1]:** This output is Lower Data bit 1 for 16-bit dual- and single-scan STN color LCDs.
			SLD1	**8-BIT STN COLOR LOWER BIT [1]:** This output is Lower Data bit 1 for 8-bit dual- and single-scan STN color LCDs.
FP6	120	O	B6	**24-BIT TFT BLUE BIT [6]:** This output is BLUE Color Data bit 6 for 24-bit TFT color LCDs.
			B4	**18-BIT TFT BLUE BIT [4]:** This output is BLUE Color Data bit 4 for 18-bit TFT color LCDs.
			B2	**12-BIT TFT BLUE BIT [2]:** This output is BLUE Color Data bit 2 for 12-bit TFT color LCDs.
			B1	**9-BIT TFT BLUE BIT [1]:** This output is BLUE Color Data bit 1 for 9-bit TFT color LCDs.
			SLD2	**16-BIT STN COLOR LOWER BIT [2]:** This output is Lower Data bit 2 for 16-bit dual- and single-scan STN color LCDs.
			SLD2	**8-BIT STN COLOR LOWER BIT [2]:** This output is Lower Data bit 2 for 8-bit dual- and single-scan STN color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP7	122	O	B7	**24-BIT TFT BLUE BIT [7]:** This output is BLUE Color Data bit 7 (MSB) for 24-bit TFT color LCDs.
			B5	**18-BIT TFT BLUE BIT [5]:** This output is BLUE Color Data bit 5 (MSB) for 18-bit TFT color LCDs.
			B3	**12-BIT TFT BLUE BIT [3]:** This output is BLUE Color Data bit 3 (MSB) for 12-bit TFT color LCDs.
			B2	**9-BIT TFT BLUE BIT [2]:** This output is BLUE Color Data bit 2 (MSB) for 9-bit TFT color LCDs.
			SLD3	**16-BIT STN COLOR LOWER BIT [3]:** This output is Lower Data bit 3 for 16-bit dual- and single-scan STN color LCDs.
			SLD3	**8-BIT STN COLOR LOWER BIT [3]:** This output is Lower Data bit 3 (MSB) for 8-bit dual- and single-scan STN color LCDs.
FP8	123	O	G0	**24-BIT TFT GREEN BIT [0]:** This output is GREEN Color Data bit 0 (LSB) for 24-bit TFT color LCDs.
FP9	125	O	G1	**24-BIT TFT GREEN BIT [1]:** This output is GREEN Color Data bit 1 for 24-bit TFT color LCDs.
FP10	126	O	G2	**24-BIT TFT GREEN BIT [2]:** This output is GREEN Color Data bit 2 for 24-bit TFT color LCDs.
			G0	**18-BIT TFT GREEN BIT [0]:** This output is GREEN Color Data bit 0 (LSB) for 18-bit TFT color LCDs.
			SUD4	**16-BIT STN COLOR UPPER BIT [4]:** This output is Upper Data bit 4 for 16-bit dual- and single-scan STN color LCDs.
FP11	127	O	G3	**24-BIT TFT GREEN BIT [3]:** This output is GREEN Color Data bit 3 for 24-bit TFT color LCDs.
			G1	**18-BIT TFT GREEN BIT [1]:** This output is GREEN Color Data bit 1 for 18-bit TFT color LCDs.
			SUD5	**16-BIT STN COLOR UPPER BIT [5]:** This output is Upper Data bit 5 for 16-bit dual- and single-scan STN color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP12	128	O	G4	**24-BIT TFT GREEN BIT [4]:** This output is GREEN Color Data bit 4 for 24-bit TFT color LCDs.
			G2	**18-BIT TFT GREEN BIT [2]:** This output is GREEN Color Data bit 2 for 18-bit TFT color LCDs.
			G0	**12-BIT TFT GREEN BIT [0]:** This output is GREEN Color Data bit 0 (LSB) for 12-bit TFT color LCDs.
			SLD4	**16-BIT STN COLOR LOWER BIT [4]:** This output is Lower Data bit 4 for 16-bit dual- and single-scan STN color LCDs.
			SUD0	**8-BIT STN COLOR UPPER BIT [0]:** This output is Upper Data bit 0 (LSB) for 8-bit dual- and single-scan STN color LCDs.
FP13	129	O	G5	**24-BIT TFT GREEN BIT [5]:** This output is GREEN Color Data bit 5 for 24-bit TFT color LCDs.
			G3	**18-BIT TFT GREEN BIT [3]:** This output is GREEN Color Data bit 3 for 18-bit TFT color LCDs.
			G1	**12-BIT TFT GREEN BIT [1]:** This output is GREEN Color Data bit 1 for 12-bit TFT color LCDs.
			G0	**9-BIT TFT GREEN BIT [0]:** This output is GREEN Color Data bit 0 (LSB) for 9-bit TFT color LCDs.
			SLD5	**16-BIT STN COLOR LOWER BIT [5]:** This output is Lower Data bit 5 for 16-bit dual- and single-scan STN color LCDs.
			SUD1	**8-BIT STN COLOR UPPER BIT [1]:** This output is Upper Data bit 1 for 8-bit dual- and single-scan STN color LCDs.
FP14	130	O	G6	**24-BIT TFT GREEN BIT [6]:** This output is GREEN Color Data bit 6 for 24-bit TFT color LCDs.
			G4	**18-BIT TFT GREEN BIT [4]:** This output is GREEN Color Data bit 4 for 18-bit TFT color LCDs.
			G2	**12-BIT TFT GREEN BIT [2]:** This output is GREEN Color Data bit 2 for 12-bit TFT color LCDs.
			G1	**9-BIT TFT GREEN BIT [1]:** This output is GREEN Color Data bit 1 for 9-bit TFT color LCDs.
			SLD6	**16-BIT STN COLOR LOWER BIT [6]:** This output is Lower Data bit 6 for 16-bit dual- and single-scan STN color LCDs.
			SUD2	**8-BIT STN COLOR UPPER BIT [2]:** This output is Upper Data bit 2 for 8-bit dual- and single-scan STN color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP15	131	O	G7	**24-BIT TFT GREEN BIT [7]:** This output is GREEN Color Data bit 7 (MSB) for 24-bit TFT color LCDs.
			G5	**18-BIT TFT GREEN BIT [5]:** This output is GREEN Color Data bit 5 (MSB) for 18-bit TFT color LCDs.
			G3	**12-BIT TFT GREEN BIT [3]:** This output is GREEN Color Data bit 3 (MSB) for 12-bit TFT color LCDs.
			G2	**9-BIT TFT GREEN BIT [2]:** This output is GREEN Color Data bit 2 (MSB) for 9-bit TFT color LCDs.
			SLD7	**16-BIT STN COLOR LOWER BIT [7]:** This output is Lower Data bit 7 (MSB) for 16-bit dual- and single-scan STN color LCDs.
			SUD3	**8-BIT STN COLOR UPPER BIT [3]:** This output is Upper Data bit 3 (MSB) for 8-bit dual- and single-scan STN color LCDs.
FP[16]	133	O	R0	**24-BIT TFT RED BIT [0]:** This output is RED Color Data bit 0 (LSB) for 24-bit TFT color LCDs.
FP[17]	134	O	R1	**24-BIT TFT RED BIT [1]:** This output is RED Color Data bit 1 for 24-bit TFT color LCDs.
FP18	135	O	R2	**24-BIT TFT RED BIT [2]:** This output is RED Color Data bit 2 for 24-bit TFT color LCDs.
			R0	**18-BIT TFT RED BIT [0]:** This output is RED Color Data bit 0 (LSB) for 18-bit TFT color LCDs.
			SUD6	**16-BIT STN COLOR UPPER BIT [6]:** This output is Upper Data bit 6 for 16-bit dual- and single-scan STN color LCDs.
FP19	136	O	R3	**24-BIT TFT RED BIT [3]:** This output is RED Color Data bit 3 for 24-bit TFT color LCDs.
			R1	**18-BIT TFT RED BIT [1]:** This output is RED Color Data bit 1 for 18-bit TFT color LCDs.
			SUD7	**16-BIT STN COLOR UPPER BIT [7]:** This output is Upper Data bit 7 (MSB) for 16-bit dual- and single-scan STN color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP20	137	O	R4	**24-BIT TFT RED BIT [4]:** This output is RED Color Data bit 4 for 24-bit TFT color LCDs.
			R2	**18-BIT TFT RED BIT [2]:** This output is RED Color Data bit 2 for 18-bit TFT color LCDs.
			R0	**12-BIT TFT RED BIT [0]:** This output is RED Color Data bit 0 (LSB) for 12-bit TFT color LCDs.
			SUD0	**16-BIT STN COLOR UPPER BIT [0]:** This output is Upper Data bit 0 (LSB) for 16-bit dual- and single-scan STN color LCDs.
FP21	138	O	R5	**24-BIT TFT RED BIT [5]:** This output is RED Color Data bit 5 for 24-bit TFT color LCDs.
			R3	**18-BIT TFT RED BIT [3]:** This output is RED Color Data bit 3 for 18-bit TFT color LCDs.
			R1	**12-BIT TFT RED BIT [1]:** This output is RED Color Data bit 1 for 12-bit TFT color LCDs.
			R0	**9-BIT TFT RED BIT [0]:** This output is RED Color Data bit 0 (LSB) for 9-bit TFT color LCDs.
			SUD1	**16-BIT STN COLOR UPPER BIT [1]:** This output is Upper Data bit 1 for 16-bit dual- and single-scan STN color LCDs.
FP22	139	O	R6	**24-BIT TFT RED BIT [6]:** This output is RED Color Data bit 6 for 24-bit TFT color LCDs.
			R4	**18-BIT TFT RED BIT [4]:** This output is RED Color Data bit 4 for 18-bit TFT color LCDs.
			R2	**12-BIT TFT RED BIT [2]:** This output is RED Color Data bit 2 for 12-bit TFT color LCDs.
			R1	**9-BIT TFT RED BIT [1]:** This output is RED Color Data bit 1 for 9-bit TFT color LCDs.
			SUD2	**16-BIT STN COLOR UPPER BIT [2]:** This output is Upper Data bit 2 for 16-bit dual- and single-scan STN color LCDs.

2.2 LCD Interface Pins *(cont.)*

Pin Name	Pin No.	Pin Type	Pin Function	Pin Description
FP23	140	O	R7	**24-BIT TFT RED BIT [7]:** This output is RED Color Data bit 7 (MSB) for 24-bit TFT color LCDs.
			R5	**18-BIT TFT RED BIT [5]:** This output is RED Color Data bit 5 (MSB) for 18-bit TFT color LCDs.
			R3	**12-BIT TFT RED BIT [3]:** This output is RED Color Data bit 3 (MSB) for 12-bit TFT color LCDs.
			R2	**9-BIT TFT RED BIT [2]:** This output is RED Color Data bit 2 (MSB) for 9-bit TFT color LCDs.
			SUD3	**16-BIT STN COLOR UPPER BIT [3]:** This output is Upper Data bit 3 for 16-bit dual- and single-scan STN color LCDs.
FPDE	108	O		**FLAT PANEL DISPLAY ENABLE:** For those LCDs that require an external display enable, this output is used to provide a display enable signal that is active when LCD panel data is valid. The FPDE function of this pin is enabled when Extension register R8X[1] is cleared to 0.
FPVDCLK	113	O		**FLAT PANEL VIDEO CLOCK:** This output is used to drive the LCD shift clock. Depending on the LCD manufacturer, on the LCD the FPVCDLK signal can have other names, including 'SHIFT', 'Clock Pulse 2' (CP2) or 'Shift Clock' (SCLK).
LFS	110	O		**LCD FRAME START:** This output provides a pulse, the 'LCD Frame Start' signal, to start a new frame on LCDs. Depending on the LCD manufacturer, on the LCD the LFS signal can have other names, including 'FRAME', 'First Line Marker' (FLM), 'Line Frame Start' (LFS), or 'Start' (S).
LLCLK	112	O		**LCD LINE CLOCK:** This output is used to drive the LCD line clock. Depending on the LCD manufacturer, on the LCD the LLCLK signal can have other names, including 'LINE', 'Line Pulse' (LP), or 'Clock Pulse 1' (CP1).
MOD	117	O		**MODULATION:** This output provides AC inversion. This pin must be connected to the MOD, FR, or DF inputs of the LCD, as appropriate. Some LCD manufacturers provide this function in the LCD circuitry, in which case this pin does not need to be connected. **NOTE:** For the description of how pin 117 is used for the FP[3] function, within this table refer to pin name FP[3].

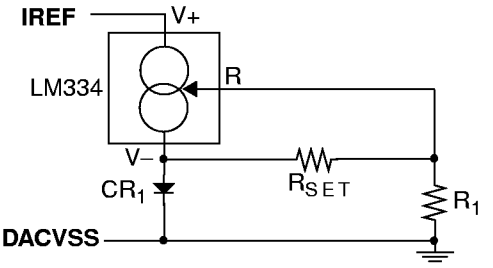
2.3 CRT Interface Pins

This section lists the CRT interface pins. For more information on the CRT interfaces, refer to the section on the CRT controller in Section 3.5.10.

Pin Name	Pin No.	Type	Pin Description
BLUE	96	O	**BLUE VIDEO:** This analog output supplies current that corresponds to the **blue** value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the lookup table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to the IREF signal as follows: $I_{full\text{-}scale} = (63/30) \times IREF$ To maintain IBM VGA compatibility, each DAC output is typically terminated to monitor ground with a 150-Ω 2% resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, yields a 50-Ω resistance to ground. For a 700 mV full-scale voltage, full-scale current output must be 14 mA.
GREEN	97	O	**GREEN VIDEO:** This analog output supplies current corresponding to the **green** value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
HSYNC	91	O-TS	**HORIZONTAL SYNC:** This tristate output supplies the horizontal synchronization pulse to the CRT monitor. The polarity of this output is programmable. This pin can be connected directly to the corresponding pin on the monitor connector.
IREF	99	I	**DAC CURRENT REFERENCE:** The current drawn from DACVDD1 and DACVDD2 through this input pin determines the full-scale output of each DAC. This pin must be connected to a constant-current source. For information on how to calculate the IREF constant current, refer to the application note "IREF Current Source" in the *CL-GD754X Application Book*.

Table 2-2. Example

R_{SET} (± 1%)	R_1 (± 1%)	Diode CR_1
15 Ω	150 Ω	Schottky diode (V_F < 0.4 V)



2.3 CRT Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
RED	98	O	**RED VIDEO:** This analog output supplies current corresponding to the **red** value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
VSYNC	93	O-TS	**VERTICAL SYNC:** This tristate output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin can be connected directly to the corresponding pin on the monitor connector.

2.4 NTSC and PAL Interface Pins

Because LCD control pins are used with NTSC and PAL interfaces, during the time that the NTSC and PAL interface pins are used, LCDs must be isolated. External AND gates must be used to force LCD control signals to the proper levels. (For design details, refer to the application note "Driving NTSC/PAL Display Signals" in the *CL-GD754X Application Book*.)

Pin Name	Pin No.	Type	Pin Description
BLUE	96	O	**BLUE VIDEO:** This analog output supplies current corresponding to the **blue** value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the lookup table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: $I_{full\text{-}scale} = (63/30) \times IREF$ When an NTSC/PAL encoder is used at the same time as the CRT, there must be a 1.4-kΩ series termination resistor between the CL-GD7548 and the R, G, and B inputs of the encoder. There is also a 0.7-kΩ resistor connected to ground from each R, G, and B input, to provide the correct input-voltage level for the encoder. To maintain a full-scale voltage of 700 mV across the CRT inputs, the full-scale current output must be 14 mA. For more termination details, refer to Section 2.3, "CRT Interface Pins".
CSYNC	95	O	**COMPOSITE SYNC:** This output provides the composite SYNC signal for the analog NTSC/PAL encoder. For NTSC/PAL interfaces, connect this CSYNC pin to the encoder SYNC input pin.
GREEN	97	O	**GREEN VIDEO:** This analog output supplies current corresponding to the **green** value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*
NTSC/PAL	94	O	**NTSC/PAL ENCODING SELECTION:** This output is used by the CL-GD7548 to select the desired NTSC or PAL encoding format. Extension register bits CR30[3:2] control the level on this pin.
RED	98	O	**RED VIDEO:** This analog output supplies current corresponding to the **red** value of the pixel being displayed. *To terminate this pin, refer to information under BLUE VIDEO.*

2.4 NTSC and PAL Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
TVON	146	O	**TV ON:** When Extension register SR25[6] = 0 and this output is: • *Low*, the power to the NTSC/PAL encoder is powered off. • *High*, the power to the NTSC/PAL encoder is powered on.
XRDACCS	146	O	**EXTERNAL RAMDAC CHIP SELECT:** When Extension register SR25[6] = 1, a high on this output is used to enable an external RAMDAC. **NOTE:** The XRDACCS function is not supported for PCI bus applications.

2.5 Dual-Frequency Synthesizer Interface Pins

For more information on the dual-frequency synthesizer, refer to Section 3.5.20.

Pin Name	Pin No.	Type	Pin Description
CLK32K	89	I	**32-kHz CLOCK:** This input can be connected to an externally supplied 32-kHz clock signal that can be used for memory refresh during Suspend mode and panel sequencing. If this pin is not used, it must be connected to the CL-GD7548 OSC pin.
MCLK	197	I or O	**MEMORY CLOCK:** The function of this pin depends on register settings. This pin is intended primarily for test purposes.
MFILTER	200	O	**MEMORY CLOCK FILTER:** This output, which results from an voltage-controlled oscillator internal to the CL-GD7548, is part of a circuit that generates the MCLK signal. • This pin *must* be connected to a π-RC filter that is returned to MAVSS. • The filter components, especially the input capacitor and the resistor, *must* be placed as close as possible to the MFILTER pin.
OSC	85	I	**OSCILLATOR INPUT:** This TTL input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.318 MHz ± 0.01% with a duty cycle of 50% ± 10%. This input can be supplied from the appropriate pin on the VL-Bus or from an oscillator.
XVCLK	85	I	**EXTENDED VIDEO CLOCK INPUT:** When a pull-up resistor is connected to the XCLKPU pin (pin 164), this pin is configured for an external clock input. This pin function is intended for test purposes only.

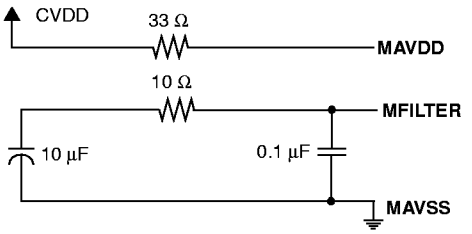


Figure 2-1. Typical Memory Clock Filter

2.5 Dual-Frequency Synthesizer Interface Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
VFILTER	83	O	**VIDEO CLOCK FILTER:** This output, which results from an voltage-controlled oscillator internal to the CL-GD7548, is part of a circuit that generates the VCLK signal. • This pin *must* be connected to a π-RC filter that is returned to VAVSS. • The filter components, especially the input capacitor and the resistor, *must* be placed as close as possible to the VFILTER pin.
XVCLK	85	I	**EXTENDED VIDEO CLOCK INPUT:** For the description of how pin 85 is used for the XVCLK function, within this table refer to pin name OSC.

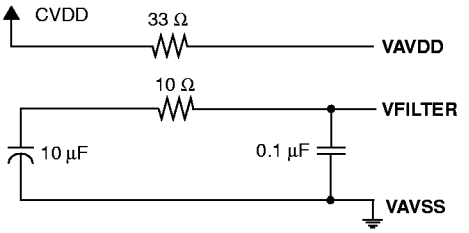


Figure 2-2. Typical Video Clock Filter

2.6 Display Memory Interface Pins

For more information on the display memory interface, refer to Section 3.2.2.

Pin Name	Pin No.	Type	Pin Description
CAS# / WE#	181	O	**COLUMN ADDRESS STROBE# / WRITE ENABLE#:** This active-low output is used to control whether CAS# (or WE#) inputs from MA[9:0] are latched into the DRAMs. The pin function depends on the state of Extension register SRF[0]. When SRF[0] is: • 0, the CL-GD7548 is configured for multiple-WE# DRAMs and: — Pin 181 is defined as CAS# and must be connected to the CAS# inputs of the DRAMS. — Pins 169–170 and 195:194 are defined as WE#. • 1, the CL-GD7548 is configured for multiple-CAS# DRAMs and: — Pin 181 is defined as WE# and must be connected to the WE# inputs of the DRAMS. — Pins 169–170 and 195:194 are defined as CAS#.
CAS[3:2]#, CAS[1:0]#	169–170, 195:194	O	**COLUMN ADDRESS STROBE [3:0]# / WRITE ENABLE [3:0]#:** These active-low outputs are used to latch the CAS# (or WE#) inputs from MA[9:0] into the DRAMs. The pin functions depend on the state of Extension register SRF[0]. (For more information, refer to the previous pin description of CAS# / WE#.)
WE[3:2]#, WE[1:0]#	169-170, 195:194	O	
MA[9:0]	171–180	O	**MEMORY ADDRESS [9:0]:** These outputs drive the address inputs of the DRAMs.
MD[31:21], MD[20:16], MD[15:10], MD[9], MD[8], MD[7:5], MD[4:2], MD[1:0]	151–161, 163–167, 186–191, 193, 196, 202–204, 206–208, 1–2	I/O	**MEMORY DATA [31:0]:** These bidirectional pins are used to transfer data between the CL-GD7548 and display memory. These pins must be connected to the data pins of the display memory DRAMs.
OE#	182	O	**OUTPUT ENABLE#:** This active-low output is used to control the Output Enables of the DRAMs. For 256K × 16 DRAMs with Dual-Write Enables, this pin must be connected to the OE# pins of all the DRAMs in the display memory array.
RAS[1:0]#	184:183	O	**ROW ADDRESS STROBE [1:0]#:** These active-low outputs are used to latch the row address from MA[9:0] into the DRAMs. Each RAS pin is used for one bank of memory, for a total of two banks. These pins must be connected to the RAS# pins of all the DRAMs in the display memory array.

2.7 Configuration Input Pins

The CL-GD7548 can be configured at system Reset for CPU bus type, sleep address, and external memory clock source. The memory pins MD[23:16] have internal pull-down resistors that are read and stored during the low-to-high transition of the Reset pulse. When external pull-up resistors of 10k ohms or less are connected to these pins as defined in the following table, the default functions are changed.

The CL-GD7548 supports the VESA VL-Bus or the PCI Bus. When no pull-up resistor is supplied on PCIPU (pin 167), the CL-GD7548 is configured for a VESA VL-Bus operation of 33 MHz or less.

For all configuration input pins, their state can be latched under either hardware or software control. When the configuration input pins are under:

- *Hardware control* – all external pull-up resistors on the memory data pins (MD25:16) have their state read and latched by the CL-GD7548 during hardware reset only.
- *Software control* – any 0-1-0 transition of Extension register bit SR24[3] stores the state of all external pull-up resistors on memory data pins (MD25:16) at any time.
  - — Software control is used whenever it is desired to read configuration pins independent of system reset.
  - — In particular, software control is appropriate when the system reset pulse is too short to read the switches that have large pull-up or pull-down resistance.

Pin Name	Pin No.	Type	Pin Description
FCPU MD25	157	I	**FEATURE CONNECTOR PORT:** When a pull-up resistor is: • *Connected* to this input pin, a logic high is read and stored in Extension register SR24[7] during the system reset. This high level configures the CL-GD7548 to supply all the Feature Connector Port signals. (Refer to Section 2.9) • *Not connected* to this pin, this pin reverts to its MD[25] function or it is disabled (that is, inputs are ignored and outputs are high-impedance).
PCIPU MD16	167	I	**PCI BUS SELECT PULL-UP:** When a pull-up resistor is: • *Connected* to this pin, at system reset, Extension register SR22[0] stores the resulting logic high. This high configures the CL-GD7548 for PCI bus operation and a minimum-grant value of 250 ns. • *Not connected* to this pin, this pin reverts to its MD[16] function or it is disabled (that is, inputs are ignored and outputs are high-impedance).
S46PU MD21	161	I	**SLEEP ADDRESS SELECT PULL-UP:** When the CL-GD7548 is configured for VL-Bus mode, the default (Extension register SR22[0] = 0), and a pull-up resistor is: • *Connected* to this pin, at system reset, Extension register SR22[5] stores the logic high. This high level configures the CL-GD7548 for the sleep address in External/General register 46E8[3], which applies when the CL-GD7548 is used with an adapter board. • *Not connected* to this pin, at system reset the CL-GD7548 is configured for the sleep address in External/General register 3C3[0], which applies when the CL-GD7548 is used with a motherboard.

2.7 Configuration Input Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
SLEEPPU	163 MD20	I	**SLEEP PULL-UP ENABLE:** When a pull-up resistor is: • *Connected* to this pin, at system reset, Extension register SR22[4] stores the logic high. This high level configures the CL-GD7548 for the sleep mode. (For an understanding of the choice of sleep modes that can be selected, refer to the S46PU description.) • *Not connected* to this pin, at system reset the CL-GD7548 is not configured for the sleep mode.
XCLKPU	164 MD19	I	**EXTERNAL CLOCK SELECT PULL-UP**: When a pull-up resistor is: • *Connected* to this pin, at system reset the CL-GD7548 is configured for external clock inputs on the SW0 / MCLK / XMCLK and OSC / XVLCK pins. This configuration is used for test purposes only. • *Not connected* to this pin, the CL-GD7548 uses internal clock sources. (No pull-up resistor should be connected during normal operation.)

NOTE: The PCI Bus Minimum Grant (PCI-MGPU) and VESA VL-Bus > 33 MHz (FVLPU) options are no longer supported on the CL-GD7548. Configuration pull-up resistors must not be connected to any pins accept the ones specified above.

2.8 Switch and Miscellaneous Configuration Input Pins

For more information on the switch and miscellaneous configuration inputs, refer to Section 3.6.7.1.

Pin Name	Pin No.	Type	Pin Description
SW0	197	I	**SWITCH 0:** This pin is configured as a hardware input. The level on this pin is read under register control and stored in Extension register SR24[0].
SW1	149	I	**SWITCH 1:** This pin is configured as a hardware input. The level on this pin is read under register control and stored in Extension register SR24[1].
SW2	150	I	**SWITCH 2:** This pin is configured as a hardware input. The level on this pin is read under register control and stored in Extension register SR24[2].
TWR#	100	I	**TEST WRITE#:** This active-low input is for factory test purposes only. For normal operation, this pin *must not* be connected to the system. It has an internal pull-up resistor connected.

2.9 Feature Connector Pins

When an external pull-up resistor:

- *Is connected* to the FCPU / MD[25] pin (pin 157), a logic high is read and stored in Extension register SR24[7] during system reset. This high level configures the CL-GD7548 for the Feature Connector signals in this section.
- *Is not connected* to the FCPU / MD[25] pin (pin 157), a logic low is read and stored in Extension register SR24[7] during system reset. In this case, if Extension register CR[50] is properly set, the CL-GD7548 is configured for the V-Port signals referenced in Section 2.10.

Pin Name	Pin No.	Type	Pin Description
FCBLANK#	101	I or O	**FEATURE-CONNECTOR BLANK#**: When FCESYNC# is: • *Low*, FCBLANK# is an active-low input that can force RGB outputs to zero current. • *High*, FCBLANK# is an active-low output that supplies a blanking signal to the Feature Connector.
FCDCLK	103	O	**FEATURE-CONNECTOR DOT CLOCK:** When the Feature Connector configuration is active, this pin provides the dot clock output to the video source subsystem that is connected to the Feature Connector. For details on register settings that enable this pin function to be selected, refer to Extension register SR24[4].
FCESYNC#	147	I	**FEATURE-CONNECTOR ENABLE SYNC#:** When this active-low input is: • *Low*, the HSYNC and VSYNC outputs are forced to high-impedance (off), and FCBLANK# is configured as an input. • *High*, the HSYNC, VSYNC, and FCBLANK# outputs are enabled.
FCEVIDEO#	86	I or O	**FEATURE-CONNECTOR ENABLE VIDEO#:** This active-low pin controls the buffers on FCP[7:0]. The function of this pin depends on the state of Extension register CR1A[3]. When CR1A[3] is: • 0, FCEVIDEO# is configured as an input. • 1, FCEVIDEO# is configured as an output.
FCP[7:4], FCP[3:2], FCP[1], FCP[0]	144:141 134:133 125, 123	I or O	**FEATURE-CONNECTOR PIXEL DATA [7:0]:** When FCEVIDEO# is: • *Low*, the FCP[7:0] pins are pixel data inputs that are driven directly into the palette DAC, and the display memory contents are ignored. (In a 16-bit/pixel LCD configuration mode, these inputs provide luminance data bits.) • *High*, the FCP[7:0] pins are pixel data outputs that copy the pixel address to the palette RAM.

2.9 Feature Connector Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
FCVCLK	114	I	**FEATURE-CONNECTOR VIDEO CLOCK:** This input works in combination with External/General register bit MISC[3] and Extension register bit SR23[7]. When SR23[7] is 1 *and*: • MISC[3] is 0, FCVCLK is sent only to the RAMDAC, enabling only that part of the CL-GD7548. • MISC[3] is 1, FCVCLK is used to drive VCLK, which clocks the entire CL-GD7548. • There is a high on the TVON pin, the TVON high signal forces MISC[3] to 1. In this case also, FCVCLK is used to drive VCLK, which clocks the entire CL-GD7548. This pin must be connected to the dot clock from the video source.
OVRW#	115	O	**OVERLAY WINDOW#:** This active-low output is asserted during the active portion of the video overlay window. It is intended to be used in applications involving video overlays. When Extension register CR1A[3:2] is used to select the color key as the dynamic overlay method, this pin goes high when a color key match occurs one or more clocks before valid data is expected on the pixel bus. For additional information, refer to the application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.

2.10 V-Port Pins

When an external pull-up resistor:

- *Is connected* to the FCPU / MD[25] pin (pin 157), a logic high is read and stored in Extension register SR24[7] during system reset. This high level configures the CL-GD7548 for the Feature Connector signals referred in Section 2.9.
- *Is not connected* to the FCPU / MD[25] pin (pin 157), a logic low is read and stored in Extension register SR24[7] during system reset. In this case, if Extension register CR[50] is properly set, the CL-GD7548 is configured for the V-Port™ signals in this section.

NOTES:

1) Operation with a 24-bit TFT LCD precludes use of V-Port features, because 24-bit LCDs use pins 114 and 115. (Refer to Section 2.2)
2) When the CL-GD7548 is used on a PCI bus, the V-Port can be 16 bits wide.
3) The V-Port pins are powered from the FPVDD and BVDD power planes. Whenever the CRTVDD is at 5.0 V, FPVDD and BVDD can be set to 3.3 V, even when the V-Port inputs are from a 5.0 V source.

Pin Name	Pin No.	Type	Pin Description
DDCC	103	O-OD	**DISPLAY DATA CHANNEL CLOCK:** This open-drain (open-collector) output provides the clock used by the DDC channel to communicate with external TV and MPEG encoder/decoder devices. For details on register settings that enable this pin function to be selected, refer to Extension register SR24[4].
DDCD	86	O-OD	**DISPLAY DATA CHANNEL DATA:** This open-drain (open-collector) output provides the serial data that is sent through the DDC channel to communicate with external TV and MPEG encoder/decoder devices.
FCP[7:4], FCP[3:2], FCP[1], FCP[0]	144:141 134:133 125, 123	I	**FEATURE-CONNECTOR PIXEL DATA [7:0]:** When the V-Port is enabled, these pins are inputs that can be used to drive the least-significant 8 bits of data to the V-Port. In a 16-bit/pixel V-Port configuration mode, these inputs provide luminance data bits.
HREFI	101	I	**HORIZONTAL REFERENCE INPUT:** This input is from an external video source horizontal sync.
VACTI	115	I	**VIDEO DATA ACTIVE INPUT:** If this pin is: • *Used*, the input for this pin typically comes from a video decoder chip, such as the CL-PX4072. • *Not used*, connect this pin to the HREFI pin.
VSI	147	I	**VERTICAL SYNC INPUT:** This input is from an external video source vertical sync.

2.10 V-Port Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
ZVP[7:5], ZVP[4:0]	26:24, 22:17	I	**V-Port PIXEL DATA [7:0]:** When the CL-GD7548 is configured for a PCI bus, these inputs are used to provide a total of 16 bits of data from the V-Port. In a 16-bit/pixel V-Port configuration mode, these inputs provide chrominance data bits.
ZVPCLKI	114	I	**V-Port CLOCK INPUT:** This input typically comes from a video decoder chip.

2.11 Power-Management Pins

For more information on power management, refer to Section 3.6.1.

Pin Name	Pin No.	Type	Pin Description
ACTI / SBYI	86	I	**ACTIVITY INPUT / STANDBY INPUT:** As described under Extension register bit SR23[6], this pin can be configured for either its ACTI or SBYI function when Extension register bit: • SR24[7] = 0 • SR2F[7] = 1 • CR50[3] = 0
(ACTI)			**ACTIVITY**: When the Extension register conditions mentioned in the pin introduction above are all true *and* Extension register SR23[6] = 1, this pin is configured for ACTI, an optional activity-sense input. In this case, any low-to-high transition on this pin can be used to reset the internal power-down timers. As a result, when the ACTI input is: • *Low*, there is no reset. • *High, and* Extension register: — CR2D[6] = 1, then ACTI resets the Standby mode timer. — CR2D[3] = 1, then ACTI resets the Backlight timer.
(SBYI)			**STANDBY INPUT:** When the Extension register conditions mentioned in the pin introduction above are all true and Extension register SR23[6] = 0, this pin is configured for SBYI, the hardware control for Standby mode. When SBYI: • Goes high, then SBYI initiates the power-down sequence that starts the Standby mode. • Is not used, then the SBYI pin must be connected to ground.
BLI / SUSPI	87	I	**BACKLIGHT INPUT / SUSPEND INPUT:** As described under Extension register bit SR23[5], this pin can be configured for either its BLI or SUSPI function when Extension register bit SR24[7] = 0.
(BLI)			**BACKLIGHT INPUT:** When Extension register bit SR24[7] = 1 and Extension register SR23[5] = 1, a high on this input turns off the backlight of the LCD display.
(SUSPI)			**SUSPEND INPUT:** When Extension register bit SR24[7] = 0 and SR23[5] = 0, a high on this internally de-bounced input initiates hardware-controlled Suspend mode. The hardware-controlled Suspend mode is the most-efficient power-saving mode for the system.

2.11 Power-Management Pins *(cont.)*

Pin Name	Pin No.	Type	Pin Description
CLK32K	89	I	**32-kHz CLOCK:** This input can be connected to an externally supplied 32-kHz clock signal that can be used for memory refresh during Suspend mode and panel sequencing. If this pin is not used, it must be connected to the CL-GD7548 OSC pin.
FPBL	105	O	**FLAT PANEL BACKLIGHT:** This output is part of LCD power sequencing. This pin must be connected to the LCD backlight enable.
FPVCC	106	O	**FLAT PANEL VCC:** This output is part of LCD power sequencing. This pin must be connected to the LCD logic power enable.
FPVEE	102	O	**FLAT PANEL VEE:** This output is part of LCD power sequencing. This pin must be connected to the LCD power enable.
PROG	148	O	**PROGRAMMABLE OUTPUT:** This output pin is forced high or low under the control of Extension register CR30[7]. It is used by the VGA BIOS to select 3.3- or 5.0-V power supplies to support the operating frequencies selected.
SBYI	86	I	**STANDBY INPUT:** For the description of how pin 86 is used for the Standby mode function, within this table refer to pin name ACTI / SBYI.
SBYST#	123	O	**STANDBY STATUS#:** This active-low output, when low, indicates that the CL-GD7548 is in Standby mode.
SLEEP#	81	I	**SLEEP#:** This active-low input is used by the external hardware to put the CL-GD7548 into bus Sleep mode. When this input is low, the memory and I/O interfaces are disabled. Once this pin is low, no other chip access is possible until this pin goes high.
SUSPI	87	I	**SUSPEND INPUT:** For the description of how pin 87 is used for the Suspend mode function, within this table refer to pin name BLI / SUSPI.
SUSPST#	125	O	**SUSPEND STATUS#:** This active-low output, when low, indicates that the CL-GD7548 is in Suspend mode.

2.12 Ground Pins

This section lists the ground pins for the CL-GD7548. However, other sections in this chapter also list information on correct grounding procedures and must also be consulted.

Pin Name	Pin No.	Pin Description
DACVSS2, DACVSS1	111, 88	**DIGITAL-TO-ANALOG CONVERTER VSS GROUND [2:1]:** These two pins are used to supply ground reference to the palette DAC of the CL-GD7548. Each pin *must* be connected to the analog ground rail, which must be isolated from VSS (digital) ground.
MAVSS	201	**MEMORY CLOCK ANALOG VSS GROUND:** This pin is used to supply ground reference to the memory clock synthesizer of the CL-GD7548. This pin *must* be connected to the analog ground rail, which must be isolated from VSS (digital) ground.
VAVSS	82	**VIDEO CLOCK ANALOG VSS GROUND:** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD7548. This pin *must* be connected to the analog ground rail, which must be isolated from VSS (digital) ground.
VSS11, VSS10, VSS9, VSS8, VSS7, VSS6, VSS5, VSS4, VSS3, VSS2, VSS1	198, 185, 168, 145, 124, 104, 80, 67, 52, 42, 6	**VSS (Digital) GROUND [11:1]:** These pins are used to supply ground reference for the core logic and pin interface groups of the CL-GD7548. • Each pin *must* be connected directly to the ground rail. • When a multi-layer board is used, each VSS pin *must* be connected to the ground plane.

2.13 Power Pins

For information on the programmable core voltage, refer to Section 3.6.4.

Pin Name	Pin No.	Pin Description
BVDD2, BVDD1	47, 73	**BUS VDD [2:1]:** These two pins are used to supply either +3.3 or +5.0 V to the bus interface pin group of the CL-GD7548. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. • When a multi-layer board is used, connect BVDD pins to the power plane.
CRTVDD	92	**CRT VDD:** This pin is used to supply +3.3 or +5.0 V to the CRT interface pin group of the CL-GD7548. • This pin *must* be connected directly to the VDD rail. • This pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible. • When a multi-layer board is used, connect the CRTVDD pin to the power plane.
CVDD4, CVDD3, CVDD2, CVDD1	192, 121, 62, 36	**CORE VDD [4:1]:** These four pins are used to supply +3.3 or +5.0 V to the internal core logic of the CL-GD7548. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. • When a multi-layer board is used, connect CVDD pins to the power plane.
DACVDD2, DACVDD1	109, 90	**DIGITAL-TO-ANALOG CONVERTER VDD [2:1]:** These two pins are used to supply voltage to the palette DAC of the CL-GD7548. • Each pin *must* be connected directly to the CVDD rail. • Each pin *must* be bypassed with 0.1- and 10-µF capacitors that have the proper high-frequency characteristics and are as close to each pin as possible. • When a multi-layer board is used, connect DACVDD pins to the power plane.
FPVDD2, FPVDD1	107, 132	**FLAT PANEL VDD [2:1]:** These two pins are used to supply +3.3 or +5.0 V to the LCD flat panel interface pin group of the CL-GD7548. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to the pin as possible. • When a multi-layer board is used, connect FPVDD pins to the power plane.

2.13 Power Pins *(cont.)*

Pin Name	Pin No.	Pin Description
MAVDD	199	**MCLK ANALOG VDD:** This pin is used to supply +3.3 or +5.0 V to the memory clock synthesizer of the CL-GD7548. This pin *must* be connected to the CVDD rail through a 33-Ω resistor and bypassed to MAVSS with 0.1- and 10-µF capacitors.
MVDD2, MVDD1	162, 205	**MEMORY VDD [2:1]:** These two pins are used to supply +3.3 or +5.0 V to the display memory interface pin group of the CL-GD7548. • Each pin *must* be connected directly to the VDD rail. • Each pin *must* be bypassed with a 0.1-µF capacitor that has the proper high-frequency characteristics and is as close to each pin as possible. • When a multi-layer board is used, connect MVDD pins to the power plane.
VAVDD	84	**VCLK ANALOG VDD:** This pin is used to supply +3.3 or +5.0 V to the video clock synthesizer of the CL-GD7548. This pin *must* be connected to the CVDD rail via a 33-Ω resistor and bypassed to VAVSS with 0.1- and 10-µF capacitors.

3. FUNCTIONAL DESCRIPTION

This section provides functional information and design guidelines for the CL-GD7548 Graphics User Interface Accelerator (GUIX) SVGA LCD Controller with enhanced MVA™.

3.1 Introduction

The CL-GD7548 provides a high-performance LCD/CRT graphics subsystem with a wide range of cost-effective multimedia features. These multimedia features include video playback acceleration of MPEG, Cinepak, Indeo, or TrueMotion files, video capture, live video, and so forth – all with continuous upscaling to resolutions up to 1024 x 768.

An additional multimedia feature is the CL-GD7548 V-Port™, which transfers a video data stream into the display memory. This feature enables a low-cost multimedia solution without the need for external video-processing hardware and additional display memory. The V-Port may also be used to enable multimedia through PCMCIA multimedia cards.

The CL-GD7548 offers a tightly integrated, high-performance motherboard solution. Multiple designs can be developed, ranging from a relatively simple GUIX solution to a portable multimedia solution capable of displaying accelerated video playback windows with graphics or live video windows with graphics. All hardware necessary for host CPU updates to memory, display refresh, and DRAM refresh is included in the CL-GD7548. By eliminating the need for an additional video frame buffer and providing a dedicated path to a PCMCIA card, the CL-GD7548 V-Port enables high-quality, low-cost multimedia options such as a single-chip NTSC/PAL decoder or MPEG decoder. A complete XGA/SVGA-compatible motherboard solution can be implemented with the CL-GD7548 plus two 256 x 16 DRAMs.

The CL-GD7548 is pin- and software-compatible with the CL-GD7543. As a result, a single hardware design and software suite may be used for both the CL-GD7548 (for high-end, full-feature multimedia applications) and the CL-GD7543 (for price-sensitive, mid-range applications requiring less features).

NOTE: For details on designing with the CL-GD7548 by using the CL-GD7543, refer to the application note "Video Upgrade Path" in the *CL-GD754X Application Book*.

3.1.1 Features Common with the CL-GD7543

The CL-GD7548 maintains many key features of the CL-GD7543, including:

- BitBLT engine
- Support for 640 x 480 and 800 x 600 color TFT and dual-scan STN LCDs with SimulSCAN™
- Compatibility with industry-standard compression formats (such as Cinepak, Indeo, and MPEG)
- 32-bit VESA VL-Bus and PCI bus interface
- Mixed-voltage operation (3.3 V and 5 V)
- Hardware cursor and hardware icons
- Hardware dithering, centering, expansion, and frame-rate modulation for an area of up to 800 x 600
- Integrated RAMDAC and frequency synthesizer
- MotionVideo Acceleration (MVA™)
  - — Multi-format frame buffer, which provides mixed graphics and video color depths
  - — Integrated color space format converter (from 4:2:2 YCrCb to RGB 8-8-8)
  - — True-color, full-motion video playback
- Interface to analog encoders for NTSC/PAL output
- 8-bit Video Overlay

3.1.2 Enhanced Features over the CL-GD7543

The CL-GD7548 enhancements over the CL-GD7543 include the following:

- Graphics performance upgrade
  - — BitBLT engine improvements: memory-mapped I/O, double buffering, and auto start
  - — Memory clock improvements: MCLK of 66 MHz at 5 V; 54 MHz at 3.3 V
  - — Optimized support for EDO DRAMs, with down to 30-ns page-cycle time
- Enhanced Video Window:
  - — Full MotionVideo™ Acceleration support for TFT and STN color LCDs
  - — Continuous upscaling capability (1x to 4x)
    - — Horizontal linear upscaling (1x to 4x) with interpolation
    - — Vertical linear upscaling (1x to 4x) with selective replication
  - — Support for AccuPak™ color space format converter:
    - — 1024 x 768 upscaling with AccuPak™ format
    - — Decompression of video data at display time
    - — Compression of video data at display time, through the V-Port™
  - — Supports the following color space formats:
    - — CCIR 601 specification for YUV
    - — RGB 5-5-5
    - — AccuPak™ (8-bit) color space formats
  - — Double-word (2- or 4-pixel) Video Window alignment
- V-Port™ (a flexible video port)
  - — Flexible interface for standard TV/video and MPEG decoders
  - — Eliminates the need for separate video windowing controller and additional video frame buffer, enabling cost-effective live-video and video-capturing solutions
  - — 8-bit V-Port™ with VESA VL-Bus to display memory
  - — 16-bit V-Port™ with PCI bus to display memory
  - — Support for low-cost multimedia interface solution, using PCMCIA cards
  - — Single-chip live video solution, with interface to CL-PX4072 that does not require external logic.
  - — Two-chip MPEG playback solution
- VPM (V-Port™ Manager) for DCI (Display Control Interface) 1.x and DirectVideo/DirectDraw
- Support for DDC 2b (VESA Display Data Channel Level 2B serial interface protocol) allows serial programming interface to decoders (video, audio, and MPEG devices)
- Independent dual apertures with PCI or VESA VL-Bus. Dual apertures allow selection of separate graphics and video data paths from the host CPU.
  - — PCI retry in second aperture.
- LCD interface enhancements:
  - — Support for 1024 x 768 color TFT LCDs (2-pixel/shift clock with external multiplexor)

3.2 Enhanced MotionVideo Acceleration (MVA™)

3.2.1 Overview

MotionVideo Acceleration (MVA™) enables a wide range of cost-effective multimedia video capabilities to be implemented with a minimal graphics sub-system, consisting of the CL-GD7548 and two 256K x 16 DRAMs. These multimedia video capabilities include:

- Full-screen, high-quality video playback of software-decompressed DCI-compatible video clips, such as CinePak, Indeo, TrueMotion, or MPEG files from a CD-ROM or hard disk. This option requires no additional hardware, and consequently, no incremental cost.
- Hardware MPEG decoder located on the motherboard or as part of a PCMCIA card option for video playback of MPEG files from a CD-ROM or hard disk. With this option, the hardware MPEG solution (for example, an MPEG decoder, 256K x 16 DRAM, and an ASIC) can be implemented at a minimal cost and with minimum use of board space, since the V-Port and MotionVideo Acceleration eliminates the need for an external video windowing controller and additional video frame buffer.
- Playback of live video from an analog source (for example, a standard television set, a VCR, or camcorder). Since MotionVideo Acceleration eliminates the need for an external video windowing controller and additional video frame buffer, a single-chip NTSC/PAL decoder can be implemented on the motherboard or as part of a PCMCIA card option for a cost-effective solution.
- Playback of live video that has been sent over the PCI or VESA VL-Bus. This option is useful for adding multimedia features to a docking station that has a PCI interface to the notebook motherboard.

With MotionVideo Acceleration, video from the above decoders is displayed with 256-color graphics on the following types of LCDs, all of which can also use the SimulSCAN option (that is, simultaneous LCD and CRT operation):

- 640 x 480 color TFT or DSTN LCDs
- 800 x 600 color TFT or DSTN LCDs
- 1024 x 768 color TFT LCDs

MVA continuously scales the video from its source size to a full-screen size. In addition, MVA maintains both the original frame rate of the video (for example, 24 to 30 frames per second) and the original color depth (for example, 32K or 16M colors).

The CL-GD7548 design is optimized for this high performance, all within the bandwidth constraints of a 32-bit display memory interface. Furthermore, the design is optimized to achieve this performance without the cost of additional components (such as two additional 256K x 16 DRAMs) to expand the interface to 64 bits or requiring the motherboard to consume additional power.

As with the CL-GD7543, the CL-GD7548 can display video data from the 8-bit Feature Connector over graphics data. In this mode of operation, video data bypasses the display memory and all the MotionVideo Acceleration circuitry. For details on this mode, refer to Section 3.4.

As shown in Figure 3-1, the CL-GD7548 MotionVideo Acceleration feature set consists of the front-end video pipeline, the MotionVideo™ Memory part of display memory, and the back-end video pipeline.

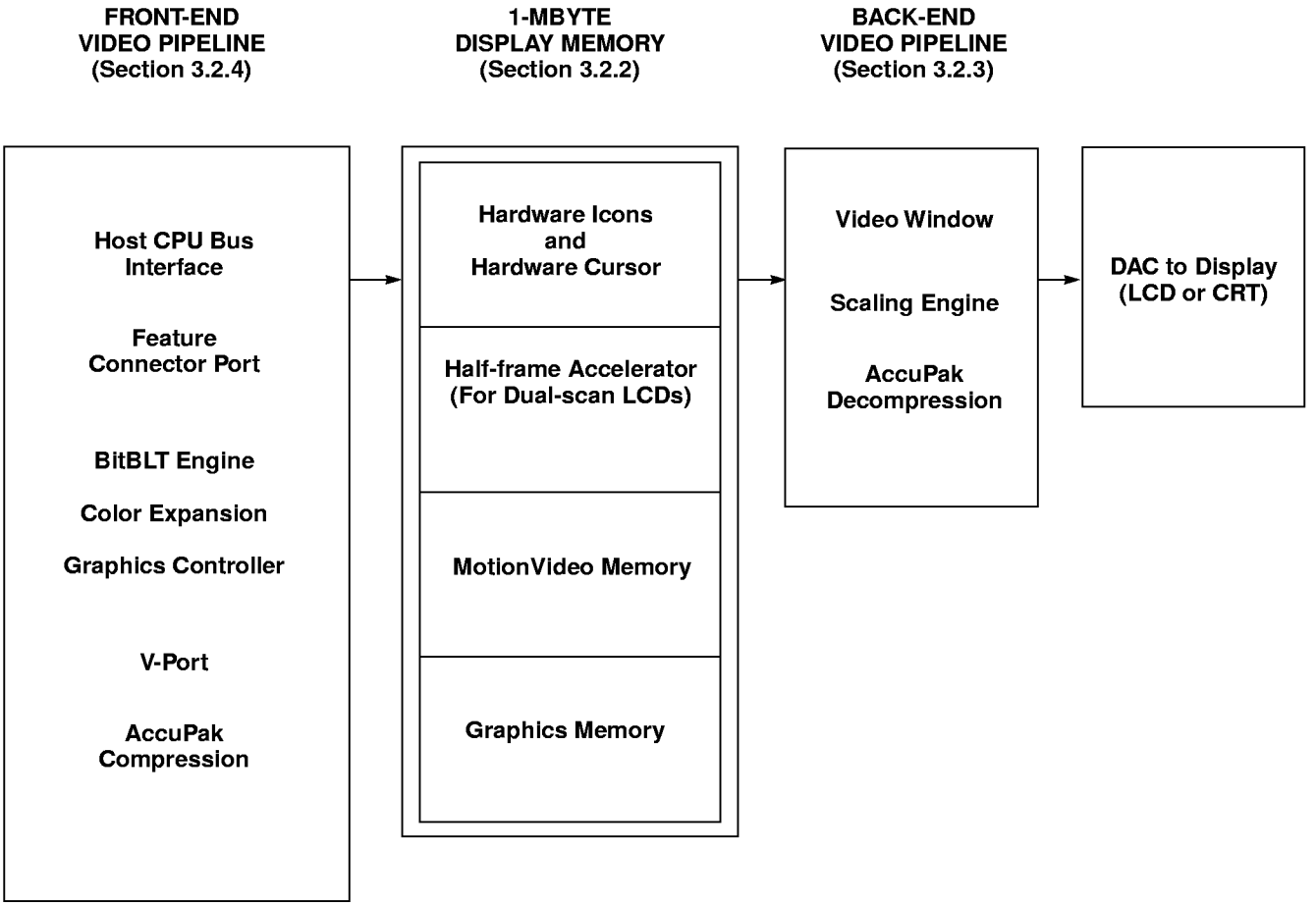


Figure 3-1. The MotionVideo™ Acceleration Feature Set

Front-End Video Pipeline

The front-end video pipeline, discussed in detail in Section 3.2.4, has two video input paths:

- **Bus Video-to-Memory Mode**: In this mode, the host CPU or other bus master transfers video data from the input sources through the PCI bus or VESA VL-Bus. With this mode, occlusion (the event that occurs when a graphics window overwrites and hides a portion of the Video Window) is not possible through hardware acceleration, but is possible through software.
- **V-Port-to-Memory Mode**: In this mode, the 8-/16-bit V-Port transfers video data directly to MotionVideo Memory for storage. This mode enables a low-cost graphics solution, since the need for an external video windowing controller and video frame buffer is eliminated. (Although occlusion of the MPEG or NTSC/PAL Video Window is not possible in the V-Port-to-Memory mode, occlusion is possible with the Video Overlay mode, as discussed in Section 3.4.)

MotionVideo Memory

MotionVideo Memory, discussed in detail in Section 3.2.2, is the video portion of the shared frame buffer that is in an area of off-screen memory. The off-screen MotionVideo Memory is independent from the on-screen graphics memory. MotionVideo Memory supports the following:

- Elimination of the need for external video windowing controller and additional video frame buffer to perform the de-interlacing and timing synchronization of the video and graphics data streams.

  As a result, a hardware MPEG or NTSC/PAL decoder can be implemented at a minimal cost and with minimum power consumption and use of board space.
- Mixed color depths to display the Video Window in a higher color depth (typically 32K or 16M colors) than the surrounding graphics mode (typically 256 colors).

  As a result, memory storage and bandwidth requirements are reduced and graphics performance is increased.

Back-End Video Pipeline

The back-end video pipeline, discussed in detail in Section 3.2.3, includes the following features:

- YUV-to-RGB color space format converter. Storing video data in the YUV color space format reduces by 50% the memory storage and bandwidth requirements.
- Control logic for flexible positioning of the Video Window.
- Upscaling engine that can continuously scale the Video Window from the size of the video source to a full-screen size (up to 1024 x 768). During upscaling, the upscaling engine maintains the color depth and frame rate of the video source.
- Video Window dithering logic for flat panels. This dithering logic is independent of the surrounding graphics. Spatial dithering can be used to eliminate contouring in images.

In all cases, in the front-end pipeline the video data is not processed (except for optional AccuPak compression in the V-Port-to-Memory mode). As a result, data can be transferred without the risk of imposing wait states on the host CPU bus. During display time, all video processing and conversion of color space formats is done in the back-end pipeline.

3.2.2 MotionVideo™ Memory

Introduction

The CL-GD7548 display memory is organized as a unified graphics / video frame buffer. As shown in Figure 3-2, MotionVideo Memory, the video portion of this shared frame buffer, is an area of off-screen memory that is:

- *Above* graphics memory (where pixel data for standard and extended VGA display modes is stored).
- *Below* the last 16 Kbytes of display memory (where data for the hardware cursor and icons is stored).

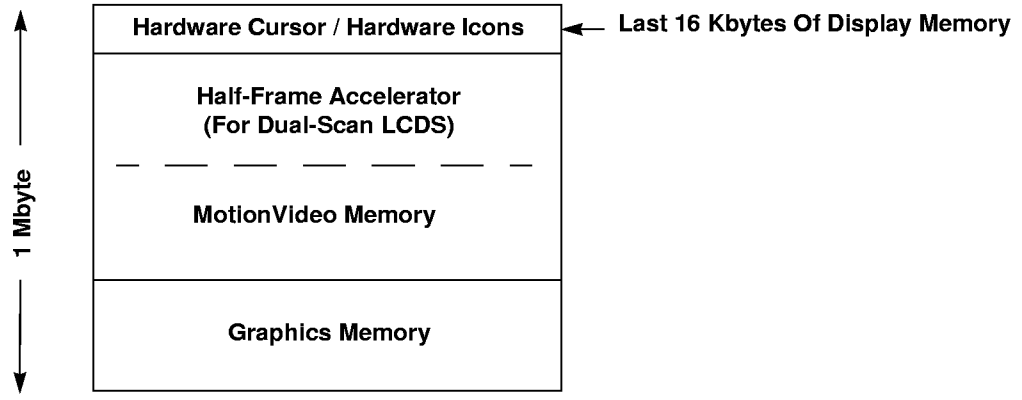


Figure 3-2. MotionVideo™ Memory – Stored as Part of Display Memory

Because MotionVideo Memory is independent from graphics data, it supports:

- Elimination of the need for an external video windowing controller and additional video frame buffer to perform the de-interlacing and timing synchronization of the video and graphics data streams. As a result, a hardware MPEG or NTSC/PAL decoder can be implemented at a minimal cost and with minimum power consumption and use of board space.
  - — For video input from an analog source (for example, a standard television, a VCR, or a camcorder), the only external hardware that is required is a low-cost, single-chip NTSC/PAL decoder (such as the CL-PX4072 or the Philips® SAA7110).
  - — For MPEG video, the only required external hardware is a single-chip MPEG decoder and MPEG frame buffer (for example, the Zoran™ 36100 or C-Cube CL-480 decoders and a single 256K x 16 DRAM).
- Mixed color depths to display the Video Window in a higher color depth (typically 32K or 16M colors) than the surrounding graphics display mode (typically 256 colors). Requirements for memory storage, bandwidth, and Windows resources are reduced. Graphics performance is increased, since the surrounding graphics operate in a 256-color display mode rather than a 32K- or 16M-color display mode.

The video data for the Video Window is stored in MotionVideo Memory, which is located in any available contiguous off-screen display memory space. The amount of display memory available for MotionVideo Memory is calculated with the following equation.

$$\text{MotionVideo Memory} = \text{DMEM} - \text{GMEM} - \text{ACEL} - 16\ \text{Kbytes} \qquad \textbf{Equation 3-1}$$

where:

DMEM	=	Total available (DRAM) memory
GMEM	=	Memory required for graphics
ACEL	=	Memory required to support the half-frame accelerator required for dual-scan STN LCDs
16 Kbytes	=	Memory reserved for hardware cursor and hardware icon

During display refresh, data is accessed from either MotionVideo Memory or graphics memory on a pixel-by-pixel basis, with options for either 2- or 4-pixel alignment. No double accesses to display memory are required, alleviating the display memory bandwidth bottleneck. Consequently, the MVA optimizes display memory bandwidth usage while minimizing the amount of display memory that is required. With only 1 Mbyte of display memory, high-quality Video Windows can be displayed in the high-resolution graphics display modes.

The Video Window resolution is determined by the source data. By using hardware scaling, the size of the Video Window can be continuously upscaled horizontally and vertically on the display without a corresponding decrease in performance.

NOTE: The Video Windows can use several aspect ratios and are not limited to a 4:3 aspect ratio.

3.2.2.1 MotionVideo Memory Color Space Formats

The MotionVideo Memory supports several color space formats:

- YUV color space format (typically used for MPEG or live video from a TV decoder)
- RGB 5-5-5 color space format (typically used for Indeo, Cinepak, or TrueMotion)
- Using AccuPak to convert color space formats. AccuPak, a proprietary Cirrus Logic algorithm, converts 4:2:2 YUV video data to an 8-bit/pixel color space format that enables the capture and display of high-color video quality.
  - — With video data coming through the V-Port-to-Memory path, AccuPak provides a 2:1 video data compression by encoding 4 pixels in 32 bits (averaging 8 bits/pixel).
  - — Compression is done through the V-Port data path, but the AccuPak color space format must be precompressed if it is coming through the local bus.
  - — For display on either a CRT monitor or a flat panel, the 8-bit/pixel color space format is decompressed (that is, converted back) to an RGB 8-8-8 color space format.

NOTE: The RGB 8-8-8 color space format is not typically used with the MotionVideo Memory. However, it is used to create a 1x clock for a 24-bit/pixel window. For more information, refer to Section 3.2.2.2.

3.2.2.2 Video Window

The MVA hardware creates a Video Window that uses off-screen memory. The Video Window is displayed on top of the VGA graphics display mode data, and the hardware icons and hardware cursor are displayed on top of the Video Window.

The Video Window functions as an overlay image that can be positioned anywhere on the display screen. The position and size of the Video Window are programmable by using Extension registers CR31–CR3F, with with options for either 1-, 2-, or 4-pixel resolution and 1-scanline vertical resolution. Using SimulSCAN, the Video Window can be displayed simultaneously on both CRT monitors and flat panels that have one of the following resolutions:

- 640 × 480
- 800 × 600
- 1024 × 768

With MVA, the display memory becomes a multi-format display memory. As a result, different color depths and data formats can be mixed in the Video Window display, as explained in the following list:

- The color depth of the Video Window is independent of the color depth of surrounding graphics.
  - For example, a Video Window can operate in a 24-bits/pixel display mode, while the surrounding graphics operate in a 8-bits/pixel dispaly mode.
- The data format of the Video Window is independent of the data format of the surrounding graphics.
  - For example, YUV video data can be stored with 8-bit RGB graphics data in display memory. Compared to RGB, YUV data requires less storage size, since YUV uses 16 bits/pixel on average to provide the same color quality as 24-bit/pixel RGB display modes for television-quality images.

If the flat panel color resolution is less than 24 bits/pixel, the MVA dithering algorithm can be used by programming Extension registers CR4D and CR4E to increase the displayed color depth to 24 bits/pixel, independently of the graphics color resolution.

3.2.3 Back-End Video Pipeline

Introduction

The MVA back-end video pipeline includes the following features:

- Control logic for positioning the Video Window
- A YUV-to-RGB color space format converter
- Upscaling engine
- Video Window dithering logic
- Video Window contrast and brightness control

3.2.3.1 Video Window Control Logic

The Video Window control logic, included in Extension registers CR33–CR3D, defines the dimensions and positioning of the Video Window, as well as the encoding logic for the Video Window. It allows for flexible positioning of the Video Window within the surrounding graphics, with 2- or 4-pixel horizontal alignment and 1-scanline vertical alignment.

In addition, special Video Window control logic features include the following:

- Faster MVA FIFO fill (Extension register CR33)
- Options for YUV-to-RGB conversion algorithms
- Options for 2's complement notation (Extension register CR36)

3.2.3.2 YUV-to-RGB Color Space Format Converter

The YUV-to-RGB color space format converter, included in the Extension registers, converts YUV video data that is stored in the MotionVideo Memory to RGB 8-8-8 for display. As a result, the converter reduces memory storage and bandwidth requirements by 50% since YUV, which is 16 bits/pixel, is a more efficient color format than the 24-bit/pixel RGB 8-8-8 format

The CL-GD7548 YUV-to-RGB color space format converter is compatible with the CCIR 601 specification. The 'Y' value is defined as having a nominal range of 16 to 235. The YUV chrominance and luminance values are defined as having a nominal range of 16 to 240. The center of this range, at 128, is set equal to zero.

3.2.3.3 Upscaling Engine

The upscaling engine, included in Extension registers CR31 and CR32, can continuously scale the Video Window from the video source size (for example, 320 x 240, 352 x 240, or 640 x 480) to a full-screen size (for example, 640 x 480, 800 x 600, or 1024 x 768). During upscaling, the upscaling engine maintains the video source color depth (typically 32K or 16M colors) and frame rate (typically 24 to 30 frames/sec).

For magnification beyond 2x, hardware integer scaling occurs as follows:

- Extension registers CR31, CR3F, and CR5D[3:0] allow the scaling of horizontal pixels. If Extension register CR3F[7] is:
  - — 0, the horizontal pixels are replicated
  - — 1, the horizontal pixels are interpolated
- Extension registers CR32 and CR5D[7:4] allow the scaling of vertical scanlines. Vertical scaling adds lines by replication only.

3.2.3.4 Video Window Dithering Logic

The Video Window dithering logic, included in the CR4C and CR4D Extension registers, defines the dithering matrix (the number of primary red, green, and blue color) to use, depending upon the combination of the color display mode being displayed and the type of display device being used. In addition, it defines the resolution of the input and output for dithering.

The dithering logic for the Video Window is independent of the surrounding graphics. Spatial dithering may be used on the flat panel to increase the color depth of the Video Window without affecting the dithering used for the surrounding graphics. By using spatial dithering, the CL-GD7548 can increase the flat panel color palette by creating up to 6 bits per primary color RGB. When using the Video Window to display images, spatial dithering is effective for eliminating contouring. However, when using the Video Window to display text, spatial dithering may create artifacts.

3.2.4 Front-End Video Pipeline

Introduction

The MVA front-end video pipeline can handle simultaneous input video data streams as long as they have the same video color space format:

- **Bus Video Mode**: In this mode, the host CPU or other bus master transfers video data from video data input sources through the PCI bus or VESA VL-Bus, and the data is stored in MotionVideo Memory.

  Examples of host CPU bus video data input sources include:

  — DCI-compatible files, which are transferred to the CL-GD7548 through the host CPU bus.

  — An MPEG or NTSC/PAL decoder that interfaces to the host CPU bus.

- **V-Port™-to-Memory Mode**: In this mode, the 8-/16-bit V-Port transfers video data directly to MotionVideo Memory for storage. This mode enables a low-cost implementation, since the need for an external video windowing controller and video frame buffer is eliminated.

  Examples of V-Port-to-Memory video data input sources include the following, both of which provide 8- or 16-bit data in a color space format:

  — An MPEG decoder

  — An NTSC/PAL decoder

With both of these modes, occlusion of the MPEG or NTSC/PAL Video Window is not possible through hardware, as the Video Window either reverts to 256 colors or to a slow frame rate through software-only control. (Occlusion refers to the event that occurs when a graphics window overwrites and hides a portion of the Video Window. For information on how the CL-GD7548 supports occlusion, refer to Section 3.4.)

3.2.4.1 Bus Video Mode

In Bus Video mode, video data is delivered through a bus from a live source or hardware/software decoders (for example, MPEG, Cinepak, or Indeo decoders) that operate on files stored on devices that are connected to the bus (for example, CD-ROM or hard disk drives).

The CL-GD7548 supports two independent 'apertures' in both PCI and VESA VL-Bus configurations. With the PCI bus, the CL-GD7548 supports two little-endian apertures (one video, one graphics) or two big-endian apertures. The video data, once it has been stored in the MotionVideo Memory, may be played back through the CL-GD7548 back-end video pipeline.

Apertures

The handling of different representations of pixel data is common in multimedia applications. Transformations from one format to another are done to reduce data rate and storage area requirements, to simplify numerical manipulation, or both. To support multiple, simultaneous views of a shared pixel data storage area, the PCI bus architecture introduced the concept of 'apertures' (that is, logical partitions).

An aperture is a 'logical' view of a pixel buffer. Apertures have attributes that distinguish them from each other and which specify the actions of the hardware controller as well as the device driver software when accesses to the aperture are made. Among these attributes are:

- Logical pixel format - color space format, and big-endian and little-endian logic
- Logical frame buffer size and organization - base-address, width, height, read-write attributes
- Physical mapping - location of the logical view within the physical buffer

Primary (Graphics) Aperture

The Primary Aperture (also known as the Graphics Aperture) is the aperture that views the frame buffer from the perspective of a Super VGA controller.

Secondary (Video) Aperture

The front-end video pipeline provides a single data path, referred to as the Secondary Aperture, into the frame buffer that is completely independent of the Graphics Aperture. The Secondary (also known as the Video Aperture) views the frame buffer through the perspective of a video subsystem with special needs for pixel depth, image resolution, storage format, and so forth.

The Secondary Aperture allows devices to place data (either video or graphics) in the frame buffer without interfering with any operations occurring at the Graphics Aperture. For example, a BitBLT operation, in Microsoft Windows, could be in progress while a live video data stream is being shown through the Secondary Aperture. Under this environment, there are no graphics artifacts such as a clock stopping. Note that a BitBLT operation always utilizes the Graphics Aperture and a video data stream must then use the Secondary Aperture.

The CL-GD7548 minimizes the software overhead required to configure graphics-specific registers because the Secondary Aperture is mapped into a unique host CPU address range that is implicitly identified with this aperture. This mapping scheme is the CL-GD7548 "dual aperture" architecture and complies with the PCI Multimedia Design Guideline version 2.0.

Both the Graphics and Secondary Apertures have their own host CPU address offset registers, and address processing is totally independent. This approach allows two independent data pipelines, one for graphics and one for video, into the frame buffer. On either a PCI bus or a VESA VL-Bus platform, any device that is a bus master can drive the bus at any time. A bus master must provide an address to the frame buffer through the Secondary Aperture, allowing it to modify data in the frame buffer without disrupting any graphics operations being executed by the system host CPU through the display driver.

Video occlusion is supported through the DCI (Display Control Interface) driver when video data is coming through the local bus. When occlusion occurs, the DCI driver manages the occlusion and hardware acceleration is disabled.

PCI Bus Universal Retry (External/General Register PCI10)

When transmitting host CPU bus video data, an important part of the automatic video aperture detection is the 'universal bus retry' mechanism. When a PCI bus master attempts to send video data over the PCI bus at the same time that a BitBLT with graphics data is in progress, contention for access to the bus must be resolved.

One method for resolving the bus contention is to try to avoid it. For example, before writing data to the address for the video aperture, the video software driver constantly polls to see if a BitBLT is in progress. However, this method of resolving bus contention is slow, and performance suffers.

A better method for resolving the bus contention is to support a PCI bus universal retry function. With this method, while a BitBLT operation is in progress in the standard aperture (that is, Aperture 0), the universal retry function automatically asserts a PCI bus retry for any memory write attempts to a video aperture (in this case, Aperture 1). This PCI bus retry function is available even in the case of system-to-screen BitBLTs.

Bus Video Mode Application Example: Video Playback

Video playback is the display of digitally stored video, from a CD-ROM or hard disk drive, onto a display-screen. Typically, video playback involves the following:

- Digitally stored video is captured at 24-bpp color depth.
- The typical frame rate of digitally stored video varies from 15 to 30 fps (frames per second). A frame rate of 24 to 30 fps is considered full-motion video (that is, video that appears to be smooth and natural, without excessive jerking).
- The typical source size (that is, the original size of the captured video clip) ranges from 160 x 120 pixels up to 352 x 240 pixels.

Through the DCI (Display Control Interface) standard, the CL-GD7548 supports video playback acceleration of MPEG or Video for Windows .AVI files. Codecs that the CL-GD7548 supports include the following:

- **Cinepak, Indeo, and TrueMotion codecs.** These software-based codecs (called 'clients') support the DCI standard. Typically, the current versions (Cinepak 1.0 and Indeo 3.2) can provide capture and playback of up to 320 x 240 video source data at up to 24 to 30 fps. (The CL-GD7548 supports the Cinepak and Indeo codecs, both of which provide 8-bit, 15-bit, and 24-bit RGB data output formats.)
- **MPEG-1 codec.** The MPEG-1 SIF (Source Image Format) codec standard defines a 352 x 240 video data source that has been captured at up to 30 fps. Traditionally, MPEG decoders have been hardware-based, but software-based decoders running on a 90-MHz Pentium can provide acceptable video playback rates.

Features that have been added to the CL-GD7548 that enhance video playback include the following:

- Continuous upscaling of source video during video playback.
- Color space format conversion enhancements: Codecs (software compressors/decompressors) that provide YUV data can have the data converted by the CL-GD7548 hardware (and thereby not use the CPU to do the software conversion) in order to provide 16M-color video display quality.
- Mixed-color depth display. While running graphics data in the Windows environment in a 256-color display mode, a video window can be simultaneously opened to 32k/64k colors (that is 15- or 16-bpp RGB) or 16M colors (YUV).

For video playback, the hardware scaling feature can be used to size the Video Window horizontally, vertically, or both horizontally and vertically. To display video data that is stored in YUV format, the integrated YUV:RGB color space format converter converts YUV to RGB 8-8-8.

Figure 3-3 shows a 4:2:2 YUV color space format 352 × 240 video clip (in RGB 8-8-8 color space format) displayed as a 16M-color 640 × 480 Video Window on a 256-color 800 × 600 display screen. This video operation can be accomplished using just 1 Mbyte of display memory. (For a description of the 24-bit/pixel RGB format, refer to Section 3.5.13.)

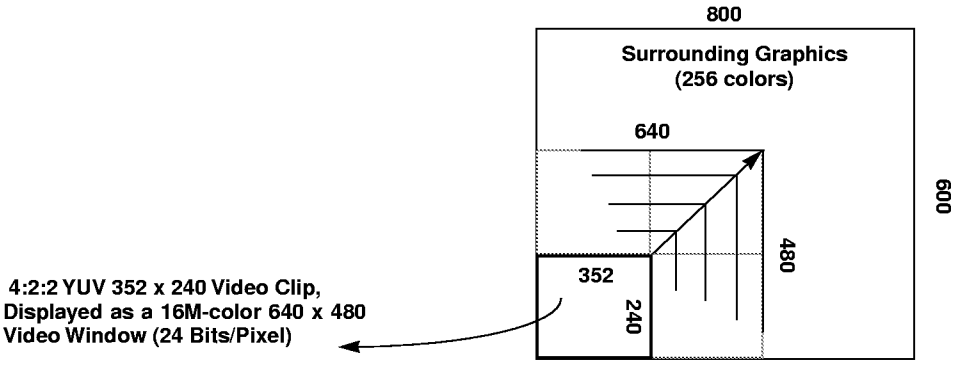


Figure 3-3. Sizing a Video Window

Table 3-1 shows the system performance that is possible when data is transferred from a video source through a local bus to a display in a 'Type 1' system, which is explained in the table note below.

Table 3-1. Bus Video Mode Performance: System Type 1 [a]

Display Resolution	Video Source		Display of Video Window			
			Single-Scan LCD / SimulSCAN™ Mode		Dual-Scan LCD / SimulSCAN™ Mode	
	Resolution	Data Format	Scaled Resolution [b]	Color Depth	Scaled Resolution [b]	Color Depth
640 x 480 256 Colors 60 Hz	320 x 240	AccuPak (8-bit)	320 x 240 ⇒ 640 x 480	~ 32K [c]	320 x 240 ⇒ 640 x 480	~ 32K [c]
		RGB 5-5-5	320 x 240 ⇒ 640 x 480	32K	320 x 240 ⇒ 640 x 480	32K
		4:2:2 YUV	320 x 240 ⇒ 640 x 480	16M	320 x 240 ⇒ 640 x 480	16M
800 x 600 256 Colors 60 Hz	320 x 240	AccuPak (8-bit)	320 x 240 ⇒ 800 x 600	~ 32K [c]	320 x 240 ⇒ 800 x 600	~ 32K [c]
		RGB 5-5-5	320 x 240 ⇒ 800 x 600	32K	640 x 480 ⇒ 800 x 600	32K
		4:2:2 YUV	320 x 240 ⇒ 800 x 600	16M	640 x 480 ⇒ 800 x 600	16M
1024 x 768 256 Colors 60 Hz	320 x 240	AccuPak (8-bit)	320 x 240 ⇒ 1024 x 768	~ 16M [c]	Not available	–

a. System Type 1 has the following features:
   - — Either 1 or 2 Mbytes of display memory.
   - — Runs at 3.3 V.
   - — MCLK runs at a maximum of 54 MHz.
   - — Video is transferrred from a video source to a display through a local bus.

b. Continuous upscaling is possible from the source resolution to the display resolution, but upscaling that is more than 2x may result in a degradation in the resolution quality.

c. This color depth results from a lossy color space format conversion.

Table 3-2 shows the system performance that is possible when data is transferred from a video source through a local bus to a display in a 'Type 2' system, which is explained in the table note below.

Table 3-2. Bus Video Mode Performance: System Type 2 [a]

Display Resolution	Video Source		Display of Video Window			
			Single-Scan LCD / SimulSCAN™ Mode		Dual-Scan LCD / SimulSCAN™ Mode	
	Resolution	Data Format	Scaled Resolution [b]	Color Depth	Scaled Resolution [b]	Color Depth
640 x 480 256 Colors 60 Hz	320 x 240	AccuPak (8-bit)	320 x 240 ⇒ 640 x 480	~ 32K [c]	320 x 240 ⇒ 640 x 480	~ 32K [c]
		RGB 5-5-5	320 x 240 ⇒ 640 x 480	32K	640 x 480	32K
		4:2:2 YUV	320 x 240 ⇒ 640 x 480	16M	640 x 480	16M
800 x 600 256 Colors 60 Hz	320 x 240	AccuPak (8-bit)	320 x 240 ⇒ 800 x 600	~ 32K [c]	320 x 240 ⇒ 800 x 600	~ 32K [c]
		RGB 5-5-5	320 x 240 ⇒ 800 x 600	32K	640 x 480 ⇒ 800 x 600	32K
		4:2:2 YUV	320 x 240 ⇒ 800 x 600	16M	640 x 480 ⇒ 800 x 600	16M
1024 x 768 256 Colors 60 Hz	320 x 240	AccuPak (8-bit)	320 x 240 ⇒ 1024 x 768	~ 16M [c]	Not available	–

a. System Type 2 has the following features:
   - — Either 1 or 2 Mbytes of display memory.
   - — Runs at 5 V.
   - — MCLK runs at a maximum of 66 MHz.
   - — Video is transferrred from a video source to a display through a local bus.

b. Continuous upscaling is possible from the source resolution to the display resolution, but upscaling that is more than 2x may result in a degradation in the resolution quality.

c. This color depth results from a lossy color space format conversion.

3.2.4.2 V-Port-to-Memory Mode

The CL-GD7548 V-Port-to-Memory mode transfers video data directly from the V-Port to MotionVideo Memory for storage. Effectively, the video and graphics data share the same display memory, eliminating the need for extra memory with a resulting low-cost multimedia solution.

In addition, the CL-GD7548 can support video data in 1024 x 768 graphics modes without violating any connector specification because the rate at which video data comes through the V-Port is totally independent from the graphics display pixel clock rate of 65 MHz (for a 1024 x 768 display running at 60Hz). However, any video window displayed through the V-Port is always going to be on top of any graphics windows.

Previous LCD VGA controllers in the CL-GD754X family (that is, the CL-GD7542 and CL-GD7543) used the Video Overlay mode, which did not have a direct data path to the frame buffer. As a result, with this mode, video data coming in through a video port must be clocked in at the current display video clock rate [that is, at a rate compatible with the pixel rate at which the display (CRT or LCD) is currently being refreshed at.] The data was then dynamically switched directly to the display device, replacing data coming from display memory.

One advantage for video overlay is that with it, video occlusion is possible. However, because video overlay uses a higher clock rate, it consumes more power and is restricted to lower graphics resolution modes. (The CL-GD7548 is a pin-compatible controller to the CL-GD754X family and does continue to support this video overlay feature.)

In contrast, with the CL-GD7548, data coming in through the V-Port can be accepted at the video source rate and either stored directly in display memory or stored in a compressed format. The data transfer rate can be different, and typically lower, than the data rate at which the display is operating. As a result, the data can be simultaneously read out of the frame buffer and displayed at the display clock rate, with real-time decompression if needed.

This decoupling of the video storage and video playback clock rates allows more flexible design options. The V-Port also allows a total video/graphics solution that can be quite cost effective. For example, the V-Port can be configured to interface with various external devices in various modes, described in the sections that follow. (However, occlusion of the MPEG or NTSC/PAL Video Window is not possible.)

The V-Port-to-Memory mode therefore enables a low-cost implementation, since it eliminates the need for an external video windowing controller and an external video frame buffer. Instead, video data is delivered through the CL-GD7548 8-/16-bit V-Port.

The V-Port-to-Memory mode eliminates the need for an external video windowing controller and additional video frame buffers to perform the de-interlacing and timing synchronization of the video and graphics data streams. As a result, a hardware MPEG or NTSC/PAL decoder can be implemented at a minimal cost and with minimum power consumption and use of board space.

Examples of V-Port-to-Memory video data input sources include the following, both of which provide 8- or 16-bit data in a color space format:

- An MPEG decoder
- An NTSC/PAL decoder

V-Port Width

In a PCI bus configuration, the CL-GD7548 can operate as an 8-bit or 16-bit interface. The 16-bit interface mode was designed to be flexible in order to use minimal external logic when interfacing to other standard video or MPEG decoders. (In contrast, in a VESA VL-Bus configuration, the CL-GD7548 V-Port can operate only in an 8-bit mode.)

The V-Port data path contains an optional color space format converter that at display time converts data that is compatible with the CCIR 601 YUV specification to AccuPak, a proprietary 2x compressed format. After converting the data, the CL-GD7548 stores it in video memory and then sends it to the back-end video pipeline for subsequent display.

The V-Port-to-Memory feature is intended for live video source support and to support ASIC interfaces to various video sources. The V-Port-to-Memory mode can accept data in several different formats (such as interlaced, non-interlaced, and so forth).

V-Port™-to-Memory Signal Definitions

- PCLK (Pixel Clock)
  - This signal is used to clock valid data into the CL-GD7548. The timing of data transfer varies according to the type of data format that is used. (For more information about data transfer formats, refer to the documentation for the external video data controller.)
  - One PCLK is generated for each 16-bit pixel, whether the data is scaled or not, during both display time and non-display time. PCLK is active during the entire Vertical non-display interval.
  - The pixel clock is free-running at either 13.5 MHz or 20.25 MHz. During the time when the CL-PX4072 VACT signal is high, the falling edge of PCLK is used to clock the data into the CL-GD7548.
- VS (Vertical Start)
  - The CL-GD7548 Vertical V-Port Window Generator has programmable registers that use the trailing edge of the VS signal as a reference for the start offset. (The start offset is a signal that delays the start of the signal delineating the width for the Video Window.)
  - A 9-bit Vertical Size Register is used to control the number of lines to be captured. (The register is programmed with the actual number of lines per field of the video data to be displayed.)
- HREF (Horizontal Reference)
  - Horizontally, no programming is required, as each falling edge of PCLK corresponds to valid data for one pixel.
- VACT (Video Active)
  - VACT, a signal from the video decoder (such as the CL-PX4072), goes high when pixel data is valid on the Y and UV lines and goes low when the data is invalid.
  - VACT allows the PCLK signal to be free running. VACT is high around the time that the falling edge of PCLK has valid data.
  - For an 8-bit-wide V-Port that has double-edge clocking, only 8 bits of data are used. VACT must bracket both PCLK edges. For the CL-PX4072, the combination of the VACT and PCLK signals are equivalent to PCLK for V-Port-to-Memory with internal scaling.
  - The VACT signal is asserted when video data is active on ports A and B.
  - When the VACT signal is not used by a video decoder, connect the VACT pin to the HREFI pin.
- Y[7:0] (Luminance)
  - These signals are 8 bits of luminance data from the external video controller that are input to the CL-GD7548.
- UV[7:0] (Chrominance)
  - These signals are 8 bits of chrominance data from the external video controller that are input to the CL-GD7548.
  - There is a 9-bit programmable delay to skip *n* HREF pulses before the internal V-Port Vertical Display Enable is asserted.

V-Port™-to-Memory Implementation

In the V-Port-to-Memory mode, communication between the CL-GD7548 and the external decoder device (or video source) is based upon a synchronous data flow, in that the external decoder device drives all the interfaces, including the PCLK.

The V-Port-to-Memory mode can be implemented in two different modes, depending on how data is latched relative to the clock edge as follows:

- Mode 1: Data latched on PCLK falling edge
- Mode 2: Data latched on PCLK rising edge

This flexibility allows the CL-GD7548 to directly interface with various TV/MPEG decoder chips. The CL-GD7548 has a serial interface consisting of a clock pin and a data pin, both of which are open-drain and which support serial programming interfaces to those chips.

A) V-Port-to-Memory Mode 1: Data Latched on PCLK Falling Edge

In V-Port-to-Memory mode 1, data is latched on the falling edge of PCLK. An example of an implementation of this mode is the interface to the Pixel Semiconductor CL-PX4072 video pixel decoder, as shown in Figure 3-4. Full implementation of this interface requires the following 20 active pins:

- PCLK (Pixel Clock signal). The falling edge of PCLK latches the data bits.
- VS (Vertical Start signal)
- HREF (Horizontal Reference Input signal)
- VACT (Vertical Active signal, used to indicate the transfer of active video data)
- 16 data bits (8 data bits for luminance and 8 data bits for chrominance)

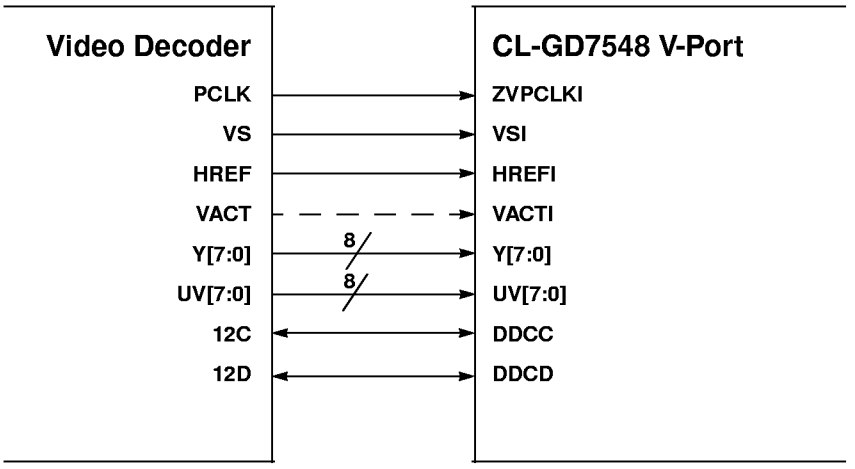


Figure 3-4. V-Port™-to-Memory Interface Signals

NOTE: The DDCC and DDCD pins are not required for the V-Port. However, if the CL-GD7548 is used in certain motherboard implementations, the DDCC and DDCD pins may need to be used in order to program a NTSC/PAL decoder (such as the CL-PX4072 or the Philips® SAA7110).

The CL-PX4072, which outputs only interlaced video data streams, supports the following standards:

- NTSC
- PAL
- SECAM
- S-VHS

For more information, refer to the CL-PX4072 documentation.

In a VESA VL-Bus configuration, it is possible for the CL-GD7548 to directly interface with the CL-PX4072 through an 8-bit V-Port. In this configuration, YUV data can either be:

- Latched on both edges of PCLK
- Compressed by the CL-PX4072 to an 8-bit/pixel AccuPak format

B) V-Port-to-Memory Mode 2: Data Latched on PCLK Rising Edge

In contrast to V-Port-to-Memory Mode 1, V-Port-to-Memory Mode 2 does not require the additional signal in the interface, VACT. Full implementation of the V-Port-to-Memory Mode 2 interface requires only the following 19 active pins:

- 16 data bits (8 data bits for luminance and 8 data bits for chrominance)
- HREFI (Horizontal Reference Input signal)
- VS (Vertical Start signal)
- PCLK (Pixel Clock signal). The rising edge of PCLK latches the data bits.

In V-Port-to-Memory Mode 2, the CL-GD7548 can support both interlaced and non-interlaced video data streams.

- The interlaced video data stream support enables a direct interface with TV decoder chips, such as the Philips SAA7110.
- The non-interlaced video data stream support enables a direct interface with MPEG decoder chips such as the C-Cube CL-480. In this type of operation, the relationship of the VS signal to the HREFI signal is 'non-interlaced' and the frame buffer addresses for the video data are generated sequentially.

V-Port-to-Memory Application Examples: The following two tables show the performance that is possible when data is transferred from a video source through the V-Port to a display.

Table 3-3 shows the system performance that is possible when data is transferred from a video source through the V-Port to a display display in a 'Type 3' system, which is explained in the table note below.

Table 3-3. V-Port™ Performance: System Type 3 [a]

Display Resolution	Video Source		Display of Video Window			
			Single-Scan LCD / SimulSCAN™ Mode		Dual-Scan LCD / SimulSCAN™ Mode	
	Resolution	Data Format	Scaled Resolution [b]	Color Depth	Scaled Resolution [b]	Color Depth
640 x 480 256 Colors 60 Hz	320 x 240	AccuPak (8-bit) [c]	320 x 240 ⇒ 640 x 480	~ 32K [d]	320 x 240 ⇒ 640 x 480	~ 16M [d]
		RGB 5-5-5	320 x 240 ⇒ 640 x 480	32K	640 x 480	32K
		4:2:2 YUV	320 x 240 ⇒ 640 x 480	16M	640 x 480	16M
	640 x 480	AccuPak (8-bit) [c]	640 x 480	~ 32K [d]	640 x 480	~ 32K [d]
800 x 600 256 Colors 60 Hz	320 x 240	AccuPak (8-bit) [c]	320 x 240 ⇒ 800 x 600	~ 32K [d]	320 x 240 ⇒ 800 x 600	~ 32K [d]
		RGB 5-5-5	640 x 480 ⇒ 800 x 600	32K	640 x 480 ⇒ 800 x 600	32K
		4:2:2 YUV	640 x 480 ⇒ 800 x 600	16M	640 x 480 ⇒ 800 x 600	16M
	640 x 480	AccuPak (8-bit) [c]	640 x 480 ⇒ 800 x 600	~ 32K [d]	640 x 480 ⇒ 800 x 600	~ 32K [d]
1024 x 768 256 Colors 60 Hz	320 x 240	AccuPak (8-bit) [c]	640 x 480 ⇒1024 x 768	~ 16M [d]	Not available	–

a. System Type 3 has the following features:
   - — Either 1 or 2 Mbytes of display memory.
   - — Runs at 3.3 V.
   - — MCLK runs at a maximum of 54 MHz.
   - — Video is transferrred from a video source to a display through the V-Port.

b. Continuous upscaling is possible from the source resolution to the display resolution, but upscaling that is more than 2x may result in a degradation in the resolution quality.

c. The CL-GD7548 can convert 4:2:2 YUV data that comes from the V-Port to the AccuPak format, at display time.

d. This color depth results from a lossy color space format conversion.

Table 3-4 shows the system performance that is possible when data is transferred from a video source through the V-Port to a display display in a 'Type 4' system, which is explained in the table note below.

Table 3-4. V-Port™ Performance: System Type 4 [a]

Display Resolution	Video Source		Display of Video Window			
			Single-Scan LCD / SimulSCAN™ Mode		Dual-Scan LCD / SimulSCAN™ Mode	
	Resolution	Data Format	Scaled Resolution [b]	Color Depth	Scaled Resolution [b]	Color Depth
640 x 480 256 Colors 60 Hz	320 x 240	AccuPak (8-bit) [c]	320 x 240 ⇒ 640 x 480	~ 32K [d]	320 x 240 ⇒ 640 x 480	~ 32K [d]
		RGB 5-5-5	320 x 240 ⇒ 640 x 480	32K	640 x 480 ⇒ 640 x 480	32k
		4:2:2 YUV	320 x 240 ⇒ 640 x 480	16M	640 x 480 ⇒ 640 x 480	16M
	640 x 480	AccuPak (8-bit) [c]	640 x 480 ⇒ 640 x 480	~ 32K [d]	320 x 240 ⇒ 640 x 480	~ 32K [d]
800 x 600 256 Colors 60 Hz	320 x 240	AccuPak (8-bit) [c]	320 x 240 ⇒ 800 x 600	~ 32K [d]	320 x 240 ⇒ 800 x 600	32k
		RGB 5-5-5	640 x 480 ⇒ 800 x 600	32k	640 x 480 ⇒ 800 x 600	32k
		4:2:2 YUV	640 x 480 ⇒ 800 x 600	16M	640 x 480 ⇒ 800 x 600	16M
	640 x 480	AccuPak (8-bit) [c]	640 x 480 ⇒ 800 x 600	~ 32K [d]	640 x 480 ⇒ 800 x 600	~ 32K [d]
1024 x 768 256 Colors 60 Hz	320 x 240	AccuPak (8-bit) [c]	320 x 240 ⇒ 1024 x 768	~ 32K [d]	Not available	–

a. System Type 4 has the following features:
   - — Either 1 or 2 Mbytes of display memory.
   - — Runs at 5 V.
   - — MCLK runs at a maximum of 66 MHz.
   - — Video is transferrred from a video source to a display through the V-Port.

b. Continuous upscaling is possible from the source resolution to the display resolution, but upscaling that is more than 2x may result in a degradation in the resolution quality.

c. The CL-GD7548 can convert 4:2:2 YUV data that comes from the V-Port to the AccuPak format, at display time.

d. This color depth results from a lossy color space format conversion.

3.3 Support for 1024 x 768 (XGA) TFT LCD Panels

The CL-GD7548 is the first Cirrus Logic controller to support an XGA TFT LCD panel, with VGA compatibility. This section describes how the CL-GD7548 supports XGA resolution, which is defined as resolution that has 1024 horizontal pixels and 768 vertical pixels.

The CL-GD7548 interface is designed to support the following two types of TFT LCD data formats:

- Data format 1 supports those TFT LCDs that have a 1-pixel/clock mode. This data format directly supports up to 24 RGB (8-bit/primary) data lines.
- Data format 2 supports those TFT LCDs that have a 2-pixel/clock mode. This data format requires double the amount of data lines normally associated with a given color depth. For example, if a TFT LCD has 6 bits per primary color (for a total of 18 bits of data lines) and the TFT LCD has a 2-pixel/clock mode, it requires 36 data lines. As a result, this data format requires the CL-GD7548 to have external circuitry to support the additional pins required for this type of interface.

When the CL-GD7548 is used with an XGA TFT LCD panel, its XGA support consists of the following:

- Support for VGA, SVGA, and XGA graphics modes (both for Centered Display and Expanded Display mode)
- Support for 2-pixel/clock mode (up to 6 bits per primary color), with minimum external circuitry
- Support for all modes in SimulSCAN™
- Support for the XGA TFT LCD control signals:
  - — SCLK (shift clock that is used to latch the panel pixel data)
  - — The LCD frame clock (vertical sync) signal
  - — The LCD line clock (horizontal sync) signal
  - — DE, the display enable signal
- Hardware expansion of resolution up to 800 x 600, in all VGA modes
- Independent expansion/centering options
- Independent shading controls for graphics and Video Window

3.3.1 XGA TFT LCD Mode of Operation

The CL-GD7548 has timing registers with display position controls that allow the CL-GD7548 to simultaneously support both an LCD panel (which has a fixed set of timing parameters) and a CRT (which needs different timing parameters for each operational mode).

- For the Expansion mode, the CL-GD7548 provides standard CRT Controller registers CR0–CR5.
- For all Native modes, the CL-GD7548 provides Extension registers R0Y, R2Y–R5Y, R0Z, and R2Z–R5Z (which are controlled by Sequencer register bit SR1[3]).

Table 3-5 and the figures from Figure 3-5 to Figure 3-9 show what images are possible on an XGA LCD or CRT that uses the CL-GD7548 with various video modes.

NOTE: In Table 3-5, the term 'Native mode' refers to the mode that occurs when an image is running at the same resolution of an LCD or CRT and consequently fills the entire display.

For example, if an LCD panel has a resolution of 640 x 480 and the image that is running on the display also has a resolution of 640 x 480, the image is said to be in the Native mode.

Table 3-5. CL-GD7548 Mode Options on an XGA LCD or CRT

Type of Video Mode	When Video Mode is Used on XGA (1024 x 768) LCD or CRT:	
	Centering Possible with VGA LCD Type Expansion Is:	Centering Possible with SVGA LCD Type Expansion Is:
EGA (640 x 350)	640 x 475	800 x 525
VGA (640 x 480)	640 x 480	800 x 600
VGA (720 x 400)	640 x 480	800 x 600
SVGA (800 x 600)	An 800 x 600 image that is centered (Non-expanded)	An 800 x 600 image that is aligned at the top left (Non-expanded)
XGA (1024 x 768)	1024 x 768 (Native mode)	1024 x 768 (Native mode)

For XGA LCDs, the CL-GD7548 has two modes of operation: either the Centered mode or the Top-Left-Aligned (Non-Centered) mode.

3.3.1.1 CL-GD7548 Centered Mode

Figure 3-5 shows how various modes appear on an 1024 x 768 XGA TFT LCD when the CL-GD7548 is used in the Centered mode.

- Example A. If the CL-GD7548 is used on an XGA TFT LCD and is programmed for an XGA graphics mode, all of the 1024 x 768 XGA LCD display is used.
- Example B. If the CL-GD7548 is used on an XGA TFT LCD and is programmed for VGA text expansion or an SVGA Centered Text mode, a 800 x 600 display image appears centered within the 1024 x 768 LCD display. Blanking occurs in that portion of the screen that is not used (that is, the 84 top scanlines, 84 bottom scanlines, 112 left columns, and 112 right columns).
- Example C. If the CL-GD7548 is used on an XGA TFT LCD and is programmed for a VGA Native Centered Text mode, a 640 x 480 display image appears centered within the 1024 x 768 LCD display. Blanking occurs in that portion of the screen that is not used (that is, the 144 top scanlines, 144 bottom scanlines, 192 left columns, and 192 right columns).

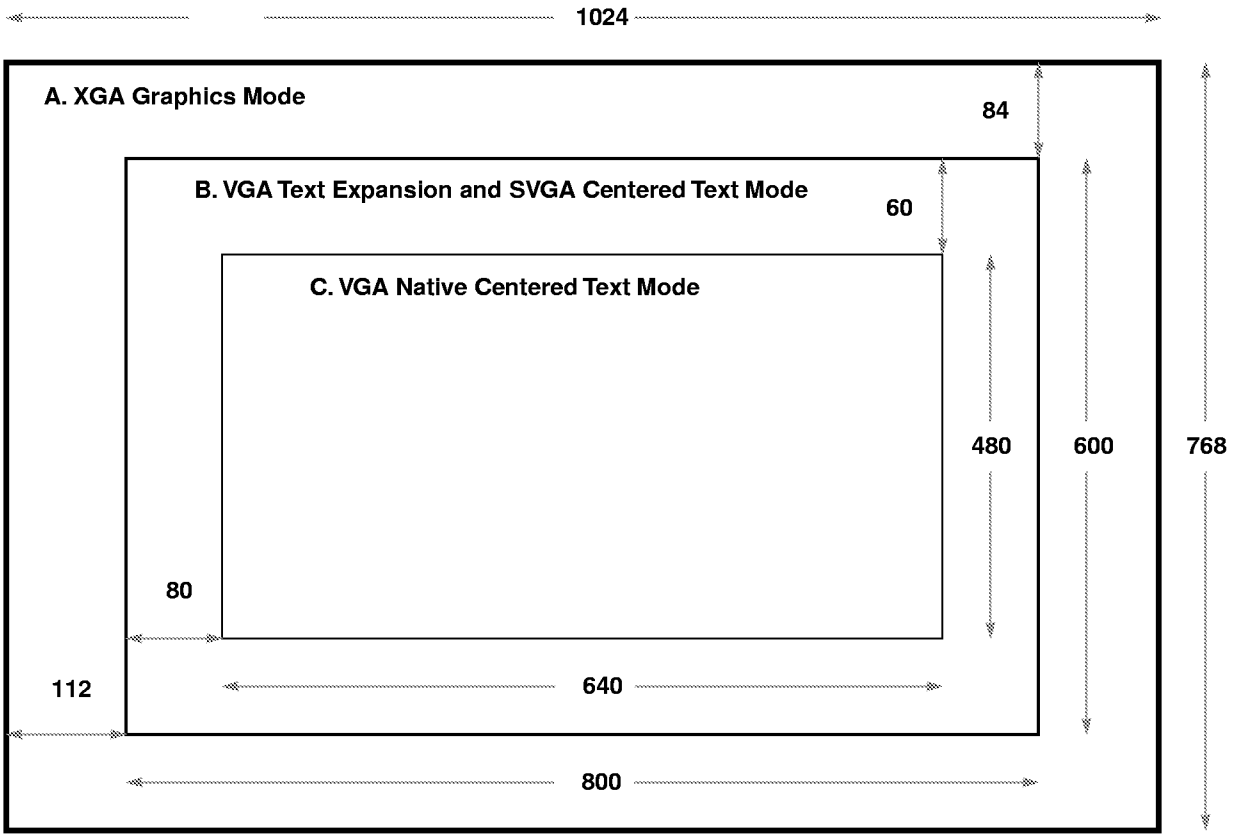


Figure 3-5. XGA TFT LCD: Appearance of Centered Modes

3.3.1.2 CL-GD7548 Top-Left-Aligned (Non-Centered) Mode

The figures in this section show how various modes appear on an 1024 x 768 XGA TFT LCD when the CL-GD7548 is in the Top-Left-Aligned mode (that is, the CL-GD7548 is *not* used in the Centered mode and Extension register CR2E is set as shown). In this case, all modes start at the top left corner of the display screen.

- If the CL-GD7548 is used on an XGA TFT LCD and is programmed for an XGA Graphics mode, but the Centered mode is not used, all of the 1024 x 768 XGA LCD display is still used.
- If the CL-GD7548 is used on an XGA TFT LCD and is programmed for VGA Text mode expansion, the 800 x 600 image is expanded. However, this image starts at the top left corner. Blanking occurs on that portion of the screen that is not used (that is, the bottom 168 scanlines and the 224 columns to the right of the used portion of the display).
- If the CL-GD7548 is used on an XGA TFT LCD and is programmed for a VGA Native Centered Text mode, a 640 x 480 image is displayed. However, this image starts at the top left corner. Blanking occurs on that portion of the screen that is not used (that is, the bottom 288 scanlines and the 384 columns to the right of the used portion of the display).

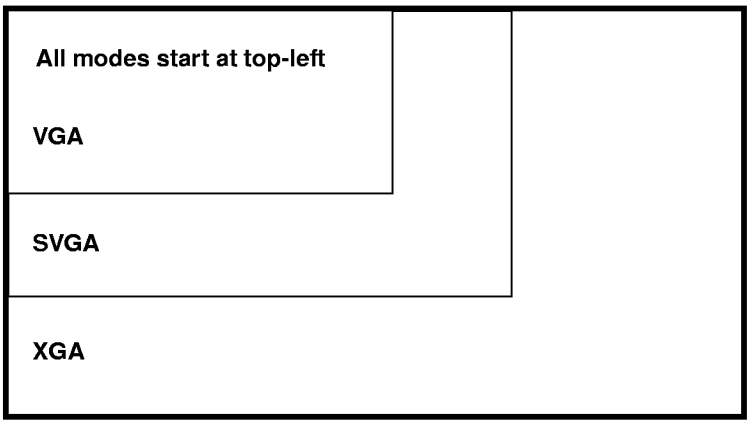


Figure 3-6. Appearance of Video Modes when Extension Register CR2E[7:0] = 00h (0000 0000b)

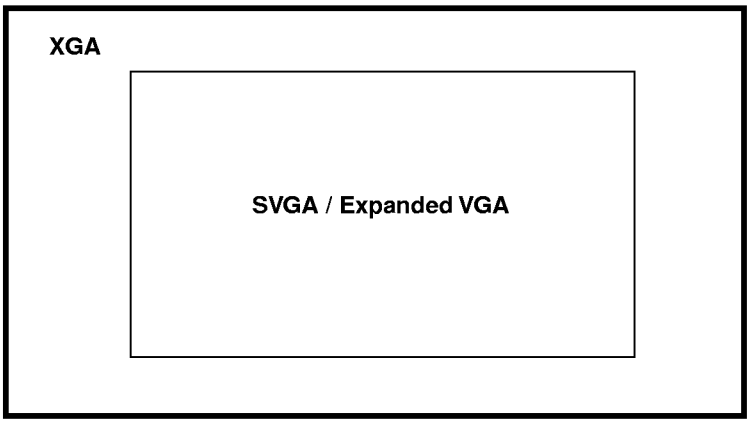


Figure 3-7. Appearance of Video Modes when Extension Register CR2E[7:0] = 2Fh (0010 1111b)

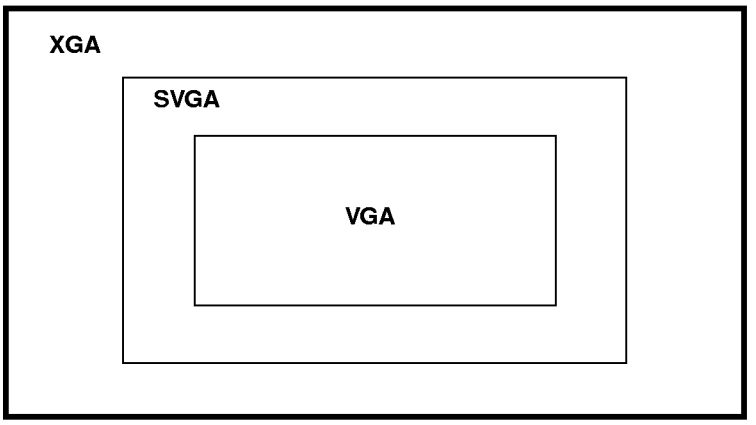


Figure 3-8. Appearance of Video Modes when Extension Register CR2E[7:0] = 20h (0010 0000b)

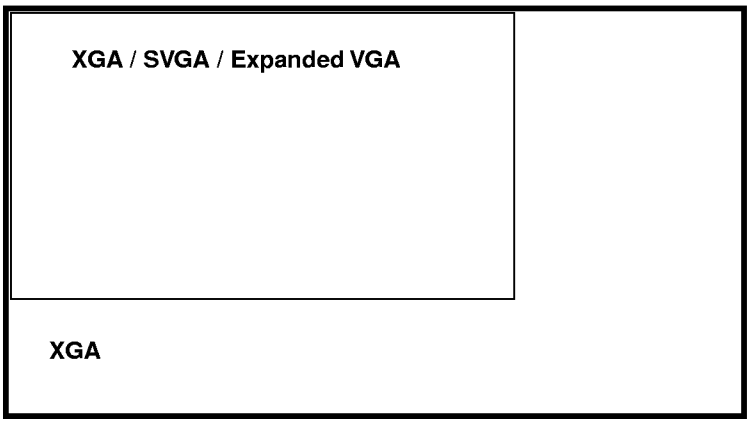


Figure 3-9. Appearance of Video Modes when Extension Register CR2E[7:0] = 0Fh (0000 1111b)

3.3.2 XGA TFT LCD Interface

The CL-GD7548 supports two types of data formats for the TFT LCD interface.

- Data format 1 is a 1-pixel-per-clock mode that directly supports up to 24 bits per pixel (that is, 8 bits for each red, green, and blue primary color).
- Data format 2 is a 2-pixel-per-clock mode that requires external latches for the even pixel data bits (that is, the Ra[5:0], Ga[5:0], and Ba[5:0] data bits).

Although the CL-GD7548 does not have all the data pins necessary to directly support an XGA TFT LCD that uses the 2-pixel-per-clock mode, the circuit shown in Figure 3-10 provides a solution. Because most LCDs have tight data set-up and hold-time requirements, if the circuit of Figure 3-10 is laid out on a printed circuit board that has cable harnesses that have high-capacitance loading, special timing analyses must be performed as follows:

1. For the LCD that is using the CL-GD7548, refer to the LCD specifications, and locate the required data set-up and hold-time for the LCD.
2. Use the CL-GD7548 VCLK of 65 MHz (that is, 15.4 ns) to determine the minimum data set-up and hold-time requirements for the LCD.
3. Depending on the LCD, the total of t_{ds} (data set-up time) $+t_{dh}$ (data hold time) can range from a best case of 9 ns to a worst case of 14 ns. Consequently, the worst-case LCD timing requirement is:

   $t_{ds} + t_{dh}$ = Best-case maximum LCD shift clock (that is, the transition time is presumed to be 0 ns).

   VCLK – ($t_{ds} + t_{dh}$) = Maximum allowed transition time

   (15.4 ns) – [(Data set-up time of 7 ns) + (Data hold time of 7 ns)] = 1.4 ns > = ($t_{rise} + t_{fall}$)

CAUTION: When designing a system, this short data transition time must be taken into account, or the LCD display may appear to be corrupted.

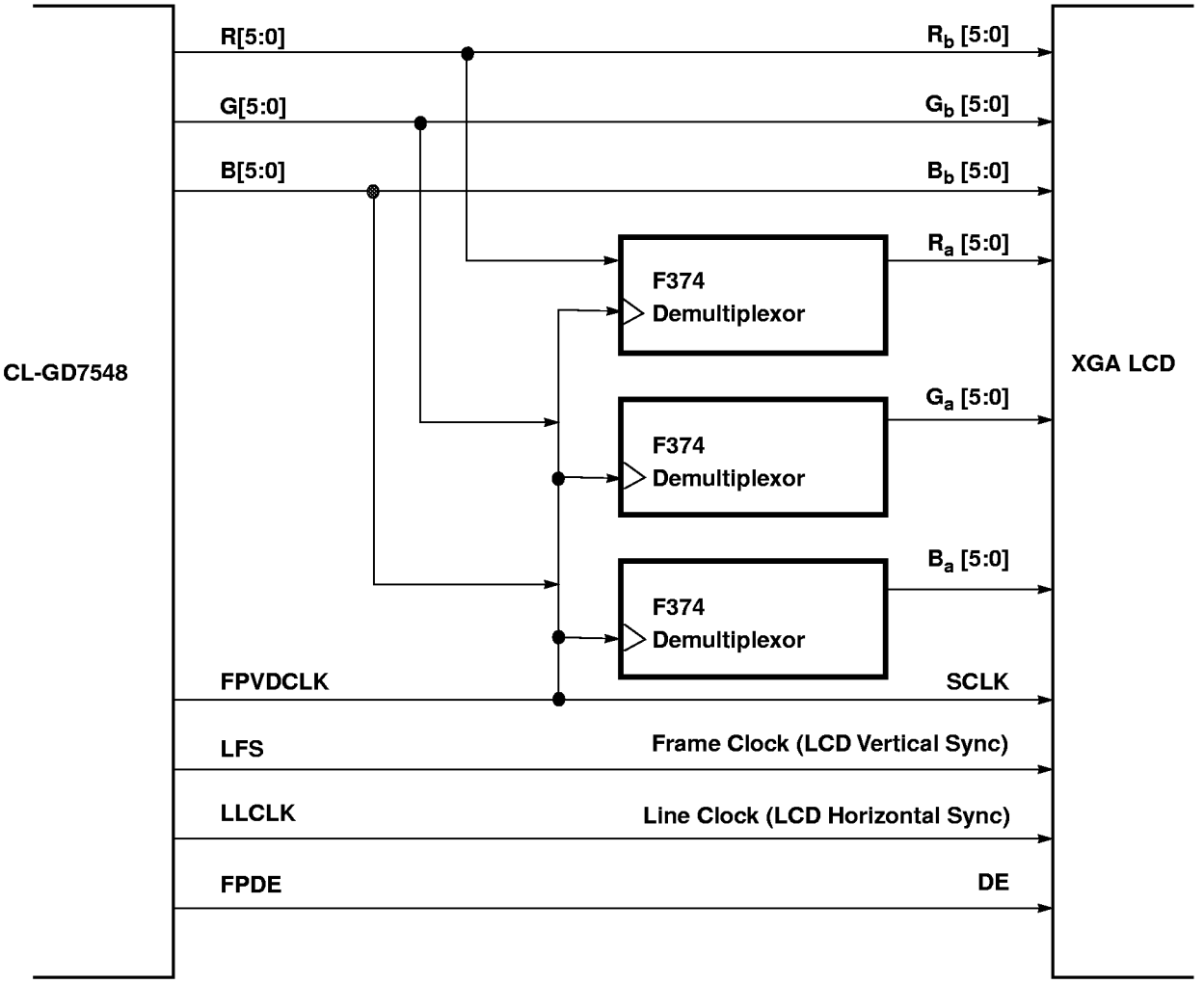


Figure 3-10. Two-Pixel-Per-Clock External Circuitry for CL-GD7548, for Use with XGA TFT LCD

3.4 Video Overlay Mode

The CL-GD7548 supports video overlay operations. During overlay operations, the video data from the 8-bit Feature Connector does not go into MotionVideo Memory. Instead, the data is overlaid on VGA graphics under control of either a color key, or window timing generated by the CL-GD7548, or both.

The data is dynamically switched to the display device, replacing data coming from display memory. The data must therefore be transferred at a rate compatible with the pixel rate at which the display (CRT or LCD) is currently being refreshed at.

The Video Overlay Mode is therefore different from the V-Port-to-Memory mode, which transfers the data that goes through the V-Port into memory. In the case of the V-Port-to-Memory mode, the data transfer rate can be different, and typically lower, than the data rate at which the display is operating.

Using on-chip window timing registers (a secondary function of the border timing control registers) and color key, the CL-GD7548 can generate occluding overlays. Although the Video Overlay Mode requires external hardware, it supports occlusion of the MPEG Video Window, which is an important feature for some MPEG applications, such as interactive games.

Examples of video overlay input data sources include:

- MPEG decoder
- NTSC/PAL decoder

The HDR Extension register (the Hidden DAC Register) allows different external pixel video data formats to be selected.

Overlay data port functions are the following:

- VESA pass-through when the FCEVIDEO# pin is driven low
- On-chip Window timing generator
- Dynamic video overlay under control of external video window timing signal FCEVIDEO#
- Dynamic video overlay with Color Key
- Dynamic video overlay with Color Key and FCEVIDEO#

The CL-GD7548 Video Overlay Port includes the following pins:

- FCP[7:0]: bi-directional 8-bit data port
- FCDCLK / DDCC: dot clock output and DDC compatible clock to connect to external devices, such as video/MPEG decoders.
- FCVCLK / VPCLK: video clock input or clock to/from MPEG or video decoder
- FCESYNC# / VSI / INCADRI / VSYNCO: enable SYNCs input, to enable the HSYNC, VSYNC, and FCBLANK# outputs; alternate functions of this pin are to synchronize vertical timing to an external video/MPEG decoder.
- FCBLANK# / HREFI / HFLI / HSYNCO: either a blanking signal output, or an input that forces RGB outputs to zero current; alternate functions of this pin are to synchronize horizontal timing to an external video/MPEG decoder.
- OVRW# / VACTI / VPFEO: Overlay Window output; alternate functions of this pin are to handshake with an external video/MPEG decoder.

The CL-GD7548 supports the Feature Connector baseline functionality such that video data may be input and displayed as an overlay video window. The CL-GD7548 supports 8-bit/pixel indexed data (FC extended mode). Note that the Video Overlay Port is not fully compatible with the VAFC specification but may be connected to VAFC video sources through suitable bridge logic.

The 8-bit data is input either by using both phases of the clock or by using a 2X clock. An 8-bit value, stored in Extension register GRC (the Color Key Compare register), is compared to the video data input from FCP[7:0] on a pixel-by-pixel basis. A match causes the pixel graphics data to be replaced with the video data input.

For more information on the Video Overlay, refer to the application note, "The 8-Bit Dynamic video Overlay" in the *CL-GD754X Application Book*.

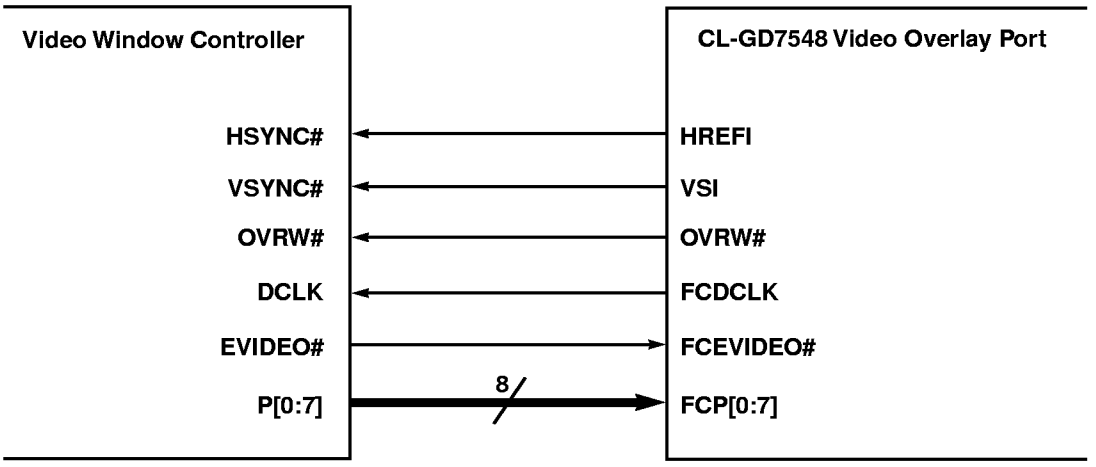


Figure 3-11. Video Overlay Interface Signals

3.4.1 Video Overlay Mode Application Examples

The following figure is a functional block diagram of the interface between external decoders and the CL-GD7548.

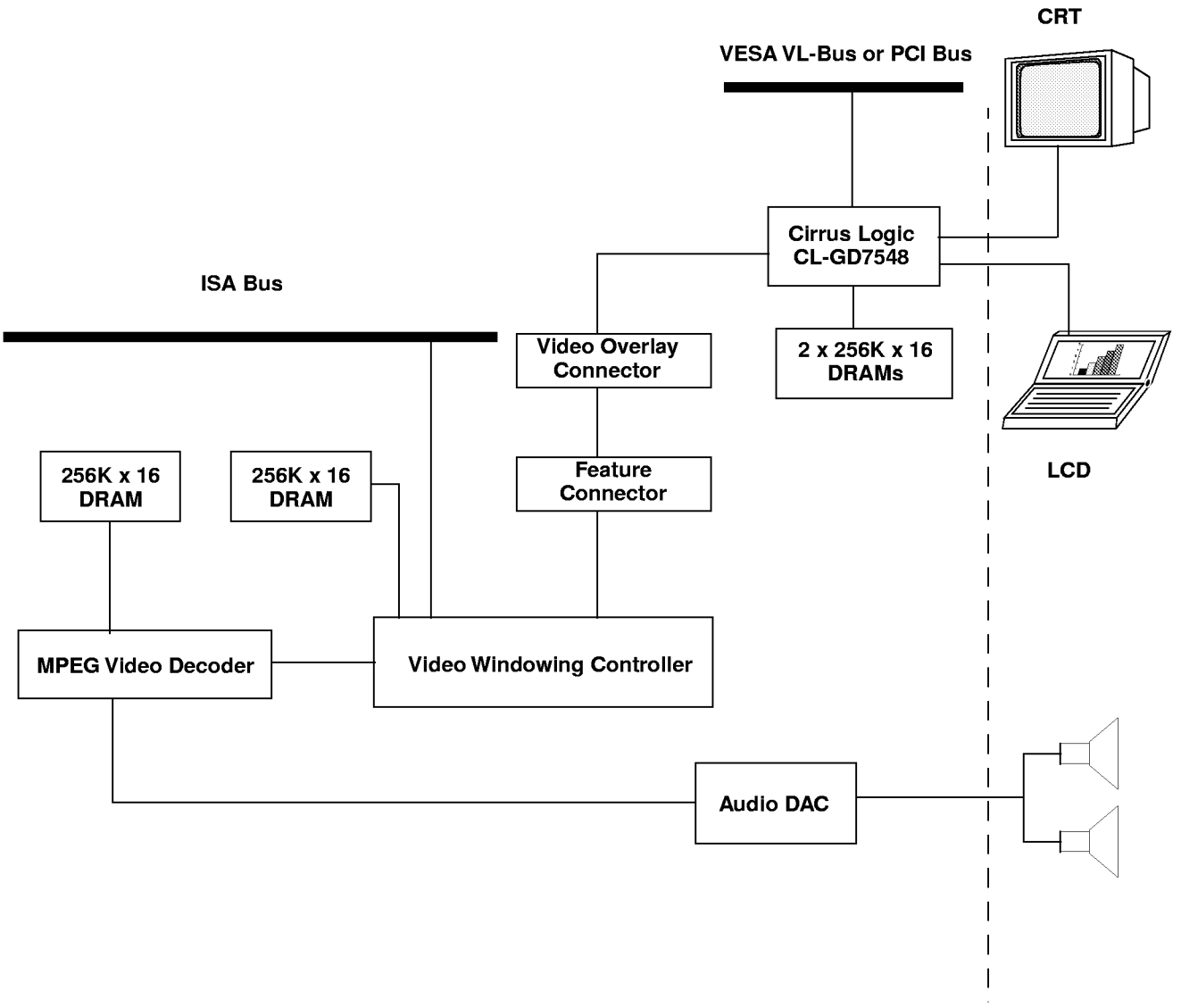


Figure 3-12. Hardware MPEG Video Overlay Functional Block Diagram

3.5 Functional Blocks

Figure 3-13 shows a simplified block diagram of the CL-GD7548 GUIX SVGA LCD Controller. The functional blocks integrated in the CL-GD7548 are described in the following sections.

3.5.1 Host CPU Bus Interface

The CL-GD7548 connects directly to a '486/VESA VL-Bus or a PCI bus. No additional logic circuitry is required to implement these bus interfaces.

NOTE: The CL-GD7548 is optimized for motherboard implementations that integrate system and VGA BIOS. As a result, the CL-GD7548 does not support external BIOSs.

'486/VL-Bus

The CL-GD7548 interfaces directly to '486DX microprocessors and the VESA VL-Bus, at MCLK speeds up to 66 MHz.

PCI Bus

The CL-GD7548 interfaces directly to the PCI bus. No additional logic is required to support the CL-GD7548 multiplexed address and data pins. The CL-GD7548 executes 32-bit I/O and memory accesses at speeds up to 33 MHz. The CL-GD7548 also supports memory burst cycles. PCI bandwidth is at least 33% more efficiently utilized with burst cycles.

In the PCI bus configuration, the CL-GD7548 supports big-endian word swapping, allowing 'X86 little-endian data or PowerPC big-endian data to load into display memory, depending upon application requirements.

Apertures

With both PCI bus and VESA VL-Bus designs, the CL-GD7548 supports a dual-aperture scheme. This scheme allows video traffic over a bus to be supported with reduced software overhead. As a result, I/O accesses to configure graphics registers are not needed. Instead, an aperture switch is done. VGA graphics and video applications can each access the entire 2-Mbyte address space through their own aperture. (For more information on apertures, refer to Section 3.2.4.1.)

Linear Memory Addressing

The CL-GD7548 supports linear memory addressing, as an alternative to the standard VGA method of accessing display memory with 64-Kbyte segments. With linear memory addressing, the CL-GD7548 is configured so that it accesses display memory as a 1- or 2-MByte linearly addressed string of bytes.

For applications or drivers that support this method, linear memory addressing improves graphics performance by simplifying access to display memory, since it is not necessary to calculate offsets into a relatively small window, nor is it necessary to test for a crossing of the window boundary.

The CL-GD7548 supports linear memory addressing of the VGA address space, which can reside within any 1-Mbyte segment above the first 16 MBytes in a 4-GByte address space. For '486 local bus interfaces that use a 32-bit address, in order to select the desired 16-Mbyte partition with the A[31:24] address line, an external decoder may be needed. However, in general, there is no need for an external decode of the host CPU addresses. Any one of the A[31] to A[24] lines can be directly connected to HIMEM0 or HIMEM1. For instance, if HIMEM1 is connected to A[31], then the CL-GD7548 is mapped into the upper 2 GBytes of the host CPU address space.

Extension register bits SR2D[7:6] extend the address space to 64 MBytes by re-mapping HIMEM0 and HIMEM1 within this address space. An external decoder may be needed only if a fully decoded 16-Mbyte partition within the 4-GByte address space is desired. The output from this address-line decoder drives the HIMEM0 and HIMEM1 inputs. Extension register bits SR7[7:4] are used to select the 1-Mbyte through 16-Mbyte range in any 16-Mbyte space allowed by the microprocessor.

NOTE: HIMEM0 and HIMEM1 are used only with the VESA VL-Bus and 32-bit local buses.

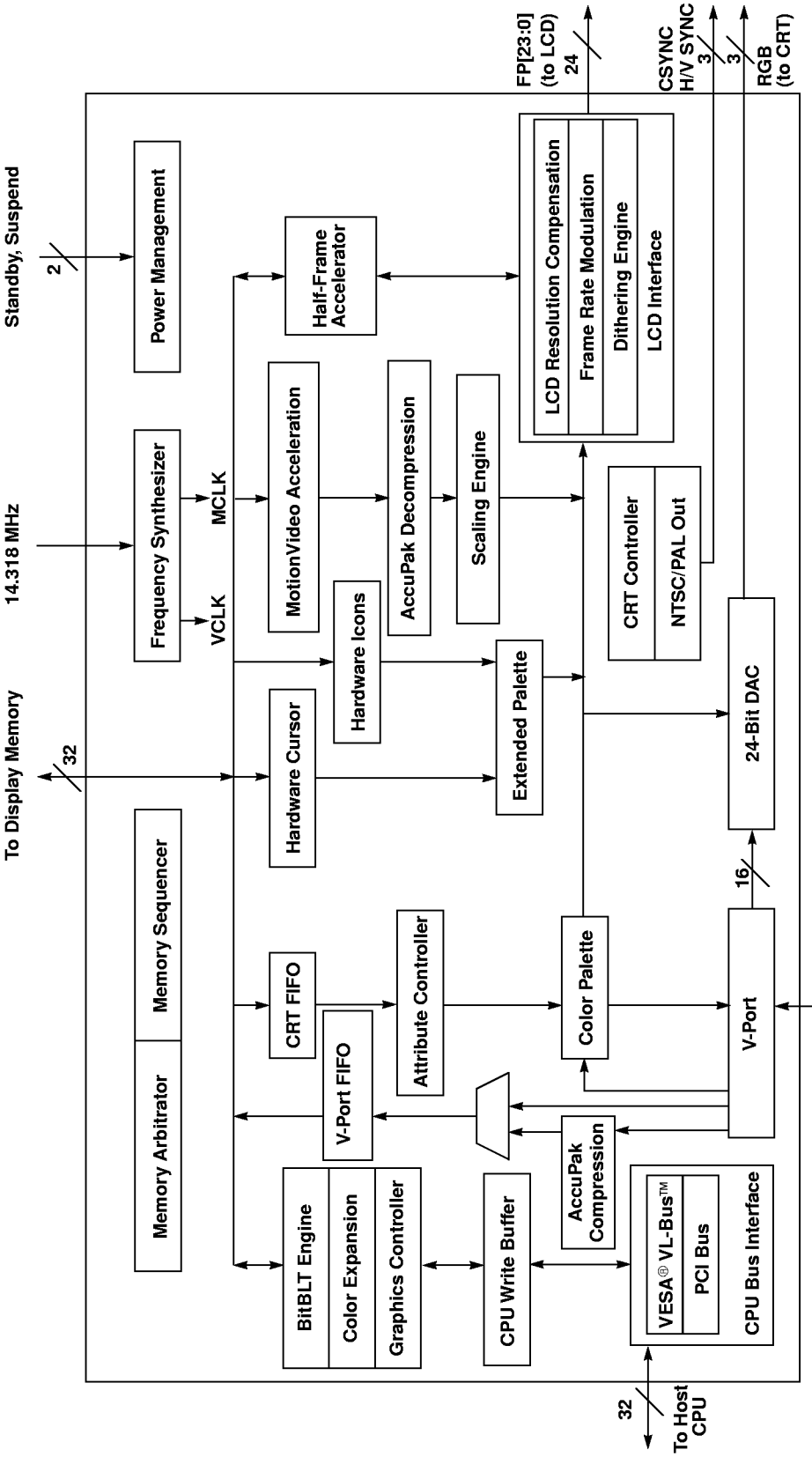


Figure 3-13. CL-GD7548 Block Diagram

3.5.2 Host CPU Write Buffer

The CPU write buffer contains a queue of host CPU write accesses to display memory that have not been executed due to memory arbitration. Maintaining this queue of write accesses allows the CL-GD7548 to release the CPU bus as soon as it has recorded the address and data. The CL-GD7548 therefore executes the operation when display memory is available, increasing CPU performance.

For all text and graphics modes, the write buffer depth is two 32-bit or four 16-bit levels. The CL-GD7548 has the capability to page CPU cycles if they are accumulated in the write buffer.

3.5.3 Graphics Controller

The graphics controller operates in either text or graphics modes and performs these major functions:

- Provides the host CPU a read/write access path to display memory
- Controls all four memory planes in planar modes
- Allows data to be manipulated prior to being written to display memory
- Formats data for use in various backward compatibility modes
- Provides color read comparators for use in color painting modes
- Reads/writes 32-bit words through the 32-bit display memory interface

The graphics controller directs data from the display memory to the host CPU. Figure 3-14 and Figure 3-15 illustrate typical write and read operations, respectively.

For a write operation, the data from the host CPU bus are combined with the data from the Set/Reset Logic in the host CPU, depending on the Write mode. In addition, the data can be combined with the contents of the read latches, and some bits or planes can be masked (that is, prevented from being changed) by using the Graphics Controller register GR8 (the Display Memory Bit Mask register). For more information, refer to the Graphics Controller registers in Chapter 10.

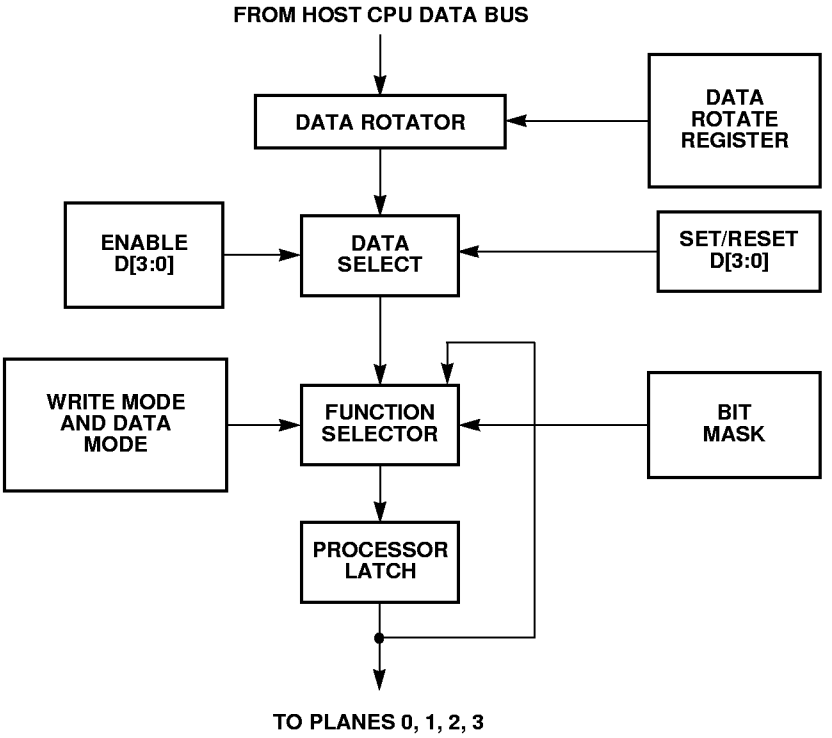


Figure 3-14. Graphics Controller Write Operation

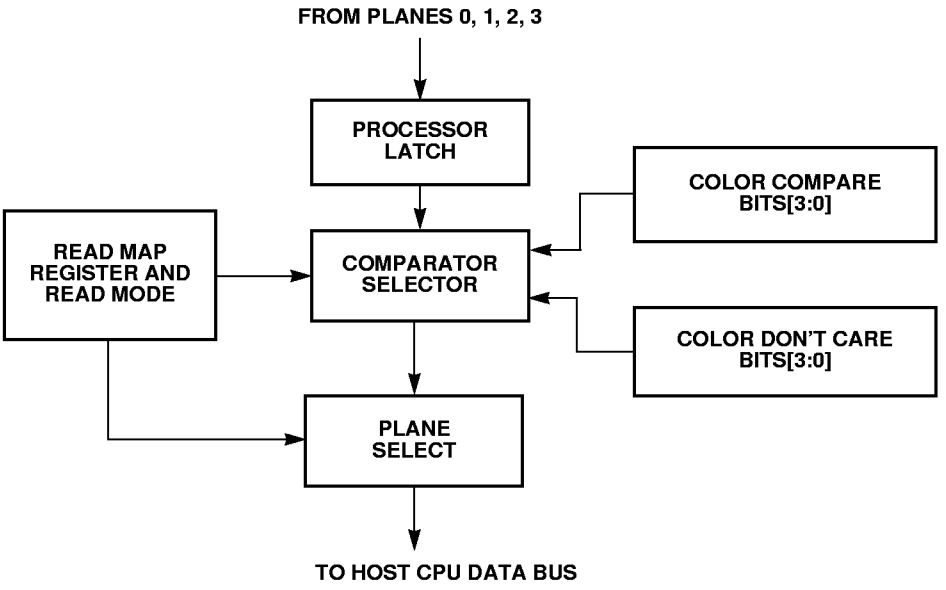


Figure 3-15. Graphics Controller Read Operation

3.5.4 Color Expansion

Color expansion is the automatic conversion of a monochrome bit map (which typically defines a character, icon, or pattern) into foreground and background color values. These values are then written into display memory and held in a CL-GD7548 register.

Color expansion improves host CPU write performance in that it optimizes use of the available host CPU bandwidth by expanding single bits across the bus into complete 8- or 16-bit pixels.

When color expansion is used, only monochrome bit maps must be transmitted across the bus. Each bit of the monochrome map is converted into 8-bit or 16-bit pixel modes. The bus traffic is reduced by a factor of 8 to 16, making it possible to use nearly all of the available display memory bandwidth.

3.5.5 Bit Block Transfer (BitBLT) Engine

The CL-GD7548 BitBLT engine moves a rectangle of data either within display memory or between system memory and display memory, with minimal host CPU intervention. The BitBLT engine can also perform pattern fills (filling an area with a repeating pattern), raster operations (using various logic operations to combine the source bytes with the destination bytes), and color expansion or transparency.

The BitBLT engine provides 16 two-operand ROPs (raster operations) to move data in packed-pixel modes from the source area to the destination area. This operation occurs in packed-pixel modes with 8-bit or 16-bit pixel transfers. The transfers from the host CPU are always taken in four-byte increments. For screen-to-system transfers, the BitBLT operation acts as a read cache. The BitBLT accelerates GUIs (Graphical User Interfaces), such as Microsoft Windows 3.1, Windows 95, and OS/2 'Warp'. For more information, refer to Appendix A.

3.5.5.1 BitBLAST Operation

The BitBLAST (Bit BLock Accelerated Setup Transfer) operation is a CL-GD7548 innovation that first was introduced in Cirrus Logic controller CL-GD5436. To implement BitBLAST, the BitBLT control registers are duplicated and a BitBLT status bit is provided. Application programs can monitor this status bit and, before the current BitBLT completes execution, program the parameters for a new BitBLT operation in a software-transparent second set of registers.

This action allows the setup time of the new BitBLT to overlap with the execution time of the previous BitBLT. Because the BitBLT setup time is done with 16-bit I/O accesses, the BitBLAST can eliminate the amount of time needed by software overhead. In addition, this overlap greatly speeds up those procedures (such as Windows drivers) that use multiple successive BitBLTs. (Using the CL-GD7548 autostart feature can start the BitBLT even faster and save additional BitBLT setup time.)

If the BitBLAST feature is enabled (Extension register GR3[7] = 1), BitBLTs start every time Extension register GR2A is written, which is as soon as the current BitBLT completes.

3.5.5.2 BitBLT Transparent Operation

The CL-GD7548 supports a transparent BitBLT operation. This operation allows the CL-GD7548 to define a color key that does not transfer when the BitBLT executes. As a result, the background color of the source video data does not have to match the background color of the destination, which reduces software overhead.

3.5.6 Memory Arbitrator

The memory arbitrator allocates bandwidth to the following functions, which compete for the limited bandwidth of display memory:

- Host CPU access
- Display refresh
- Display memory refresh
- BitBLAST
- Half-Frame Accelerator (for dual-scan STN LCDs)
- Hardware cursor
- Hardware icons

Display memory refresh is handled invisibly by allocating a selectable number of CAS#-before-RAS# refresh cycles at the beginning of each scanline. Cycles are allocated to display refresh and CPU/BitBLT according to the FIFO-control parameters, with priority given to display refresh.

3.5.7 Memory Sequencer

The memory sequencer generates for display memory all the necessary timing and control signals, including RAS#, CAS#, and multiplexed-address timing, as well as WE# and OE# timing. The sequencer generates CAS#-before-RAS# refresh, random-read, random-early-write, fast-page-mode read, and early-write cycles.

For more information on memory configurations, refer to Appendix F.

The memory sequencer generates multiple-CAS# or multiple-WE# signals, depending on the memory type being used. The CL-GD7548 supports both multiple-CAS# and multiple-WE# 256K × 16 DRAMs. The CL-GD7548 supports the following memory configurations, which have a 32-bit-wide memory interface:

- Two 256K x 16 DRAMs for 1-MByte display memory
- Four 256K x 16 DRAMs for a 2-MByte display memory
- Four 512K x 8 DRAMs (symmetric only) for a 2-MByte display memory
- Two 256K × 16 Extended-Data-Out (or 'Hyper-Page') DRAMs for 1-Mbyte display memory
- Four 256K × 16 Extended-Data-Out (or 'Hyper-Page') DRAMs for a 2-Mbyte display memory

The memory sequencer ensures that the necessary display refresh transfer cycles and dynamic memory refresh cycles are executed and that the remaining memory cycles are made available for host CPU read/write operations.

The CL-GD7548 fully supports all the standard IBM VGA memory organizations, along with the following extended graphics memory modes:

- 2-color packed-pixel modes (1-bit/pixel) in linear 32-bit words or VGA-style 8-bit words
- 256-color packed-pixel modes (8 bits/pixel)
- Direct-color (32K or 64K colors) packed-pixel modes (16 bits/pixel)
- Mixed 32K- and 256-color packed-pixel modes (15 bits/pixel)
- True-Color 16M-color packed-pixel modes (24 bits/pixel)

In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. This storage method is in contrast with the storage method used by VGA chain-4 addressing, a type of addressing that stores consecutive pixels at every fourth byte address in display memory. For more information, refer to Appendix E and Appendix K.

3.5.8 CRT FIFO

The CRT FIFO (first-in, first-out) is a register that allows the memory sequencer to execute display memory accesses needed for display refresh at maximum memory speed, rather than at the display refresh rate. This register makes it possible to take advantage of the DRAM fast-page mode operation. The CRT FIFO register is 20 words deep and 32 bits wide.

3.5.9 Attribute Controller

The attribute controller formats the display for the screen. If performs the following:

- Serialization of memory data
- Display color selection
- Text blinking
- Underlining in both text and graphics modes

The attribute controller is described in Chapter 11. Figure 3-16 is a functional block diagram of the attribute controller.

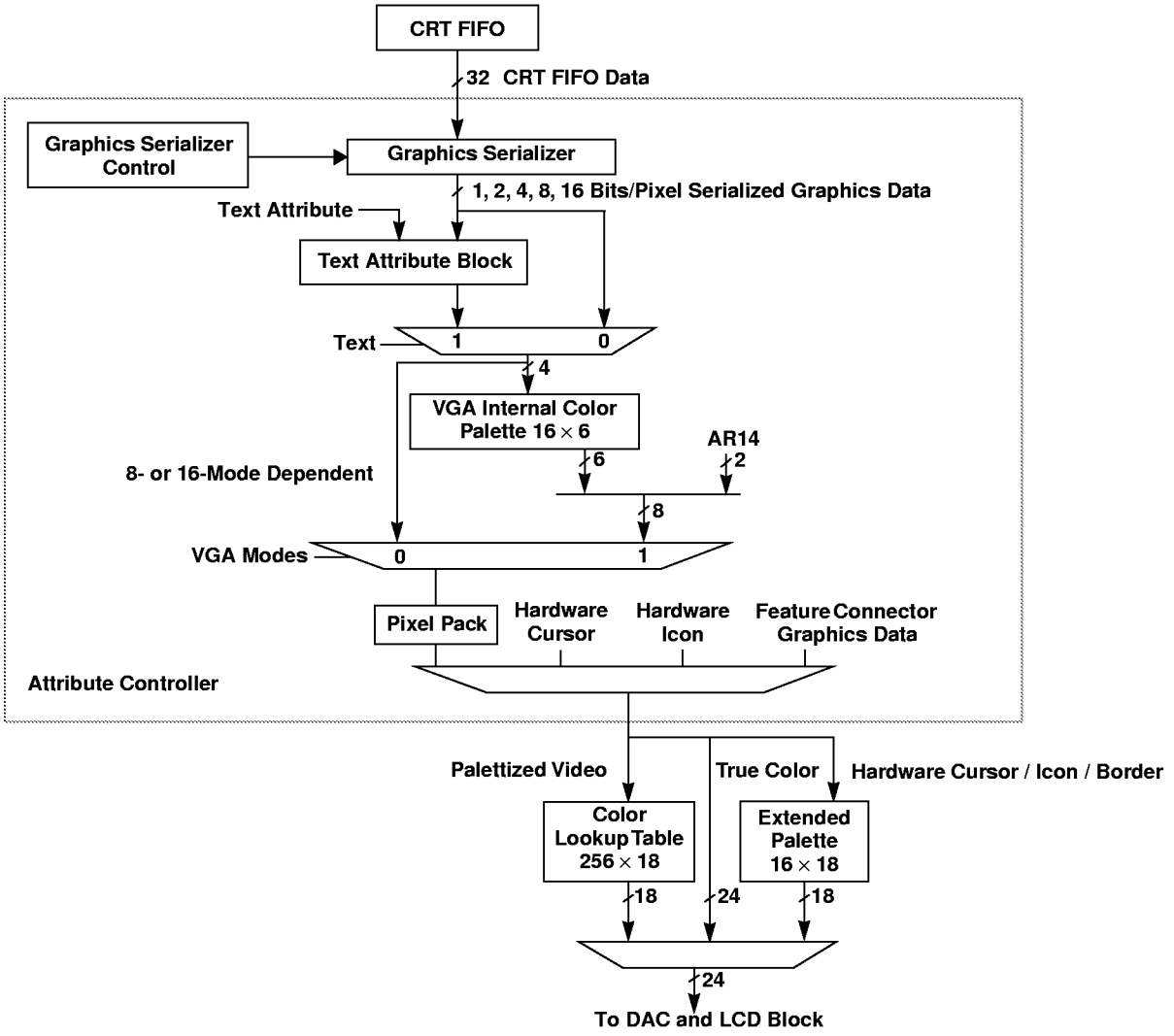


Figure 3-16. Attribute Controller Functional Block Diagram

3.5.10 CRT Controller

The CRT controller (CRTC) generates horizontal and vertical synchronization signals (HSYNC and VSYNC) for the CRT display. The CRTC registers generate BLANK# signals required by the palette DAC. They also support standard VGA-compatible modes and extended modes and provide for the following:

- Configuration options (including user-configurable horizontal/vertical timing and polarity)
- Cursor positioning
- Horizontal scanlines
- Pixel and byte panning
- Split-screen capability and smooth scrolling

The CL-GD7548 supports standard VGA text modes and the following additional text modes: 132 × 25, 132 × 43, and 132 × 50.

The CL-GD7548 supports standard VGA graphics modes and the following extended graphics modes:

- For CRTs:
  - — 1280 × 1024 interlaced, up to 256 colors
  - — 1024 × 768 non-interlaced, up to 256 colors
- For CRTs and LCDs (non-interlaced)
  - — 800 × 600, up to 64K colors
  - — 640 × 480, up to 16M colors

SimulSCAN mode, the simultaneous display capability, is supported at resolutions of 640 × 480 or 800 × 600. (For a complete listing of all modes supported by the CL-GD7548, refer to Chapter 4.) Up to 1024 × 768 16-bit/pixel modes (that is, RGB 5-5-5 direct-color modes) are supported with either a 1× VCLK (pixel rate is equal to VCLK) or with a 2× VCLK (pixel rate is equal to twice the VCLK). The 640 × 480 24-bit/pixel modes (that is, RGB 8-8-8 true-color modes) are supported with a 3× VCLK (that is, the pixel rate is equal to three times the VCLK).Figure 3-17 is a functional block diagram of the CRT controller.

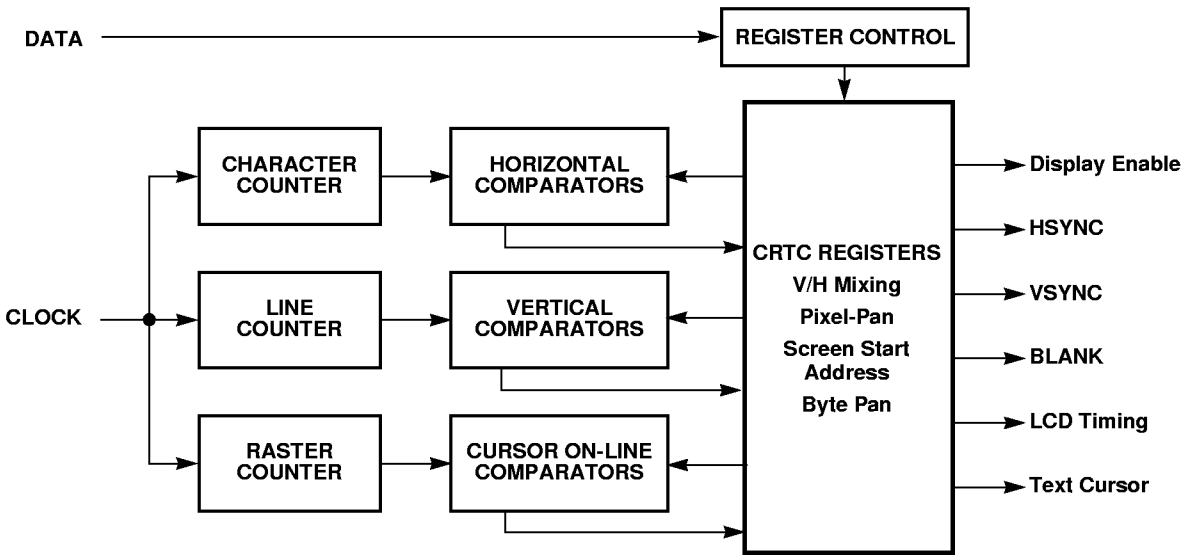


Figure 3-17. CRT Controller Functional Block Diagram

3.5.11 Hardware Cursor

The hardware cursor replaces the software mouse pointer commonly used by GUI applications. The hardware cursor eliminates the need for application software to save and restore the display data as the mouse pointer position changes. The application software typically initializes the hardware cursor once, and from that point it needs only to update the cursor (x,y) position to move the cursor on the display.

The hardware cursor offers a smoothly moving mouse pointer with improved performance, as compared to a software cursor. The hardware cursor is always displayed on top of graphics, video, or the hardware icons.

The hardware cursor consists of either 64 × 64 two-bit pixels or 32 × 32 two-bit pixels. Each pixel in the hardware cursor can be either transparent or one of two colors from an 18-bit palette.

The hardware cursor palette is stored in the extended palette, such that it can be different from the VGA color palette.The first bit of each pixel in the hardware cursor defines whether or not the pixel is transparent. If the pixel is not transparent, the second bit defines the pixel color depth. The second bit selects one of two 18-bit colors in the extended palette.

The following types of 2-bit hardware cursor patterns can be loaded into upper display memory:

- 64 × 64 hardware cursor patterns — up to 8 patterns
- 32 × 32 hardware cursor patterns — up to 32 patterns

After the hardware cursor patterns are loaded into upper display memory, application programs can quickly select one pattern as the active cursor pattern. The hardware cursor is available in all modes except text modes and graphics mode 13h. The hardware cursor is supported only in 1× video clocking modes. For more information, refer to Appendix B.

3.5.12 Hardware Pop-up Icons

The CL-GD7548 provides hardware pop-up icons for displaying small, on-screen symbols that indicate system status (for example, a battery 'fuel gauge'). These hardware icons are stored in upper display memory and can be displayed at the touch of a key. The hardware icons are independent of the graphics mode being used. (For more information on the hardware icon, refer to Appendix C.)

The CL-GD7548 supports two hardware icon modes:

Hardware Icon Mode 1

Up to four icons, each 64 × 64 pixels in size, can be displayed simultaneously in a vertical column. Each icon is independently controlled for color (up to four colors or three colors plus transparency). Each icon can be expanded either horizontally by pixel doubling, vertically by scanline doubling, or both horizontally or vertically to a maximum size of 128 × 128 pixels per icon.

- When one of the icons is doubled vertically, that icon extends down, which forces the icons below it down.
- When one of the icons is doubled horizontally, that icon expands to the right.
- Each of the four icons is allocated two memory maps. (A total of eight hardware icon memory maps can be stored in display memory.)

Hardware Icon Mode 2

One 64 × 64 pixel hardware icon, from a menu of eight hardware icon memory maps, can be displayed. Each icon is independently controlled for color (up to four colors or three colors plus transparency) and for all other icon attributes (for example, blink, horizontal and vertical doubling, icon enable, and memory map selection).

Hardware icon(s) are supported in all text and graphics modes, except 24-bit/pixel modes with a 3× clock, 16-bit/pixel modes with a 2× clock, and interlaced modes. Hardware icon(s) are independent of the hardware cursor. When both a hardware cursor and hardware icon(s) are displayed, the hardware cursor passes on top of the hardware icon(s). The CL-GD7548 priority of display overlays is as follows:

- Hardware cursor – always displayed on top
- Hardware icon
- Video Window data, or VGA graphics, or text data

3.5.13 Color Palette

The color palette consists of a 256 18-bit-word CLUT (color lookup table). Each 18-bit word consists of three 6-bit values, one for each primary color (red, green, and blue). The 18-bit word defines one of 2^{18} or 262,144 (referred to as '256K') colors. The CLUT converts an 8-bit color code that specifies the color of a pixel into an 18-bit value, such that 256 simultaneous colors are displayed from a palette of 256K colors. Refer to Figure 3-18.

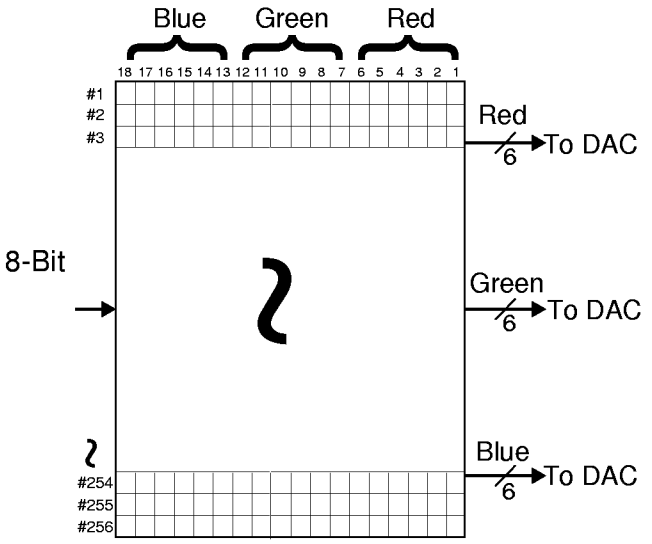


Figure 3-18. Color Lookup Table (CLUT)

The CLUT contents are accessed through its 8-bit-wide host CPU interface. An 8-bit address value applied to the pixel-address inputs defines the memory location for reading an 18-bit color data word from the CLUT. An internal synchronizing circuit allows the color value accesses to be completely asynchronous to the pixel display operation. Special display operations, such as flashing objects and overlays, are possible because the palette incorporates a pixel word mask to allow the incoming pixel address to be altered. As a result, changes to the contents of the CLUT can be made immediately. The CLUT has anti-sparkle circuitry to reduce random noise on the display during host CPU accesses to the palette.

3.5.13.1 Direct-Color and True-Color Modes

In addition to graphics modes that use the 256 × 18 CLUT, the CL-GD7548 supports the following Direct-Color and True-Color modes, which are useful in graphics and multimedia applications:

- **RGB 5-5-5 32K Direct-Color Mode.** This mode bypasses the CLUT. Each pixel is represented by 15 bits, consisting of five bits each of red, green, and blue color information to provide 32,768 (2^{15}) simultaneously displayed colors.
- **RGB 8-8-8 16M True- Color Mode.** This mode bypasses the CLUT. Each pixel is represented by 24 bits, consisting of one byte each of red, green, and blue color information to provide 16,777,216 (2^{24}) simultaneously displayed colors.

For a block diagram showing the above-mentioned modes bypassing the CLUT, refer to Figure 3-19. For more information on true-color modes, refer to Appendix E.

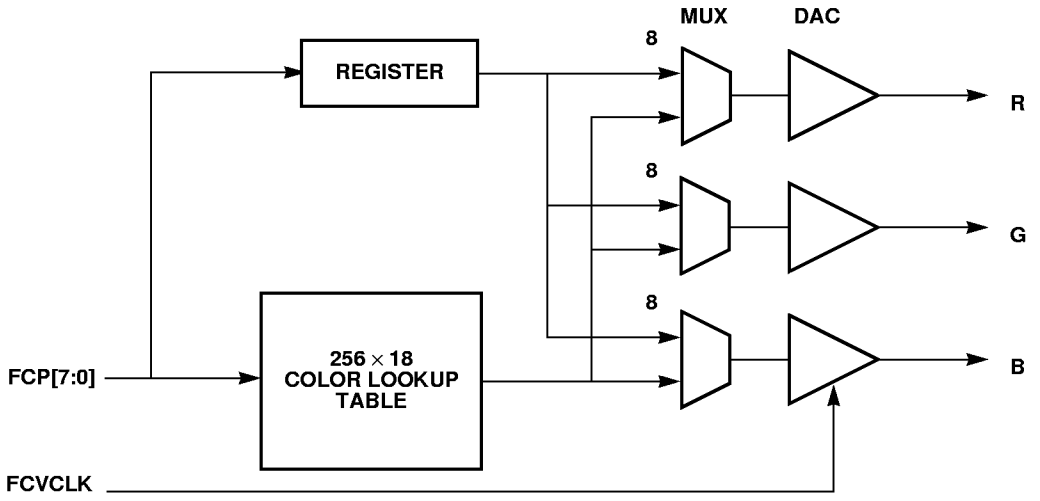


Figure 3-19. 256-Color Direct-Color Palette DAC

3.5.14 Extended Palette RAM

The extended palette RAM provides 18-bit/pixel data (RGB 6-6-6) for the following functions:

- Hardware cursor
- Hardware icon
- Overscan border color

As shown in Table 3-6, the extended palette RAM enables the colors of the hardware cursor, hardware icons, and the border to be programmed independently from the standard 256 × 18 CLUT.

Table 3-6. Extended Palette RAM

I/O Address	Physical RAM Location	Function
X0h	256	Hardware cursor background color
XFh	257	Hardware cursor foreground color
X2h	258	Fix color of overscan (the border)
X3h	259	Hardware icon color #0 (not for 3-colors-and-transparent mode)
X4h	260	Hardware icon color #1
X5h	261	Hardware icon color #2
X6h	262	Hardware icon color #3
XAh	266	Used by VGA BIOS
XBh	267	Used by VGA BIOS
XCh	268	Used by VGA BIOS
XDh	269	Used by VGA BIOS
XEh	270	Used by VGA BIOS

3.5.15 Triple DAC

The DAC includes three 8-bit DACs (digital-to-analog converters). The DAC outputs drive the red, green, and blue color display inputs to the CRT. The DAC outputs are designed to produce a 0.7-volt peak-white amplitude when supplied with a reference current (IREF). The IREF current is supplied with the circuit shown in the IREF pin description in Chapter 2 For all IREF values and output loading:

- $V_{Black\ Level} = 0$ volts
- $V_{Maximum\ White} = 0.7$ volts

To detect the type of CRT monitor that is connected, two sense methods can be used — analog and digital. With the analog sense method, the CL-GD7548 places specific color values on the RGB lines and then compares the resulting voltage level against a known internal reference voltage.

For more information on CRT-only modes, refer to Section 4.1.

3.5.16 TV-Out

With the addition of an analog encoder and minimal additional logic circuitry, portable computer with the CL-GD7548 can output digital RGB data in an interlaced format to one of the following, for use with a standard TV monitor or VCR (video cassette recorder):

- An external composite encoder, such as a NTSC (National Television Standards Committee) encoder
- An external component encoder such as S-VHS
- An external encoder such as a PAL (phase alternation line-rate) encoder

The CL-GD7548 can operate in a locked interlaced mode. In this case, the LCD support shadowing mechanism (which shadows the Horizontal and Vertical CRTC registers) is used to prevent an application from changing any part of the CRT Controller setup, including the dot clock frequency. Horizontal and vertical display enable is open to the application.

The CL-GD7548 outputs analog RGB, a composite synchronization signal, an NTSC/PAL standard select signal, and TV-On (a power-management signal). Due to differences in the standards between PC displays and CRT monitors, the NTSC/PAL output is limited to graphics modes 1h, 3h, 12h, 13h, 5Fh, and 64h. (A special windows driver allows use of graphics mode 5Fh for Windows®.)

Because televisions use interlaced display refresh and have an aspect ratio different than many standard VGA modes, support for additional VGA modes was not included in the CL-GD7548, as such support would result in unusable displays.

The NTSC/PAL functionality provided in the CL-GD7548 is targeted primarily for entertainment use, for display of graphic images, and within certain guidelines, for presentations. However, this functionality was not intended as a direct replacement for a PC CRT. For more information on NTSC/PAL functionality, refer to the application note “Driving NTSC/PAL Display Signals” in the *CL-GD754X Application Book*.

3.5.17 Half-Frame Accelerator

The CL-GD7548 integrates a half-frame accelerator, required by dual-scan LCDs. With the half-frame accelerator, a dual-scan LCD runs at a twice the CRT refresh rate. The CL-GD7548 provides simultaneous CRT and LCD display operation (SimulSCAN) for the following dual-scan LCDs:

- For 640 x 480 STN dual-scan LCDs, the half-frame accelerator provides all the standard VGA modes and extended VGA modes that have a screen format of up to 640 x 480
- For 800 x 600 STN dual-scan LCDs, the half-frame accelerator provides all the standard VGA modes and extended VGA modes that have a screen format of up to 800 x 600.

3.5.18 LCD Interface

The CL-GD7548 interfaces directly with a variety of LCDs (and CRTs, for SimulSCAN operations). These LCDs include the following:

- Color 640 x 480 and 800 x 600 dual-scan and single-scan STN LCDs (with 8- and 16-bit interfaces)
- Color 640 x 480 and 800 x 600 TFT LCDs (from 9 to 24 bits per pixel)
- Color 1024 x 768 TFT LCDs, with the following interfaces:
  - 12-bit (4 bits each for RGB, and 1 pixel per shift clock)
  - 18-bit (6 bits each for RGB, and 1 pixel per shift clock)
  - 24-bit (8 bits each for RGB, and 1 pixel per shift clock)
  - 24-bit (4 bits each for RGB, and 2 pixels per shift clock, with external latch circuitry)
  - 36-bit (6 bits each for RGB, and 2 pixels per shift clock, with external latch circuitry)
  - 48-bit (8 bits each for RGB, and 2 pixels per shift clock, with external latch circuitry)

3.5.18.1 LCD Resolution Compensation

With its LCD resolution compensation, the CL-GD7548 allows a spectrum of PC applications, originally written for analog CRT monitors that use various VGA modes, to run transparently on LCDs. This LCD resolution compensation feature is necessary, in that unlike CRTs, LCDs have a fixed horizontal and vertical resolution. As a result, when a PC application is selected, VGA modes that are concurrently selected can use a resolution that is lower than the fixed resolution of the LCD. Consequently, unless LCD resolution compensation is used, a section of the LCD is left blank.

For example, when VGA text mode 3, which consists of 400 lines, is displayed on a 640 $\times$ 480 LCD that does not have use of LCD resolution compensation, 80 blank lines remain at the bottom of the LCD. (For a list of various horizontal and vertical resolutions for standard VGA modes, refer to Chapter 4.)

To remove blank space, the CL-GD7548 LCD resolution compensation presents these options:

- Automatic expansion of VGA text modes
- Custom text fonts to replace standard VGA text fonts
- Horizontal centering of displayed lines
- Horizontal expansion of VGA graphics modes
- Vertical centering of displayed lines
- Vertical expansion of VGA graphics modes

Resolution Compensation for 640 x 480 LCDs

For 640 × 480 LCDs, the CL-GD7548 provides the following LCD resolution compensation options to display lower-resolution VGA text and graphics:

- **Automatic Text Expansion.** Automatic text expansion of a VGA text font makes the text font consistent across the LCD and eliminates any breaks or artifacts in text fonts that connect to adjacent text fonts.
  - — The 9-pixel-wide VGA text (used in the popular standard VGA text modes 3h and 7h) is horizontally displayed as 8-pixel-wide text. As a result, 80 characters fill all 640 pixels across.

  The following methods automatically vertically expand VGA character text to 19 pixels. As a result, 475 lines of the 480 vertical lines of the LCD are filled.
  - — The 8 × 8 (200-line) VGA text is double-scanned, vertically expanding the text to equal 16 pixel lines. An extra top pixel line and two extra bottom pixel lines are added to each character row of the text, further vertically expanding the text to 19 pixel lines.
  - — For 8 × 14 (350-line) VGA text, two extra top pixel lines and three extra bottom pixel lines are added to each character row to vertically expand the text to 19 pixel lines.
  - — For the 8 × 16 (400-line) VGA text, an extra top pixel line and two extra bottom pixel lines are added to each character row to vertically expand the text to 19 pixel lines.
- **Custom Text Fonts.** Standard VGA text fonts (8 × 8, 8 × 14, and 9 × 16) can be replaced with a custom 8 × 19 text font to fill 640 × 475 pixels on a 640 × 480 LCD.
- **Vertical Centering of Displayed Lines**
  - — If automatic text expansion or a custom text font is used, the 475 lines that result can be vertically centered on the 480-line LCD.
  - — If automatic text expansion or a custom text font is not used, 200-, 350-, or 400-line VGA text or graphics modes can also be vertically centered on the 480-line LCD.
- **Vertical Graphics Expansion.** On a 640 × 480 LCD, vertical graphics expansion can be used to run PC application programs that use lower-resolution VGA graphics modes.
  - — The 200-line VGA graphics modes are vertically expanded to 475 lines by expanding every 8 lines to 19 lines, using a pattern of 2,2,3,2,2,3,2,3 (double- and triple-scan).
  - — The 350-line VGA graphics modes are vertically expanded to 475 lines by expanding every 14 lines to 19 lines using a pattern of 1,1,2,1,1,2,1,2,1,1,2,1,1,2 (single- and double-scan).

Popular GUI-based applications, such as Windows or OS/2, use a CL-GD7548 driver that selects the proper VGA graphics mode (such as 2-, 16-, 256-, 32K-, 64K-, or 16M-color modes) to run application programs at the full resolution of the 640 × 480 LCD.

Resolution Compensation for 800 x 600 LCDs

For 800 × 600 LCDs, the CL-GD7548 provides the following LCD resolution compensation options to display lower-resolution VGA text and graphics.

NOTE: Resolution compensation applies to modes less than or equal to 8 bits/pixel.

- **Automatic-Text Expansion.** Automatic-text expansion of a VGA text font makes the text consistent across the LCD and eliminates any breaks or artifacts in text that connects to adjacent text.
  - — The 9-pixel-wide VGA text (used in the popular VGA text modes 3h and 7h) is horizontally displayed as 10-pixel-wide text, by replicating the last pixel once. As a result, 80 characters fill all 800 pixels across.

The following methods vertically expand the VGA character text.

- — The 8 × 8 (200-line) VGA text is triple-scanned, vertically expanding the text to equal 24 pixel lines. As a result, all of the LCD 600 vertical lines are filled.
- — For the 8 × 14 (350-line) VGA text, every odd scanline is replicated to vertically expand the text to 21 lines. As a result, 525 lines of the LCD 600 vertical lines are filled.
- — For the 8 × 16 (400-line) VGA text, every odd scanline is replicated to vertically expand the text to 24 lines. As a result, all of the LCD 600 vertical lines are filled.

- **Custom Text Fonts.** Standard VGA text fonts (8 × 8, 8 × 14, and 9 × 16) can be replaced with a custom 10 × 24 text font to fill all 800 × 600 pixels on a 800 × 600 LCD.
- **Horizontal Centering**
  - — VGA text modes that are 720 pixels wide can be horizontally centered, leaving 40 blank pixels each on the left and right sides of the 800 × 600 LCD display.
  - — VGA text modes that are 640 pixels wide can be horizontally centered, leaving 80 blank pixels each on the left and right sides of the 800 × 600 LCD display.
- **Horizontal Graphics Expansion.** VGA graphics modes that are 640 pixels wide can be horizontally expanded to 800 pixels by replicating every fourth pixel. (However, currently this expansion is not available for VGA graphics modes that have either 2× dot clocks with 16-bits/pixel or 3× dot clocks with 24-bits/pixel).
- **Vertical Centering**
  - — If automatic-text expansion or vertical graphics expansion is used, the 525 lines that result can be vertically centered on the 600-line LCD.
  - — If automatic-text expansion is not used, the 200-, 350-, or 400-line VGA text or graphics modes can also be vertically centered on the 600-line LCD.
- **Vertical Graphics Expansion.** On a 800 × 600 LCD, vertical graphics expansion can be used to run PC application programs that use lower-resolution VGA graphics modes.

  For example, VGA graphics modes that are:
  - — 350 lines are vertically expanded to 525 lines by replicating all odd scanlines.
  - — 400 lines are vertically expanded to 600 lines by replicating all odd scanlines.
  - — 480 lines are vertically expanded to 600 lines by replicating every fourth scanline.

Popular GUI-based applications, such as Windows or OS/2, use a CL-GD7548 driver that selects the proper VGA graphics mode (for example, 2-, 16-, 256-, 32K-, or 64K-color modes) to run the application programs at the full resolution of the 800 × 600 LCD.

3.5.19 Frame Rate Modulation

The CL-GD7548 employs a new, improved FRM (frame rate modulation) algorithm to create shades on color STN LCDs. Over multiple frames in time, the FRM algorithm modulates the 'on' and 'off' times of individual pixels in the LCD, such that the eye integrates the superimposed pixels as perceptible grayscales.

Proprietary techniques reduce or eliminate entirely the grayscale artifacts (for example, flicker, noise and pattern motion). On state-of-the-art STN LCDs with fast response times of approximately 100 ms, the result is an outstanding display quality.

The CL-GD7548 provides three FRM options:

- **16-frame FRM.** This FRM option modulates the pixel over 16 frames in time to create 16 shades for each red, green, and blue (RGB) primary color, for 4,096 (16^3) colors total. This option is intended to support STN LCDs currently available and in development, including STN LCDs with very fast response times of approximately 100 ms. This algorithm allows masking of undesirable grayscales (that is, those that exhibit flicker or pattern motion).
  - — By setting register RBX[4], grayscales 7 and 9 can be converted to grayscales 6 and 8, respectively.
  - — By setting register RBX[3], grayscales 1 and 15 can be converted to grayscales 0 and 16, respectively.
  - — If two grayscales are masked, the FRM algorithm produces 2,744 (14^3) colors.
  - — If four grayscales are masked, the FRM algorithm produces 1,728 (12^3) colors.
- **8-frame FRM.** This FRM option modulates the pixel over 8 frames in time to create 8 shades for each RGB primary color, for 512 (8^3) colors total. This option is intended to reduce flicker and 'submarining' (that is, the temporary disappearance of the mouse pointer) on future STN LCDs that may have response times that are too fast for the 16-frame FRM option.
- **4-frame FRM.** This FRM option modulates the pixel over 4 frames in time to create 4 shades for each RGB primary color, for 64 (4^3) colors total. This option is intended to reduce flicker and 'submarining' on future STN LCDs that may have response times that are too fast for both the 16- and 8-frame FRM options.

In summary, the FRM algorithm produces 2, 3, or 4 bits of color depth for each RGB primary color on STN LCDs.

- To add up to 6 bits of color depth to each primary color, the dithering engine can be used with an FRM algorithm.
- To add up to 8 bits of color depth to each primary color (or 256 grayscales for each primary color) for a total of 16M colors, the dithering engine can be used with only a 4-frame FRM algorithm.

3.5.19.1 Dithering Engine

The dithering engine increases the number of perceived colors displayed on the LCD and/or CRT, relative to what the display can physically produce without dithering.

A proprietary intercalating spatial dithering technique preserves the spatial resolution of the displayed image. For example, when a 640 × 480 resolution image is dithered, its resolution is maintained, instead of being reduced to 320 × 240.

The dithering engine works by automatically selecting a dithering pattern. As shown in Table 3-7, an increase in the dithering pattern increases the number of displayed bits per RGB primary color, depending upon the color depth of the image.

Table 3-7. Effective Dithering Patterns

Effective Dithering Pattern	Increased Number of Displayed Bits per RGB Primary Color
2 × 1	1 bit
2 × 2	2 bits
4 × 2	3 bits
4 × 4	4 bits
8 × 4	5 bits
8 × 8	6 bits

The dithering engine can automatically add up to 6 bits per primary color, and it can be used for color STN LCDs and TFT LCDs. (By programming Extension register CR4C, this automatic feature can be overridden and the number of bits per primary color limited to a programmable number.)

As shown in block diagram Figure 3-13 in Section 3.4, in the data path, the dithering engine function comes after the LCD resolution compensation, so that dithering is applied to the expanded image. The dithering engine contains these separate dithering registers:

- Dithering register for standard/extended VGA modes
- Dithering register for Video Overlay
- Dithering register for Video Window

To render the appropriate colors, the CL-GD7548 dynamically switches dithering between the surrounding graphics and the Video Window.

Table 3-8 shows the number of displayed colors on a color STN LCD with various FRM and dithering options. The total number of colors is equal to 3× the number of color per primary color (RGB).

Table 3-8. Number of Colors on Color STN LCDs

Primary Color RGB			Resulting Image on Color STN LCD That Has:	
Frame-Rate-Modulation Option	Generated by LCD		32K Colors (15 bits)	256K Colors (18 bits)
	Dithering Pattern	No. of Bits		
4 frames (2 bits)	None	0	64 (2^6)	
	2 × 1	1	512 (2^9)	
	2 × 2	2	4K (2^{12})	
	4 × 2	3	32K (2^{15})	
	4 × 4	4	Illegal[a]	256K (2^{18})
	8 × 4	5	Illegal	
	8 × 8	6	Illegal	
8 frames (3 bits)	None	0	512 (2^9)	
	2 × 1	1	4K (2^{12})	
	2 × 2	2	32K (2^{15})	
	4 × 2	3	Illegal	256K (2^{18})
	4 × 4	4	Illegal	
	4 × 8	5	Illegal	
16 frames (4 bits)	None	0	4K (2^{12})	
	2 × 1	1	32K (2^{15})	
	2 × 2	2	Illegal	256K (2^{18})
	4 × 2	3	Illegal	
	4 × 4	4	Illegal	

[a] 'Illegal' indicates an illegal combination.

Table 3-9 shows the number of colors that various dithering patterns produce on 512-color TFT LCDs. If an image using the standard VGA 18-bit color palette is displayed on a 512-color TFT LCD (that is, a TFT LCD that has only a 9-bit color palette), significant banding or contour lines are readily apparent.

Consequently, the dithering engine automatically uses a 4×2 pattern to increase the number of displayed colors from the 3 bits per primary color that the LCD produces to the full 6 bits per primary color in order to meet the 18-bit VGA color palette requirement upon the displayed image's color depth.

Table 3-9. Number of Colors on 512-Color TFT LCDs

Primary Color RGB Generated by LCD		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	No. of Bits	32K Colors (15 bits)	256K Colors (18 bits)	16M Colors (24 bits)
None	0	512 (2^9)		
2×1	1	4K (2^{12})		
2×2	2	32K (2^{15})		
4×2	3	Illegal[a]	256K (2^{18})	
4×4	4	Illegal		2M (2^{21})
8×4	5	Illegal		16M (2^{24})

[a] 'Illegal' indicates an illegal combination.

Table 3-10 shows the number of colors various dithering patterns produce on 4K-color TFT LCDs.

Table 3-10. Number of Colors on 4K-Color TFT LCDs

Primary Color RGB Generated by LCD		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	No. of Bits	32K Colors (15 bits)	256K Colors (18 bits)	16M Colors (24 bits)
None	0	4K (2^{12})		
2×1	1	32K (2^{15})		
2×2	2	Illegal[a]	256K (2^{18})	
4×2	3	Illegal		2M (2^{21})
4×4	4	Illegal		16M (2^{24})

[a] 'Illegal' indicates an illegal combination.

Table 3-11 shows the number of colors that dithering patterns produce on 256K-color TFT LCDs.

Table 3-11. Number of Colors on 256K-Color TFT LCDs

Primary Color RGB Generated by LCD		Resulting Image on Color TFT LCD That Has:		
Dithering Pattern	**No. of Bits**	**32K Colors (15 bits)**	**256K Colors (18 bits)**	**16M Colors (24 bits)**
None	0	32K (2^{15})	256K (2^{18})	256K (2^{18})
2 × 1	1			2M (2^{21})
2 × 2	2			16M (2^{24})

3.5.20 Frequency Synthesizer

The frequency synthesizer generates all clock frequencies for the operation of VGA modes and VGA extension modes. Using a single reference frequency of 14.318 MHz that is supplied from an external TTL-level source, the frequency synthesizer generates two fully programmable clocks — the video clock (VCLK) and the memory clock (MCLK).

For a functional diagram of the frequency synthesizer, refer to Figure 3-20.

- VCLK
  - — VCLK (video clock) is the fundamental video timing clock that generates all clocks needed for video display timing signals (for example, HSYNC and VSYNC) and for the pixel clock.
  - — VCLK must be changed to support various display resolutions and refresh rates.
  - — The VCLK frequencies are programmed with Extension registers SRB–SRE and SR1B –SR1F.
  - — The CL-GD7548 supports VCLKs up to 80 MHz at 5 V or 77 MHz at 3.3 V.
- MCLK
  - — MCLK (memory clock) generates all clocks needed for memory timing signals (for example, RAS#, CAS#).
  - — MCLK must be optimized for the speed of the display memory used.
  - — MCLK frequencies are programmed with Extension register SR1F.
  - — For optimal selection of DRAM speeds, the CL-GD7548 supports MCLKs up to 66 MHz at 5 V or 54 MHz at 3.3 V.

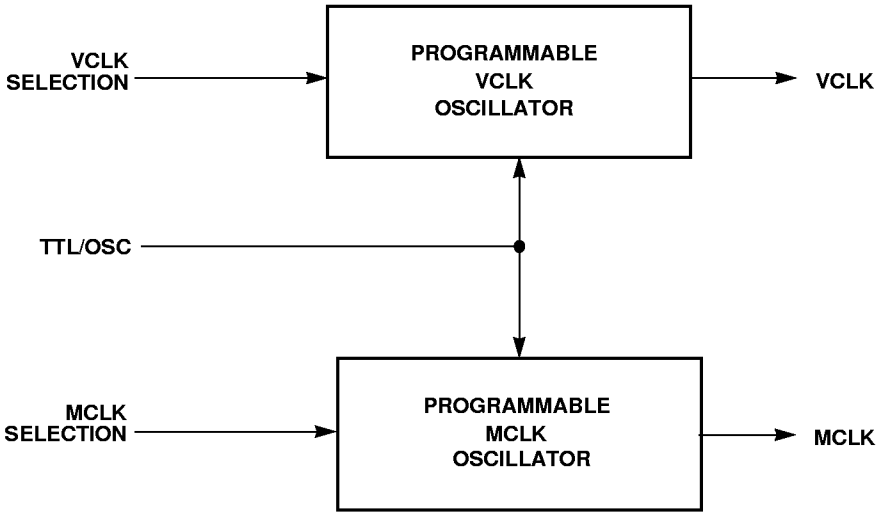


Figure 3-20. Programmable Dual-Frequency Synthesizer Functional Diagram

3.6 Controller Operation

3.6.1 Power Management

The CL-GD7548 supports power-management techniques to maximize battery life, including:

- **LCD-only power savings.** During LCD-only operations, the video DAC (including its monitor sense comparators) is powered down, and the video clock (VCLK) can be reduced to a level that still minimizes flicker.
- **LCD power-up/down sequence control.** To protect the LCD, the FPVEE and FPVCC output signals control the LCD power-up and power-down sequence. The FPBL output signal controls the LCD backlight enable.

CAUTION: Damage can occur if VEE (the LCD high-voltage power) is applied without VDD (the LCD logic power).

- **Mixed-voltage interfaces.** The host CPU bus, display memory, LCD, and CRT interfaces can each be implemented at either 3.3 or 5 V. The voltages used for each interface can be mixed in any combination.
- **Standby mode.** This mode reduces power consumption by turning off the display while allowing application programs to continue to run normally in the background.
  - — Standby is entered either by way of the SBYI pin, by using the internal Standby Counter, or by programming a register.
  - — During Standby mode, using proper power sequencing, the LCD and CRT are turned off, the video clock (VCLK) is stopped, and the video DAC is powered down. The host CPU can still access and modify the display memory and palette.
  - — The Standby mode is exited as it is entered, either by way of the SBYI pin, by using the internal Standby Counter, or by programming a register.
- **Suspend Mode.** This mode reduces power consumption when the system remains inactive for a relatively long period of time, while maintaining the contents of the controller registers, palette, and display memory. Unlike Standby mode, however, during the Suspend mode, applications are suspended and do not continue to run normally in the background.
  - — Hardware-controlled Suspend is entered by way of the SUSPI pin. Software-controlled Suspend is entered by setting Extension register CR20[3]. In contrast to hardware-controlled Suspend, software-controlled Suspend allows the host CPU to access the internal registers, which requires an active clock and I/O capability, and therefore, more power.
  - — During hardware-controlled Suspend, the display is turned off, the video (VCLK) and memory (MCLK) clocks are both stopped, and host CPU accesses to the display memory, palette, and I/O registers cease. The CL-GD7548 configures display memory for self-refresh or uses the 32-kHz clock for memory refresh.
  - — Hardware-controlled Suspend is exited by way of the SUSPI pin. When Suspend mode is exited, any application programs that were previously running can be quickly re-started from the point at which they suspended.
- **VESA Display Power Management. T**o comply with the U.S. Environmental Protection Agency's Energy Star Computer qualifications, the CL-GD7548 supports the VESA Display Power Management Signaling specification for CRT power management. For more information, refer to Appendix H.

3.6.2 Performance

The CL-GD7548 is designed with the following performance-enhancing features:

- **BitBLT engine.** The BitBLT engine is used to accelerate GUIs (graphical user interfaces), such as Microsoft Windows. It operates at an MCLK of either 54 MHz (for 3.3-V systems) or 66 MHz (for 5-V systems), and it supports the following:
  - — BitBLAST
  - — Transparent BitBLT
  - — Memory-mapped I/O
  - — Support for EDO DRAMs
- **Bus interface choices.** The CL-GD7548 provides a choice of bus interfaces for optimum performance:
  - — 32-bit VESA VL-Bus
  - — '486 local-bus interface
  - — PCI bus interface with burst mode
- **Host CPU interfaces to I/O registers and memory.** For increased performance, the CL-GD7548 supports the following host CPU interfaces:
  - — 32-bit CPU interface to display memory, for faster host CPU access to memory for all modes, including planar modes
  - — 16-bit CPU interface to I/O registers, for faster host CPU access to the registers
- **Extended-write modes.**
  - — For faster host CPU write performance, the extended-write modes can be used on 8 pixels at a time in 8- or 16-bit/pixel graphics modes that have packed-pixel addressing.
  - — These write modes can be used for faster text writing, pattern filling, and block-moving operations in graphics modes.

    For more information, refer to Appendix D.
- **Hardware cursor.** GUI performance can be improved by using the 32×32 or the 64×64 hardware cursor.
- **Memory data fast access.** To access display memory fast, the CL-GD7548 supports the following:
  - — 32-bit display memory data bus
  - — DRAM fast-page mode operations
- **Video FIFO.** Video FIFO minimizes memory contention.
- **Zero-wait-state performance.** For faster host CPU access for writes to display memory, the CL-GD7548 provides zero-wait-state performance and a CPU write buffer.

3.6.3 RAMDAC Operation

3.6.3.1 Writing to the Color Lookup Table (CLUT)

To write a color definition to the CLUT, a value specifying an address location in the CLUT is first written to the External/General register 3C8 (the Pixel Address Write Mode register). The color values for the red, green, and blue intensities are then written in succession to External/General register 3C9 (the Pixel Data register). After the blue data bits are latched, the new color data bits are then written into the CLUT at the defined address, and the CL-GD7548 automatically increments the Pixel Address Write Mode register.

Since the CL-GD7548 increments the Pixel Address Write Mode register after each transfer of data to the CLUT, it is best to write a set of consecutive locations at once. The start address of the set of locations is first written to External/General Register 3C8 (the Pixel Address Write Mode Address). The color data bits for each address location are then sequentially written to the Pixel Data register. After each host CPU transfer of three bytes of color data, the CL-GD7548 automatically writes data to the CLUT and automatically increments the Pixel Address Write Mode register.

3.6.3.2 Reading from the CLUT

To read color data from the CLUT, a value specifying the address location of the data is written to the External/General Register 3C7 (the Pixel Address Read Mode Register). After the address is latched, data bits from this location are automatically read out to the External/General register 3C9 (the Pixel Data register), and the CL-GD7548 automatically increments the Pixel Address Write Mode register.

The color intensity values are then read from External/General register 3C9 by a sequence of three read (RD*) commands. After the blue value is transferred out, new data bits are read from the CLUT current address to External/General register 3C9, which causes the CL-GD7548 to automatically increment the the Pixel Address Write Mode register.

If the CL-GD7548 loads the Address register to be used with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This action occurs for both read and write operations.

3.6.4 Programmable Core Voltage

The CL-GD7548 supports selective switching of the core VDD between 3.3 V and 5 V. As a result, based upon the video mode used, the designer can select either optimum graphics performance or minimal power consumption, as necessary. (For more information, refer to the application note, "A Programmable Core Voltage Solution" in the *CL-GD754X Application Book*.)

3.6.4.1 3.3-V Core Voltage

When the CL-GD7548 operates at 3.3 V, the CL-GD7548 MCLK operates up to 54 MHz, which is sufficient for the following pixel modes:

- 800 × 600 8-bit/pixel
- 640 × 480 16-bit/pixel

The core VDD and analog VDDs *must always* be at the same voltage.

3.6.4.2 5.0-V Core Voltage

When the CL-GD7548 operates at 5.0 V, the CL-GD7548 MCLK must be at 66 MHz to maximize performance in the following pixel modes:

- 1024 × 768 8-bit/pixel
- 800 × 600 16-bit/pixel
- 640 × 480 24-bit/pixel

The core VDD and analog VDDs (which *must always* be at the same voltage) must be 5 V with an MCLK of 66 MHz.

3.6.5 Compatibility

The CL-GD7548 includes all registers and data paths required for standard VGA controllers. It supports various 132-column text modes as well as the following extended VGA modes:

- 1024 x 768 with 256 colors (interlaced and non-interlaced modes)
- 1280 x 1024 with 256 colors (interlaced modes)

While expanding or centering VGA modes on 640 x 480 or 800 x 600 LCDs, the appropriate VGA registers are shadowed for VGA compatibility.

3.6.6 Testability

The CL-GD7548 is testable by using pin-scan testing and a signature generator.

- Pin-scan testing tests the signal state of every pin on the chip. The test detects any pins that are not connected to the board, or that are shorted to a neighboring pin or trace. For more information, refer to Appendix J.
- The signature generator allows the entire system, including display memory, to be tested at speed. For more information, refer to Appendix I.

3.6.7 Configuration Inputs

To configure the CL-GD7548 for operation, the CL-GD7548 uses hardware and software combined.

3.6.7.1 Hardware Configuration Inputs

Pull-up resistors are used on some memory data pins (MD25, MD23:21, MD19:18, and MD16), which are read during the low-to-high transition of the system reset or when Extension register SR24[3] (the External Pull-Up Reset register bit)] is toggled.

- **32-bit PCI bus.** This configuration selects the 32-bit PCI bus with Min-grant timing of 8 PCI CLKs (~250 ns at 33 MHz).
- **32-bit PCI bus with Min-grant extended.** This configuration selects the 32-bit PCI bus, but with Min-grant timing extended from 8 PCI CLKs (~250 ns at 33 MHz) to 16 PCI CLKs (~500 ns at 33 MHz), allowing burst write mode capability.
- **Enable Feature Connector.** This configuration uses the appropriate pins for the Feature Connector V-Port™. (For the affected pins, refer to the pin descriptions in Chapter 1 and Chapter 2.)
- **Sleep address select.** This configuration selects a sleep address of either I/O address 46E8h or 3C3h (the default).
- **VESA VL-Bus with Bus CLK greater than 33 MHz.** This configuration sets the VL-Bus for >33-MHz local bus operation.

If no resistors are present, the previously mentioned memory data pins are read as low because of the internal pull-down resistors. The status of these inputs is stored in Extension registers SR22 and SR24.

Three hardware switch inputs (SW[2:0]) are read during each horizontal retrace period. These inputs are used by the VGA BIOS to monitor external activities that can affect the chip operation. The status of these three inputs is stored in Extension register SR24[2:0].

For more information on hardware configuration, refer to Appendix L.

3.6.7.2 Software Configuration Inputs

Software-programmable registers are used to select the desired function of some multi-function pins as defined below:

- **ACTI / DDCD / FCEVIDEO# / SBYI select.** Extension registers SR23[6] and SR24[7] configure the ACTI / DDCD / FCEVIDEO# / SBYI input (pin 86) as either the Activity Sense input or the hardware-controlled Standby input.
- **BLI / SUSPI enable.** Extension registers SR23[5] and SR24[7] configure the BLI / SUSPI input (pin 87) as either the backlight input control or the hardware-controlled Suspend input.
- **FCDCLK output select.** Extension register SR24[4] is used to configure the DDCC / FCDCLK / VCLK output pin (pin 103) for either FCDCLK or VCLK output.
- **FCVCLK enable.** Extension register SR23[7] selects whether FCVCLK is sent to the RAMDAC only or is also used for VCLK generation.
- **VCLK output enable.** Extension registers SR23[4] and SR24[7] either make the VCLK output pin low or output the internal VCLK on the DDCC / FCDCLK / VCLK output (pin 103).

For more configuration information, refer to Chapter 2 and Appendix L.

3.7 Software Support

The Cirrus Logic CL-GD7548 VGA BIOS is a high-quality, feature-rich firmware product designed to take maximum advantage of the CL-GD7548 controller, especially in the areas of display quality, power management, and graphics performance. The key features of the VGA BIOS are:

- Super VGA-compatible BIOS
- Supports SimulSCAN™ operation (simultaneous LCD and CRT display)
- Supports the power-management modes
- Supports display-enhancement features
- Can be integrated with the System BIOS
- Supports switchless configuration
- Can be customized without source code through using utility programs such as OEMSI
- Provides VESA-compatible modes and 1.2-function support for VGA BIOS Extensions (VBE)
- Supports multiple monitor refresh rates

A VGA BIOS, compatible with the standard IBM VGA BIOS and the INT 10h graphics service functions, is available from Cirrus Logic and third-party BIOS vendors.

The CL-GD7548 VGA controller and its BIOS can be implemented as an adapter board or placed directly on the system board. The core BIOS requires 48 Kbytes linear addressing. The VESA VL-Bus BIOS can be located at C000h or E000h. The BIOS may also be used for PCI bus implementations.

3.7.1 Software Support for OEMs

This section lists CL-GD7548 software utilities that Cirrus Logic provides for OEM development use.

- **CLDemo**. This utility is a suite of programs that test and demonstrate some of the various features in the CL-GD7548, including hardware icon functions and dithering quality.
- **CL_STEST.** This utility is a DOS-based screen-testing utility that provides the following:
  - CL-STEST enables the user to display and adjust the position and RGB color of a variety of patterns (including color bars, lines, and rectangles) to test the display quality.
  - CL-STEST can operate with pixel resolutions of:
    - 640×400 or 640×480
    - 800×600
    - 1024×768
- **LOADROM.** This utility loads the VGA BIOS into RAM segment 9000h. It is used with the CL-GD7548 PCI Demonstration Board or to quickly test BIOS variations and modifications before loading the BIOS into an EPROM.
- **OEMSI.** This utility is a Cirrus Logic VGA BIOS-customization utility for OEM use.
- **PCLRegs.** This utility is a DOS-based VGA controller register viewer/editor utility that provides the following:
  - PCLRegs enables users to view and edit CL-GD7548 standard and extension VGA registers and the color palette.
  - The PCLRegs Help screen provides a brief explanation of each bit in each register.
  - PCLRegs enables register values to be changed by typing in a new hex value or toggling individual bits.
  - PCLRegs displays a variety of CL-GD7548 configuration data, including the status of the CRT controller, the graphics mode being used, information about the VGA BIOS, and hardware cursor information.

3.7.2 Software Support for End Users

Cirrus Logic provides the following CL-GD7548 software utilities for distribution to end users:

- **CLMode.**

  This utility, a DOS-based graphics-mode and display-configuration utility, provides the following:

  — VGA Configuration menu: User-friendly menu that enables end users to turn 'on' and 'off' a variety of graphics configuration options, including the following:

    — Selection between CRT, LCD, and SimulSCAN™ display options

    — Selection between PAL and NTSC television modes

  — Monitor Type Setup menu: Enables end users to set CRT monitor resolution and refresh rate.

  — VGA Modes Preview menu: Enables end users to display the various VGA modes.

  — End users can enable new settings of the above options by using the AUTOEXEC.BAT file.

- **Drivers.** The CL-GD7548 simplifies driver support for third-party sources because it is based on the industry-leading CL-GD542X VGA controller design. As a result, a driver supplier can easily modify an existing CL-GD542X driver to support the CL-GD7548. At a minimum, this utility allows the CL-GD7548 to operate within the restrictions of the older CL-GD542X driver. The CL-GD7548 supports the following drivers:

  — AutoCAD®, AD1 4.2

  — OS/2®, version 3.0

  — Windows 3.X drivers

    — DCI 1.x drivers for Video for Windows 1.1.d or later

  — Windows 95™ drivers (including DirectDraw and DirectVideo)

  — Windows NT, version 3.5

  — Driver support for the Japanese version of Windows and OS/2 is also available.

  — V-Port™ management with DCI (Display Control Interface) 1.x and DirectDraw/DirectVideo compliance.

- **WinMode.** This utility is a multi-language Windows application to configure the Windows display driver. WinMode determines the language that is in use by Windows, and when possible, WinMode displays user and help dialogues in that language. A unique feature of the WinMode utility is the ability to automatically switch the display resolution without relaunching Windows. This feature ensures that a portable user always sees a Windows display, even though they may dynamically switch from using a high-resolution CRT to an LCD of lower resolution. This feature also enables the user to avoid running the Windows Setup application in order to find and switch driver resolutions. (However, color depth changes still require Windows to restart.)
  - — WinMode allows end users to set high refresh rates for CRT monitors.
  - — WinMode enables end users to set the CRT to the following resolutions:
    - — 640 × 400 or 640 × 480
    - — 800 × 600
    - — 1024 × 768
    - — 1280 × 1024
  - — WinMode enables end users to select bit depth used on either the CRT or LCD (such as 256, 64K, 16M).
  - — WinMode enables end users to turn mouse trails 'on' and 'off'.
  - — WinMode enables end users to make the text size normal or large.
  - — The WinMode utility allows end users to enable new settings of the above options by using the AUTOEXEC.BAT and SYSTEM.INI files.
  - — WinMode also defines the resolution and bit-depth of the CL-GD7548 Windows driver. The WinMode utility provides the following:
    - — Selection between display options: CRT, LCD, and SimulSCAN™, as well as PAL and NTSC monitors
    - — Selection to display WinMode in different foreign languages
    - — Selection for virtual display (pan and scroll capability)

4. MODE TABLES

This chapter lists tables for configuring the CL-GD7548 for various CRT and LCD graphics and text modes. For detailed information on specific LCDs that the CL-GD7548 can drive, refer to the "Panel Interface Guide" in the *CL-GD754X Application Book*.

NOTE: The parameters detailed in the tables of this chapter define standard capabilities of the CL-GD7548 when it is used with the Cirrus Logic VGA BIOS. Consult with the appropriate BIOS vendor for information about modes and parameters supported by BIOSs that are not from Cirrus Logic.

4.1 CRT-Only Mode Tables

This section lists tables for IBM Standard VGA and Cirrus Logic Extended CRT-only modes.

4.1.1 IBM® Standard VGA CRT-Only Modes

The IBM® Standard VGA BIOS supports the CRT-only modes listed in Table 4-1

Table 4-1. IBM® Standard VGA CRT-Only Display Modes

Standard VGA Display Mode Number (hex)	VESA® Display Mode Number	Number of Colors	Characters × Rows	Character Cell (pixels)	Display Screen Format, Column × Row (pixels)	Type of Display Mode	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
00, 01	–	16/256K	40 × 25	8 × 8	320 × 200	Text	31.5	70
00*, 01*	–	16/256K	40 × 25	8 × 14	320 × 350	Text	31.5	70
00+, 01+	–	16/256K	40 × 25	9 × 16	360 × 400	Text	31.5	70
02, 03	–	16/256K	80 × 25	8 × 8	640 × 200	Text	31.5	70
02*, 03*	–	16/256K	80 × 25	8 × 14	640 × 350	Text	31.5	70
02+, 03+	–	16/256K	80 × 25	9 × 16	720 × 400	Text	31.5	70
04, 05	–	4/256K	40 × 25	8 × 8	320 × 200	Graphics	31.5	70
06	–	2/256K	80 × 25	8 × 8	640 × 200	Graphics	31.5	70
07*	–	Mono.	80 × 25	9 × 14	720 × 350	Text	31.5	70
07+	–	Mono.	80 × 25	9 × 16	720 × 400	Text	31.5	70
0D	–	16/256K	40 × 25	8 × 8	320 × 200	Graphics	31.5	70
0E	–	16/256K	80 × 25	8 × 8	640 × 200	Graphics	31.5	70
0F	–	Mono.	80 × 25	8 × 14	640 × 350	Graphics	31.5	70
10	–	16/256K	80 × 25	8 × 14	640 × 350	Graphics	31.5	70
11	–	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	60
12	–	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	60
13	–	256/256K	40 × 25	8 × 8	320 × 200	Graphics	31.5	70

4.1.2 Cirrus Logic Extended CRT-Only Modes

The Cirrus Logic VGA BIOS supports the extended CRT-only modes listed in Table 4-2.

- Columns one and two compare the hex number of the Cirrus Logic extended CRT-only mode with the hex number of the equivalent VESA VL-Bus CRT-only mode.
- If the BIOS used is not the Cirrus Logic VGA BIOS, modes may differ.
- Some modes are not supported by all CRT monitors.

Table 4-2. Cirrus Logic Extended VGA CRT-Only Display Modes

Extended VGA Display Mode No. (hex)	VESA Display Mode No. (hex)	Number of Colors	Char. × Rows	Char. Cell (pixels)	Display Screen Format, Column × Row (pixels)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	VCLK (MHz)	Mini-mum MCLK (MHz)	Required CVDD Voltage (Volts)
Text Display Modes										
14	–	16/256K	132 × 25	8 × 16	1056 × 400	31.5	70	41.5	45	3.3
54	10A	16/256K	132 × 43	8 × 8	1056 × 350	31.5	70	41.5	45	3.3
55	109	16/256K	132 × 25	8 × 14	1056 × 350	31.5	70	41.5	45	3.3
Graphics Display Modes										
11	–	2/256K	80 × 30	8 × 16	640 × 480	37.9	72	31.5	40	3.3
						37.5	75	31.5	40	3.3
12	–	16/256K	80 × 30	8 × 16	640 × 480	37.9	72	31.5	40	3.3
						37.5	75	31.5	40	3.3
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	35.2	56	36	45	3.3
						37.8	60	40	45	3.3
						48.1	72	50	45	3.3
						46.875	75	50	45	3.3
5C	103	256/256K	100 × 37	8 × 16	800 × 600	35.2	56	36	45	3.3
						37.9	60	40	45	3.3
						48.1	72	50	45	3.3
						46.875	75	50	45	3.3
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	35.5	43.5 87†	44.9	45	3.3
						48.3	60	65	45	3.3
						56	70	75	45	3.3
						58	72	77	45	5.0
						60	75	78.75	45	5.0
5E	100	256/256K	80 × 25	8 × 16	640 × 400	31.5	70	25	40	3.3

Table 4-2. Cirrus Logic Extended VGA CRT-Only Display Modes *(cont.)*

Extended VGA Display Mode No. (hex)	VESA Display Mode No. (hex)	Number of Colors	Char. × Rows	Char. Cell (pixels)	Display Screen Format, Column × Row (pixels)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)	VCLK (MHz)	Mini-mum MCLK (MHz)	Required CVDD Voltage (Volts)
5F	101	256/256K	80 × 30	8 × 16	640 × 480	31.5	60	25	40	3.3
						37.9	72	31.5	40	3.3
						37.5	75	31.5	40	3.3
60	105	256/256K	128 × 48	8 × 16	1024 × 768	35.5	43.5 87†	44.9	45	3.3
						48.3	60	65	45	3.3
						56	70	75	50	3.3
						58	72	77	50	5.0
						60	75	78.75	50	5.0
64	111	64K	–	–	640 × 480	31.5	60	25	45	3.3
						37.9	72	31.5	45	3.3
						37.5	75	31.5	45	3.3
65	114	64K	–	–	800 × 600	35.2	56	36	45	3.3
						37.8	60	40	50	3.3
						48.1	72	50	60	5.0
						46.875	75	50	60	5.0
66	110	32K‡	–	–	640 × 480	31.5	60	25	45	3.3
						37.9	72	31.5	45	3.3
						37.5	75	31.5	45	3.3
67	113	32K‡	–	–	800 × 600	37.8	60	40	50	3.3
6C	106	16/256K	160 × 64	8 × 16	1280 × 1024	48	43.5 87†	75	45	3.3
6D	–	256/256K	160 × 64	8 × 16	1280 × 1024	48	43.5 87†	75	45	3.3
71	112	16M	80 × 30	8 × 16	640 × 480	31.5	60	25	50	3.3
74	–	64K	–	–	1024 × 768	35.5	43.5 87†	44.9	45	3.3

NOTE: † indicates interlaced mode.
‡ indicates 32K direct-color/256-color mixed mode.

4.2 LCD-Only/SimulSCAN™ Mode Tables

This section lists tables for the LCD-only/SimulSCAN modes that the Cirrus Logic VGA BIOS supports.

4.2.1 Cirrus Logic LCD-Only/SimulSCAN™ Modes for 800 x 600 LCDs

For 800 x 600 LCDs, the Cirrus Logic VGA BIOS supports the LCD-only/SimulSCAN modes in Table 4-3. (Unless otherwise noted, all screen formats expand to 800 x 600 pixels to fill the entire LCD screen.)

- If the BIOS used is not the Cirrus Logic VGA BIOS, modes may differ.
- Some modes are not supported by all CRT monitors.
- The values listed in these tables are preliminary and are subject to change.

Table 4-3. Cirrus Logic Extended Panel-Only Display Modes for 800 × 600 LCDs

Extended VGA Display Mode Number (hex)	VESA Display Mode Number (hex)	Number of Colors	Char. × Rows	Char. Cell (pixels)	Display Screen Format, Column × Row (pixels)	Expansion of 640 × 480 to 800 × 600?	Graphics Panel Type	Dot Clock (MHz)	Mini-mum MCLK (MHz)	Require CVDD Voltage (Volts)
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	–	DSTN	37.8	53.5	3.3
							TFT	38.66	45	3.3
5C	103	256/256K	100 × 37	8 × 16	800 × 600	–	DSTN	37.8	53.5	3.3
							TFT	38.66	45	3.3
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Yes	DSTN	37.8	53.5	3.3
							TFT	38.66	45	3.3
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Yes	DSTN	37.8	53.5	3.3
							TFT	38.66	45	3.3
64	111	64K	–	–	640 × 480	No	TFT	38.66	50	3.3
65	114	64K	–	–	800 × 600	–	TFT	38.66	50	3.3
66	110	32K	–	–	640 × 480	No	TFT	38.66	50	3.3
67	113	32K	–	–	800 × 600	–	TFT	38.66	50	3.3

4.2.2 Cirrus Logic LCD-Only/SimulSCAN™ Modes for 640 x 480 LCDs

For 640 x 480 LCDs, the Cirrus Logic VGA BIOS supports the LCD-only/SimulSCAN modes in Table 4-4. (Unless otherwise noted, all screen formats expand to 640 x 480 pixels to fill the entire LCD screen.)

- If the BIOS used is not the Cirrus Logic VGA BIOS, modes may differ.
- Some modes are not supported by all CRT monitors.
- The values listed in these tables are preliminary and are subject to change.

Table 4-4. Cirrus Logic Extended Panel-Only Display Modes for 640 × 480 LCDs

Extended VGA Display Mode Number (hex)	VESA Display Mode Number (hex)	Number of Colors	Char. × Rows	Char. Cell (pixels)	Display Screen Format, Column × Row (pixels)	Graphics Panel Type	Dot Clock (MHz)	Mini-mum MCLK (MHz)	Required CVDD Voltage (Volts)
5E	100	256/256K	80 × 25	8 × 16	640 × 400	DSTN/TFT	25	45	3.3
5F	101	256/256K	80 × 30	8 × 16	640 × 480	DSTN/TFT	25	45	3.3
64	111	64K	–	–	640 × 480	DSTN/TFT	25	45	3.3
66	110	32K‡	–	–	640 × 480	DSTN/TFT	25	45	3.3
71	112	16M	80 × 30	8 × 16	640 × 480	TFT	25	50	3.3

5. VGA REGISTER PORT MAP

Table 5-1. VGA Register Port Map

Address	Port	Port Type
3B4	CRT Controller Index — Monochrome	Read/Write
3B5	CRT Controller Data — Monochrome	Read/Write
3BA	Feature Control — Monochrome	Write
	Input Status Register 1 — Monochrome	Read
3C0	Attribute Controller Index / Data	Write
3C1	Attribute Controller Index / Data	Read
3C2	Miscellaneous Output	Write
	Input Status Register 0	Read
3C3	Motherboard Sleep	Read/Write
3C4	Sequencer Index	Read/Write
3C5	Sequencer Data	Read/Write
3C6	Video DAC Pixel Mask (R/W), Hidden DAC Register	Read/Write
3C7	Pixel Address Read mode	Write
	DAC State	Read
3C8	Pixel Mask Write Mode	Read/Write
3C9	Pixel Data	Read/Write
3CA	Feature Control Readback	Read
3CC	Miscellaneous Output Readback	Read
3CE	Graphics Controller Index	Read/Write
3CF	Graphics Controller Data	Read/Write
3D4	CRT Controller Index — Color	Read/Write
3D5	CRT Controller Data — Color	Read/Write
3DA	Feature Control — Color	Write
	Input Status Register 1 — Color	Read
46E8	Adapter Sleep	Read/Write

6. REGISTER SUMMARY

The registers summarized in this chapter include standard VGA registers, as well as Extension registers that Cirrus Logic has added.

6.1 Summary of External/General Registers in Chapter 7

The External and General registers in the CL-GD7548 are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
MISC	Miscellaneous Output	–	3C2 (Write)	147
MISC	Miscellaneous Output	–	3CC (Read)	147
FC	Feature Control	–	3?A (Write)	150
FC	Feature Control	–	3CA (Read)	150
FEAT	Input Status Register 0	–	3C2	151
STAT	Input Status Register 1	–	3?A	152
3C3	Sleep Mode	–	3C3	153
3C6	Pixel Mask	–	3C6	154
3C7	Pixel Address Read Mode	–	3C7 (Write)	155
3C7	DAC State	–	3C7 (Read)	156
3C8	Pixel Address Write Mode	–	3C8	157
3C9	Pixel Data	–	3C9	158
PCI00	PCI Device ID / PCI Vendor ID	–	00	159
PCI04	PCI Command	–	04	160
PCI04	PCI Status	–	04	161
PCI10	PCI Base Address	–	10	162
PCI3C	PCI Interrupt Pin and PCI Interrupt Line	–	3C	163
46E8	Alternate Sleep Mode	–	46E8	164

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.2 Summary of Sequencer Registers in Chapter 8

The CL-GD7548 Sequencer registers are summarized in the following table. Note that there are Extension registers that are accessed using the Sequencer ports.

Abbreviation	Register Name	Index	Port	Page
SRX	Sequencer Index	–	3C4	165
SR0	Reset	0	3C5	167
SR1	Clocking Mode	1	3C5	168
SR2	Plane Mask	2	3C5	170
SR3	Character Map Set Select	3	3C5	171
SR4	Memory Mode	4	3C5	173

6.3 Summary of CRT Controller Registers in Chapter 9

The CL-GD7548 CRT Controller registers are summarized in the following table. Note that there are Extension registers that are accessed using the CRT Controller ports.

Abbreviation	Register Name	Index	Port	Page
CRX	CRT Controller Index	–	3?4	175
CR0	Horizontal Total	0	3?5	176
CR1	Horizontal Display End	1	3?5	179
CR2	Horizontal Blanking Start	2	3?5	180
CR3	Horizontal Blanking End	3	3?5	181
CR4	Horizontal Sync Start	4	3?5	183
CR5	Horizontal Sync End	5	3?5	184
CR6	Vertical Total	6	3?5	186
CR7	Overflow	7	3?5	187
CR8	Screen A Preset Row Scan	8	3?5	188
CR9	Character Cell Height	9	3?5	189
CRA	Text Cursor Start	A	3?5	190
CRB	Text Cursor End	B	3?5	191
CRC	Screen A Start Address High	C	3?5	192
CRD	Screen A Start Address Low	D	3?5	193
CRE	Text Cursor Location High	E	3?5	194
CRF	Text Cursor Location Low	F	3?5	195
CR10	Vertical Sync Start	10	3?5	196
CR11	Vertical Sync End	11	3?5	197
CR12	Vertical Display End	12	3?5	199
CR13	Offset	13	3?5	200
CR14	Underline Row Scanline	14	3?5	201
CR15	Vertical Blanking Start	15	3?5	202
CR16	Vertical Blanking End	16	3?5	203
CR17	Mode Control	17	3?5	204
CR18	Line Compare	18	3?5	206
CR22	Graphics Controller Data Latches Readback	22	3?5	207
CR24	Attribute Controller Toggle Readback	24	3?5	208
CR26	Attribute Controller Index Readback	26	3?5	209

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

6.4 Summary of Graphics Controller Registers in Chapter 10

The CL-GD7548 Graphics Controller registers are summarized in the following table. Note that there are Extension registers that are accessed using the Graphics Controller port.

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index	–	3CE	211
GR0	Set / Reset	0	3CF	212
GR1	Set / Reset Enable	1	3CF	213
GR2	Color Compare	2	3CF	214
GR3	Data Rotate	3	3CF	215
GR4	Read Map Plane Select	4	3CF	215
GR5	Mode	5	3CF	217
GR6	Miscellaneous	6	3CF	221
GR7	Color Don't Care Plane	7	3CF	222
GR8	Display Memory Bit Mask	8	3CF	223

6.5 Summary of Attribute Controller Registers in Chapter 11

The CL-GD7548 Attribute Controller registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index	–	3C0/3C1	225
AR0–ARF	Attribute Controller Palette	0–F	3C0/3C1	226
AR10	Attribute Controller Mode	10	3C0/3C1	227
AR11	Overscan (Border) Color	11	3C0/3C1	229
AR12	Color Plane Enable	12	3C0/3C1	230
AR13	Pixel Panning	13	3C0/3C1	232
AR14	Color Select	14	3C0/3C1	233

6.6 Summary of Extension Registers in Chapter 12

The CL-GD7548 Extension registers are summarized in the following table:

Abbreviation	Register Name	Index	Port	Page
SR6	Unlock All Extension Registers	6	3C5	235
SR7	Extended Sequencer Mode	7	3C5	236
SR8	Miscellaneous Control Register 1	8	3C5	239
SR9	Scratchpad 0	9	3C5	241
SRA	Scratchpad 1	A	3C5	242
SRB	VCLK0 Numerator	B	3C5	242
SRC	VCLK1 Numerator	C	3C5	242
SRD	VCLK2 Numerator	D	3C5	242
SRE	VCLK3 Numerator	E	3C5	242
SRF	Display Memory Control	F	3C5	244
SR10	HW Cursor and HW Icon Coarse Horizontal Position	10	3C5	247
SR11	HW Cursor and HW Icon Coarse Vertical Position	11	3C5	250
SR12	Video Data Path Control	12	3C5	251
SR13	Hardware Cursor Pattern Address Offset	13	3C5	254
SR14	Scratchpad 2	14	3C5	255
SR15	Scratchpad 3	15	3C5	255
SR16	Performance Tuning	16	3C5	256
SR17	BitBLT Memory Map I/O Address Control	17	3C5	259
SR18	Signature Generator Control	18	3C5	260
SR19	Signature Generator Result Low	19	3C5	262
SR1A	Signature Generator Result High	1A	3C5	263
SR1B	VCLK0 Denominator and Post-scalar Value	1B	3C5	264
SR1C	VCLK1 Denominator and Post-scalar Value	1C	3C5	264
SR1D	VCLK2 Denominator and Post-scalar Value	1D	3C5	264
SR1E	VCLK3 Denominator and Post-scalar Value	1E	3C5	264
SR1F	MCLK Frequency and VCLK Source Select	1F	3C5	266
SR20	Miscellaneous Control Register 2	20	3C5	267
SR21	Dual-Scan Color Control	21	3C5	270
SR22	Hardware Configuration Read Register 1	22	3C5	271
SR23	Software Configuration Register 1	23	3C5	273
SR24	LCD-Type Switches and Feature Connector Enable	24	3C5	275
SR25	Timer-Software Reset and Hardware Configuration 2	25	3C5	277
SR26	Shader Signature Low	26	3C5	279
SR27	Shader Signature High	27	3C5	280
SR28	Scratchpad 5	28	3C5	281
SR29	Scratchpad 6	29	3C5	281
SR2A	Hardware Icon #0 Control	2A	3C5	282
SR2B	Hardware Icon #1 Control	2B	3C5	283
SR2C	Hardware Icon #2 Control and Miscellaneous PCI	2C	3C5	285
SR2D	Hardware Icon #3 Control and HIMEM Select	2D	3C5	286
SR2E	Hardware Cursor Horizontal Position Extension	2E	3C5	288
SR2F	Half-Frame Accelerator FIFO Threshold	2F	3C5	290
SR2G–SR31	Reserved	–	–	–
SR32	HFA FIFO Threshold in MWV / PCI Bus Speed	32	3C5	292
SR33	CRT FIFO Request Threshold Extend	33	3C5	294
SR34	CPU Stop Control	34	3C5	296

Summary of Extension Registers in Chapter 12 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
Graphics Controller Extension Registers				
GR9	Offset Register 0	9	3CF	298
GRA	Offset Register 1	A	3CF	300
GRB	Graphics Controller Mode Extensions	B	3CF	301
GRC	Color Key Compare	C	3CF	303
GRD	Color Key Compare Mask	D	3CF	304
GRE	PCI Bus Burst-Write and Green PC Control	E	3CF	305
GRF	Reserved	–	–	–
GR10	16-Bit Pixel Background Color High	10	3CF	307
GR11	16-Bit Pixel Foreground Color High	11	3CF	308
GR12–GR1F	Reserved	–	–	–
GR20	BitBLT Width Low	20	3CF	309
GR21	BitBLT Width High	21	3CF	310
GR22	BitBLT Height Low	22	3CF	311
GR23	BitBLT Height High	23	3CF	312
GR24	BitBLT Destination Pitch Low	24	3CF	313
GR25	BitBLT Destination Pitch High	25	3CF	314
GR26	BitBLT Source Pitch Low	26	3CF	315
GR27	BitBLT Source Pitch High	27	3CF	316
GR28	BitBLT Destination Start Low	28	3CF	317
GR29	BitBLT Destination Start Middle	29	3CF	318
GR2A	BitBLT Destination Start High	2A	3CF	319
GR2B	Reserved	–	–	–
GR2C	BitBLT Source Start Low	2C	3CF	320
GR2D	BitBLT Source Start Middle	2D	3CF	321
GR2E	BitBLT Source Start High	2E	3CF	322
GR2F	Reserved	–	–	–
GR30	BitBLT Mode	30	3CF	323
GR31	BitBLT Start/Status	31	3CF	326
GR32	BitBLT Raster Operation Function	32	3CF	328
GR33	Reserved	–	–	–
GR34	BitBLT Transparent Color Select Low	34	3CF	330
GR35	BitBLT Transparent Color Select High	35	3CF	331
GR36–GR37	Reserved	–	–	–
GR38	BitBLT Transparent Color Mask Low	38	3CF	332
GR39	BitBLT Transparent Color Mask High	39	3CF	333

Summary of Extension Registers in Chapter 12 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
CRT Controller Extension Registers				
CR19	Interlace End	19	3?5	334
CR1A	Miscellaneous Control	1A	3?5	335
CR1B	Extended Display Controls	1B	3?5	337
CR1C	Reserved	–	–	–
CR1D	Video Overlay Mode	1D	3?5	340
CR1E	LCD Shading	1E	3?5	341
CR1F	LCD Modulation Control	1F	3?5	343
CR20	Power Management	20	3?5	345
CR21	Power-Down Timer Control	21	3?5	348
CR22	Reserved	–	–	–
CR23	SUSPI Pin Input Switch Debounce Timer	23	3?5	350
CR24	Reserved	–	–	–
CR25	Manufacturing Revision Identification	25	3?5	352
CR26	Reserved	–	–	–
CR27	Device ID and Manufacturing Revision Identification	27	3?5	353
CR28	Reserved	–	–	–
CR29	Status	29	3?5	354
CR2A–CR2B	Reserved	–	–	–
CR2C	LCD Interface	2C	3?5	355
CR2D	LCD Display Controls	2D	3?5	359
CR2E	LCD High-Resolution Control	2E	3?5	361
CR2F	Driver and BIOS Revision	2F	3?5	362
CR30	TV-OUT Control	30	3?5	363
Video Window Control Registers				
CR31	VW Horizontal Upscaling Coefficient Low	31	3?5	365
CR32	VW Vertical Upscaling Coefficient Low	32	3?5	366
CR33	VW Horizontal Start (XS) / Width (XW) Extension	33	3?5	367
CR34	VW Horizontal Start (XS)	34	3?5	369
CR35	VW Horizontal Width (XW)	35	3?5	370
CR36	YUV-to-RGB Conversion / VW Vertical-Position High	36	3?5	371
CR37	VW Vertical Position Start (YS)	37	3?5	373
CR38	VW Vertical Height (YH)	38	3?5	374
CR39	VW Surrounding Address Offset	39	3?5	375
CR3A	VW Memory Start Address High	3A	3?5	376
CR3B	VW Memory Address Offset	3B	3?5	377
CR3C	VW Horizontal Pixel Width, Enable, and Encoding	3C	3?5	378
CR3D	VW Horizontal Pixel Width	3D	3?5	379
CR3E	VW Memory Start Address Middle	3E	3?5	381
CR3F	VW Memory Start Address Low	3F	3?5	382

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

Summary of Extension Registers in Chapter 12 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
LCD Timing Control Registers				
CR40	LCD Horizontal-Display-Enable Start – No Centering	40	3?5	383
CR41	LCD HDE Start to Center 720-Dot Image	41	3?5	385
CR42	LCD HDE Start to Center 640-Dot Image	42	3?5	386
CR43	LCD Dot Clock Delay Control	43	3?5	387
CR44	LCD Horizontal Width	44	3?5	389
CR45	Reserved	–	–	–
CR46	Shift Clock Delay Control	46	3?5	390
CR47	TFT HSYNC Horizontal Start	47	3?5	391
CR48	TFT HSYNC and Vertical Size for LCD Extension	48	3?5	392
CR49	Vertical Size for Upper Half of Dual-Scan STN LCDs	49	3?5	393
CR4A	Vertical Size for LCDs	4A	3?5	394
CR4B	Reserved for Scratchpad	4B	3?5	395
CR4C	Graphics Input-Resolution Override for Dithering	4C	3?5	396
CR4D	Output Resolution for Dithering	4D	3?5	399
CR4E	VW / Video Overlay Input-Resolution Override	4E	3?5	400
CR4F	Reserved	–	–	–
CR50	V-PORT™ Control	50	3?5	402
CR51	V-PORT™ Data Format	51	3?5	404
CR52	V-PORT™ Horizontal Downscaling Coefficient	52	3?5	406
CR53	V-PORT™ Vertical Downscaling Coefficient	53	3?5	407
CR54	V-PORT™ Capture Window Horizontal Start	54	3?5	408
CR55	V-PORT™ Capture Window Horizontal Width	55	3?5	409
CR56	V-PORT™ Capture Window Vertical Start	56	3?5	410
CR57	V-PORT™ Capture Window Vertical Height	57	3?5	411
CR58	V-PORT™ Capture Window Extension	58	3?5	412
CR59	V-PORT™ Capture Window Start Address High	59	3?5	412
CR5A	V-PORT™ Cycle and FIFO Control	5A	3?5	413
CR5B	VW YUV Data Format Brightness Control	5B	3?5	414
CR5C	V-PORT™ FIFO / CRT FIFO Cycle Control at VW Period End	5C	3?5	417
CR5D	VW Horizontal/Vertical Upscaling Coefficients High	5D	3?5	419
CR5E	V-PORT™ Capture Window Start Address Middle	5E	3?5	420
CR5F	V-PORT™ Capture Window Start Address Low	5F	3?5	421
HDR	Hidden DAC Register	–	3C6	422
R1X	XGA TFT LCD HSYNC Width Control	2	3?5	424
R2X	LCD Timing — LFS Vertical Position #1	2	3?5	426
R3X	LCD Timing — LFS Vertical Position #2	3	3?5	429
R4X	LCD Timing — LFS Vertical Position #3	4	3?5	430
R5X	LCD Timing — LFS Vertical Position #4	5	3?5	431
R6X	LCD Timing — Extension Bits for LFS Signal Compare	6	3?5	432
R7X	LCD Timing — Signal Control for Color TFT LCDs	7	3?5	433
R8X	LCD Timing — Shift Clock and Data Select	8	3?5	435
R9X	TFT LCD Data Format	9	3?5	437
RAX	Reserved	–	–	–
RBX	Shade Conversion and Extra LCD Line Clock Insertion	B	3?5	438
RCX	LCD Timing — LFS Vertical Position for 525-Line Modes	C	3?5	440
RDX	LCD Timing — LFS Vertical Position #6	D	3?5	441
REX	RDX and RCX Extension	E	3?5	442

Summary of Extension Registers in Chapter 12 *(cont.)*

Abbreviation	Register Name	Index	Port	Page
LCD Horizontal Timing Control Shadow Registers				
R0Y	Horizontal Total Shadow	0	3?5	443
R1Y	Reserved	–	–	–
R2Y	Horizontal Blanking Start Shadow	2	3?5	444
R3Y	Horizontal Blanking End Shadow	3	3?5	445
R4Y	Horizontal Sync Start Shadow	4	3?5	446
R5Y	Horizontal Sync End Shadow	5	3?5	447
R0Z	Horizontal Total Shadow	0	3?5	448
R1Z	Reserved	–	–	–
R2Z	Horizontal Blanking Start Shadow	2	3?5	449
R3Z	Horizontal Blanking End Shadow	3	3?5	450
R4Z	Horizontal Sync Start Shadow	4	3?5	451
R5Z	Horizontal Sync End Shadow	5	3?5	452

NOTES:

1) '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.
2) The RnX registers are indexed through the settings of CR2D.
3) The R0Y–R5Y and R0Z–R5Z registers are indexed through the settings of CR2C.

7. EXTERNAL/GENERAL REGISTERS

NOTE: The '?' in the I/O port address of the registers in the next sections implies 'B' in Monochrome mode and 'D' in Color mode.

7.1 MISC: Miscellaneous Output Register

I/O Port Address: 3C2 (Write) 3CC (Read)

Index: –

Bit	Description	Reset State
7	Vertical Sync Polarity	0
6	Horizontal Sync Polarity	0
5	Page Select	0
4	Reserved	
3	Clock Select [1]	0
2	Clock Select [0]	0
1	Display Memory Enable	0
0	CRTC I/O Address	0

This standard VGA register has an assortment of bits that have nothing in common.

Bit **Description**

7 **Vertical Sync Polarity:**
When this bit is programmed to:
- 0, Vertical Sync is normally low. A high indicates beginning sync time.
- 1, Vertical Sync is normally high. A low indicates beginning sync time.

6 **Horizontal Sync Polarity:**
- When this bit is programmed to:
  — 0, Horizontal Sync is normally low. A high indicates beginning sync time.
  — 1, Horizontal Sync is normally high. A low indicates beginning sync time.
- For some monitors, the combined polarity of Vertical and Horizontal Sync is used to indicate the number of scanlines per frame, as shown in the table.
- When Extension register CR20[5] = 1 *and* MISC[7:6] = 00, the value of MISC[7:6] is redefined from reserved to an 800 × 600 LCD.

MISC		Vertical Size	Vertical Overscan	Vertical Total =
[7] Vertical Sync Polarity	[6] Horizontal Sync Polarity	(Scanlines appearing on screen)	(Scanlines appearing off screen)	(Vertical Size + Vertical Overscan)
0 (+)	0 (+)	Reserved	Reserved	Reserved
0 (+)	1 (–)	400	14	414
1 (–)	0 (+)	350	12	362
1 (–)	1 (–)	480	16	496

7.1 MISC: Miscellaneous Output Register *(cont.)*

Bit 5 — Page Select:
When Sequencer register SR4[2] is 1, MISC[5] affects how display memory addresses are selected.
- When SR4[2] = 1, and this bit = 0, only odd memory locations are selected.
- When SR4[2] = 1, and this bit = 1, only even memory locations are selected.
- This bit takes effect for Graphics modes 6h, Dh, Eh, 11h, and 12h.
- This bit is ignored if either of the following are true:
  - — Graphics Controller register GR6[1] = 1.
  - — Sequencer register SR4[3] = 1.

Bit 4 — Reserved

Bit 3:2 — Clock Select [1:0]:
This field is used with Extension register bits to choose a video clock source for the CL-GD7548, as shown in the following table.

SR22 [3]	SR23 [7]	MISC [3]	MISC [2]	SR1F [6]	SR1E [0]	Video Clock Source for CL-GD7548
0	0	0	0	0	X	SR0B (N) / SR1B (D) [a]
0[b]	X	X	X	0	X	OSC if TV-out enabled
X	X	X	X	1	0	MCLK
X	X	X	X	1	1	MCLK ÷ 2 [c]
0	0	0	1	0	X	SR0C (N) / SR1C (D) [a]
0	0	1	0	0	X	SR0D (N) / SR1D (D) [a]
0	0	1	1	0	X	SR0E (N) / SR1E (D) [a]
0	1	0	X	0	X	FCVCLK to only DAC
0	1	1	X	0	X	FCVCLK to both DAC and CRTC
1	1	0	X	0	X	OSC (pin)

[a] These are Numerator/Denominator registers. For information on programming alternative frequencies, refer to Appendix G.

[b] True only if Extension register CR30[3] = 1 and Extension register SR25[4] = 1.

[c] True only if Extension register SR12[4] = 1.

Bit 1 — Display Memory Enable:
When this bit is programmed to:
- 0, the CL-GD7548 does not respond to display memory accesses.
- 1, the CL-GD7548 responds normally to display memory accesses.

7.1 MISC: Miscellaneous Output Register *(cont.)*

Bit	Description
0	**CRTC I/O Address:** This bit selects either monochrome or color I/O addresses.

MISC[0]	Mode	Input Status / Feature Control	CRTC Index	CRTC Data
0	Monochrome	3BA	3B4	3B5
1	Color	3DA	3D4	3D5

7.2 FC: Feature Control Register

I/O Port Address: 3?A (Write) 3CA (Read)

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	CRT VSYNC Control	0
2	Reserved	
1	Reserved	
0	Reserved	

This register is one of the original IBM PC registers. Nearly all the bits are no longer used.

Bit	Description
7:4	**Reserved**
3	**CRT VSYNC Control:** This bit is normally used for CRTs that have a internal vertical display enable signal pin. Program this bit to: • 0 to keep the CRT VSYNC signal unchanged and maintain IBM compatibility. • 1 to logically OR the CRT VSYNC signal with the CL-GD7548 internal vertical display enable signal prior to sending it to the VSYNC pin.
2:0	**Reserved**

7.3 FEAT: Input Status Register 0

I/O Port Address: 3C2

Index: –

Bit	Description	Reset State
7	Vertical Interrupt Request Pending	0
6	Reserved	
5	Reserved	
4	DAC Switch Sensing	1
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

The bits in this read-only register are nearly all undefined.

Bit	Description
7	**Vertical Interrupt Request Pending:** When this bit is: • 0, there is no vertical interrupt request pending. • 1, there is a vertical interrupt request pending. For more information on the CL-GD7548 vertical interrupt system, refer to CRT Controller register CR11.
6:5	**Reserved**
4	**DAC Switch Sensing:** This read-only bit is used to report the on-off status of one of four analog comparator RAMDAC sense switches, as selected by MISC[3:2]. This bit is: • 0 when the selected DAC sense switch is off. • 1 when the selected DAC sense switch is on.
3:0	**Reserved**

7.4 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Diagnostic [1]	1
4	Diagnostic [0]	1
3	Vertical Retrace	0
2	Reserved	
1	Reserved	
0	Video Display Enable	1

This read-only register contains some status bits.

Bit — **Description**

7:6 — **Reserved**

5:4 — **Diagnostic [1:0]:**

- As a standard VGA feature, these bits reflect the status of 2 bits selected from the 8 output bits of Attribute Controller register bits AR12[5:4]. (The table indicates how the 2 bits are selected.)

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	Pixel Bus bit [2] Red	Pixel Bus bit [0] Blue
0	1	Pixel Bus bit [3] Secondary Blue	Pixel Bus bit [1] Green
1	0	Pixel Bus bit [5] Secondary Red	Pixel Bus bit [4] Secondary Green
1	1	Pixel Bus bit [7]	Pixel Bus bit [6]

- As a feature of the CL-GD7548, for debugging, the STAT[5:4] bits can reflect data on the Feature Connector FCP[7:0] if both of the following are true:
  - — The Feature Connector is enabled.
  - — The Feature Connector is configured to input data into the CL-GD7548.

3 — **Vertical Retrace**:
A 1 on this bit indicates that vertical retrace is in progress.

2:1 — **Reserved**

0 — **Video Display Enable:**

- When this bit is 0, video data bits are being serialized and displayed.
- When this bit is 1, vertical or horizontal blanking is active.

7.5 3C3: Sleep Mode Register

I/O Port Address: 3C3

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Sleep Mode Readback	1
0	Sleep Mode Write / Readback	1

The CL-GD7548 may be put into the Sleep mode in one of several ways.

1) Sleep Mode Method 1:
This 3C3 Sleep Mode register is normally recommended for motherboard applications.

2) Sleep Mode Method 2:
When the S46 / MD[21] pin has an external pull-up resistor attached, the alternate Sleep Mode register, 46E8, is selected. (The 3C3 Sleep Mode register is then inactive.)

3) Sleep Mode Method 3:
The Sleep mode may also be activated when the input to the SLEEP# pin is low.

Bit	Description
7:2	**Reserved**
1	**Sleep Mode Readback**: This bit is read-only. When 3C3[0] is: • 0, this bit is also 0 • 1, this bit is also 1.
0	**Sleep Mode Write / Readback:** This read/write bit is normally 1. When this bit is: • 0, the CL-GD7548 turns off the interface to the display memory, the interface to the CPU I/O, and the displays. Also, no other chip accesses except those to 3C3 are allowed until this bit is set to 1. • 1, the CL-GD7548 is active and can respond to normal bus and display activity.

7.6 3C6: Pixel Mask Register

I/O Port Address: 3C6

Index: –

Bit	Description	Reset State
7	Pixel Mask [7]	1
6	Pixel Mask [6]	1
5	Pixel Mask [5]	1
4	Pixel Mask [4]	1
3	Pixel Mask [3]	1
2	Pixel Mask [2]	1
1	Pixel Mask [1]	1
0	Pixel Mask [0]	1

The bits in this read-only register form the pixel mask for the palette DAC. Typically, the Cirrus Logic BIOS programs all these bits to 1. This same 3C6 address is used to access the Hidden DAC register, described in the Extension registers in Chapter 12.

Bit	Description
7:0	**Pixel Mask [7:0]:** This field is the pixel mask for the palette DAC. When a bit in this field is programmed to 0, the corresponding bit in the pixel data is ignored in looking up an entry in the CLUT.

7.7 3C7: Pixel Address Read Mode Register (Write Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Reset State
7	Pixel Address Read Mode [7]	0
6	Pixel Address Read Mode [6]	0
5	Pixel Address Read Mode [5]	0
4	Pixel Address Read Mode [4]	0
3	Pixel Address Read Mode [3]	0
2	Pixel Address Read Mode [2]	0
1	Pixel Address Read Mode [1]	0
0	Pixel Address Read Mode [0]	0

The bits in this write-only register form the Pixel Address Read mode for the palette DAC. This pixel address is then used to specify the CLUT entry that is to be read.

Bit	Description
7:0	**Pixel Address Read Mode [7:0]:** This field is the Pixel Address Read mode for an entry in the CLUT. At the conclusion of every third read of the Pixel Data register (3C9), this address is incremented by one.

7.8 3C7: DAC State Register (Read Only)

I/O Port Address: 3C7

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	DAC State [1]	0
0	DAC State [0]	0

The bits in this read-only register indicate whether a read or a write to the CLUT occurred last.

Bit	Description
7:2	**Reserved**
1:0	**DAC State [1:0]:** This 2-bit field indicates which pixel address register was accessed last. • Both bits in this field are always the same digit. • When the bits are: — '00', a write operation is in progress, meaning that the last accessed register for the CLUT was the Pixel Address Write register. — '11', a read operation is in progress, meaning that the last accessed register for the CLUT was the Pixel Address Read register.

7.9 3C8: Pixel Address Write Mode Register

I/O Port Address: 3C8

Index: –

Bit	Description	Reset State
7	Pixel Address Write Mode [7]	0
6	Pixel Address Write Mode [6]	0
5	Pixel Address Write Mode [5]	0
4	Pixel Address Write Mode [4]	0
3	Pixel Address Write Mode [3]	0
2	Pixel Address Write Mode [2]	0
1	Pixel Address Write Mode [1]	0
0	Pixel Address Write Mode [0]	0

The bits in this registers form the Pixel Address Write mode for the palette DAC. This pixel address is then used to specify the CLUT entry that is to be written.

Bit	Description
7:0	**Pixel Address Write Mode [7:0]:** This field is the Pixel Address Write mode for an entry in the CLUT. At the conclusion of every third write to the Pixel Data register (3C9), this address is incremented by one.

7.10 3C9: Pixel Data Register

I/O Port Address: 3C9

Index: –

Bit	Description	Reset State
7	Pixel Data [7]	0
6	Pixel Data [6]	0
5	Pixel Data [5]	0
4	Pixel Data [4]	0
3	Pixel Data [3]	0
2	Pixel Data [2]	0
1	Pixel Data [1]	0
0	Pixel Data [0]	0

This register contains the pixel data for the palette DAC.

Bit	Description
7:0	**Pixel Data [7:0]**: These read/write register bits store the pixel data for the palette DAC. Writing to this register occurs as follows: 1. Prior to writing to this register, register 3C8 (the Pixel Address Write Mode register) is written with the first or only pixel address. 2. Three values, corresponding to the red, green, and blue values for the pixel, are then written to this address. 3. Following the third write, values are transferred to the CLUT. 4. The Pixel Address is incremented, in case new values for the next pixel address are to be written. Reading from this register occurs as follows: 1. Prior to reading from this register, register 3C7 (the Pixel Address Read Mode register) is written with the first or only pixel address. 2. Three values, corresponding to the red, green, and blue values for the pixel, are then read from this address. 3. Following the third read, the Pixel Address is incremented, in case new values for the next pixel address are to be read.

7.11 PCI00: PCI Device ID / PCI Vendor ID Register

PCI Configuration Address: 00

Index: –

Bit	Description	Reset State
31	PCI Device ID [15]	0
30	PCI Device ID [14]	0
29	PCI Device ID [13]	0
28	PCI Device ID [12]	0
27	PCI Device ID [11]	0
26	PCI Device ID [10]	0
25	PCI Device ID [9]	0
24	PCI Device ID [8]	0
23	PCI Device ID [7]	Value in Extension register CR27[7]
22	PCI Device ID [6]	Value in Extension register CR27[6]
21	PCI Device ID [5]	Value in Extension register CR27[5]
20	PCI Device ID [4]	Value in Extension register CR27[4]
19	PCI Device ID [3]	Value in Extension register CR27[3]
18	PCI Device ID [2]	Value in Extension register CR27[2]
17	PCI Device ID [1]	0
16	PCI Device ID [0]	0
15	PCI Vendor ID [15]	0
14	PCI Vendor ID [14]	0
13	PCI Vendor ID [13]	0
12	PCI Vendor ID [12]	1
11	PCI Vendor ID [11]	0
10	PCI Vendor ID [10]	0
9	PCI Vendor ID [9]	0
8	PCI Vendor ID [8]	0
7	PCI Vendor ID [7]	0
6	PCI Vendor ID [6]	0
5	PCI Vendor ID [5]	0
4	PCI Vendor ID [4]	1
3	PCI Vendor ID [3]	0
2	PCI Vendor ID [2]	0
1	PCI Vendor ID [1]	1
0	PCI Vendor ID [0]	1

This register is accessible and effective only if the CL-GD7548 is configured for PCI bus. It contains the PCI Device ID and the PCI Vendor ID required for PCI compliance.

Bit	Description
31:16	**PCI Device ID [15:0]:** When the CL-GD7548 is configured for PCI bus, this read-only field returns the PCI device ID assigned by Cirrus Logic.
15:0	**PCI Vendor ID [15:0]:** When the CL-GD7548 is configured for PCI bus, this read-only field returns 1013h, the PCI vendor ID assigned to Cirrus Logic by the PCI Special Interest Group.

7.12 PCI04: PCI Command Register

PCI Configuration Address: 04

Index: –

Bit	Description	Reset State
15	Reserved	
14	Reserved	
13	Reserved	
12	Reserved	
11	Reserved	
10	Reserved	
9	Reserved	
8	Reserved	
7	Reserved	
6	Reserved	
5	PCI Bus DAC Shadowing Enable	0
4	Reserved	
3	Reserved	
2	Reserved	
1	Display Memory Access Enable	0
0	I/O Access Enable	0

This 16-bit register is accessible and effective only if the CL-GD7548 is configured for PCI bus. It consists of the least-significant 2 bytes of the 4-byte PCI Status / PCI Command register.

Bit	Description
15:6	**Reserved:** These bits are reserved and *must* be programmed to 0.
5	**PCI Bus DAC Shadowing Enable:** This bit is not supported.
4:2	**Reserved:** These bits are reserved and *must* be programmed to 0.
1	**Display Memory Access Enable:** When the CL-GD7548 is configured for PCI bus and this bit is: • 0, display memory accesses are not enabled to the CL-GD7548 • 1, display memory accesses are enabled to the CL-GD7548.
0	**I/O Access Enable:** • When the CL-GD7548 is configured for PCI bus and this bit is: — 0, I/O accesses are not enabled to the CL-GD7548. — 1, I/O accesses are enabled to the CL-GD7548. • Regardless of the state of this bit, I/O accesses to PCI configuration registers (PC100, PC104, PC110, and PC13C) are always enabled.

7.13 PCI04: PCI Status Register

PCI Configuration Address: 04

Index: –

Bit	Description	Reset State
31	Reserved	
30	Reserved	
29	Reserved	
28	Reserved	
27	Reserved	
26	DEVSEL# Timing [1]	0
25	DEVSEL# Timing [0]	0
24	Reserved	
23	Reserved	
22	Reserved	
21	Reserved	
20	Reserved	
19	Reserved	
18	Reserved	
17	Reserved	
16	Reserved	

This 16-bit register, which is accessible and effective only if the CL-GD7548 is configured for PCI bus, consists of the most-significant 2 bytes of the 4-byte PCI Status / PCI Command register.

Bit	Description
31:27	**Reserved**
26:25	**DEVSEL# Timing [1:0]:** When the CL-GD7548 is configured for PCI bus, this read-only field always returns the value '00' to indicate fast DEVSEL# timing.
24:16	**Reserved**

7.14 PCI10: PCI Bus Base Address Register

PCI Configuration Address: 10

Index: –

Bit	Description	Reset State
31	PCI Bus Base Address for Display Memory [31]	0
30	PCI Bus Base Address for Display Memory [30]	0
29	PCI Bus Base Address for Display Memory [29]	0
28	PCI Bus Base Address for Display Memory [28]	0
27	PCI Bus Base Address for Display Memory [27]	0
26	PCI Bus Base Address for Display Memory [26]	0
25	PCI Bus Base Address for Display Memory [25]	0
24	PCI Bus Base Address for Display Memory [24]	0
23:1	Reserved	
0	Display Memory / I/O Indicator	0

This 32-bit register, which is accessible and effective only when the CL-GD7548 is configured for PCI bus, contains the PCI Base Address for display memory.

Bit	Description
31:24	**PCI Bus Base Address for Display Memory [31:24]:** When the CL-GD7548 is configured for PCI bus, this field contains the base address of the contiguous 16-Mbyte display memory block reserved for the CL-GD7548.
23:1	**Reserved**
0	**Display Memory / I/O Indicator:** • When the CL-GD7548 is configured for PCI bus, this bit is used to indicate the type of address space requested, either display memory or I/O. When this bit is: — 0, a display memory address space is requested. — 1, an I/O address space is requested. • For the PCI bus BIOS, this bit is read/write. • For the VGA VL-Bus BIOS, this bit is read-only.

7.15 PCI3C: PCI Bus Interrupt Pin and PCI Bus Interrupt Line Register

PCI Configuration Address: 3C

Index: –

Bit	Description	Reset State
15	PCI Bus Interrupt Pin [7]	0
14	PCI Bus Interrupt Pin [6]	0
13	PCI Bus Interrupt Pin [5]	0
12	PCI Bus Interrupt Pin [4]	0
11	PCI Bus Interrupt Pin [3]	0
10	PCI Bus Interrupt Pin [2]	0
9	PCI Bus Interrupt Pin [1]	0
8	PCI Bus Interrupt Pin [0]	1
7	PCI Bus Interrupt Line [7]	0
6	PCI Bus Interrupt Line [6]	0
5	PCI Bus Interrupt Line [5]	0
4	PCI Bus Interrupt Line [4]	0
3	PCI Bus Interrupt Line [3]	0
2	PCI Bus Interrupt Line [2]	0
1	PCI Bus Interrupt Line [1]	0
0	PCI Bus Interrupt Line [0]	0

This 16-bit register, which is accessible and effective only when the CL-GD7548 is configured for PCI bus, contains data from the PCI bus interrupt pin and PCI bus interrupt line.

Bit	Description
15:8	**PCI Bus Interrupt Pin [7:0]:** When the CL-GD7548 is configured for PCI bus, this read-only field contains the value '01h'. This value indicates the CL-GD7548 INTR# interrupt request pin is connected to the PCI bus INTA# interrupt request pin.
7:0	**PCI Bus Interrupt Line [7:0]:** When the CL-GD7548 is configured for PCI bus, this read/write field contains an 8-bit value that has no direct effect on the CL-GD7548. This field is used to transfer an interrupt pointer from the PCI system BIOS to the CL-GD7548 VGA BIOS.

7.16 46E8: Alternate Sleep Mode Register

I/O Port Address: 46E8

Index: –

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Alternate Sleep Mode Select	1
2	Reserved	
1	Reserved	
0	Reserved	

This register is active only when the following two conditions are both filled:

1) There is a low-to-high transition of the system reset signal.

2) An external pull-up resistor is on the MD[21] / S46PU pin, which disables the 3C3 Sleep Mode register.

Unless both conditions are filled, register 3C3 is the Sleep Mode register.

Bit	Description
7:4	**Reserved**
3	**Alternate Sleep Mode Select:** When there is a pull-up resistor on the CL-GD7548 pin MD[21] / S46PU (that is, Extension register SR22[5] reads back a 1) *and* when this bit is: • 0, the CL-GD7548: — Is disabled and does not affect the video display activity. — Responds normally to BIOS access. — Does not respond to accesses to I/O, except to those addressed to 46E8. — Does not respond to any accesses to display memory. • 1, the CL-GD7548: — Is enabled. — Can respond to normal bus and video display activity.
2:0	**Reserved**

8. SEQUENCER REGISTERS

8.1 SRX: Sequencer Index Register

I/O Port Address: 3C4

Index: –

Bit	Description	Reset State
7	HW Cursor and HW Icon Fine Position [2]	0
6	HW Cursor and HW Icon Fine Position [1]	0
5	HW Cursor and HW Icon Fine Position [0] Sequencer Index [5]	0
4	Sequencer Index [4]	0
3	Sequencer Index [3]	0
2	Sequencer Index [2]	1
1	Sequencer Index [1]	0
0	Sequencer Index [0]	0

Depending on this register's index value, this register has one of two possible purposes:

1) The primary purpose is to extend the sequencer index from 3 to 6 bits. The index specifies which register in the CL-GD7548 sequencer block is to be accessed by the next I/O read or write to Address 3C5. If an index number is greater than 5, the index points to the Extension registers in Chapter 12.

2) The secondary purpose is to specify the fine position (both horizontal and vertical) of the hardware cursor and the hardware icon.

Bit	Description
7:5	**Hardware Cursor and Hardware Icon Fine Positions:** **Hardware Cursor and Hardware Icon Fine Vertical Positions [2:0]:** When Extension register SR11 is programmed, bits SRX[7:5] define in scanlines the fine vertical position of the hardware cursor and icon. **Hardware Cursor and Hardware Icon Fine Horizontal Positions [2:0]:** When Extension register SR10 is programmed, bits SRX[7:5] define in dot clocks (pixels) the fine horizontal position of the hardware cursor and icon. For special modes requiring extra dot clocks for fine position adjustments, a fourth, most-significant bit is available either in Extension register SR2A or SR2E. • Hardware Cursor bit: Extension register SR2E[0] — For the fine horizontal position of the hardware cursor, SR2E[0] is an added fourth and most-significant bit. — This bit is used in horizontally expanded graphics modes. • Hardware Icon bit: Extension register SR2A[6] — For the fine horizontal position of the hardware icon, SR2A[6] is an added fourth and most-significant bit. — This bit is used in horizontally expanded graphics modes and for 9-dot and 10-dot text modes (such as for expanding 640 × 480 displays to 800 × 600).

8.1 SRX: Sequencer Index Register *(cont.)*

Bit	Description
5:0	**Sequencer Index [5:0]:** • When writing to any CL-GD7548 sequencer index *except* 10h or 11h: — These bits become a 6-bit sequencer index field, SRX[5:0]. — The SRX[5:0] field selects the register to be accessed with the next I/O read or I/O write to I/O Port Address 3C5. • When writing *to* CL-GD7548 sequencer index Extension register SR10 or SR11: — These bits become a 5-bit sequencer index field, SRX[4:0]. — The SRX[4:0] field selects the sequencer index, SRX[7:5], used to define the fine position for the hardware cursor and hardware icon. — Extension registers SR2A[6] and SR2E[0]) also define the fine position for the hardware cursor and hardware icon.

8.2 SR0: Reset Register

I/O Port Address: 3C5

Index: 0

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Synchronous Reset	0
0	Asynchronous Reset	0

This register is used to reset the CL-GD7548 sequencer. These bits are for VGA-standard compatibility only, and after reset they need never be used.

Bit	Description
7:2	**Reserved**
1	**Synchronous Reset:** When this bit is programmed to: • 0, the sequencer is cleared and halted, which disables screen refresh and display memory refresh. • 1 *and* when SR0[0] is 1, the sequencer operates normally.
0	**Asynchronous Reset:** When this bit is programmed to: • 0, the sequencer is cleared and halted, and SR3 is cleared. • 1 *and* when SR0[1] is 1, the sequencer operates normally.

8.3 SR1: Clocking Mode Register

I/O Port Address: 3C5

Index: 1

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Full Display Memory Bandwidth	0
4	Shift and Load 32 Data Bits	0
3	Dot Clock Generation	0
2	Shift and Load 16 Data Bits	0
1	Reserved	
0	8/9 Dot Clock	0

This register is used to control miscellaneous functions in the CL-GD7548 sequencer.

Bit — **Description**

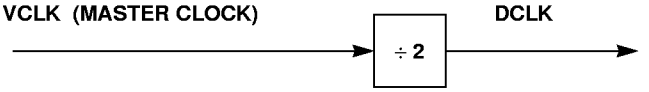
7:6 — **Reserved**

5 — **Full Display Memory Bandwidth:**
When this bit is programmed to:
- 0, the CRT screen is turned on, and the CL-GD7548 operates normally.
- 1, the CRT screen is turned off. In addition:
  - — The CPU uses nearly 100% of the display memory bandwidth.
  - — HSYNC and VSYNC continue normally.
  - — The BLANK# signal goes active and stays active.
  - — The refresh for the display memory continues normally.

4 — **Shift and Load 32 Data Bits:**
This bit, in combination with SR1[2], controls how often 32-bit graphics controller display data shifters are loaded, according to the following table:

SR1		Frequency with Which Graphics Controller Data Shifters Are Loaded
[4]	[2]	
0	0	Every character clock
0	1	Every 2nd character clock
1	X	Every 4th character clock

8.3 SR1: Clocking Mode Register *(cont.)*

Bit	Description
3	**Dot Clock Generation:** When this bit is programmed to: • 0, VCLK (the master clock) is not divided. In this case, the clock that is used as the dot clock is the same frequency as the master clock.  • 1, VCLK (the master clock) is divided by 2 to generate DCLK, a dot clock that is half the frequency of the master clock. This dot clock is used for low-resolution Graphics modes such as 0h, 1h, 4h, 5h, and Dh. 
2	**Shift and Load 16 Data Bits:** This bit controls how often 16-bit graphics controller display data shifters are loaded. When this bit is: • 0, display data shifters are loaded every character clock • 1, display data shifters are loaded every second character clock
1	**Reserved**
0	**8/9 Dot Clock:** For a display that is 80 characters per horizontal scanline, this bit must be: • 0 to generate character clocks that are 9 dots wide, as required by modes that use 720 horizontal dots. • 1 to generate character clocks that are 8 dots wide, as required by modes that use 320 or 640 horizontal dots.

8.4 SR2: Plane Mask Register

I/O Port Address: 3C5

Index: 2

Bit	Description	Reset State
7	Pixel Data Write Enable [7] / Reserved	0
6	Pixel Data Write Enable [6] / Reserved	0
5	Pixel Data Write Enable [5] / Reserved	0
4	Pixel Data Write Enable [4] / Reserved	0
3	Pixel Data Write Enable [3] / Bit Map Plane 3 Enable	0
2	Pixel Data Write Enable [2] / Bit Map Plane 2 Enable	0
1	Pixel Data Write Enable [1] / Bit Map Plane 1 Enable	0
0	Pixel Data Write Enable [0] / Bit Map Plane 0 Enable	0

This register has two uses.

1) Its first use is to control the writing of up to eight pixels.

2) Its second use is to enable or disable writing to the four bit map planes of display memory.

Bit	Description
7:0	**Pixel Data Write Enable [7:0]:** • These bits can control whether individual pixel data bits [7:0] are written. • To enable an individual pixel, the corresponding Pixel Data Write Enable bit must be set to 1, and *one* of the following conditions must be met: — Extended Write mode 4 or Extended Write mode 5 is selected with Graphics Controller register bits GR5[2:0]. — Write mode 1 is selected with Graphics Controller register bits GR5[2:0], and Extension register GRB[2] is set to 1. • This field is also used to write protect the BitBLT (bit block transfer) engine.
7:4	**Reserved:** These 4 bits are reserved when Extended Write modes 4 and 5 are disabled (that is, Graphics Controller register bit GR5[2] = 0), which would be the case for VGA-compatibility modes.
3:0	**Bit Map Plane Enable [3:0]:** These 4 bits are used to control whether individual display memory bit-map planes [3:0] are written with Write modes [3:0].

8.5 SR3: Character Map Set Select Register

I/O Port Address: 3C5

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Character Map Set Select [2]	0
4	Primary Character Map Set Select [2]	0
3	Secondary Character Map Set Select [1]	0
2	Secondary Character Map Set Select [0]	0
1	Primary Character Map Set Select [1]	0
0	Primary Character Map Set Select [0]	0

This register is used to specify the primary and the secondary character map sets (fonts). This register applies only to text modes.

Bit	Description
7:6	**Reserved**
5, 3:2	**Secondary Character Map Set Select:** These 3 bits select from among the secondary character map sets, according to the following table:

SR3			Secondary Character Map Set	Address Offset (Kbytes)
[5]	[3]	[2]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

8.5 SR3: Character Map Set Select Register *(cont.)*

Bit	Description

4, 1:0 **Primary Character Map Set Select:**
These 3 bits select from among the primary character map sets, according to the following table:

SR3			Primary Character Map Set	Address Offset (Kbytes)
[4]	[1]	[0]		
0	0	0	0	0
0	0	1	1	16
0	1	0	2	32
0	1	1	3	48
1	0	0	4	8
1	0	1	5	24
1	1	0	6	40
1	1	1	7	56

NOTES:

1) In text video display modes:
   1. Character Map Plane 0 stores the ASCII text character code.
   2. Character Map Plane 1 stores the attribute byte.
   3. Character Map Plane 2 stores the character map set (the font).

2) Bit 3 of the attribute byte normally controls the intensity of the foreground color.

   This bit may be redefined to be a switch between character sets, allowing 512 displayable characters.

   This switch is enabled whenever SR4[1] is a 1 *and* there is a difference between the values of the Primary Character Map Set Select and the values of the Secondary Character Map Set Select.

3) The format for the Character Map Plane 2 font address bits [15:0] is:

   F2 F1 F0 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0

   where:

   F[2:0] is the character map set select
   C[7:0] is the ASCII text character code
   R[4:0] is the character row (the scanline in the character cell)

8.6 SR4: Memory Mode Register

I/O Port Address: 3C5

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Chain-4	0
2	Odd/Even Mode	0
1	Extended (Display) Memory	0
0	Reserved	

This register is used to control miscellaneous functions in the CL-GD7548 sequencer.

Bit	Description
7:4	**Reserved**
3	**Chain-4:** When this bit is programmed to 1: • This bit takes priority over SR4[2] (Odd/Even mode) and Graphics Controller register GR5[4] (Odd/Even Addressing mode). • Its effect is similar to SR4[2] (Odd/Even mode), except BE0–4# (CBE0–4# for PCI bus). — Address A0 provides display memory Plane Select Bit [0]. — Address A1 provides display memory Plane Select Bit [1]. • The Graphics Controller GR4 register (Read Map register) is ignored.
2	**Odd/Even Mode:** • When this bit is programmed to 0, the sequencer is in Odd/Even mode. • This bit *must* be programmed to a 0 for text modes. • The value of this bit must track Graphics Controller register GR5[4] (Odd/Even Addressing mode), and the value of this register must be opposite the value of GR5[4]. — The even CPU addresses access display memory planes 0 and 2. — The odd CPU addresses access display memory planes 1 and 3. • This bit may be overridden by the SR4[3] bit.
1	**Extended (Display) Memory:** When this bit is programmed to: • 0, effective memory size is 64 Kbytes, regardless of actual installed memory. (EGA modes require this to be the case.) • 1, effective memory size equals actual installed memory.
0	**Reserved**

9. CRT CONTROLLER REGISTERS

NOTE: The '?' in the I/O port address of the registers in the next sections implies 'B' in Monochrome mode and 'D' in Color mode.

9.1 CRX: CRT Controller Index Register

I/O Port Address: 3?4

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	CRTC Index [5]	0
4	CRTC Index [4]	0
3	CRTC Index [3]	0
2	CRTC Index [2]	0
1	CRTC Index [1]	0
0	CRTC Index [0]	0

This index register is used to specify the register in the CRTC (CRT Controller) block to be accessed by the next I/O read or I/O write to Address 3?5. Registers at indexes 19, 1A, 1B, 25, and 27 are described in the Extension registers in Chapter 12.

Bit	Description
7:6	**Reserved**
5:0	**CRTC Index [5:0]:** The value resulting from these bits point to the register to be accessed in the next I/O read or I/O write to address 3?5. (Note that registers above 18 were never documented by IBM.)

9.2 CR0: Horizontal Total Register

I/O Port Address: 3?5

Index: 0

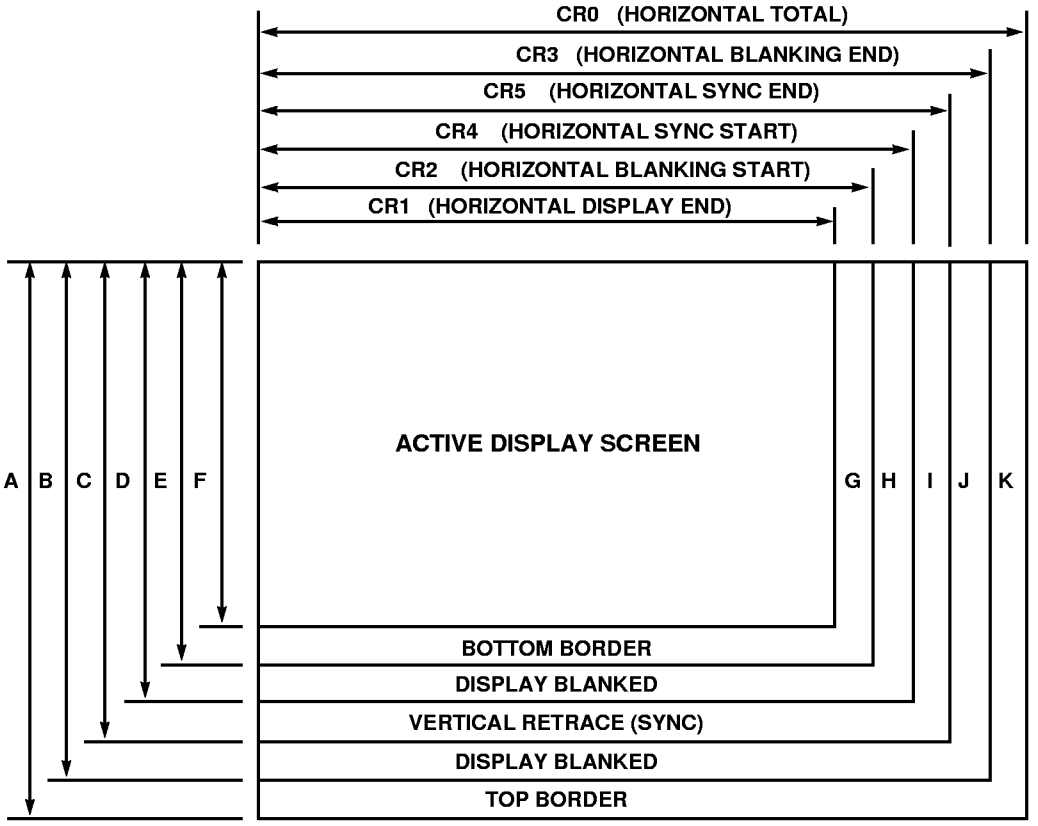
Bit	Description	Reset State
7	Horizontal Total [7]	
6	Horizontal Total [6]	
5	Horizontal Total [5]	
4	Horizontal Total [4]	
3	Horizontal Total [3]	
2	Horizontal Total [2]	
1	Horizontal Total [1]	
0	Horizontal Total [0]	

This register is used to specify the total number of character clocks per horizontal period.

NOTE: This register can be write-protected by CRT Controller register CR11[7].

Bit	Description
7:0	**Horizontal Total:** • This 8-bit field specifies the total number of character clocks per horizontal period as follows: 1. The VCLK signal provides the character clock. (The character clock is derived from VCLK, according to the character width.) 2. The character counter counts the total number of character clocks. 3. The value in the character counter is then compared with the value in this register to provide the basic horizontal timing. (All horizontal and vertical timing is eventually derived from the basic horizontal timing in this register.) • The value of the horizontal total for this register is calculated as follows: FROM: Total number of character clocks (from character counter) SUBTRACT: – 5 character clocks (for standard VGA compatibility) TO OBTAIN: = Horizontal total Example: If 80 characters are desired per horizontal scanline, then a value of 75 must be loaded into this register. • Figure 9-1 indicates the way the horizontal and vertical timing is defined. — The horizontal timing is calculated in terms of character clock periods. — The vertical timing is calculated in terms of horizontal periods. Table 9-1 indicates how the various CRTC registers are extended.

9.2 CR0: Horizontal Total Register *(cont.)*



A - CR6 (VERTICAL TOTAL)
B - CR16 (VERTICAL BLANKING END)
C - CR11 (VERTICAL SYNC END)
D - CR10 (VERTICAL SYNC START)
E - CR15 (VERTICAL BLANKING START)
F - CR12 (VERTICAL DISPLAY END)

G - RIGHT BORDER
H - DISPLAY BLANKED
I - HORIZONTAL RETRACE (SYNC)
J - DISPLAY BLANKED
K - LEFT BORDER

Figure 9-1. CRT Controller Timing Registers

9.2 CR0: Horizontal Total Register *(cont.)*

Table 9-1 is a guide to the location of the CRT Controller registers and accompanying extension and overflow bits.

- An extension bit is a bit added by Cirrus Logic to the standard VGA controller bits.
- An overflow bit is a standard VGA controller bit that results from using more than 8 bits to define a field.

Table 9-1. Summary of CRT Controller Register Bits[a]

Parameter	CRT Controller Register Bit Position					
	[9]	[8]	[7]	[6]	[5]	[4:0]
Horizontal Total			CR0[7]	CR0[6]	CR0[5]	CR0[4:0]
Horizontal Display End			CR1[7]	CR1[6]	CR1[5]	CR1[4:0]
Horizontal Blanking Start			CR2[7]	CR2[6]	CR2[5]	CR2[4:0]
Horizontal Blanking End			**CR1A[5]**	**CR1A[4]**	CR5[7]	CR3[4:0]
Horizontal Sync Start			CR4[7]	CR4[6]	CR4[5]	CR4[4:0]
Horizontal Sync End						CR5[4:0]
Vertical Total	CR7[5]	CR7[0]	CR6[7]	CR6[6]	CR6[5]	CR6[4:0]
Vertical Sync Start	CR7[7]	CR7[2]	CR10[7]	CR10[6]	CR10[5]	CR10[4:0]
Vertical Sync End						CR11[3:0]
Vertical Display End	CR7[6]	CR7[1]	CR12[7]	CR12[6]	CR12[5]	CR12[4:0]
Vertical Blanking Start	CR9[5]	CR7[3]	CR15[7]	CR15[6]	CR15[5]	CR15[4:0]
Vertical Blanking End	**CR1A[7]**	**CR1A[6]**	CR16[7]	CR16[6]	CR16[5]	CR16[4:0]
Line Compare	CR9[6]	CR7[4]	CR18[7]	CR18[6]	CR18[5]	CR18[4:0]
Offset		**CR1B[4]**	CR13[7]	CR13[6]	CR13[5]	CR13[4:0]

[a] Bits shown in **bold** text are Cirrus Logic extensions.

9.3 CR1: Horizontal Display End Register

I/O Port Address: 3?5

Index: 1

Bit	Description	Reset State
7	Horizontal Display End [7]	
6	Horizontal Display End [6]	
5	Horizontal Display End [5]	
4	Horizontal Display End [4]	
3	Horizontal Display End [3]	
2	Horizontal Display End [2]	
1	Horizontal Display End [1]	
0	Horizontal Display End [0]	

This register is used to specify the number of character clocks during horizontal display time.

NOTE: This register can be write-protected by CRT Controller register CR11[7].

Bit	Description
7:0	**Horizontal Display End [7:0]:** For the horizontal display time, this register specifies the number of character clocks, *minus 1*, as calculated for both text modes and graphics modes. • For text modes: CR1[7:0] = "Number of character clocks" – 1 Where number of character clocks = Number of characters • For graphics modes: CR1[7:0] = "Number of character clocks" – 1 Where number of character clocks = (Number of pixels/scanline) ÷ (Number of pixels/character clock) For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.4 CR2: Horizontal Blanking Start Register

I/O Port Address: 3?5

Index: 2

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	
6	Horizontal Blanking Start [6]	
5	Horizontal Blanking Start [5]	
4	Horizontal Blanking Start [4]	
3	Horizontal Blanking Start [3]	
2	Horizontal Blanking Start [2]	
1	Horizontal Blanking Start [1]	
0	Horizontal Blanking Start [0]	

This register is used to specify the character count at which horizontal blanking starts.

NOTE: This register can be write-protected by CRT Controller register CR11[7].

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** This register specifies the character count at which horizontal blanking starts. • For text modes: Character count where horizontal blanking starts = Number of characters • For graphics modes: Character count at which horizontal blanking starts = (Number of pixels/scanline) ÷ (Number of pixels/character clock) • For both text modes and graphics modes: The value programmed into CR2 must always be larger than the value programmed into CRT Controller register CR1. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.5 CR3: Horizontal Blanking End Register

I/O Port Address: 3?5

Index: 3

Bit	Description	Reset State
7	Compatible Read	
6	Display Enable Delay [1]	
5	Display Enable Delay [0]	
4	Horizontal Blanking End [4]	
3	Horizontal Blanking End [3]	
2	Horizontal Blanking End [2]	
1	Horizontal Blanking End [1]	
0	Horizontal Blanking End [0]	

This register is used to determine the horizontal blanking period width. Also, this register controls access to CRT Controller registers CR10 and CR11 and the display enable delay.

NOTE: This register can be write-protected by CRT Controller register CR11[7].

Bit **Description**

7 **Compatible Read:**
When this bit is:
- 0, CRT Controller registers CR10 and CR11 are write-only registers.
- 1, CRT Controller registers CR10 and CR11 are read/write registers.

6:5 **Display Enable Delay [1:0]:**
This 2-bit field is used to specify the number of character clocks that the display enable signal is delayed from the horizontal total. This delay is necessary to compensate for the accesses of the character code, attribute byte, font, etc.

The following table indicates programming for the display enable signal delay:

CR3		Delay for Display Enable Signal (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character clock (typical setting)
1	0	2 character clocks
1	1	3 character clocks

NOTE: If the delay is programmed too low, the left-most character repeats.
If the delay is programmed too high, one or more characters disappear at the left of each character row.

9.5 CR3: Horizontal Blanking End Register *(cont.)*

Bit	Description
4:0	**Horizontal Blanking End [4:0]:** • The horizontal blanking end field determines the width of the horizontal blanking period. This field consists of these 5 bits (and as needed, a sixth bit in CR5[7]). • The least-significant 5 (or 6) bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal blanking period ends. • The horizontal blanking end value to be programmed into this register is calculated as follows: FROM: Horizontal blanking start (value programmed into CR2) SUBTRACT: – Horizontal blanking period (as desired) TO OBTAIN: Horizontal blanking end • The horizontal blanking period: — Must never be programmed to extend past the horizontal total. — Is limited to 63 character-clock times. • The horizontal blanking end field is extended as follows: — CR5[7] is the horizontal blanking end field bit [5], which increases this field to 6 bits. — When either Extension register CR1B[5] is 1 or Extension register CR1B[7] is 1, Extension register bits CR1A[5:4] further extend the horizontal blanking end field to 8 bits with bits [7:6]. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.6 CR4: Horizontal Sync Start Register

I/O Port Address: 3?5

Index: 4

Bit	Description	Reset State
7	Horizontal Sync Start [7]	
6	Horizontal Sync Start [6]	
5	Horizontal Sync Start [5]	
4	Horizontal Sync Start [4]	
3	Horizontal Sync Start [3]	
2	Horizontal Sync Start [2]	
1	Horizontal Sync Start [1]	
0	Horizontal Sync Start [0]	

This register specifies the time when horizontal synchronization becomes active.

NOTE: This register can be write-protected by CRT Controller register CR11[7].

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** This field specifies the character count at which the horizontal synchronization signal becomes active. Adjusting the value in this field moves the display horizontally on the screen. • The horizontal sync start must be programmed to a value either equal to or greater than horizontal display end. • The time from horizontal sync start to horizontal total must be either equal to or greater than four character-clock times. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.7 CR5: Horizontal Sync End Register

I/O Port Address: 3?5

Index: 5

Bit	Description	Reset State
7	Horizontal Blanking End [5]	
6	Horizontal Sync Delay [1]	
5	Horizontal Sync Delay [0]	
4	Horizontal Sync End [4]	
3	Horizontal Sync End [3]	
2	Horizontal Sync End [2]	
1	Horizontal Sync End [1]	
0	Horizontal Sync End [0]	

This register specifies the position where the horizontal synchronization pulse ends, effectively specifying the width of the pulse. In addition, this register contains an overflow bit and a field for the horizontal synchronization delay.

NOTE: This register can be write-protected by CRT Controller register CR11[7].

Bit **Description**

7 **Horizontal Blanking End [5]:**
This overflow bit increases by one bit the horizontal blanking end value of CR3[4:0].

6:5 **Horizontal Sync Delay [1:0]:**
This 2-bit field is used to specify the number of character clocks that the external horizontal synchronization pulse is delayed from the horizontal synchronization start position implied in CR4.

In some graphics modes, this horizontal synchronization delay is necessary to allow internal timing signals that are triggered from horizontal synchronization start to begin, prior to display enable.

The following table summarizes programming for the horizontal synchronization delay:

CR5		Delay for Horizontal Synchronization Pulse (in number of character clocks)
[6]	[5]	
0	0	No delay
0	1	1 character-clock delay
1	0	2 character-clock delay
1	1	3 character-clock delay

9.7 CR5: Horizontal Sync End Register *(cont.)*

Bit	Description
4:0	**Horizontal Sync End [4:0]:** • The horizontal synchronization end field determines the width of the horizontal synchronization pulse. • The least-significant 5 bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal synchronization pulse ends. • The horizontal synchronization end value to be programmed into this register is calculated as follows: FROM: Horizontal synchronization start (value programmed in CR4) SUBTRACT: – Horizontal synchronization pulse width (as desired) TO OBTAIN: = Horizontal synchronization end • The horizontal synchronization pulse: — Has a width limited to 31 character-clock times. — Must never be programmed to extend past the horizontal total of CR0. — Must always end during the horizontal blanking period. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.8 CR6: Vertical Total Register

I/O Port Address: 3?5

Index: 6

Bit	Description	Reset State
7	Vertical Total [7]	
6	Vertical Total [6]	
5	Vertical Total [5]	
4	Vertical Total [4]	
3	Vertical Total [3]	
2	Vertical Total [2]	
1	Vertical Total [1]	
0	Vertical Total [0]	

This register contains the least-significant 8 bits of the 10-bit Vertical Total Field that specifies the total number of scanlines per frame.

Bit	Description
7:0	**Vertical Total [7:0]:** • This vertical total field, a 10-bit field that consists of these 8 bits and the 2 bits in CR7[5] and CR7[0], defines the total number of scanlines per frame. • The value of the Vertical Total field to be programmed is calculated as follows: FROM: Total number of horizontal scanlines SUBTRACT: – 2 scanlines TO OBTAIN: = Vertical Total field (total number of scanlines per frame) When the value in the scanline counter equals the value of the Vertical Total field, a vertical retrace period begins. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1. **NOTE:** This register can be write-protected by CRT Controller register CR11[7].

9.9 CR7: Overflow Register

I/O Port Address: 3?5

Index: 7

Bit	Description	Reset State
7	Vertical Sync Start [9]	
6	Vertical Display End [9]	
5	Vertical Total [9]	
4	Line Compare [8]	
3	Vertical Blanking Start [8]	
2	Vertical Sync Start [8]	
1	Vertical Display End [8]	
0	Vertical Total [8]	

This register contains overflow bits for various vertical count fields. For a summary of all CRT Controller registers, refer to Figure 9-1 and Table 9-1.

NOTE: Except for CR7[4], which can always be written, this register can be write-protected by CRT Controller register CR11[7].

Bit	Description
7	**Vertical Sync Start [9]:** With CR7[2], this bit increases the Vertical Sync Start field (CR10) to 10 bits.
6	**Vertical Display End [9]:** With CR7[1], this bit increases the Vertical Display End field (CR12) to 10 bits.
5	**Vertical Total [9]:** With CR7[0], this bit increases the Vertical Total field (CR6) to 10 bits.
4	**Line Compare [8]:** With CR9[6], this bit increases the Line Compare field (CR18) to 10 bits. This bit can always be written.
3	**Vertical Blanking Start [8]:** With CR9[5], this bit increases the Vertical Blanking Start field (CR15) to 10 bits.
2	**Vertical Sync Start [8]:** With CR7[7], this bit increases the Vertical Sync Start field (CR10) to 10 bits.
1	**Vertical Display End [8]:** With CR7[6], this bit increases the Vertical Display End field (CR12) to 10 bits.
0	**Vertical Total [8]:** With CR7[5], this bit increases the Vertical Total field (CR6) to 10 bits.

9.10 CR8: Screen A Preset Row Scan Register

I/O Port Address: 3?5

Index: 8

Bit	Description	Reset State
7	Reserved	
6	Byte (Coarse) Panning [1]	
5	Byte (Coarse) Panning [0]	
4	Screen A Preset Row Scan [4]	
3	Screen A Preset Row Scan [3]	
2	Screen A Preset Row Scan [2]	
1	Screen A Preset Row Scan [1]	
0	Screen A Preset Row Scan [0]	

This register specifies the row scanline at which Screen A starts. This register also allows two types of scrolling:

- Scrolling on a character row (scanline) basis (also called coarse panning).
- Scrolling on a scanline (row) basis, also called fine scroll.

In addition, this register specifies byte (coarse) panning.

Bit — **Description**

7 — **Reserved**

6:5 — **Byte (Coarse) Panning [1:0]:**
This 2-bit field controls coarse panning. (For fine panning on a pixel-by-pixel basis, refer to Attribute Controller register AR13.)
- This field can specify a coarse pan of up to 24 pixels, with 8-pixel resolution.
- Values for CR8[6:5] are interpreted as indicated in the following table:

CR8		Resulting Pan (in bytes)	Resulting Pan (in pixels)
[6]	[5]		
0	0	0	0
0	1	1	8
1	0	2	16
1	1	3	24

4:0 — **Screen A Preset Row Scan [4:0]:**
This field specifies the scanline at which the first character row begins.
- This specification provides scrolling on a scanline basis (soft scrolling).
- The contents of this field must be changed only during vertical retrace.

9.11 CR9: Character Cell Height Register

I/O Port Address: 3?5

Index: 9

Bit	Description	Reset State
7	Scanline Double Control	
6	Line Compare [9]	
5	Vertical Blanking Start [9]	
4	Character Cell Height [4]	
3	Character Cell Height [3]	
2	Character Cell Height [2]	
1	Character Cell Height [1]	
0	Character Cell Height [0]	

This register specifies the number of scanlines in the character cell. In addition, it contains two overflow bits and one control bit.

Bit	Description
7	**Scanline Double Control:** When this bit is 1, every scanline is displayed twice in succession. • Scanlines double for those specifications based on scanline counter addressing, such as Character Height, Cursor Start, Cursor End, and Cursor Underline location. • Typically, this bit is used to double a 200-scanline display to 400 scanlines. • The scanline doubling function is not available in interlaced graphics modes.
6	**Line Compare [9]:** With CR7[4], this bit increases the line compare field (CR18) to 10 bits.
5	**Vertical Blanking Start [9]:** With CR7[3], this bit increases the vertical blanking start field (CR15) to 10 bits.
4:0	**Character Cell Height [4:0]:** This field specifies the vertical size of the character cell in terms of scanlines. The value programmed into this field equals the actual size of the character cell (in scanlines) minus 1.

9.12 CRA: Text Cursor Start Register

I/O Port Address: 3?5

Index: A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Text Cursor Disable	
4	Text Cursor Start [4]	
3	Text Cursor Start [3]	
2	Text Cursor Start [2]	
1	Text Cursor Start [1]	
0	Text Cursor Start [0]	

This register contains a bit that can disable the text cursor. In addition, this register specifies the scanline at which the text cursor is to start.

Bit	Description
7:6	**Reserved**
5	**Text Cursor Disable:** When this bit is: • 0, the text cursor functions normally • 1, the text cursor is disabled (that is, it is removed).
4:0	**Text Cursor Start [4:0]:** This field specifies the scanline within the character cell at which the text cursor is to start. When the Text Cursor Start value is: • Less than or greater than the Text Cursor End value, no text cursor displays. • Equal to the Text Cursor End value, the text cursor displays on a single scan-line.

9.13 CRB: Text Cursor End Register

I/O Port Address: 3?5

Index: B

Bit	Description	Reset State
7	Reserved	
6	Text Cursor Delay [1]	
5	Text Cursor Delay [0]	
4	Text Cursor End [4]	
3	Text Cursor End [3]	
2	Text Cursor End [2]	
1	Text Cursor End [1]	
0	Text Cursor End [0]	

This register specifies the scanline at which the text cursor is to end. It also contains a field that allows the text cursor display to be delayed from the location specified in CRE and CRF.

Bit	Description
7	**Reserved**
6:5	**Text Cursor Delay [1:0]:** This 2-bit field specifies a delay, given in character clocks, from the text cursor location specified in CRE and CRF to the actual display of the text cursor.
4:0	**Text Cursor End [4:0]:** This field specifies the scanline within the character cell at which the text cursor is to end. When the Text Cursor End value is: • Less than or equal to the character cell height, no text cursor displays. • Greater than the character cell height, the effective text cursor end value is equal to the character cell height.

9.14 CRC: Screen A Start Address High Register

I/O Port Address: 3?5

Index: C

Bit	Description	Reset State
7	Screen A Start Address [15]	
6	Screen A Start Address [14]	
5	Screen A Start Address [13]	
4	Screen A Start Address [12]	
3	Screen A Start Address [11]	
2	Screen A Start Address [10]	
1	Screen A Start Address [9]	
0	Screen A Start Address [8]	

This register, along with CRD and Extension register bits CR1B[3:2, 0], specifies the display memory location where data to be displayed on the screen starts.

Bit	Description
7:0	**Screen A Start Address [15:8]:** The 19-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the screen. • Bits [18:16] are in Extension register CR1B[3:2,0]. • Bits [15:8] are in this register. • Bits [7:0] are in CRT Controller register CRD.

9.15 CRD: Screen A Start Address Low Register

I/O Port Address: 3?5

Index: D

Bit	Description	Reset State
7	Screen A Start Address [7]	
6	Screen A Start Address [6]	
5	Screen A Start Address [5]	
4	Screen A Start Address [4]	
3	Screen A Start Address [3]	
2	Screen A Start Address [2]	
1	Screen A Start Address [1]	
0	Screen A Start Address [0]	

This register, along with CRC and Extension register CR1B[3:2, 0], specify the display memory location where data to be displayed on the screen starts.

Bit	Description
7:0	**Screen A Start Address [7:0]:** The 19-bit Screen A Start Address field contains a value that specifies the starting display memory location for data to be displayed on the screen. • Bits [18:16] are in Extension register CR1B[3:2,0]. • Bits [15:8] are in CRT Controller register CRC. • Bits [7:0] are in this register.

9.16 CRE: Text Cursor Location High Register

I/O Port Address: 3?5

Index: E

Bit	Description	Reset State
7	Text Cursor Location [15]	
6	Text Cursor Location [14]	
5	Text Cursor Location [13]	
4	Text Cursor Location [12]	
3	Text Cursor Location [11]	
2	Text Cursor Location [10]	
1	Text Cursor Location [9]	
0	Text Cursor Location [8]	

This register, along with CRF, specifies the display memory location where the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [15:8]:** The Text Cursor Location is a 16-bit field that specifies the display memory location where the text cursor is to be displayed. • Bits [15:8] are in this register. • Bits [7:0] are in CRT Controller register CRF. • The value contained in this field specifies an address in display memory, not an offset from the beginning of the screen. When the value of the Screen A Start is changed without a compensating change in the Text Cursor Location field, the text cursor moves on the screen.

9.17 CRF: Text Cursor Location Low Register

I/O Port Address: 3?5

Index: F

Bit	Description	Reset State
7	Text Cursor Location [7]	
6	Text Cursor Location [6]	
5	Text Cursor Location [5]	
4	Text Cursor Location [4]	
3	Text Cursor Location [3]	
2	Text Cursor Location [2]	
1	Text Cursor Location [1]	
0	Text Cursor Location [0]	

This register, with CRE, specifies the display memory location where the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [7:0]:** The Text Cursor Location is a 16-bit field that specifies the display memory location where the text cursor is to be displayed. • Bits [15:8] are in CRT Controller register CRE. • Bits [7:0] are in this register.

9.18 CR10: Vertical Sync Start Register

I/O Port Address: 3?5

Index: 10

Bit	Description	Reset State
7	Vertical Sync Start [7]	
6	Vertical Sync Start [6]	
5	Vertical Sync Start [5]	
4	Vertical Sync Start [4]	
3	Vertical Sync Start [3]	
2	Vertical Sync Start [2]	
1	Vertical Sync Start [1]	
0	Vertical Sync Start [0]	

The Vertical Sync Start field specifies the scanline at which the Vertical Sync pulse is to become active.

Access to this register is controlled by CRT Controller register CR3[7]. When CR3[7] is

- 1, this register is read/write.
- 0, this register is write-only.

Bit	Description
7:0	**Vertical Sync Start [7:0]:** The Vertical Sync field specifies the scanline at which the Vertical Sync pulse is to become active. • This register contains the least-significant 8 bits [7:0] of that field. • Bits [9:8] in CRT Controller register CR7[7,2] increase this field to 10 bits. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.19 CR11: Vertical Sync End Register

I/O Port Address: 3?5

Index: 11

Bit	Description	Reset State
7	CRT Controller Registers CR0–CR7 Write Protect	
6	Refresh Cycle Control	
5	Vertical Interrupt Disable	
4	Vertical Interrupt Clear	
3	Vertical Sync End [3]	
2	Vertical Sync End [2]	
1	Vertical Sync End [1]	
0	Vertical Sync End [0]	

This register specifies the scanline at which the Vertical Sync pulse is to become inactive, thereby effectively specifying the Vertical Sync pulse width. In addition, this register contains controls for the vertical interrupt and two miscellaneous control bits, CR11[7:6].

Access to this register is controlled by CRT Controller register CR3[7]. When CR3[7] is

- 0, this register is write-only.
- 1, this register is read/write.

Bit	Description
7	**CRT Controller Registers CR0–CR7 Write Protect:** When this bit is: • 0, CR0 through CR7 can be written normally. • 1, CR0 through CR7 cannot be written, except for CR7[4], which can always be written.
6	**Refresh Cycle Control:** When this bit is: • 0, three refresh cycles execute per scanline. • 1, five refresh cycles execute per scanline.
5	**Vertical Interrupt Disable:** When this bit is: • 0, vertical interrupt is enabled and functions normally. • 1, vertical interrupt is disabled, and the INTR/INTR# pin cannot go active.
4	**Vertical Interrupt Clear:** When this bit is: • 0, the External/General register (FEAT[7]) clears to 0, and the INTR/INTR# pin is forced inactive. • 1, it has no effect.

9.19 CR11: Vertical Sync End Register *(cont.)*

Bit	Description
3:0	**Vertical Sync End [3:0]:** This field determines the width of the Vertical Sync pulse. • The value of this field is compared with the least-significant 4 bits of the Scan-line Counter. When a match occurs, the Vertical Sync pulse is ended. • The Vertical Sync pulse is limited to 15 scanlines. • The vertical sync end value to be programmed into this register may be calculated as follows: FROM: Vertical sync start (value programmed in CR10 and CR7[7,2]) SUBTRACT: – Vertical sync width (as desired) TO OBTAIN: = Vertical sync end • The Vertical Sync pulse must never be programmed to extend past the Vertical Total. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.20 CR12: Vertical Display End Register

I/O Port Address: 3?5

Index: 12

Bit	Description	Reset State
7	Vertical Display End [7]	
6	Vertical Display End [6]	
5	Vertical Display End [5]	
4	Vertical Display End [4]	
3	Vertical Display End [3]	
2	Vertical Display End [2]	
1	Vertical Display End [1]	
0	Vertical Display End [0]	

The Vertical Display End field is used to specify the scanline at which the display is to end.

Bit	Description
7:0	**Vertical Display End [7:0]:** The Vertical Display End field is used to specify the scanline at which the display is to end. • The least-significant 8 bits [7:0] of this field are in this register. • The most-significant 2 bits [9:8] are in CRT Controller register CR7[6,1]. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.21 CR13: Offset Register

I/O Port Address: 3?5

Index: 13

Bit	Description	Reset State
7	Offset [7]	
6	Offset [6]	
5	Offset [5]	
4	Offset [4]	
3	Offset [3]	
2	Offset [2]	
1	Offset [1]	
0	Offset [0]	

This register specifies the display 'pitch,' which is the distance in the display memory between the beginnings of adjacent character rows or scanlines.

Bit	Description
7:0	**Offset [7:0]:** This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This field is extended to 9 bits with Extension register CR1B[4]. Except for the first scanline, to calculate the address from which to begin fetching data, add the contents of this register CR13 to the beginning address of the previous scanline or character row. As a result, depending on the value of CRT Controller register CR17[6], the offset shifts left either zero or one bit position.

9.22 CR14: Underline Row Scanline Register

I/O Port Address: 3?5

Index: 14

Bit	Description	Reset State
7	Reserved	
6	Double-word Addressing Mode for Display Memory	
5	Count by Four	
4	Underline Scanline [4]	
3	Underline Scanline [3]	
2	Underline Scanline [2]	
1	Underline Scanline [1]	
0	Underline Scanline [0]	

This register is used to enable or disable access to the Extension registers.

Bit	Description
7	**Reserved**
6	**Double-word Addressing Mode for Display Memory:** When this bit is: • 0, CR17[6] controls whether the CL-GD7548 uses the byte-address mode or the word-address mode. • 1, double-word addressing mode is selected. — The CRTC Memory Address Counter is rotated left for two bit positions. — As a result, display memory address bits MA[1] and MA[0] are sourced from CRTC Address Counter bits [13] and [12], respectively.
5	**Count by Four:** When double-word Addressing mode is: • Disabled (CR14[6] is 0), this bit must be cleared to 0. • Enabled (CR14[6] is 1), this bit must be set to 1 to clock the Memory Address Counter with Character Clock divided by four.
4:0	**Underline Scanline [4:0]:** Within a character cell, this field specifies the scanline at which the underline occurs.

9.23 CR15: Vertical Blanking Start Register

I/O Port Address: 3?5

Index: 15

Bit	Description	Reset State
7	Vertical Blanking Start [7]	
6	Vertical Blanking Start [6]	
5	Vertical Blanking Start [5]	
4	Vertical Blanking Start [4]	
3	Vertical Blanking Start [3]	
2	Vertical Blanking Start [2]	
1	Vertical Blanking Start [1]	
0	Vertical Blanking Start [0]	

This register specifies the scanline at which blanking is to become active.

Bit	Description
7:0	**Vertical Blanking Start [7:0]:** This 10-bit field specifies the scanline at which vertical blanking is to start. • The least-significant 8 bits [7:0] of this field are in this register. • The most-significant 2 bits [9:8] of this field are in CRT Controller registers CR9[5] and CR7[3]. For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.24 CR16: Vertical Blanking End Register

I/O Port Address: 3?5

Index: 16

Bit	Description	Reset State
7	Vertical Blanking End [7]	
6	Vertical Blanking End [6]	
5	Vertical Blanking End [5]	
4	Vertical Blanking End [4]	
3	Vertical Blanking End [3]	
2	Vertical Blanking End [2]	
1	Vertical Blanking End [1]	
0	Vertical Blanking End [0]	

The Vertical Blanking End field specifies the scanline at which vertical blanking is to end.

Bit	Description
7:0	**Vertical Blanking End [7:0]:** The Vertical Blanking End field specifies the scanline at which vertical blanking is to end. When Extension register CR1B[5] is: • 0, the entire field is the 8 bits of CRT Controller register CR16[7:0]. • 1, the field is extended to 10 bits with Extension register CR1A[7:6]. The contents of the Vertical Blanking End field are compared to the scanline counter to determine when to terminate vertical blanking. If Extension register CR1B[5] is: • 0, this comparison limits the duration of vertical blanking to 255 scanlines. • 1, this comparison does not limit the duration of vertical blanking to 255 scanlines. (That is, the duration of vertical blanking may be more than 255 scanlines.) For a summary of all CRTC registers, refer to Figure 9-1 and Table 9-1.

9.25 CR17: Mode Control Register

I/O Port Address: 3?5

Index: 17

Bit	Description	Reset State
7	CRT Controller Timing Logic Enable	
6	Byte/Word Address Mode Control	
5	Address Rotation	
4	Reserved	
3	Count by Two	
2	Multiply Vertical Registers by Two	
1	Compatibility-Mode (Hercules) Support	
0	Compatibility-Mode (CGA) Support	

This register contains a number of miscellaneous control bits.

Bit	Description
7	**CRT Controller Timing Logic Enable:** When this bit is: • 0, CRT Controller timing logic is disabled, forcing a reset condition. • 1, CRT Controller timing logic is enabled and functions normally.
6	**Byte/Word Address Mode Control:** When this bit is: • 0: — The Word-Address mode is enabled. — Before the contents of the CRTC Address Counter are sent to display memory, they are rotated left one bit position. • 1: — The Byte-Address mode is enabled. — Before the contents of the CRTC Address Counter are sent to display memory, they are not rotated.
5	**Address Rotation:** • When CR17[6] is 0 *and* this bit is: — 0, the left rotation described in CR17[6] above involves 14 bits of the CRTC Address Counter. — 1, the left rotation described in CR17[6] above involves 16 bits of the CRTC Address Counter. • When CR17[6] is 1, this bit is ignored.
4	**Reserved**

9.25 CR17: Mode Control Register *(cont.)*

Bit	Description
3	**Count by Two:** When this bit is: • 0, the CL-GD7548 clocks the Memory Address Counter with the Character Clock. • 1, the CL-GD7548 clocks the Memory Address Counter with the Character Clock, divided by two.
2	**Multiply Vertical Registers by Two:** When this bit is: • 0, the Scanline Counter is clocked with Horizontal Sync. — As a result, the number of scanlines is 1024. • 1, the Scanline Counter is clocked with Horizontal Sync, divided by two. (In effect, the Vertical registers are multiplied by two.) — This division allows the number of scanlines to be doubled to 2048. — All periods become even multiples of two scanlines.
1	**Compatibility-Mode (Hercules) Support:** When this bit is: • 0, Scanline Counter bit [1] is substituted for CRTC Address Counter [14]. This substitution provides for Hercules™ compatibility. • 1, the substitution described above does not occur.
0	**Compatibility-Mode (CGA) Support:** When this bit is: • 0, Scanline Counter bit [0] is substituted for CRTC Address Counter [14]. This substitution provides for CGA compatibility. • 1, the substitution described above does not occur.

9.26 CR18: Line Compare Register

I/O Port Address: 3?5

Index: 18

Bit	Description	Reset State
7	Line Compare [7]	
6	Line Compare [6]	
5	Line Compare [5]	
4	Line Compare [4]	
3	Line Compare [3]	
2	Line Compare [2]	
1	Line Compare [1]	
0	Line Compare [0]	

The Line Compare field is used to specify where Screen A ends and Screen B starts for a vertically split screen.

Bit	Description
7:0	**Line Compare [7:0]:** The 10-bit Line Compare field is used to implement a vertically split screen by specifying where Screen A ends and Screen B starts. • This register contains the least-significant 8 bits [7:0] of this field. • The most-significant 2 bits are in CRT Controller registers CR9[6] and CR7[4]. The top portion of the split screen is called Screen A. • Screen A may start anywhere in display memory. • Screen A can be panned and scrolled on a pixel-by-pixel basis. The bottom portion of the split screen is called Screen B. • Screen B always starts at location 0 in display memory. • Screen B cannot be panned or scrolled.

9.27 CR22: Graphics Controller Data Latches Readback Register

I/O Port Address: 3?5

Index: 22

Bit	Description	Reset State
7	Graphics Controller Data Latch *n* Readback [7]	
6	Graphics Controller Data Latch *n* Readback [6]	
5	Graphics Controller Data Latch *n* Readback [5]	
4	Graphics Controller Data Latch *n* Readback [4]	
3	Graphics Controller Data Latch *n* Readback [3]	
2	Graphics Controller Data Latch *n* Readback [2]	
1	Graphics Controller Data Latch *n* Readback [1]	
0	Graphics Controller Data Latch *n* Readback [0]	

This register address is used to read the graphics controller data latches.

Bit	Description
7:0	**Graphics Controller Data Latch *n* Readback [7:0]:** This read-only register is used to read back the contents of one of the four VGA graphics controller display memory data latches. • The number *n* of the display memory data latch that is read back is selected with Graphics Controller register GR4[1:0]. • The graphics controller data latches are loaded whenever display memory is read by the CPU.

9.28 CR24: Attribute Controller Toggle Readback Register

I/O Port Address: 3?5

Index: 24

Bit	Description	Reset State
7	Attribute Controller Data-Index Toggle Readback	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Reserved	
0	Reserved	

This read-only register provides access to the attribute controller toggle readback.

Bit	Description
7	**Attribute Controller Data-Index Toggle Readback:** When this bit is: • 0, on the next access, the attribute controller reads or writes an index value. • 1, on the next access, the attribute controller reads or writes a data value.
6:0	**Reserved**

9.29 CR26: Attribute Controller Index Readback Register

I/O Port Address: 3?5

Index: 26

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Video Enable Status	
4	Attribute Controller Index Readback [4]	
3	Attribute Controller Index Readback [3]	
2	Attribute Controller Index Readback [2]	
1	Attribute Controller Index Readback [1]	
0	Attribute Controller Index Readback [0]	

This read-only register provides access to the current Attribute Controller Index.

Bit	Description
7:6	**Reserved**
5	**Video Enable Status:** This bit provides the status of the Attribute Controller Index register ARX[5].
4:0	**Attribute Controller Index Readback [4:0]:** This field reads back the value in Attribute Controller Index register ARX[4:0].

Notes

10. GRAPHICS CONTROLLER REGISTERS

10.1 GRX: Graphics Controller Index Register

I/O Port Address: 3CE

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Graphics Controller Index [5]	0
4	Graphics Controller Index [4]	0
3	Graphics Controller Index [3]	1
2	Graphics Controller Index [2]	0
1	Graphics Controller Index [1]	0
0	Graphics Controller Index [0]	0

This register is used to specify a particular Graphics Controller register.

Bit	Description
7:6	**Reserved**
5:0	**Graphics Controller Index [5:0]:** This field specifies one of the following: • A register in the Graphics Controller group. • An Extension register that is accessed by the next I/O read or I/O write to I/O port address 3CF.

10.2 GR0: Set / Reset Register

I/O Port Address: 3CF

Index: 0

Bit	Description	Reset State
7	Write Mode 5 Background Color [7] / Reserved	1
6	Write Mode 5 Background Color [6] / Reserved	1
5	Write Mode 5 Background Color [5] / Reserved	1
4	Write Mode 5 Background Color [4] / Reserved	1
3	Write Mode 5 Background Color [3] / Display Memory Plane 3 Set/Reset	1
2	Write Mode 5 Background Color [2] / Display Memory Plane 2 Set/Reset	1
1	Write Mode 5 Background Color [1] / Display Memory Plane 1 Set/Reset	1
0	Write Mode 5 Background Color [0] / Display Memory Plane 0 Set/Reset	1

This register specifies:

- The background color, when Extended Write mode 5 is selected.
- Values to be written into the respective display memory planes, when the processor executes a Write mode 0 or Write mode 3 operation.

For an overview of the Write modes, refer to the description in Graphics Controller register GR5.

Bit	Description
7:0	**Write Mode 5 Background Color [7:0]:** • When Graphics Controller register GR5[2:0] selects Extended Write mode 5, these bits [7:0] specify the background color for Extended Write mode 5.
7:4	**Reserved:** • When Graphics Controller register GR5[2:0] does not select Extended Write mode 5, these bits [7:4] are reserved. • When Extension register GRB[2] is: — 0, writes to these bits are ignored, and reads return zeroes. — 1, these bits are read/write, but bit contents are not used.
3:0	**Display Memory Plane [3:0] Set/Reset:** When Graphics Controller register GR5[2:0] does not select Extended Write mode 5, these bits [3:0] control the values written into the respective display memory planes for Write mode 3 and Write mode 0.

10.3 GR1: Set / Reset Enable Register

I/O Port Address: 3CF

Index: 1

Bit	Description	Reset State
7	Write Mode 4, 5 Foreground Color [7] / Reserved	1
6	Write Mode 4, 5 Foreground Color [6] / Reserved	1
5	Write Mode 4, 5 Foreground Color [5] / Reserved	1
4	Write Mode 4, 5 Foreground Color [4] / Reserved	1
3	Write Mode 4, 5 Foreground Color [3] / Display Memory Plane 3 Set/Reset Enable	1
2	Write Mode 4, 5 Foreground Color [2] / Display Memory Plane 2 Set/Reset Enable	1
1	Write Mode 4, 5 Foreground Color [1] / Display Memory Plane 1 Set/Reset Enable	1
0	Write Mode 4, 5 Foreground Color [0] / Display Memory Plane 0 Set/Reset Enable	1

This register:

- Defines the foreground color when Extended Write mode 4 or 5 is selected.
- Is used with Graphics Controller register GR0 to determine values to be written into the respective display memory planes when Write mode 0 is selected.

For an overview of the Write modes, refer to the description in Graphics Controller register GR5.

Bit	Description
7:0	**Write Mode 4, 5 Foreground Color [7:0]:** These bits specify the foreground color for an Extended Write mode when the mode selected is: • Extended Write mode 4 (Graphics Controller register GR5[2:0] is '100'). • Extended Write mode 5 (Graphics Controller register GR5[2:0] is '101').
7:4	**Reserved:** • When Graphics Controller register GR5[2:0] selects Extended Write mode 4 or 5, these bits [7:4] are reserved. • When Extension register GRB[2] is: — 0, writes to these bits are ignored, and reads return zeroes. — 1, these bits are read/write, but bit contents are not used.
3:0	**Display Memory Plane [3:0] Set/Reset Enable:** When Write mode 0 is selected (Graphics Controller register GR5[2:0] is '000') *and* when a bit in this field is: • 0, the corresponding value from the CPU data bus is written into the corresponding display memory plane. • 1, the corresponding value in Graphics Controller register GR0[3:0] is written into the corresponding display memory plane.

10.4 GR2: Color Compare Register

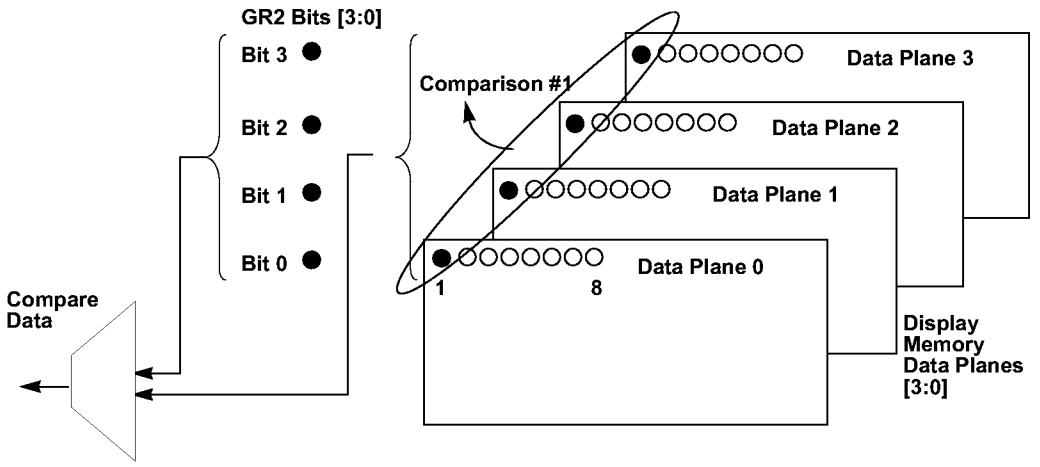
I/O Port Address: 3CF

Index: 2

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Compare Plane [3]	1
2	Color Compare Plane [2]	1
1	Color Compare Plane [1]	1
0	Color Compare Plane [0]	1

This register specifies the color compare plane(s) for Read mode 1.

Bit	Description
7:4	**Reserved**
3:0	**Color Compare Plane [3:0]:** This field represents a color comparison value consisting of 1 to 4 bits. • GR5[3] must be set to 1 (Read mode 1 is selected) to enable this field. • GR7[3:0] bits select display memory data planes for the comparison shown below. • For each selected display memory data plane, the color value of the corresponding bit in this field is compared to the color of the eight neighboring horizontal pixels in the corresponding display memory data plane. (For display memory data planes that are not chosen, their data is forced to match the values of the other data planes, becoming a 'don't care' in the process.) • The 8 bits from the comparison are read into the CPU.



10.5 GR3: Data Rotate Register

I/O Port Address: 3CF

Index: 3

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Logical Function Select [1]	1
3	Logical Function Select [0]	1
2	Data Rotate Count [2]	1
1	Data Rotate Count [1]	1
0	Data Rotate Count [0]	1

This register contains two fields that are used with Write modes 0 and 3.

Bit — **Description**

7:5 — **Reserved**

4:3 — **Logical Function Select [1:0]:**

- This 2-bit field is used for Write mode 0 only (Graphics Controller register GR5[2:0] is '000').
- In addition, this 2-bit field selects the logical function operation that takes place between the data in the CPU data latches and the data from the CPU or Set/Reset Logic. The result of the functional operation is written into display memory.

The logical function operations are summarized in the following table:

GR3		Logical Function Operation
[4]	[3]	
0	0	None: The data in the latches are ignored.
0	1	Data in latches is logically AND'ed with data from CPU or Set/Reset Logic
1	0	Data in latches is logically OR'ed with data from CPU or Set/Reset Logic
1	1	Data in latches is logically XOR'ed with data from CPU or Set/Reset Logic

2:0 — **Data Rotate Count [2:0]:**
This field allows data from the CPU bus to be rotated up to seven bit positions prior to being altered by the Set/Reset logic.

10.6 GR4: Read Map Plane Select Register

I/O Port Address: 3CF

Index: 4

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	Display Memory Data Plane Select [1]	1
0	Display Memory Data Plane Select [0]	1

This register is used to select a display memory data plane for Read mode 0. (For an overview of the Write modes, refer to the description in GR5.)

Bit — **Description**

7:2 — **Reserved**

1:0 — **Display Memory Data Plane Select [1:0]:**

- This field is used only when Read mode 0 is selected (Graphics Controller register GR5[3] is 1).
- This field also specifies the display memory data plane selected for a read by Read mode 0, as shown in the following table:

GR4		Display Memory Data Plane Selected for Read by Read Mode 0
[1]	[0]	
0	0	Display Memory Data Plane 0
0	1	Display Memory Data Plane 1
1	0	Display Memory Data Plane 2
1	1	Display Memory Data Plane 3

10.7 GR5: Mode Register

I/O Port Address: 3CF

Index: 5

Bit	Description	Reset State
7	Reserved	
6	256-Color Mode	1
5	Graphics Data Shift Register Mode	1
4	Odd/Even Addressing Mode	1
3	Read Mode	0
2	Write Mode [2]	0
1	Write Mode [1]	1
0	Write Mode [0]	1

This register specifies the Write mode and Read mode. In addition, it controls the configuration of the graphics data shift registers.

Bit	Description
7	**Reserved**
6	**256-Color Mode:** When this bit is: • 0, graphics data shift registers are configured for 16-, 4-, or 2-color graphics modes. • 1, graphics data shift registers are configured for 256-color graphics modes, and Graphics Controller register GR5[5] is ignored.
5	**Graphics Data Shift Register Mode:** When this bit is: • 0, graphics data shift registers are configured for EGA compatibility. • 1, graphics data shift registers are configured for CGA compatibility, which is used for graphics modes 4h and 5h.
4	**Odd/Even Addressing Mode:** • When this bit is 1, the CL-GD7548 is configured for odd/even addressing mode. • This bit must always be programmed to the opposite value as Sequencer register SR4[2].

10.7 GR5: Mode Register *(cont.)*

Bit **Description**

3 **Read Mode:**
This bit specifies whether the CL-GD7548 is in Read mode 0 or Read mode 1.

GR5[3]	Read Mode	CPU Read Source
0	Read mode 0	CPU reads data directly from display memory
1	Read mode 1	CPU reads data that results from the color-compare logic of GR2

Read Mode 0:

- During Read mode 0, the CPU reads data directly from display memory.
- Read mode 0 returns an adjacent 8 bits of the display memory data plane specified in GR4[1:0].
- Read mode 0 does not use the color-compare logic of Graphics Controller register GR2.
- A Read mode 0 operation can be forced with an I/O read of CRT Controller register CR22.

Read Mode 1:

- During Read mode 1, the CPU reads data that results from the color-compare logic of Graphics Controller register GR2.
- Read mode 1 allows eight adjacent pixels (16-color modes) to be compared to a specified color value in a single operation. Each of the 8 bits returned to the CPU indicates the result of a comparison between the 4 bits of the Color Compare (Graphics Controller register GR2[3:0]) and the bits from the four display memory planes.
- When the 4 bits of the Color Compare operation match the 4 bits from the display memory data planes, a 1 is returned for the corresponding bit position.
- When any bits in the Color Don't Care Plane (Graphics Controller register GR7[3:0]) are zeroes, the value in the corresponding display memory data plane is forced to match the values of the other data planes, becoming a 'don't care' in the process.

10.7 GR5: Mode Register *(cont.)*

Bit **Description**

2:0 **Write Mode Select [2:0]:**
These bits, in combination with Extension register bit GRB[2], specify when the CL-GD7548 is in Write or Extended Write mode. When GRB[2] is:

- 0, GR5[2] is forced to 0.
- 1, GR5[2] is enabled to be written to either 0 or 1.

GRB[2]	GR5			Write Mode Selected
	[2]	[1]	[0]	
When GRB[2] is 0, GR5[2] is forced to 0.	0	0	0	Write mode 0
	0	0	1	Write mode 1
	0	1	0	Write mode 2
	0	1	1	Write mode 3
GRB[2] must be 1 for GR5[2] to be set to 1.	1	0	0	Extended Write mode 4
	1	0	1	Extended Write mode 5
	1	1	0	Reserved
	1	1	1	Reserved

Write Mode 0:

- Each of the four display memory data planes is written with the host CPU data rotated by the number of counts in Graphics Controller register GR3[2:0].
- When Extension register bit SR7[0] is:
  - 0 *and* a bit in Graphics Controller register GR1[3:0] is:
    - 0, the corresponding display memory data plane is written with the contents of the corresponding value from the host CPU.
    - 1, the corresponding display memory data plane is written with the contents of the corresponding bit in GR0[3:0].
  - 1, the corresponding display memory data plane is written with the contents of the corresponding host CPU value, regardless of GR1[3:0].

Write Mode 1:

- Each of the four display memory data planes is written with data in CPU data latches, loaded from display memory by a previous read.
- Write mode 1 ignores Graphics Controller register GR8.

Write Mode 2:

- Display memory data planes [3:0] are written with CPU data bit values [3:0].
- Bit planes are enabled with Sequencer register SR2[3:0].
- Bit positions are enabled with Graphics Controller register GR8.
- Write mode 2 ignores the data rotator, set/reset, and function-select fields.

10.7 GR5: Mode Register *(cont.)*

Bit	Description
2:0 *(cont.)*	**Write Mode 3:** • Display memory plane data comes from corresponding bits of GR0[3:0]. • The bit-position-enable field is formed with the logical AND of Graphics Controller register GR8 and the rotated CPU data. • Write mode 3 ignores the set/reset and function-select fields. **Extended Write Mode 4:** • The contents of Graphics Controller register GR1[7:0] are written into up to eight adjacent pixels. • The CPU data bits are used to control whether a pixel is written. — When a CPU data bit is a 0, the corresponding pixel is not changed. — When a CPU data bit is a 1, the corresponding pixel is written. • This mode can be used for 256-color text expansion for which the background is to be preserved. • This mode can also be used for 64K-color text expansion for which the background is to be preserved. **Extended Write Mode 5:** • The contents of either Graphics Controller register GR1[7:0] or GR0[7:0] are written into each of eight adjacent pixels. • For each of the eight pixels, the choice between GR1 and GR0 is made according to the value of the corresponding bit of the CPU data, summarized in the following table.

CPU Data	GR0 / GR1	Note
0	GR0	Background
1	GR1	Foreground

• This mode is intended for 256-color text expansion, for which both the foreground and background are to be written.
• This mode can also be used for 64K-color text expansion for which both the foreground and background are to be written.

10.8 GR6: Miscellaneous Register

I/O Port Address: 3CF

Index: 6

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Display Memory Map [1]	1
2	Display Memory Map [0]	1
1	Chain Odd Maps to Even	1
0	Graphics Mode	1

This register contains miscellaneous control bits.

Bit — **Description**

7:4 **Reserved**

3:2 **Display Memory Map [1:0]:**
This field specifies the beginning address and size of the display memory in the CPU host address space. This field is summarized in the following table:

GR6 [3]	GR6 [2]	Display Memory Map Plane	Display Memory Address in CPU Host Address Space	Display Memory Size (Kbytes)	Affected Mode(s)
0	0	0	A000:0 to BFFF:F	128	Extended
0	1	1	A000:0 to AFFF:F	64	EGA / VGA
1	0	2	B000:0 to BFFF:F	32	Hercules
1	1	3	B800:0 to BFFF:F	32	CGA

1 **Chain Odd Maps to Even:**
- When this bit is 1, CPU Address Bit[0] is replaced with a higher-order address bit. This replacement causes the even host addresses to access Planes 0 and 2, and the odd host addresses to access Planes 1 and 3.
- This mode is useful for MDA emulation.

0 **Graphics Mode Enable:**
When this bit is:
- 0, the CL-GD7548 functions in text (alphanumeric) modes.
- 1, the CL-GD7548 functions in graphics (all-points-addressable) modes.

10.9 GR7: Color Don't-Care Plane Register

I/O Port Address: 3CF

Index: 7

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Don't-Care Plane [3]	1
2	Color Don't-Care Plane [2]	1
1	Color Don't-Care Plane [1]	1
0	Color Don't-Care Plane [0]	1

This register is used with Graphics Controller register GR2 for Read mode 1 accesses. (For an overview of the Read modes, refer to the description in Graphics Controller register GR5.)

Bit	Description
7:4	**Reserved**
3:0	**Color Don't-Care Plane [3:0]:** These 4 bits are used to control color compare logic for the four Color Don't-Care Planes. If a bit is: • 0, the corresponding plane is not involved in color compares. • 1, the corresponding plane is involved in color compares.

10.10 GR8: Display Memory Bit Mask Register

I/O Port Address: 3CF

Index: 8

Bit	Description	Reset State
7	Display Memory Bit Write Enable [7]	1
6	Display Memory Bit Write Enable [6]	1
5	Display Memory Bit Write Enable [5]	1
4	Display Memory Bit Write Enable [4]	1
3	Display Memory Bit Write Enable [3]	1
2	Display Memory Bit Write Enable [2]	1
1	Display Memory Bit Write Enable [1]	1
0	Display Memory Bit Write Enable [0]	1

This register is used to control writing to display memory on a bit basis in Write modes 0, 2, and 3.

Bit	Description
7:0	**Display Memory Bit Write Enable [7:0]:** Each bit in this register controls whether the corresponding bit in display memory is written in Write modes 0, 2, or 3. When a bit is: • 0, the corresponding bit in display memory is not written. • 1, the corresponding bit in display memory is written.

11. ATTRIBUTE CONTROLLER REGISTERS

11.1 ARX: Attribute Controller Index Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: (n/a)

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	AR11 Video Source Enable	0
4	Attribute Controller Index [4]	0
3	Attribute Controller Index [3]	0
2	Attribute Controller Index [2]	0
1	Attribute Controller Index [1]	0
0	Attribute Controller Index [0]	0

This register is used to specify the register in the Attribute Controller block that is accessed with the next I/O write to 3C0 or I/O read to 3C1.

For the Attribute Controller block, both the index and data registers are at the same port addresses, unlike other blocks, for which index and data registers are at different port addresses.

Alternate writes to ARX toggle between index and data. The CRT Controller register CR24 provides access to the Attribute Controller Toggle, which reads or writes either a data value or an index value.

Bit	Description
7:6	**Reserved**
5	**AR11 Video Source Enable:** When this bit is: • 0, the screen displays the color in Attribute Controller register AR11. • 1, the screen displays normal video.
4:0	**Attribute Controller Index [4:0]:** This field is the index to the Attribute Controller data registers. When CRT Controller register CR24[7] is 0, the CRT Controller register bits CR26[4:0] read back the bits in ARX[4:0].

11.2 AR0–ARF: Attribute Controller Palette Registers

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 0:F

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Secondary Red	1
4	Secondary Green / Intensity	1
3	Secondary Blue / Monochrome	1
2	Red	1
1	Green	1
0	Blue	1

These bits act as pointers to palette entries.

Bit	Description
7:6	**Reserved**
5:0	**Palette Entries:** In 16-color text and graphics modes, the digital attribute controller palette entries in this register are chosen by the 4 bits of pixel data, and they point to palette memory entries. • The palette memory entries are normally programmed, and so the DAC outputs reflect these values. • As a result, palette memory is programmed to simulate standard EGA colors.

11.3 AR10: Attribute Controller Mode Control Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 10

Bit	Description	Reset State
7	AR14 Video Source Enable	0
6	Pixel Double-Clock Select	0
5	Pixel Panning Compatibility	0
4	Reserved	
3	Character Blink Enable	0
2	Line Graphics Enable	0
1	Display Type	0
0	Graphics Mode	0

This register contains some miscellaneous control bits for the Attribute Controller.

Bit	Description
7	**AR14 Video Source Enable:** • When an 8-, 16-, or 24-bit pixel mode is chosen, this bit is ignored. • When this bit is: — 0, Attribute Controller registers AR0 to ARF[5:4] are the source for CLUT address bits [5:4]. — 1, Attribute Controller register bits AR14[1:0] are the source for CLUT address bits [5:4], which allows rapid selection of four 16-color palettes.
6	**Pixel Double-Clock Select:** When this bit is: • 0, pixels are clocked on every cycle. • 1, pixels are clocked on every other clock cycle. Also: — Registers AR0 to ARF are bypassed. — This bit setting is used with graphics mode 13h. — The CL-GD7548 sequencer logic operates at twice the pixel clock rate.
5	**Pixel Panning Compatibility:** When this bit is: • 0, the two parts of a split screen pan together. • 1, a line compare match in the CRTC forces the output of the AR13 Pixel Panning register to a 0 until the next VSYNC occurs. This action allows the panning of Screen A without Screen B.
4	**Reserved**
3	**Character Blink Enable:** When this bit is: • 0, character blinking is disabled • 1, character blinking is enabled at the frequency rate of vertical refresh, divided by 32.

11.3 AR10: Attribute Controller Mode Control Register *(cont.)*

Bit | **Description**

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2 — **Line Graphics Enable:**
When this bit is:
- 0, bit 9 of a 9-bit-wide character cell is the same as the background.
- 1, bit 9 of a 9-bit-wide character cell is made the same value as bit 8. This value is used for those character sets that have special characters associated with line graphics, for characters codes in the range C0 through DF.

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1 — **Display Type:**
This bit is used only if the CL-GD7548 is in alphanumeric modes. When this bit is:
- 0, the Attribute Byte contents are treated as color attributes.
- 1, the Attribute Byte contents are treated as MDA-compatible attributes.

The following table shows examples of monochrome attributes.

Bit Definitions for Attribute Byte								Hex Code of Attribute Byte	Monochrome Attribute Byte
Blink Bit	Background Bits			Intensity Bit	Foreground Bits				
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]		
0	0	0	0	0	1	1	1	07h	Normal
0	0	0	0	1	1	1	1	0Fh	Intense
0	0	0	0	0	0	0	1	01h	Underline
0	0	0	0	1	0	0	1	09h	Underline Intense
0	1	1	1	0	0	0	0	70h	Reverse
1	1	1	1	0	0	0	0	F0h	Blinking Reverse

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0 — **Graphics Mode Enable:**
When this bit is:
- 0, the Attribute Controller functions in text (alphanumeric) modes.
- 1, the Attribute Controller functions in graphics (all-points-addressable) modes.

11.4 AR11: Overscan (Border) Color Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 11

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	(Border Color Bit) Secondary Red	0
4	(Border Color Bit) Secondary Green	0
3	(Border Color Bit) Secondary Blue	0
2	(Border Color Bit) Red	0
1	(Border Color Bit) Green	0
0	(Border Color Bit) Blue	0

This register points to the entry in the CLUT that defines the border color.

- As shown in Figure 9-1 at the description of CRT Controller register CR0 in Chapter 9, the border is defined as that portion of the raster between blanking and active video, on all four sides of the screen.
- Typically, the CLUT entries are programmed, and so the color defined by the bits above is the color that results.

Bit	Description
7:6	**Reserved**
5:0	**Border Color Bits [5:0]:** Depending on if the CGA or EGA mode is in use, either four of these bits (for CGA) or six of these bits (for EGA) are used to select the CLUT entry for the border color in CGA and EGA modes.

11.5 AR12: Color Plane Enable Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 12

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Video Status Multiplexor [1]	1
4	Video Status Multiplexor [0]	1
3	Color Plane Enable [3]	1
2	Color Plane Enable [2]	1
1	Color Plane Enable [1]	1
0	Color Plane Enable [0]	1

This register contains:

- One field that chooses the inputs for diagnostic bits in External/General register STAT[5:4].
- Another field that enables the 4 color planes in the Attribute Controller Palette registers.

Bit	Description
7:6	**Reserved**
5:4	**Video Status Multiplexor [1:0]:** This field chooses the inputs for the diagnostic status bits in External/General register STAT[5:4] as indicated in the following table:

AR12		STAT	
[5]	[4]	[5]	[4]
0	0	Pixel Bus bit [2] Red	Pixel Bus bit [0] Blue
0	1	Pixel Bus bit [3] Secondary Blue	Pixel Bus bit [1] Green
1	0	Pixel Bus bit [5] Secondary Red	Pixel Bus bit [4] Secondary Green
1	1	Pixel Bus bit [7]	Pixel Bus bit [6]

11.5 AR12: Color Plane Enable Register *(cont.)*

Bit	Description
3:0	**Color Plane Enable [3:0]:** This field controls which display memory data plane sends data to a corresponding attribute controller color palette register, as shown in the following table:

AR12 Bit / State	Display Memory Data Plane	Result
AR12[3] is 0	Plane 3	Plane 3 disabled.
AR12[3] is 1		Plane 3 data selected for Color Palette register 3.
AR12[2] is 0	Plane 2	Plane 2 disabled.
AR12[2] is 1		Plane 2 data selected for Color Palette register 2.
AR12[1] is 0	Plane 1	Plane 1 disabled.
AR12[1] is 1		Plane 1 data selected for Color Palette register 1.
AR12[0] is 0	Plane 0	Plane 0 disabled.
AR12[0] is 1		Plane 0 data selected for Color Palette register 0.

11.6 AR13: Pixel Panning Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 13

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Pixel Panning [3]	1
2	Pixel Panning [2]	1
1	Pixel Panning [1]	1
0	Pixel Panning [0]	1

This register:

- Specifies the number of pixels the display data are shifted to the left.
- Functions both in the graphics (all-points-addressable) and text (alphanumeric) modes.

Bit	Description
7:4	**Reserved**
3:0	**Pixel Panning [3:0]:** This field controls fine panning on a pixel-by-pixel basis by specifying the number of pixels the display data are shifted to the left. The values programmed into AR13[3:0] are interpreted as indicated in the following table:

AR13				Hex Code	Shift for 9-Bit Characters	Shift for 8-Bit Characters	Shift for Video Mode 13h
[3]	[2]	[1]	[0]				
0	0	0	0	0h	1 bit left	No shift	No shift
0	0	0	1	1h	2 bits left	1 bit left	–
0	0	1	0	2h	3 bits left	2 bits left	1 bit left
0	0	1	1	3h	4 bits left	3 bits left	–
0	1	0	0	4h	5 bits left	4 bits left	2 bits left
0	1	0	1	5h	6 bits left	5 bits left	–
0	1	1	0	6h	7 bits left	6 bits left	3 bits left
0	1	1	1	7h	8 bits left	7 bits left	–
1000 to 1111				8h - Fh	No shift	1 bit right	–

11.7 AR14: Color Select Register

I/O Port Address: 3C0 (Write) 3C1 (Read)

Index: 14

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Color Bit C [7]	0
2	Color Bit C [6]	0
1	Color Bit C [5]	0
0	Color Bit C [4]	0

This register contains two fields that are involved in the selection of addresses into the CLUT.

Bit	Description
7:4	**Reserved**
3:2	**Color Bits C [7:6]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • These 2 bits are concatenated with the 6 bits from the Attribute Controller Palette registers AR0 to ARF to form the address into the CLUT.
1:0	**Color Bits C [5:4]:** • In 8-, 16-, and 24-bit pixel modes, these bits are ignored. • When AR10[7] is: — 0, these 2 bits are ignored. — 1, these 2 bits replace the corresponding 2 bits from the Attribute Controller Palette registers AR0 to ARF to form the address into the CLUT.

12. EXTENSION REGISTERS

12.1 SR6: Unlock All Extension Registers

I/O Port Address: 3C5

Index: 6

Bit	Description	Reset State
7	Not Used	Not applicable
6	Not Used	Not applicable
5	Not Used	Not applicable
4	Unlock All Extension Registers	0
3	Not Used	Not applicable
2	Unlock All Extension Registers	1
1	Unlock All Extension Registers	1
0	Unlock All Extension Registers	1

This register is used to enable or disable access to the CL-GD7548 Extension registers.

Bit	Description
7:5, 3	**Not Used**
4, 2:0	**Unlock All Extension Registers (Access Value):** All Extension registers are: • Unlocked (enabled) for read/write access when bits 4, 2:0 equal the following: — Bit 4 = 0 — Bit 2 = 1 — Bit 1 = 1 — Bit 0 = 1 • Locked (disabled) for read/write access when bits 4, 2:0 are any other value other than the ones shown above.

12.2 SR7: Extended Sequencer Mode Register

I/O Port Address: 3C5

Index: 7

Bit	Description	Reset State
7	Display Memory Segment Select [3]	0
6	Display Memory Segment Select [2]	0
5	Display Memory Segment Select [1]	0
4	Display Memory Segment Select [0]	0
3	Reserved	
2	CRT Controller Character Clock Divider [1] Select	1
1	CRT Controller Character Clock Divider [0] Select	1
0	High-Resolution Packed-Pixel Mode Select	1

This register has several purposes which are described in the following bit descriptions.

Bit	Description
7:4	**Display Memory Segment Select [3:0]:** When the value of this 4-bit field is programmed to: • '0000': — The CL-GD7548 is configured for standard VGA display memory addressing, responding to memory accesses at Axxx:x, or Bxxx:x, or both, as specified by Graphics Controller register bits GR6[3:2]. • Other than '0000': — The CL-GD7548 is configured for 1-Mbyte linear memory addressing. — The CL-GD7548 responds to any memory access where CPU address bits A[23:20] match this field value. • Other than '0000' *and*: — When there is a full 1 Mbyte of display memory installed, *and* the CL-GD7548 is configured for extended 256-color chain-4, then the 1-Mbyte address range has one-to-one mapping to the 1 Mbyte of installed display memory. — When the CL-GD7548 is configured for unchained, ×8, or ×16 addressing, then it responds to the entire 1-Mbyte range, but address wrapping takes place. — Extension register GRB[5] is programmed to a 1, then SR7[4] becomes a 'don't-care' bit, and the CL-GD7548 responds to a 2-Mbyte address.
3	**Reserved**

12.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit	Description
2:1	**CRT Controller Character Clock Divider Select [1:0]:** This field selects how the CRTC Character Clock is divided down, resulting in various pixel data rates, as indicated in the following table:

SR7		Resulting Pixel Data
[2]	[1]	
0	0	8 bit/pixel data with 1× VCLK (CRTC Character Clock is not divided down.) (Normal operation.)
0	1	16 bit/pixel data with 2× VCLK (CRTC Character Clock ÷ 2)
1	0	24 bit/pixel data with 3× VCLK (CRTC Character Clock ÷ 3)
1	1	16 bit/pixel data with 1× VCLK (CRTC Character Clock is not divided down.)

16-Bit/Pixel Data with 2× VCLK (SR7[2:1] is 01)
When this mode is selected:
- The DAC and the Video Shift register are clocked at the VCLK data byte rate.
- The CRTC is clocked with a character clock of 8 pixels (16 VCLKs).

The above clocking allows:
- The CRTC timing value for 640 × 480 modes and 800 × 600 modes with 16-bit pixels to be programmed in units of an 8-pixel character clock.
- CRT Controller register CR13 to be set to:
  — A0h for 640 × 480 mode
  — C8h for 800 × 600 mode
- The hardware cursor horizontal position to be set in pixel units.
- The Cursor Data Invert function to operate on 15-, 16-, or 18-bit RGB data presented to the DAC.

24-Bit/Pixel Data with 3× VCLK (SR7[2:1] is 10)
When this mode is selected:
- The DAC and the Video Shift register is clocked at the VCLK data byte rate.
- The CRTC is clocked with a character clock of 8 pixels (24 VCLKs).

The above clocking allows:
- The CRTC timing value for 640 × 480 modes with 24-bit pixels to be programmed in units of an 8-pixel character clock.
- CRT Controller register CR13 to be set to F0h.

The hardware cursor is not supported in this configuration.

12.2 SR7: Extended Sequencer Mode Register *(cont.)*

Bit	Description
2:1 *(cont.)*	**Select CRTC Character Clock Divider [1:0]** *(cont.)*: **16-Bit/Pixel Data with 1× VCLK (SR7[2:1] is 11)** When this mode is selected: • The sequencer provides 16-bit data to the palette DAC at the displayed pixel rate. This action allows RGB 5-5-5 color modes to be selected with a 1× VCLK. • The data output on the FCP[7:0] pins is only the low byte of the pixel data. (In this case, the high byte of the pixel data is not available externally.) • This mode also provides for 1024 × 768 display modes, with RGB 5-5-5 color modes, and with VCLK equal to the pixel rate.
0	**High-Resolution Packed-Pixel Mode Select:** When this bit is 1: • The CL-GD7548 video shift registers are configured so that one character clock equals 8 pixels. • True packed-pixel memory addressing is enabled. • This mode may be used with 16- and 24-bit pixel modes. (Refer to SR7[2:1].) • This mode may not be used with Graphics Display mode 13h, which is packed pixel, but not high resolution. (For the high-resolution Graphics Display mode 13h, set Attribute Controller register AR10[6] to 1.) **NOTE:** In true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. In contrast, with chain-4 addressing, consecutive pixels are stored at every fourth address in display memory. • Graphics Controller registers GR0 and GR1: — Function as color registers only — Have their set/reset function for display memory disabled • Writes from write mode 0 write the CPU data, regardless of the state of Graphics Controller register bits GR1[3:0].

12.3 SR8: Miscellaneous Control Register 1

I/O Port Address: 3C5

Index: 8

Bit	Description	Access	Reset State
7	DDCD Output Status	R	0
6	DDCC/DDCD Pinout Configuration	R/W	0
5	Reserved		
4	Reserved		
3	Dynamic CPU Cycle Termination Enable	R/W	0
2	DDCC Output Status	R	0
1	DDCD Output Control	R/W	0
0	DDCC Output Control	R/W	0

Bit	Description
7	**DDCD Output Status:** If the FCPU pin is low, *and* the ACTI / DDCD / FCEVIDEO# / SBYI pin is configured for DDCD (that is, Extension register CR50[3] is 1), *and* this bit is: • 0, the DDCD pin output is low. (That is, a peripheral on the bus is pulling down the DDCC signal, as reflected in this bit state). • 1, the DDCD pin output is high. (That is, on the bus there is no peripheral. Instead, an external pull-up resistor is driving the bus high).
6	**DDCC/DDCD Pinout Configuration:** When the FCPU pin is low *and* this bit is: • 0: — The DDCC / FCDCLK / VCLK pin is configured for either FCDCLK or VCLK, depending on the settings described under Extension register bits SR23[4] and SR24[4]. — The ACTI / DDCD / FCEVIDEO# / SBYI is configured for ACTI, FCEVIDEO#, or SBYI, depending on the settings described under Extension register bit SR23[6]. • 1 (*or* Extension register bit CR50[3] is 1): — The DDCC / FCDCLK / VCLK is configured for DDCC. — The ACTI / DDCD / FCEVIDEO# / SBYI is configured for DDCD.
5:4	**Reserved**

12.3 SR8: Miscellaneous Control Register 1 *(cont.)*

Bit	Description
3	**Dynamic CPU Cycle Termination Enable:** When a CRT memory cycle request is present *and* when this bit is: • 1, the CPU cycle is forced to end when CAS# completes, even if the CPU Write Buffer is not empty and remaining CPU accesses were paged. — Setting this bit to 1 reduces the delay from a CRT memory cycle request to the start of a CRT memory cycle, allowing CRT modes to still run even when memory bandwidth is marginal. — This bit must be set to 1 only for those graphics modes in which extra memory bandwidth is needed to run the CRT mode. • 0, the CPU cycle completes only when the CPU Write Buffer becomes empty (as long as remaining CPU accesses were paged).
2	**DDCC Output Status:** If the FCPU pin is low, *and* the DDCC / FCDCLK / VCLK pin is configured for DDCC (that is, Extension register CR50[3] is 1), *and* this bit is: • 0, the DDCC pin output is low. (That is, a peripheral on the bus is pulling down the DDCC signal, as reflected in this bit state.) • 1, the DDCC pin output is high. (That is, on the bus there is no peripheral. Instead, an external pull-up resistor is driving the bus high.)
1	**DDCD Output Control:** If the FCPU pin is low and the ACTI / DDCD / FCEVIDEO# / SBYI pin is configured for DDCD (that is, Extension register CR50[3] is 1), *and* the CL-GD7548: • Is in Suspend mode, the DDCD pin output is tristate. • Is not in Suspend mode *and* this bit is: — 0, the DDCD pin output is low (0) — 1, the DDCD pin output is tristate
0	**DDCC Output Control:** If the FCPU pin is low and the DDCC / FCDCLK / VCLK pin is configured for DDCC (that is, Extension register CR50[3] is 1), *and* the CL-GD7548: • Is in Suspend mode, the DDCD pin output is tristate. • Is not in Suspend mode *and* this bit is: — 0, the DDCC pin output is low (0) — 1, the DDCC pin output is tristate

12.4 SR9, SRA: Scratchpad 0 and 1 Registers

I/O Port Address: 3C5

Index: 9, A

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD7548 BIOS and must never be written by any application program. They are listed here only for completeness.

Bit	Description
7:0	**Reserved:** These bits are reserved for the Cirrus Logic BIOS.

12.5 SRB, SRC, SRD, SRE: VCLK0,1,2,3 Numerator Registers

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description	Access	Reset State
7	Reserved		
6	VCLK Numerator [6]	R/W	See the following table
5	VCLK Numerator [5]	R/W	See the following table
4	VCLK Numerator [4]	R/W	See the following table
3	VCLK Numerator [3]	R/W	See the following table
2	VCLK Numerator [2]	R/W	See the following table
1	VCLK Numerator [1]	R/W	See the following table
0	VCLK Numerator [0]	R/W	See the following table

These registers are used in combination with Extension registers SR1B to SR1E to establish the frequency of the four possible video clocks. The video clock used is selected by External/General register MISC[3:2].

This register establishes the numerator value. For information on denominator and post-scalar values, refer to Section 12.17. For more information on clock options, refer to Appendix G.

Each video clock frequency is determined by the following equation.

$$VCLKn\ (\text{MHz}) = \frac{OSC \times NR}{DR \times [P+1]}$$

Equation 12-1

where:

VCLK n	=	Video clock frequency n, where n = 0, 1, 2, 3
OSC	=	Input clock frequency of 14.318 MHz
Numerator **R**egister	=	Value of register bits SRi [6:0], where i = B, C, D, E
Denominator **R**egister	=	Value of register bits SR1i [5:1], where i = B, C, D, E
Post-scalar	=	Value of register bits SR1i [0], where i = B, C, D, E

If n = 0, then i = B.
If n = 1, then i = C.
If n = 2, then i = D.
If n = 3, then i = E.

The following table shows the reset values of the registers that determine the video clock frequency. The table also shows the corresponding video clock frequency at system reset.

12.5 SRB, SRC, SRD, SRE: VCLK0,1,2,3 Numerator Registers *(cont.)*

VCLKn and Reset Frequency		VCLKn Numerator Values			VCLKn Denominator Values			
Clock VCLKn	VCLKn Frequency at Reset	Numerator Register and Hex Value in Register		*NR* = Value Used in Equation Numerator	Denominator Register and Hex Value in Register		*DR* = Value Used in Equation Denominator, Resulting from Post-scalar	*P* = Post-scalar Value Used in Equation Denominator
	MHz	Register (SRi)	Hex	Decimal Equivalent of Hex Value	Register (SRi)	Hex	Decimal	Decimal
VCLK0	25.180	SRB	66h	102	SR1B	3Bh	29	1
VCLK1	28.325	SRC	5Bh	91	SR1C	2Fh	23	1
VCLK2	41.165	SRD	45h	69	SR1D	30h	24	0
VCLK3	36.082	SRE	7Eh	126	SR1E	33h	25	1

Bit	Description
7	**Reserved**
6:0	**VCLK Numerator [6:0]:** These bits determine the numerator value (*N*) used to select the video clock frequency.

12.6 SRF: Display Memory Control Register

I/O Port Address: 3C5

Index: F

Bit	Description	Reset State
7	Display Memory Bank Select	0
6	CPU-Write FIFO Fast-Page-Detection Mode Disable	0
5	CRT FIFO Depth Control	0
4	Display Memory Data Bus Width [1]	0
3	Display Memory Data Bus Width [0]	1
2	Display Memory RAS# Cycle 6- or 7-MCLK Select	1
1	Reserved	
0	Display Memory Multiple-CAS# / Multiple-WE# Select	1

This register is used to control the display memory.

Bit	Description
7	**Display Memory Bank Select:** • This bit is used with SRF[4:3] to specify the display memory data bus width according to the number of banks of display memory used. • When this bit is: — 0, the CL-GD7548 is configured for one bank of display memory (four 512K × 8 DRAMs, or two 256K × 16 DRAMs). — 1, the CL-GD7548 is configured for two banks of display memory (four 256K × 16 DRAMs).
6	**CPU Write FIFO Fast-Page-Detection Mode Disable:** • To avoid CPU write buffer under-runs, this bit *must* be programmed to 1, either when loading text data for page-mode access, or when performing multiple color-expand writes in 16-bit pixel modes. • When this bit is: — 0, consecutive CPU writes to display memory are executed as fast-page mode writes, whenever possible. — 1, CPU writes to display memory take place as random cycles.

Continued

12.6 SRF: Display Memory Control Register *(cont.)*

Bit	Description
5	**CRT FIFO Depth Control:** • This bit is used in combination with Extension register SR20[2] to control the CRT FIFO write buffer depth as well as when the CRT FIFO is requested, as shown in the table below. • If both SR20[2] and SRF[5] are set to 1, then Extension register bits SR33[3:0] are used to extend the programming for the CRT FIFO.

SR20[2]	SRF[5]	CRT FIFO Depth that Results from CRT FIFO Request	When CRT FIFO Request Is Generated
0	0	8 levels deep x 32 bits wide	These bit settings must be used with Text modes.
0	1	20 levels deep x 32 bits wide	These bit settings are used when the CRT FIFO is less than 100% full.
1	0	20 levels deep x 32 bits wide	These bit settings are used when the CRT FIFO is either 50% full or less than 50% full.
1	1	20 levels deep x 32 bits wide	These bit settings are used in combination with Extension register SR33[3:0] to program the threshold for when to empty the CRT FIFO.

Continued

12.6 SRF: Display Memory Control Register *(cont.)*

Bit **Description**

4:3 **Display Memory Data Bus Width [1:0]:**
This 2-bit field is used with SRF[7] to specify the display memory data bus width according to the following table:

SRF			Display Memory Data Bus Width	Memory Organization	Total Memory
[7]	[4]	[3]			
0	0	0	–	Reserved	Reserved
0	0	1	–	Reserved	Reserved
0	1	0	32 bits wide	Two 256K × 16 DRAMs	1 Mbyte
				Four 512K × 8 (symmetric) DRAMs	2 Mbytes
0	1	1	–	Reserved	Reserved
1	1	0	32 bits wide	Four 256K × 16 DRAMs (two banks)	2 Mbytes
1	1	1	–	Reserved	Reserved

These bits have one level of buffering. At the end of each horizontal scanline refresh interval (that is, when horizontal blanking begins), the state of each of these bits is transferred to the timing logic. This transfer avoids changing the timing logic in the middle of a scanline.

2 **Display Memory RAS# Cycle 6- or 7-MCLK Select**:
To achieve optimal performance, the display memory RAS# cycle timing must match the total number of MCLKs used.

- This bit selects a display memory RAS# cycle that is either 6 or 7 MCLKs long, as shown in the table that follows.
- The default is a display memory RAS# cycle of 6 MCLKs.
- For a display memory RAS# cycle that is longer than 7 MCLKs, refer to Extension register SR20[6].

SRF[2]	Length of RAS# Cycle	Type of RAS Cycle
0 (default)	7 MCLKs	3 MCLKs high and 4 MCLKs low
1	6 MCLKs	2.5 MCLKs high and 3.5 MCLKs low

1 **Reserved**

0 **Display Memory Multiple-CAS# / Multiple-WE# Select:**

- A 0 selects multiple-WE# display memory support.
- A 1 selects multiple-CAS# display memory support, which is the default.

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Reset State
7	HW Cursor and HW Icon Coarse Horizontal Position [10]	0
6	HW Cursor and HW Icon Coarse Horizontal Position [9]	0
5	HW Cursor and HW Icon Coarse Horizontal Position [8]	0
4	HW Cursor and HW Icon Coarse Horizontal Position [7]	0
3	HW Cursor and HW Icon Coarse Horizontal Position [6]	0
2	HW Cursor and HW Icon Coarse Horizontal Position [5]	0
1	HW Cursor and HW Icon Coarse Horizontal Position [4]	0
0	HW Cursor and HW Icon Coarse Horizontal Position [3]	0

This register, and the Sequencer register index bits SRX[7:5] that are used to access it, is used to define in character clocks the coarse horizontal (X) pixel offset of the graphics hardware cursor and icon. For more information on the hardware cursor and icon, refer to both Appendix B and Appendix C.

For all 8-bit text modes and non-expanded graphics modes and text modes which do not require the fourth expansion bit, the entire 12-bit cursor or icon horizontal position can be written in a single 16-bit I/O write as follows:

- Extension register bits SR2A[6] and SR2E[0], which are cleared to 0, are ignored.
- The offset must be placed in AX[15:5].
- AX[4:0] must be '10000'.
- DX must be 3C4h.

When 10, 30, 50...F0 is written to 3C4h without writing to 3C5h (a byte write), then a read of 3C4h returns the previously stored three bits of the cursor or icon position.

NOTE: Changes programmed in register SR10 do not take effect until register SR11 has been written.

Bit	Description
7:0	**Hardware Cursor and Hardware Icon Coarse Horizontal Position [10:3]:** Extension register SR12[3] selects whether the value in this register refers to the hardware cursor or the hardware icon. Cursor 12-bit horizontal position • When Extension register SR12[3] is 0, the hardware cursor is selected. • SR10[7:0] are the most-significant 8 coarse horizontal position bits. • Sequencer register bits SRX[7:5] are the least-significant 3 fine horizontal position bits, defined in dot clocks. • Extension register bit SR2E[0] extends the cursor fine horizontal position by one most-significant bit for horizontally expanded graphics modes. This extra bit is valid only with a 10-dot character clock. • For text modes and Graphics mode 13h, the hardware cursor is not available.

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position *(cont.)*

Bit	Description
7:0 *(cont.)*	**HW Cursor and HW Icon Coarse Horizontal Position [10:3]** *(cont.)*:

Icon 12-bit Horizontal Position

- When Extension register SR12[3] is 1, the hardware icon is selected.
- Bits SR10[7:0] form the upper-eight bits of the 11-bit icon horizontal offset.
- Sequencer register bits SRX[7:5] form the lower-three bits of the 11-bit icon horizontal offset.
- Extension register bit SR2A[6] is bit 4 of a dot-clock-level delay used with 9-dot or 10-dot text modes, when in text or horizontally expanded graphics modes.
- The icon is supported in all modes, except interlaced, 24 bpp with 3× clock, and 16 bpp with 2× clock. (The latter does not support horizontal doubling.)

To program the horizontal position of the hardware icon:

1. Place the icon hot point (top left) at pixel n (with 0 as the first pixel).
2. Program the coarse horizontal position as: Integer [(n + (k – 1)) ÷ k]. (k = the number of dots in a character clock.)
3. Program the fine horizontal position as: Remainder [(n + (k – 1)) ÷ k].

For example, to place the icon:

- At pixel 10, which is 11 pixels from the left (that is, n = 10),
- With an 8-dot character clock, as in graphics mode 12h (that is, k = 8),

Then program:

- The coarse position = Integer [(10 + (8 – 1)) ÷ 8] = Integer [17 ÷ 8] = 2h
- The fine position = Remainder [17 ÷ 8] = 1h

12.7 SR10: Hardware Cursor and Hardware Icon Coarse Horizontal Position *(cont.)*

Bit **Description**

7:0 *(cont.)* **HW Cursor and HW Icon Coarse Horizontal Position [10:3]** *(cont.)*:

An example of programming for an 8-dot character clock is in the table below.

Pixel Position	Horizontal Position Programmed	
	Coarse	Fine
0	0	7
1	1	0
2	1	1
3	1	2
4	1	3
5	1	4
6	1	5
7	1	6
8	1	7
9	2	0
10	2	1

There are only three cases of character clock width.

- 10 dots — used for text and graphics expansion on 800 × 600 LCD
- 9 dots — used for text on 800 × 600 and 1024 x 768 LCDs, when 720 dots are displayed
- 8 dots — used in all other cases

12.8 SR11: Hardware Cursor and Hardware Icon Coarse Vertical Position

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Reset State
7	HW Cursor and HW Icon Coarse Vertical Position [10]	0
6	HW Cursor and HW Icon Coarse Vertical Position [9]	0
5	HW Cursor and HW Icon Coarse Vertical Position [8]	0
4	HW Cursor and HW Icon Coarse Vertical Position [7]	0
3	HW Cursor and HW Icon Coarse Vertical Position [6]	0
2	HW Cursor and HW Icon Coarse Vertical Position [5]	0
1	HW Cursor and HW Icon Coarse Vertical Position [4]	0
0	HW Cursor and HW Icon Coarse Vertical Position [3]	0

This register, and the Sequencer register index bits SRX[7:5] that are used to access it, is used to define in scanlines the coarse vertical (Y) scanline offset of the graphics hardware cursor and icon. For more information on the hardware cursor and icon, refer to Appendix B and Appendix C.

The entire 11-bit cursor or icon vertical position can be written in a single 16-bit I/O write as follows:

- The offset must be placed in AX[15:5].
- AX[4:0] must be '10001'.
- DX must be 03C4h.

When 11, 31, 51...F1 is written to 3C4h without writing to 3C5h (a byte write), then a read of 3C4h returns the previously stored three bits of the cursor or icon vertical position.

Bit	Description
7:0	**Hardware Cursor and Hardware Icon Coarse Vertical Position [10:3]:** Extension register SR12[3] selects whether the value in this register refers to the hardware cursor or the hardware icon. Cursor and icon 11-bit vertical position: • When SR12[3] is: — 0, the hardware cursor is selected. — 1, the hardware icon is selected. • SR11[7:0] are the upper 8 coarse vertical position bits. • Sequencer register bits SRX[7:5] are the lower 3 fine vertical position bits, defined in scanlines.

12.9 SR12: Video Data Path Control Register

I/O Port Address: 3C5

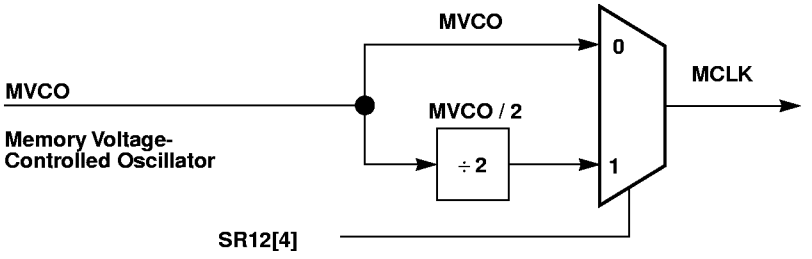
Index: 12

Bit	Description	Reset State
7	Overscan Color Protect	0
6	Display Memory Pins All Tristate	0
5	VCLK = (VCO ÷ 4)	0
4	MCLK = (MVCO ÷ 2)	0
3	Hardware Cursor and Hardware Icon Position Modification	0
2	Hardware Cursor-Size Select	0
1	CPU Access to DAC Extended Colors	0
0	Hardware Cursor Enable	0

This register is used to enable or disable the CL-GD7548 4-bit packed-pixel addressing.

Bit	Description
7	**Overscan Color Protect:** When this bit is: • 0, the overscan color comes from Attribute Controller register AR11[5:0]. • 1, the overscan color comes from Extension register HDR (the Hidden DAC register, the 16-cell RAMDAC RAM extension). As a result, the border color is locked to a value dictated by environmental requirements, and it cannot be changed by the application.
6	**Display Memory Pins All Tristate:** When this bit is: • 0, all display memory pins operate normally. • 1, all display memory pins are forced to a tristate high-impedance off state. The display memory pins can then be multiplexed for use with another graphics controller.
5	**VCLK = (VCO ÷ 4):** When this bit is 1, the video clock (VCLK) signal is derived from the voltage-controlled oscillator (VCO) frequency divided by four. **NOTE:** Extension register bits SR1B[0], SR1C[0], SR1D[0], and SR1E[0] divide the VCO signal by 2 to produce the VCLK signal. While the VCO is within its operating range, as appropriate for the desired VCLK frequency, divide by 2 or by 4. • This bit must be used to get VCLK frequencies of 20 MHz or less. For example, to get 20 MHz: — Program VCO for 80 MHz. — Set SR12[5] to 1, which divides the VCO signal by four. — As a result, VCLK = 20 MHz. • This bit is useful in 5-V core VDD systems where at low frequencies, the VCO frequency range is not good enough.

12.9 SR12: Video Data Path Control Register *(cont.)*

Bit	Description
4	**MCLK = (MCLK ÷ 2):** • This bit is used to get MCLK (memory clock signal) frequencies outside the memory VCO frequency range for a given core VDD value and frequency. • When this bit is: — 0, MCLK is the same as the MVCO (memory voltage-controlled oscillator) signal. — 1, MCLK is derived by dividing by two the original memory clock signal from MVCO. 
3	**Hardware Cursor and Hardware Icon Position Modification:** This bit selects whether the CPU can modify the position (both horizontal and vertical) of either the hardware cursor or the hardware icon. The same registers are used to modify both hardware cursor and hardware icon positions. • When this bit is 0, the CPU can modify the hardware cursor position. • When this bit is 1, the CPU can modify the hardware icon position. • This bit does not affect Extension register bits SR2A[6] or SR2E[0], which are always accessible by the CPU.
2	**Hardware Cursor-Size Select:** This register bit must be programmed the same as SR21[4]. When this bit is: • 0, the 32 × 32-pixel hardware cursor is selected. • 1, the 64 × 64-pixel hardware cursor is selected.
1	**CPU Access to DAC Extended Colors:** When this bit is: • 0, the CPU accesses the standard VGA 256 × 18 CLUT. • 1, the CPU accesses the extended CLUT, that is, the DAC extended colors, which are included in 16 additional 18-bit wide RAMDAC RAM locations. — Some locations have a specific purpose, such as hardware cursor colors (2 locations), hardware icon colors (4 locations), and border color (1 location). — Other locations are not used, or they can be used as scratchpad registers by the BIOS and drivers. *Continued*

12.9 SR12: Video Data Path Control Register *(cont.)*

Bit **Description**

1 *(cont.)* **CPU Access to DAC Extended Colors** *(cont.)*:
The address map for the DAC extended colors is given in the following table:

I/O Address	Physical RAM Location	Function
X0h	256	Hardware cursor background color
XFh	257	Hardware cursor foreground color
X2h	258	Fix color of overscan (the border)
X3h	259	Hardware icon color #0. (This function is not used, if in 3-colors-and-transparent mode.)
X4h	260	Hardware icon color #1
X5h	261	Hardware icon color #2
X6h	262	Hardware icon color #3
XB, XC, XD, XE	269, 270	Used by Video BIOS

0 **Hardware Cursor Enable:**
- When this bit is:
  - — 0, the hardware cursor is disabled and does not appear on-screen.
  - — 1, the hardware cursor is enabled and appears on-screen.
- To select the hardware cursor size, refer to SR12[2].

12.10 SR13: Hardware Cursor Pattern Address Offset Register

I/O Port Address: 3C5

Index: 13

Bit	Description	Reset State
7	Not Used	Not applicable
6	Not Used	Not applicable
5	Reserved	
4	Hardware Cursor Pattern Select [4]	0
3	Hardware Cursor Pattern Select [3]	0
2	Hardware Cursor Pattern Select [2]	0
1	Hardware Cursor Pattern Select [1] / Reserved	0
0	Hardware Cursor Pattern Select [0] / Reserved	0

This register is used to select one of the following:

- One of the 32 possible cursor patterns for the 32 × 32 hardware cursor.
- One of the 8 possible cursor patterns for the 64 × 64 hardware cursor.

For a complete programming guide for the hardware cursor, refer to Appendix B.

Bit	Description
7:6	**Not Used**
5	**Reserved**
4:0	**Hardware Cursor Pattern Select (32 × 32 Cursor):** When SR12[2] is 0: • This 5-bit field can select 1 of 32 cursor patterns for the 32 × 32 cursor. • The patterns are stored in 8 Kbytes of the top 32 Kbytes of display memory.
4:2	**Hardware Cursor Pattern Select (64 × 64 Cursor):** When SR12[2] is 1: • This 3-bit field can select 1 of 8 cursor patterns for the 64 × 64 cursor. • The patterns are stored in 8 Kbytes of the top 32 Kbytes of display memory.
1:0	**Reserved:** These bits are reserved when SR12[2] is 1.

12.11 SR14, SR15: Scratchpad 2, 3 Registers

I/O Port Address: 3C5

Index: 14, 15

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD7548 BIOS and must never be written by any application program. They are listed here only for completeness.

Bit	Description
7:0	**Reserved:** These bits are reserved for the Cirrus Logic BIOS.

12.12 SR16: Performance Tuning Register

I/O Port Address: 3C5

Index: 16

Bit	Description	Reset State
7	Extra Wait State for VESA VL-Bus	0
6	VESA VL-Bus RDY# / PCI-Bus TRDY# Delay for I/O Read/Write	0
5	VESA VL-Bus RDY# / PCI-Bus TRDY# Delay for Memory Write [1]	0
4	VESA VL-Bus RDY# / PCI-Bus TRDY# Delay for Memory Write [0]	0
3	CPU Cycle Release Threshold [3]	1
2	CPU Cycle Release Threshold [2]	1
1	CPU Cycle Release Threshold [1]	1
0	CPU Cycle Release Threshold [0]	1

This register is used to control the delay from ADS# to RDY# and FRAME# to TRDY# and to control the threshold at which the CRT FIFO is refilled. This register must never be written by an application program. It is listed here for completeness only.

Bit — **Description**

7 — **Extra Wait State for VESA VL-Bus:**

- When this bit is 1, and when the CL-GD7548 is configured for the VESA VL-Bus, one extra wait state is added to both I/O and memory accesses.
- This bit must be 1 if the bus clock is fast, compared to the memory clock.
- In combination with the state of SR16[6], this bit controls the CPU1X clock delay from ADS# to RDY# for I/O cycles.
- For further explanation, refer to the tables in SR16[6] and SR16[5:4].

6 — **VESA VL-Bus RDY# / PCI-Bus TRDY# Delay for I/O Read/Write:**

- When the CL-GD7548 is configured for **VL-Bus**, this bit, along with SR16[7], controls the CPU1X clock delay from ADS# to RDY# for I/O read/write cycles.
- When the CL-GD7548 is configured for **PCI Bus**, this bit alone controls the PCI Clock delay from FRAME# to TRDY# for PCI read/write cycles.

SR16 [7]	SR16 [6]	VL-Bus CPU1X Clock Delay (in wait states)
0	0	1 wait state
0	1	2 wait states
1	0	2 wait states
1	1	3 wait states

SR16 [6]	PCI Bus Clock Delay (in wait states)
0	0 wait state
1	1 wait state

12.12 SR16: Performance Tuning Register *(cont.)*

Bit	Description
5:4	**VESA VL-Bus RDY# Delay for Memory Write [1:0]:** • When the CL-GD7548 is configured for VESA VL-Bus (or other local bus), this field is used in combination with SR16[7] to control the delay from ADS# to RDY# for memory write cycles. • To program this field, values in the table must satisfy the following inequality: [(1 + wait state value from table) × CPU Clock Period] ≥ [(3 × MCLK Period) + 2 ns]

SR16			VL-Bus CPU1X Clock Delay (in wait states)
[7]	[5]	[4]	
0	0	0	2 wait states
0	0	1	3 wait states
0	1	0	4 wait states
0	1	1	5 wait states
1	0	0	3 wait states
1	0	1	4 wait states
1	1	0	5 wait states
1	1	1	6 wait states

Bit	Description
5:4	**PCI Bus TRDY# Delay for Memory Write [1:0]:** • When the CL-GD7548 is configured for PCI bus, this field is used to control the delay from IRDY# to TRDY# for memory write cycles. • To program this field, values in the table must satisfy the following inequality: [(wait state value from table) × CPU Clock Period] ≥ [(4 × MCLK Period) + 2 ns]

SR16		PCI-Bus Clock Delay (in wait states)
[5]	[4]	
0	0	2 wait states
0	1	3 wait states
1	0	4 wait states
1	1	5 wait states

12.12 SR16: Performance Tuning Register *(cont.)*

Bit	Description
3:0	**CPU Cycle Release Threshold [3:0]:** • The value written to this field selects the level at which the sequencer begins cycles to refill the CRT FIFO (and thereby hold off CPU cycles). — The greater the value written to this field, the higher the priority of CRT FIFO access over CPU cycles. — An exception to the above rule is the value '0000', which gives the highest priority to the CRT FIFO access. • For each Graphics mode, this field has an optimum value that uses the display memory bandwidth most efficiently. **NOTE:** When SR16[3:0] is 0, in this special case, encoding 20 – 16 for the CRT FIFO request results in a CRT FIFO request delay of 4 CRT FIFO reads.

SR16				CRT FIFO Request Delay (in CRT FIFO reads)
[3]	[2]	[1]	[0]	
0	0	0	0	(20 levels – 16 levels) = 4 CRT FIFO reads
0	0	0	1	19 CRT FIFO reads
0	0	1	0	18 CRT FIFO reads
0	0	1	1	17 CRT FIFO reads
0	1	0	0	16 CRT FIFO reads
0	1	0	1	15 CRT FIFO reads
0	1	1	0	14 CRT FIFO reads
0	1	1	1	13 CRT FIFO reads
1	0	0	0	12 CRT FIFO reads
1	0	0	1	11 CRT FIFO reads
1	0	1	0	10 CRT FIFO reads
1	0	1	1	9 CRT FIFO reads
1	1	0	0	8 CRT FIFO reads
1	1	0	1	7 CRT FIFO reads
1	1	1	0	6 CRT FIFO reads
1	1	1	1	5 CRT FIFO reads

12.13 SR17: BitBLT Memory Map I/O Address Control Register

I/O Port Address: 3C5

Index: 17

Bit	Description	Reset State
7	Reserved	
6	BitBLT Memory Map I/O Address Control	0
5	Reserved	
4	Reserved	
3	Reserved	
2	BitBLT Memory Map I/O Address Control Enable	1
1	Reserved	
0	Reserved	

This register is used to control the placement of the BitBLT memory map, in order to allow the BitBLT to be programmed in 32-bit segments.

Bit	Description
7	**Reserved**
6	**BitBLT Memory Map I/O Address Control**: • When linear memory mode is enabled [that is, either SR7[7:4] is non-zero or, (for PCI bus only) SR2D[7:6] is non-zero] *and* this bit is 1, then: — If display memory consists of 1 Mbyte of DRAM, the BitBLT memory I/O physical address space is mapped at 3FF00h to 3FFFFh. — If display memory consists of 2 Mbytes of DRAM, the BitBLT memory I/O physical address space is mapped at 7FF00h to 7FFFFh. • When linear memory mode is disabled, this bit is a 'don't care'.
5:3	**Reserved**
2	**BitBLT Memory Map I/O Address Control Enable:** When this bit is: • 0, the BitBLT memory map I/O address is disabled. • 1, the BitBLT registers are addressable, allowing faster access.
1:0	**Reserved**

12.14 SR18: Signature Generator Control Register

I/O Port Address: 3C5

Index: 18

Bit	Description	Reset State
7	Signature Generator for LCD Enable / Status	0
6	Reserved	
5	Reserved	
4	Signature Generator Input from Pixel Data Bus [2]	0
3	Signature Generator Input from Pixel Data Bus [1]	0
2	Signature Generator Input from Pixel Data Bus [0]	0
1	Signature Generator Reset	0
0	Signature Generator for CRT Enable / Status	0

This register is used to control and monitor the status of the CL-GD7548 signature generator, which is used for board-level testing of the video sub-system. For a complete description of the signature generator, refer to Appendix I.

Bit — **Description**

7 — **Signature Generator for LCD Enable / Status:**
- When this bit is 1, the signature generator is enabled for the LCD.
- By monitoring the status of this bit, the program can determine when the signature is complete for the LCD.

6:5 — **Reserved**

4:2 — **Signature Generator Input from Pixel Data Bus [2:0]:**
This field is used to select the Feature Connector Pixel Data Bus bit that is used as the input for the signature generator according to the following table:

SR18			Input to Signature Generator from Feature Connector Pixel Data Bus
[4]	[3]	[2]	
0	0	0	FCP[0]
0	0	1	FCP[1]
0	1	0	FCP[2]
0	1	1	FCP[3]
1	0	0	FCP[4]
1	0	1	FCP[5]
1	1	0	FCP[6]
1	1	1	FCP[7]

12.14 SR18: Signature Generator Control Register *(cont.)*

Bit	Description
1	**Signature Generator Reset:** When this bit is: • 0, the signature generator is allowed to run under the control of SR18[0]. • 1, the signature generator is reset to an initial, defined condition.
0	**Signature Generator for CRT Enable / Status:** • When this bit is 1, the signature generator is enabled for a CRT. The signature generator begins operation on the next VSYNC from the Feature Connector Pixel Data Bus bit chosen by SR18[4:2], it accumulates a signature for one video frame, and then it stops, forcing this bit to 0. • By monitoring the status of this bit, the program can determine when the signature is complete for the CRT.

12.15 SR19: Signature Generator Result Low Register

I/O Port Address: 3C5

Index: 19

Bit	Description	Reset State
7	Signature Generator Result [7]	0
6	Signature Generator Result [6]	0
5	Signature Generator Result [5]	0
4	Signature Generator Result [4]	0
3	Signature Generator Result [3]	0
2	Signature Generator Result [2]	0
1	Signature Generator Result [1]	0
0	Signature Generator Result [0]	0

For a complete description of the signature generator refer to Appendix I.

Bit	Description
7:0	**Signature Generator Result [7:0]**: • This register is used to read the least-significant byte of the signature generator result. • The most-significant byte of the signature generator result is read by SR1A.

12.16 SR1A: Signature Generator Result High Register

I/O Port Address: 3C5

Index: 1A

Bit	Description	Reset State
7	Signature Generator Result [15]	0
6	Signature Generator Result [14]	0
5	Signature Generator Result [13]	0
4	Signature Generator Result [12]	0
3	Signature Generator Result [11]	0
2	Signature Generator Result [10]	0
1	Signature Generator Result [9]	0
0	Signature Generator Result [8]	0

For a complete description of the signature generator refer to Appendix I.

Bit	Description
7:0	**Signature Generator Result [15:8]**: • This register is used to read the most-significant byte of the signature generator result. • The least-significant byte of the signature generator result is read by SR19.

12.17 SR1B,SR1C,SR1D,SR1E: Denominator/Post-scalar for VCLK 0,1,2,3

I/O Port Address: 3C5

Index: 1B, 1C, 1D, 1E

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	VCLK Denominator [4]	R/W	See table below
4	VCLK Denominator [3]	R/W	See table below
3	VCLK Denominator [2]	R/W	See table below
2	VCLK Denominator [1]	R/W	See table below
1	VCLK Denominator [0]	R/W	See table below
0	VCLK Post-Scalar	R/W	See table below

These registers are used in combination with Extension registers SRB to SRE to establish the frequency of the four possible video clocks. The video clock used is selected by Extension/General register MISC[3:2].

This register establishes the denominator and post-scalar values. For information on the numerator, refer to Section 12.5. For more information on clock options, refer to Appendix G.

Each video clock frequency is determined by the following equation.

$$VCLKn\ (\text{MHz}) = \frac{OSC \times NR}{DR \times [P+1]}$$

Equation 12-2

where:

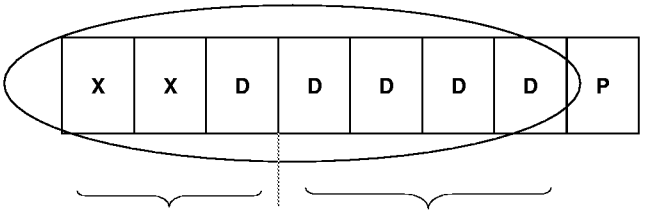
VCLK n	=	Video clock frequency n, where n = 0, 1, 2, 3
OSC	=	Input clock frequency of 14.318 MHz
Numerator **R**egister	=	Value of register bits SRi [6:0], where i = B, C, D, E
Denominator **R**egister	=	Value of register bits SR1i [5:1], where i = B, C, D, E
Post-scalar	=	Value of register bits SR1i [0], where i = B, C, D, E

If n = 0, then i = B.
If n = 1, then i = C.
If n = 2, then i = D.
If n = 3, then i = E.

The following table shows the reset values of the registers that determine the video clock frequency. The table also shows the corresponding video clock frequency at system reset.

12.17 SR1B, SR1C, SR1D, SR1E: Denominator/Post-scalar for VCLK 0,1,2,3 *(cont.)*

VCLKn Frequency		VCLKn Numerator Values			VCLKn Denominator Values			
Clock VCLKn	VCLKn Frequency at Reset	Numerator Register and Hex Value in Register		*NR* = Value Used in Equation Numerator	Denominator Register and Hex Value in Register		*DR* = Value Used in Equation Denominator, Resulting from Post-scalar	*P* = Post-Scalar Value Used in Equation Denominator
	MHz	Register (SRi)	Hex	Decimal Equivalent of Hex Value	Register (SRi)	Hex	Decimal	Decimal
VCLK0	25.180	SRB	66h	102	SR1B	3Bh	29	1
VCLK1	28.325	SRC	5Bh	91	SR1C	2Fh	23	1
VCLK2	41.165	SRD	45h	69	SR1D	30h	24	0
VCLK3	36.082	SRE	7Eh	126	SR1E	33h	25	1

Bit	Description
7:6	**Reserved**
5:1	**VCLK Denominator [4:0]:** These bits determine the denominator value (*D*) used to determined the video clock frequency. For the equation, the post-scalar bit (*P*) is ignored, which has the effect of shifting all bits in the register to the right.  **UPPER VALUE = VALUES IN XXD LOWER VALUE = VALUES IN DDDD** **Circled area contains the value that is extracted, converted to decimal, and substituted in the equation.**
0	**VCLK Post-scalar:** This bit determines the post-scalar value (*P*) used to determine the video clock frequency. This bit defines a divide-by-one or divide-by-two operator in the denominator. (If the post-scalar is 1, then the voltage-controlled oscillator is running at two times OSC, the input clock frequency.)

12.18 SR1F: MCLK Frequency and VCLK Source Select Register

I/O Port Address: 3C5

Index: 1F

Bit	Description	Reset State
7	Not Used	Not applicable
6	VCLK Source Select	0
5	MCLK Frequency [5]	(Refer to MCLK Table below)
4	MCLK Frequency [4]	(Refer to MCLK Table below)
3	MCLK Frequency [3]	(Refer to MCLK Table below)
2	MCLK Frequency [2]	(Refer to MCLK Table below)
1	MCLK Frequency [1]	(Refer to MCLK Table below)
0	MCLK Frequency [0]	(Refer to MCLK Table below)

This register is used to program the MCLK frequency. This register must never be programmed by an application program. It is listed here only for completeness.

Bit **Description**

7 **Not Used**

6 **VCLK Source Select:**

- When this bit is 0, the VCLK synthesizer operates normally.
- When this bit is 1, VCLK is derived from MCLK as follows:

SR1F[6]	SR1E[0]	VCLK Source
0	X	VLCK (Normal Operation)
1	0	VCLK = MCLK
1	1	VCLK = (MCLK ÷ 2)

5:0 **MCLK Frequency [5:0]:**

- This register must never be programmed by an application program.
- To directly program the MCLK frequency, use the following equation: SR1F[5:0] × [Reference Frequency ÷ 8] = Desired MCLK Frequency.
- For DRAM requirements for MCLK frequencies, refer to Appendix F.
- This field may be programmed with values from 21 to 38 (decimal).
- The following table assumes a reference frequency of 14.318 MHz.

SR1F[5:0] in Decimal and Hex	[Reference Frequency ÷ 8] =	Desired MCLK Frequency
21 (15h)	14.318 ÷ 8 = 1.79	37.585 MHz
23 (17h)		41.165 MHz
24 (18h, the default value at reset)		**42.955 MHz**
25 (19h)		44.744 MHz
26 (1Ah)		46.534 MHz
28 (1Ch)		50.114 MHz

12.19 SR20: Miscellaneous Control Register 2

I/O Port Address: 3C5

Index: 20

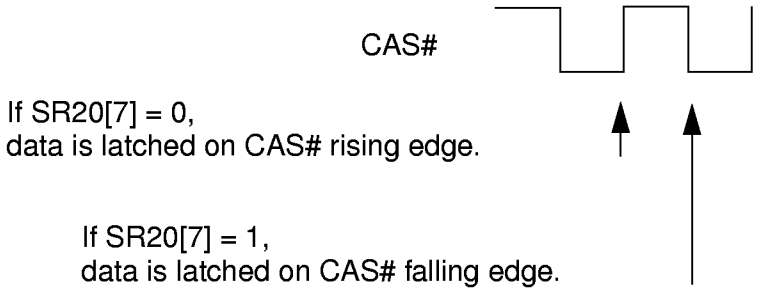
Bit	Description	Reset State
7	Display Memory Data Latch Select on Next CAS# Rising Edge	0
6	Display Memory Extended RAS# Cycle Time Select	0
5	LCD Data and Control Pins Tristated	0
4	Reserved	
3	LCD Power-Sequencing Pins Tristated	0
2	CRT FIFO Request Threshold Select	0
1	Display Memory Interface-Input Threshold Select	0
0	CPU Bus Interface-Input Threshold Select	0

This register is reserved exclusively for the CL-GD7548 BIOS and must never be written by an application program. It is listed here only for completeness.

Bit **Description**

7 **Display Memory Data Latch Select on Next CAS# Rising Edge:**
Program this bit to:

- 0:
  - — To latch display memory data bits on the CAS# rising edge.
  - — To use 60-ns 256K × 16 EDO DRAMs. (In a 5-V core VDD system, the CL-GD7548 supports these DRAMs with an MCLK of 66 MHz and with a 7-MCLK RAS# cycle setup that does not require a late latch.)
- 1:
  - — To latch display memory data bits on the next CAS# falling edge.
  - — To use most EDO/Hyper-Page-Mode DRAMs. (Use SR20[6] to select the necessary RAS# cycle length of either 8 or 9 MCLKs, as appropriate.)



12.19 SR20: Miscellaneous Control Register 2 *(cont.)*

Bit — **Description**

6 — **Display Memory Extended RAS# Cycle Time Select:**

- This bit must be used only for EDO (Extended-Data-Out) DRAMs.
- This bit works in combination with Extension register SRF[2] to extend the length of the display memory RAS# cycle time up to 8 and 9 MCLKs, as shown in the following table:

SR20[6]	SRF[2]	Length of RAS# Cycle	Type of RAS# Cycle
0	0	7 MCLKs	4 MCLKs low and 3 MCLKs high
0	1	6 MCLKs	3.5 MCLKs low and 2.5 MCLKs high
1	0	9 MCLKs	5 MCLKs low and 4 MCLKs high
1	1	8 MCLKs	4.5 MCLKs low and 3.5 MCLKs high

5 — **LCD Data and Control Pins Tristated:**

When this bit is:

- 0, LCD data and control pins operate normally. (This condition is the default.)
- 1, LCD data and control pins are tristated.
  - — The following LCD data and control pins are tristated for all LCD panels: SUD[7:0], SLD[7:0], FP[3]/MOD, FP2, FPVDCLK, LLCLK, LFS, and FPDE.
  - — The following LCD data and control pins are tristated only if a 24-bit TFT panel is selected (that is, Extension register bits R9X[1:0] are set to '11'): FP[0], FP[1], FP[8], FP[9], FP[16], and FP[17].
  - — The following LCD panel power-management pins are not affected by SR20[5]: FPVCC, FPBL, and FPVEE. Although these pins are panel-related, they are instead controlled by SR20[3].

4 — **Reserved**

3 — **LCD Power-Sequencing Pins Tristated:**

This bit affects the LCD power pins FPVCC, FPBL, and FPVEE. When this bit is:

- 0, the above-mentioned LCD power pins operate normally and are driving. (This condition is the default.)
- 1, the above-mentioned LCD power pins are tristated.

12.19 SR20: Miscellaneous Control Register 2 *(cont.)*

Bit — **Description**

2 — CRT FIFO Request Threshold Select:

- This bit is used in combination with Extension register SRF[5] to select the threshold for when a CRT FIFO request is generated, as well as the CRT FIFO depth, as shown in the table below.
- If both SR20[2] and SRF[5] are set to 1, then Extension register bits SR33[3:0] are used to extend the programming for the CRT FIFO.

SR20[2]	SRF[5]	CRT FIFO Depth that Results from CRT FIFO Request	When CRT FIFO Request Is Generated
0	0	8 levels deep x 32 bits wide	These bit settings are used when the CRT FIFO is no longer 100% full. (This setting must be used in Text modes.)
0	1	20 levels deep x 32 bits wide	These bit settings are used when the CRT FIFO is no longer 100% full. (This setting must be used in Graphics modes.)
1	0	20 levels deep x 32 bits wide	These bit settings are used when the CRT FIFO is either 50% full or less than 50% full.
1	1	20 levels deep x 32 bits wide	These bit settings are used in combination with Extension register SR33[3:0]. In this case, a value *n* is programmed into SR33[3:0], where the *n* value represents the levels of the CRT FIFO that are empty (that is, the threshold for when to fill the CRT FIFO).

1 — Display Memory Interface-Input Threshold Select:
When this bit is:

- 0, display memory interface-input thresholds are at TTL levels.
- 1, display memory interface-input thresholds are at CMOS levels.

0 — CPU Bus Interface-Input Threshold Select:
When this bit is:

- 0, CPU bus interface-input thresholds are at TTL levels.
- 1, CPU bus interface-input thresholds are at CMOS levels.

12.20 SR21: Dual-Scan Color Control Register

I/O Port Address: 3C5

Index: 21

Bit	Description	Reset State
7	Refresh-Per-Scanline Select	0
6	Color Dual-Scan STN Select	0
5	Frame Buffer Cycle Stop	0
4	Hardware Cursor-Size Select	0
3	Inverted Voltage-Controlled Oscillator Output Used as VCLK	0
2	Reserved	
1	Reserved	
0	Reserved	

This register contains a field for selecting either single-scan or dual-scan STN color modes.

Bit	Description
7	**Refresh-Per-Scanline Select:** • When this bit is 0, CRT Controller register CR11[6] selects either three or five refresh cycles per scanline. (This default state of this bit is 0.) • When this bit is 1, one refresh cycle per scanline is selected.
6	**Color Dual-Scan STN Select**: • Extension register bits CR2C[7:6] must be set to '10' to select STN color LCDs. • When CR2C[7:6] is '10' *and* this bit is: — 0, single-scan STN color mode is selected. — 1, dual-scan STN color mode is selected.
5	**Frame Buffer Cycle Stop:** When this bit is 1, at the end of a display memory RAS# cycle, any requests for a frame buffer are stopped. This bit is for test purposes only.
4	**Hardware Cursor-Size Select**: • Extension register SR12[2] must be programmed the same as this bit. • When SR12[0] is 1 *and* this bit is: — 0, the 32 × 32-pixel hardware cursor is selected. — 1, the 64 × 64-pixel hardware cursor is selected. • For hardware cursor pattern choices, refer to Extension register SR13[4:0].
3	**Inverted Voltage-Controlled Oscillator Output Used as VCLK:** • When this bit is 0, VCLK is the same as the output from the VCO. This bit setting allows the CL-GD7548 to take advantage of the VCO duty cycle skew to maximize high-frequency operations. • When this bit is 1, VCLK is the inverse of the output from the VCO.
2:0	**Reserved:** These bits are for test purposes only.

12.21 SR22: Hardware Configuration Read Register 1

I/O Port Address: 3C5

Index: 22

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Sleep Mode Address Select	R	= MD[21]
4	SLEEP# Pin Enable Select	R	= MD[20]
3	External Clock Select	R	= MD[19]
2	Reserved		
1	Reserved		
0	PCI Bus 32-Bit Select	R	= MD[16]

This register contains a read-only field that allows the BIOS to determine configuration information for bus type, sleep address, and external clock by reading the level on the indicated MD pins during the low-to-high transition of the system reset pulse.

- All these MD pins have pull-down resistors internally, and so the default readings are all 0.
- An external 10k-Ω pull-up resistor is needed to establish a high ('1') on these pins.

Bus-select bits SR22[7,2,0] are mutually exclusive. Only *one* can be high at any time.

- If there are no external pull-ups on SR22 bus-select bits 2 and 0, the CL-GD7548 is configured for VESA VL-Bus operation ≤ 33 MHz.
- If there are no external pull-ups on *any* of the SR22 bus-select bits, the CL-GD7548 is configured for VESA VL-Bus operation ≤ 33 MHz. In addition, the CL-GD7548 is configured with internal clock synthesizers and a sleep address of 3C3h.

For a summary of the hardware configurations refer to Appendix L.

Bit	Description
7:6	**Reserved**
5	**Sleep Mode Address Select:** • No external pull-up on MD21 / S46PU reads back a 0, indicating the selection of Sleep mode address 3C3h, the default. • An external pull-up on MD21 / S46PU reads back a 1, indicating the selection of I/O address 46E8h as the Sleep mode address.
4	**SLEEP# Pin Enable Select:** • No external pull-up on MD20 / SLEEPPU reads back a 0, which selects the ZVPCTL output of the SLEEP# / ZVPCTL pin, indicating the normal mode for the CL-GD7548 (the default). • An external pull-up on MD20 / SLEEPPU reads back a 1, which selects the SLEEP# input of the SLEEP# / ZVPCTL pin.

12.21 SR22: Hardware Configuration Read Register 1 *(cont.)*

Bit	Description
3	**External Clock Select:** • No external pull-up on MD19 / XCLKPU reads back a 0, so that the internal clock MCLK and VCLK are used by default. • An external pull-up on MD19 / XCLKPU reads back a 1, powering down the internal clock for MCLK and VCLK, and enabling the external XMCLK and XVCLK clock inputs. (This external pull-up is used for manufacturing test and for logic simulations by Cirrus Logic.)
2:1	**Reserved**
0	**PCI Bus 32-bit Select:** • No external pull-up on MD16 / PCIPU reads back a 0, configuring the CL-GD7548 for a VESA VL-Bus operation. • An external pull-up on MD16 / PCIPU reads back a 1, configuring the CL-GD7548 for 32-bit PCI bus operation.

12.22 SR23: Software Configuration Register 1

I/O Port Address: 3C5

Index: 23

Bit	Description	Reset State
7	FCVCLK Enable	0
6	ACTI / DDCD / FCEVIDEO# / SBYI Select	0
5	BLI / SUSPI Select	0
4	VCLK Output Enable	0
3	Extended-Data-Out / Hyper-Page-Mode DRAM Select	0
2	Reserved	
1	PCI Bus Cycle Retry	0
0	SW0 / MCLK / XMCLK Select	0

This register contains a read-only field that allows for miscellaneous configurations.

Bit **Description**

7 **FCVCLK Enable:**
A 1 in this bit enables the FCVCLK input to drive either the RAMDAC or the video clock (VCLK), depending on the state of External/General register MISC[3]. When SR23[7] is 1 *and*:

- MISC[3] is 0, FCVCLK is sent only to the RAMDAC, enabling only that part of the CL-GD7548.
- MISC[3] is 1, FCVCLK is used to drive VCLK, which clocks the entire CL-GD7548.
- There is a high on the TVON pin, the TVON high signal forces MISC[3] to 1. In this case also, FCVCLK is used to drive VCLK, which clocks the entire CL-GD7548.

6 **ACTI / DDCD / FCEVIDEO# / SBYI Select:**
This bit is used in combination with other bits to chose from among the functions provided by the ACTI / DDCD / FCEVIDEO# / SBYI pin. The following table indicates settings for the various pin functions.

SR24[7]	SR2F[7]	SR23[6]	CR50[3]	Function Chosen for ACTI / DDCD / FCEVIDEO# / SBYI Pin
0	0	X	1	DDCD
0	1	0	0	SBYI
0	1	1	0	ACTI
1	X	X	X	FCEVIDEO#

12.22 SR23: Software Configuration Register 1 *(cont.)*

Bit	Description
5	**BLI / SUSPI Select:** When SR24[7] is 0 *and* this bit is: • 0, the BLI / SUSPI pin is configured for SUSPI, the hardware-controlled Suspend Input control. • 1, the BLI / SUSPI pin is configured for BLI, the Backlight Input control.
4	**VCLK Output Enable:** When this bit is: • 0 (the default) *and* SR24[7] is 0, the DDCC / FCDCLK / VCLK pin is used as a DDCC open-drain output for DDC support. • 1, the internal VCLK is available for testing on the DDCC / FCDCLK / VCLK pin, independent of SR22[3] (the external/internal clock selection).
3	**Extended-Data-Out / Hyper-Page-Mode DRAM Select:** Before any access can be made to video memory, this bit *must* be set properly according to the type of DRAM that is installed in the system. Set this bit to: • 0 when standard DRAMs are installed and standard DRAM timing is required. • 1 when either EDO (Extended-Data-Out) DRAMs or Hyper-Page-Mode DRAMs have been installed in the system, and EDO DRAM timing is required.
2	**Reserved**
1	**PCI Bus Cycle Retry:** This bit enables a PCI bus cycle retry for a PCI bus master that is using a second aperture. When this bit is: • 0, the PCI bus cycle retry occurs only for the PCI bus burst cycles. • 1, the PCI bus cycle retry occurs for all PCI bus cycles. — For example, if the CL-GD7548 is executing a BitBLT at the same time that a PCI bus master is using the second aperture and requesting a PCI bus cycle, the CL-GD7548 sends a PCI bus cycle retry until the CL-GD7548 is free to accept the request for the PCI bus cycles. — This operation allows a PCI bus master to wait for a BitBLT to compete, without software intervention. (However, if this bit is reset, software must poll the BitBLT register until the BitBLT completes.) — The retry occurs for all PCI bus cycles, not only the PCI bus burst cycles.
0	**SW0 / MCLK / XMCLK Select**: This bit works in combination with SR22[3] to determine the configuration of the SW0 / MCLK / XMCLK pin as shown in the following table:

SR22[3]	SR23[0]	SW0 / MCLK/ XMCLK Pin Status
0	0	SW0 Input
0	1	MCLK Output
1	'Don't care'	XMCLK Input

12.23 SR24: LCD-Type Switches and Feature Connector Enable

I/O Port Address: 3C5

Index: 24

Bit	Description	Reset State
7	Feature Connector Port Enable	= MD[25]
6	FCVCLK Invert Enable	0
5	Fast 16-Bit CPU Bus Access Enable	0
4	FCDCLK Output Select	0
3	External Pull-Ups All Read under Software Control	Pull-up Values
2	SW2 Pin Read	Switch Value
1	SW1 Pin Read	Switch Value
0	SW0 Pin Read	Switch Value

Bit	Description
7	**Feature Connector Port Enable:** When this bit is: • 0, or no pull-up is used: — Then in combination with Extension register SR23[5], the BLI / SUSPI pin can be configured for either BLI or SUSPI. — Those pins mentioned under the condition for when this bit = 1 revert to their other functions or are disabled (that is, inputs are ignored and outputs are high-impedance). • 1, or an external pull-up resistor is connected to MD25 / FCPU: — All appropriate pins are configured for the Feature Connector. (Refer to pin descriptions in Chapter 2.) — The ACTI / DDCD / FCEVIDEO# / SBYI pin is configured for FCEVIDEO#. — This bit is used in combination with SR2F[6] to configure these pins: — FCP [0] / FP[8] / SBYST# — FCP [1] / FP[9] / SUSPST#
6	**FCVCLK Invert Enable:** When this bit is 1, the normally active-high FCVCLK signal is inverted to active-low. This bit is used internally to latch data.
5	**Fast 16-Bit CPU Bus Access Enable:** This bit works with both the VESA VL-Bus and the PCI bus. When this bit is: • 0, the RDY# / TRDY# output is delayed for 16-bit accesses by one bus-clock cycle to minimize bus contention problems. (Normally, this bit must be 0.) • 1, the clock delay is removed, which allows faster bus access.

12.23 SR24: LCD-Type Switches and Feature Connector Enable *(cont.)*

Bit **Description**

4 **FCDCLK Output Select:**
This bit is used in combination with other bits to select the function for the DDCC / FCDCLK / VCLK pin, as shown in the following table.

SR24[7]	SR23[4]	SR24[4]	CR50[3]	Function Selected
0	0	X	1	DDCC
X	X	0	0	FCDCLK
X	X	1	0	VCLK

3 **External Pull-Ups All Read Under Software Control:**
This bit must be programmed to:
- 0 for hardware control of external pull-ups.
- 0-1-0 for software control of external pull-ups.
  - — Any 0-1-0 transition of this bit allows the state of all external pull-ups on the memory data pins to be read and latched by the CL-GD7548 at any time, not just at hardware reset.
  - — Software control is used when the system reset pulse is too short to read the switches that have large pull-up or pull-down resistance.

2:0 **SW2 to SW0 Pin Read:**
These read-only bits reflect the inverse of the active level of switch inputs SW2 to SW0 respectively.
- During normal operation, switch inputs SW2 to SW0 are directly read continuously on the I/O bus, and so they are not latched at hardware reset. As a result, they do not need a software read for a save or restore operation. They are not affected by SR24[3].
- These bits are normally for BIOS use.

12.24 SR25: Timer-Software Reset and Hardware Configuration 2

I/O Port Address: 3C5

Index: 25

Bit	Description	Reset State
7	Reserved	
6	External RAMDAC Address / Chip Select	0
5	1-Bit/Pixel Packed-Pixel Mode Enable	0
4	External XVCLK Input Enable	0
3	4-Bit/Pixel Packed-Pixel Mode Enable	1
2	Effect of CR1B[1] on CRT Address Disable	1
1	Standby Mode Timer Reset by I/O Read to Keyboard	1
0	Backlight Timer Reset by I/O Read to Keyboard	1

Bit	Description
7	**Reserved**
6	**External RAMDAC Address / Chip Select:** • When this bit is 0, the TVON pin is controlled by Extension register CR30[3]. • When this bit is 1, — The TVON output becomes the external RAMDAC Chip Select. At system reset, both the TVON and RAMDAC Select functions are inactive-low. As a result, no matter how the chip comes up, external RAMDAC is not affected. — It disables the internal DAC and RAMDAC RAM I/O readback. The RAM continues to be updated by RAMDAC writes, but it does not respond to any RAMDAC read except 3C7. — In VESA VL-Bus mode, the CL-GD7548 does not assert LDEV# and RDY. — In PCI bus mode, the CL-GD7548 does not support external RAMDAC related to I/O select or shadowing. • This bit must be set to 1, *before* TV-OUT feature is enabled CR30[3] is 1), to ensure that the TVON pin becomes the external RAMDAC Chip Select.
5	**1-Bit/Pixel Packed-Pixel Mode Enable:** When this bit is 1, the 1-bit-per-pixel packed-pixel mode is enabled.
4	**External XVCLK Input Enable:** When this bit is 1 and when SR22[3] is 0, an external 14.318-MHz input must be connected to the OSC / XVCLK input pin. (However, in this case MCLK does not use this input. Instead, it still uses the internal MVCO source.) • On VCLK generation, this bit is OR'ed with SR22[3]. • This bit is to be used for NTSC-Out.
3	**4-Bit/Pixel Packed-Pixel Mode Enable:** When this bit is 1, a 4-bit-per-pixel packed-pixel mode is enabled.

12.24 SR25: Timer-Software Reset and Hardware Configuration 2 *(cont.)*

Bit 2 — Effect of CR1B[1] on CRT Address Disable:

For CRT addresses, this bit overrides Extension register CR1B[1], which has the effect of limiting the CRT and CPU addresses.

- When this bit is 0:
  - — The CRT display can access only the display memory for standard VGA modes. In contrast, the CPU can access the entire display memory.
  - — *And* CR1B[1] is 1, this bit setting is used to update hardware icon and hardware cursor mapping in standard VGA modes.
- When this bit is 1:
  - — Both the CRT display and the CPU can access the entire display memory.
  - — This bit setting is used with extended graphics modes that require more display memory than the display memory for standard VGA modes.
  - — Display memory for standard VGA modes must be reduced in size in order to wrap around (an effect used by many applications for fast scrolling).
  - — The table below gives the bit settings that result in extended memory access for the CPU and CRT.

SR25[2]	CR1B[1]	CPU Memory Accesses	CRT Memory Accesses
0	0	Access limited to VGA	Access limited to VGA
0	1	Extended memory access	Access limited to VGA
1	0	Access limited to VGA	Access limited to VGA
1	1	Extended memory access	Extended memory access

Bit 1 — Standby Mode Timer Reset by I/O Read to Keyboard:

This bit is used to reset the internal Standby mode timer, when there is an I/O read to the keyboard controller (port 60h).

Bit 0 — Backlight Timer Reset by I/O Read to Keyboard:

This bit is used to reset the internal backlight timer, when there is an I/O read to the keyboard controller (port 60h).

12.25 SR26: Shader Signature Low Register

I/O Port Address: 3C5

Index: 26

Bit	Description	Reset State
7	Shader Signature [7]	0
6	Shader Signature [6]	0
5	Shader Signature [5]	0
4	Shader Signature [4]	0
3	Shader Signature [3]	1
2	Shader Signature [2]	1
1	Shader Signature [1]	1
0	Shader Signature [0]	1

The Shader Signature field is used only for factory testing of the CL-GD7548 shader logic. Application programs must not use the Shader Signature registers, which are listed here only for completeness.

Bit	Description
7:0	**Shader Signature [7:0]:** This register contains the least-significant byte for the Shader Signature. For the most-significant byte, refer to SR27.

12.26 SR27: Shader Signature High Register

I/O Port Address: 3C5

Index: 27

Bit	Description	Reset State
7	Shader Signature [15]	0
6	Shader Signature [14]	0
5	Shader Signature [13]	0
4	Shader Signature [12]	0
3	Shader Signature [11]	1
2	Shader Signature [10]	1
1	Shader Signature [9]	1
0	Shader Signature [8]	1

The Shader Signature field is used only for factory testing of the CL-GD7548 shader logic. Application programs must not use the Shader Signature registers, which are listed here only for completeness.

Bit	Description
7:0	**Shader Signature [15:8]:** This register contains the most-significant byte for the Shader Signature. For the least-significant byte, refer to SR26.

12.27 SR28 and SR29 Scratchpad Registers 5 and 6

I/O Port Address: 3C5

Index: 28 and 29

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

These two registers are reserved for the exclusive use of the CL-GD7548 BIOS. They must never be written by any application program.

There are a total of thirteen 18-bit scratchpad registers available in the RAMDAC RAM. They are accessed as any RAMDAC RAM register, in groups of three I/O accesses. These registers are listed here only for completeness.

Bit	Description
7:0	**Reserved:** These bits are reserved for the use of CL-GD7548 BIOS.

12.28 SR2A: Hardware Icon #0 Control Register

I/O Port Address: 3C5

Index: 2A

Bit	Description	Reset State
7	Reserved	
6	Hardware Icon Fine Horizontal Position [3]	0
5	Hardware Icon #0 Display Memory Map Selection	0
4	Hardware Icon #0 Vertical Scanline Doubling	0
3	Hardware Icon #0 Horizontal Pixel Doubling	0
2	Hardware Icon #0 Blink Enable	0
1	Hardware Icon #0 Display Mode Select	0
0	Hardware Icon #0 Display Enable	0

Bit	Description
7	**Reserved**
6	**Hardware Icon Fine Horizontal Position [3]:** This bit is the most-significant bit of a 4-bit field used with text that has 9- or 10-dot fonts (character clocks), when in text or horizontally expanded graphics modes. • The least-significant bits [2:0] are in Sequencer register SRX[7:5]. • The coarse horizontal position is in Extension register SR10. **NOTE:** When horizontal expansion from 640 to 800 is enabled, the hardware icon must be positioned within 10 dots.
5	**Hardware Icon #0 Display Memory Map Selection:** • When this bit is 0, display memory map 0 is selected for Icon #0. • When this bit is 1, display memory map 1 is selected for Icon #0.
4	**Hardware Icon #0 Vertical Scanline Doubling:** When this bit is 1: • Icon #0 displays 128 scanlines, and each scanline is replicated vertically. • Icon #0 extends down and forces all other icons down.
3	**Hardware Icon #0 Horizontal Pixel Doubling:** When this bit is 1: • Icon #0 displays 128 pixels, and each pixel is replicated horizontally. • Icon #0 expands to the right on the display.
2	**Hardware Icon #0 Blink Enable:** • When this bit is 0, icon #0 is steady state. • When this bit is 1, icon #0 blinks at one-half the text-cursor blink rate.
1	**Hardware Icon #0 Display Mode Select:** The hardware icon is always 2 bits/pixel and is controlled by these 2 bits. • When this bit is 0, the 4-color display mode for icon #0 is selected. • When this bit is 1, the 3-colors-and-transparent display mode is selected.
0	**Hardware Icon #0 Display Enable:** When this bit is 1, icon #0 is enabled to display.

12.29 SR2B: Hardware Icon #1 Control Register

I/O Port Address: 3C5

Index: 2B

Bit	Description	Reset State
7	FPVDCLK and LLCLK High Drive	0
6	Monitor Sense Assist Bit	0
5	Hardware Icon #1 Display Memory Map Selection	0
4	Hardware Icon #1 Vertical Scanline Doubling	0
3	Hardware Icon #1 Horizontal Pixel Doubling	0
2	Hardware Icon #1 Blink Enable	0
1	Hardware Icon #1 Display Mode Select	0
0	Hardware Icon #1 Display Enable	0

Bit	Description
7	**FPVDCLK and LLCLK High Drive:** When this bit is 1, FPVDCLK and LLCLK have double the normal output drive to support high-load LCDs.
6	**Monitor Sense Assist Bit:** When this bit is 1: • The internal BLANK# signal to the DAC is disabled, thus allowing border color during the entire non-display time. • *And* Attribute Controller register ARX[5] is 0, this bit can be used to force a monitor display for accurate monitor sense, independent of the following: — CPU speed — CPU interrupts — The Graphics mode
5	**Hardware Icon #1 Display Memory Map Selection:** When this bit is: • 0, display memory map 0 for is selected for icon #1. • 1, display memory map 1 for is selected for icon #1.
4	**Hardware Icon #1 Vertical Scanline Doubling:** When this bit is 1: • Icon #1 displays 128 scanlines, and each scanline is replicated vertically. • Icon #1 extends down and forces all other icons down.
3	**Hardware Icon #1 Horizontal Pixel Doubling:** When this bit is 1: • Icon #1 displays 128 pixels, and each pixel is replicated horizontally. • Icon #1 expands to the right on the display.

12.29 SR2B: Hardware Icon #1 Control Register *(cont.)*

Bit	Description
2	**Hardware Icon #1 Blink Enable:** When this bit is: • 0, icon #1 is steady state. • 1, icon #1 blinks at one-half the text-cursor blink rate.
1	**Hardware Icon #1 Display Mode Select:** The hardware icon is always 2 bits/pixel and is controlled by this bit. When this bit is: • 0, the 4-color display mode for icon #1 is selected. • 1, the 3-colors-and-transparent display mode is selected.
0	**Hardware Icon #1 Display Enable:** When this bit is 1, icon #1 is enabled to display.

12.30 SR2C: Hardware Icon #2 Control and Miscellaneous PCI Register

I/O Port Address: 3C5

Index: 2C

Bit	Description	Reset State
7	PCI Bus Base Register 14h Enable [31:24]	0
6	PCI Bus Base Register 14h Byte Swap [31:24]	0
5	Hardware Icon #2 Display Memory Map Selection	0
4	Hardware Icon #2 Vertical Scanline Doubling	0
3	Hardware Icon #2 Horizontal Pixel Doubling	0
2	Hardware Icon #2 Blink Enable	0
1	Hardware Icon #2 Display Mode Select	0
0	Hardware Icon #2 Display Enable	0

Bit	Description
7	**PCI Bus Base Register 14h Enable:** • When this bit is 0, this address range is ignored. • When this bit is 1 and the CL-GD7548 is in PCI bus mode, Base register 14h bits [31:24] are decoded as a valid address range.
6	**PCI Bus Base Register 14h Byte Swap:** When this bit is 1 and the CL-GD7548 is in PCI bus mode: • Byte swapping is enabled for the Base register 14h[31:24] address range. • Byte[0] is swapped with byte[1], and byte[2] is swapped with byte[3].
5	**Hardware Icon #2 Display Memory Map Selection:** • When this bit is 0, display memory map 0 is selected for icon #2. • When this bit is 1, display memory map 1 is selected for icon #2.
4	**Hardware Icon #2 Vertical Scanline Doubling:** When this bit is 1: • Icon #2 displays 128 scanlines, and each scanline is replicated vertically. • Icon #2 extends down and forces all other icons down.
3	**Hardware Icon #2 Horizontal Pixel Doubling:** When this bit is 1: • Icon #2 displays 128 pixels, and each pixel is replicated horizontally. • Icon #2 expands to the right on the display.
2	**Hardware Icon #2 Blink Enable:** • When this bit is 0, icon #2 is steady state. • When this bit is 1, icon #2 blinks at one-half the text-cursor blink rate.
1	**Hardware Icon #2 Display Mode Select:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. • When this bit is 0, the 4-color display mode for icon #2 is selected. • When this bit is 1, the 3-colors-and-transparent display mode is selected.
0	**Hardware Icon #2 Display Enable:** When this bit is 1, icon #2 is enabled to display.

12.31 SR2D: Hardware Icon #3 Control and HIMEM Select Register

I/O Port Address: 3C5

Index: 2D

Bit	Description	Reset State
7	HIMEM[1] Reference Bit	0
6	HIMEM[0] Reference Bit	0
5	Hardware Icon #3 Display Memory Map Selection	0
4	Hardware Icon #3 Vertical Scanline Doubling	0
3	Hardware Icon #3 Horizontal Pixel Doubling	1
2	Hardware Icon #3 Blink Enable	1
1	Hardware Icon #3 Display Mode Select	1
0	Hardware Icon #3 Display Enable	1

Bit	Description
7:6	**HIMEM[1:0] Reference Bits:** These bits are extensions of display memory segment select bits in Extension register SR7[7:4]. The CL-GD7548 compares the value in these bits with the levels on the HIMEM[1:0] pins to define the valid upper-address space. • In VESA VL-Bus operations, when CPU bus address bits HIMEM[1:0] = SR2D[7:6] and CPU bus address bits A[23:20] = SR7[7:4], then the CL-GD7548 identifies the upper address as its CPU address-mapped area. • In PCI bus operations, when: — These two bits are non-zero, the chip is in linear memory mode. — Either these two bits or SR7[7:4] are non-zero, the PCI memory map is defined by PCI bus Base registers 10h or 14h (upper bytes). • For segmented addressing mode, these bits must be 0.
5	**Hardware Icon #3 Display Memory Map Selection:** • When this bit is 0, display memory map 0 is selected for icon #3. • When this bit is 1, display memory map 1 is selected for icon #3.
4	**Hardware Icon #3 Vertical Scanline Doubling:** When this bit is 1: • Icon #3 displays 128 scanlines, and each scanline is replicated vertically. • Icon #3 extends down and forces all other icons down.
3	**Hardware Icon #3 Horizontal Pixel Doubling:** When this bit is 1: • Icon #3 displays 128 pixels, and each pixel is replicated horizontally. • Icon #3 expands to the right on the display.
2	**Hardware Icon #3 Blink Enable:** When this bit is: • 0, icon #3 is steady state. • 1, icon #3 blinks at one-half the text-cursor blink rate.

12.31 SR2D: Hardware Icon #3 Control and HIMEM Select Register *(cont.)*

Bit	Description
1	**Hardware Icon #3 Display Mode Select:** The hardware icon is always 2 bits/pixel and is controlled by these two bits. When this bit is: • 0, the 4-color display mode for hardware icon #3 is selected. • 1, the 3-colors-and-transparent display mode is selected.
0	**Hardware Icon #3 Display Enable:** When this bit is 1, hardware icon #3 is enabled to display.

12.32 SR2E: Hardware Cursor Horizontal Position Extension Register

I/O Port Address: 3C5

Index: 2E

Bit	Description	Reset State
7	Early OVRW# Signal Delay [2]	0
6	Early OVRW# Signal Delay [1]	0
5	Early OVRW# Signal Delay [0]	0
4	Display Memory-Write Cycle Delay [1]	0
3	Display Memory-Write Cycle Delay [0]	1
2	Hardware Icon #0 Address Map Select [1]	1
1	Hardware Icon #0 Address Map Select [0]	1
0	Hardware Cursor Fine Horizontal Position [3]	1

Bit **Description**

7:5 **Early OVRW# Signal Delay [2:0]:**
These 3 bits define the time interval between the Video Overlay Window output from the CL-GD7548 and the data input from the external TV decoder.

- This time interval is used for a time differential adjustment that is intended to compensate for the Feature Connector system delay:
  - — *From* the time the OVRW# output is generated
  - — *To* the time Feature Connector data is presented to the CL-GD7548
- The FCEVIDEO# input must be externally synchronized from the OVRW# output to the data input.
- The table that follows shows early clock cycles for either 1× or 2× DCLKs.
  - — The programmed number of early clock cycles defines the delay between the assertion and de-assertion of OVRW# and the corresponding start and end of the Video Overlay Window.
  - — The 1× DCLKs are typically 25-MHz clocks that are used in clocking Graphics mode 1 for 16-bit pixels.
  - — The 2× DCLKs are typically 50-MHz clocks that are used in clocking Graphics mode 2 for 16-bit pixels.

SR2E			Total Early Clock Cycles	
[7]	[6]	[5]	1× DCLK	2× DCLK
0	0	0	0	3
0	0	1	Don't use	4
0	1	0	Don't use	5
0	1	1	0	6
1	0	0	1	7
1	0	1	2	8
1	1	0	Don't use	2
1	1	1	Don't use	1

12.32 SR2E: Hardware Cursor Horizontal Position Extension Register *(cont.)*

Bit | **Description**

4:3 **Display Memory Write Cycle Delay [1:0]:**

This 2-bit field is used to optimize the CL-GD7548 operation with respect to the system bus speed.

- This field affects only double-word (32-bit) display memory write cycles.
- After the CPU starts a 16-bit bus command, this field delays the start of a second 16-bit write cycle for display memory.
- The delays, which are in units of MCLKs, are programmed as explained in the table below. (The delays are in addition to the 1 MCLK delay.)

SR2E [4]	SR2E [3]	Delay Start of Display Memory Write Cycle By:	Conditions Under Which to Use:
0	0	3 MCLKs	Use for worst-case timing conditions.
0	1	2 MCLKs	Optimize the 33-MHz PCI bus. Optimize the 50-MHz VESA VL-Bus.
1	0	1 MCLK	Optimize the 33-MHz VESA VL-Bus.
1	1	0 MCLKs	Optimize the 20-MHz VESA VL-Bus.

2:1 **Hardware Icon #0 Address Map Select [1:0]:**

- When this field is zero, each icon has two memory maps assigned to it.
- When this field is non-zero, only hardware icon #0 can be used.
  - — Hardware icon #0 can have up to eight memory maps.
  - — The other hardware icons #1:#3 must be disabled.
  - — The number in SR2E[2:1] points to the pair of two icon maps selected by SR2A[5], but in this case, all maps go to icon #0 for display.
  - — In this order of significance, SR2E[2:1] and SR2A[5] select the eight memory maps for icon #0.

0 **Hardware Cursor Fine Horizontal Position [3]:**

This bit is the most-significant bit of a 4-bit field that is used with text that has 10-dot fonts (that is, character clocks), when in text or horizontally expanded graphics modes.

- The least-significant bits [2:0] are in Sequencer register SRX[7:5].
- When Extension register SR12[3] is 0, the CPU can modify the hardware cursor horizontal position.
- In non-expanded graphics modes, this bit is always 0.
- The coarse horizontal position is in Extension register SR10.

NOTE: When enabling a horizontal expansion from 640 to 800, the hardware cursor must be positioned within 10 dots.

12.33 SR2F: Half-Frame Accelerator FIFO Threshold for Surrounding Graphics

I/O Port Address: 3C5

Index: 2F

Bit	Description	Reset State
7	Standby Mode Enabled by Input on SBYI Pin	0
6	SUSPST# and SBYST# Configuration Select	0
5	Dual-Aperture Retry Enable	0
4	PCLK Disable	0
3	HFA FIFO Threshold for Surrounding Graphics [3]	1
2	HFA FIFO Threshold for Surrounding Graphics [2]	1
1	HFA FIFO Threshold for Surrounding Graphics [1]	1
0	HFA FIFO Threshold for Surrounding Graphics [0]	1

Bit	Description
7	**Standby Mode Enabled by Input on SBYI Pin:** If this bit is: • 0: — The Standby mode is disabled. — The ACTI / DDCD / FCEVIDEO# / SBYI pin is configured for DDCD. • 1, the Standby mode is enabled: — By input on the ACTI / DDCD / FCEVIDEO# / SBYI pin, if this pin is configured for the SBYI function (that is, SR23[6] is programmed for 0). The default configuration for this pin is SBYI. — By activity on the ACTI / DDCD / FCEVIDEO# / SBYI pin, if this pin is configured for the ACTI function (that is, SR23[2]6 is programmed for 1).
6	**SUSPST# and SBYST# Configuration Select:** This bit is used to configure the FCP[0] / FP[8] / SBYST# and FCP[1] / FP[9] / SUSPST# pins. • If this bit is 0, *and* SR24[7] is 1: — The FCP[0] / FP[8] / SBYST# pin is configured to output FCP[0]. — The FCP[1] / FP[9] / SUSPST# pin is configured to output FCP[1]. • If this bit is 1: — The FCP[0] / FP[8] / SBYST# pin is configured to output SBYST#. — The FCP[1] / FP[9] / SUSPST# pin is configured to output SUSPST#. • If this bit is 0, *and* SR24[7] is 0: — The FCP[0] / FP[8] / SBYST# pin is configured to input FCP[0]. — The FCP[1] / FP[9] / SUSPST# pin is configured to input FCP[1].
5	**Dual-Aperture Retry Enable:** When this is 1, it enables a dual-aperture retry only under the following conditions: • The CL-GD7548 is using the PCI bus Base 14h big-endian register. • The CL-GD7548 is not in the PCI bus Base 14h byte swap mode. • A BitBLT is in progress.

12.33 SR2F: Half-Frame Accelerator FIFO Threshold for Surrounding Graphics *(cont.)*

Bit	Description
4	**PCLK Disable:** This bit controls the LCD internal clock signal, PCLK. If this bit is: • 0, the clock is enabled at all times. • 1, the clock is enabled only if the LCD panel is enabled.
3:0	**Half-Frame Accelerator FIFO Threshold for Surrounding Graphics:** This 4-bit field affects the half-frame accelerator read FIFO for dual-scan LCDs. The half-frame accelerator read FIFO is 16 data stages deep and 32 bits wide. This field controls how many 32-bit data stages can be empty in the half-frame accelerator read FIFO before a new request can be made for a refill of the half-frame accelerator read FIFO. (At the same time that the half-frame accelerator read FIFO is emptied, it is refilled.) Example: If SR2F[3:0] = 4h, after only 4 of the 32 half-frame accelerator read FIFO stages are empty, a new request is made for new half-frame accelerator cycles. For this example, program a read FIFO threshold that is: • Low (2h to 4h) for 2 to 4 data stages for dual-scan monochrome STN panels. • Low (2h to 4h) for 2 to 4 data stages for 16-bpp and 24-bpp modes, even for a dual-scan color STN LCD, in order to minimize CRT-FIFO latency. • High (4h to 7h) for 4 to 7 data stages for dual-scan color STN panels. • Less than Ah for all other cases. • Never higher than Ah.

12.34 SR32: HFA FIFO Threshold in VW / PCI Bus Speed Register

I/O Port Address: 3CF

Index: 32

Bit	Description	Reset State
7	PCI Bus Speed Setup [1]	0
6	PCI Bus Speed Setup [0]	0
5	On-Chip DAC IREF Circuit Power Control	0
4	Cycle Chaining in Surrounding Graphics Area Enable	0
3	Cycle Chaining in VW Enable	0
2	Half-Frame Accelerator FIFO Threshold in VW	0
1	Half-Frame Accelerator FIFO Threshold in VW	0
0	Half-Frame Accelerator FIFO Threshold in VW	0

Bit **Description**

7:6 **PCI Bus Speed Setup [1:0]:**
These bits set the read-strobe generation timing, as shown in the following table:

SR32		When Resulting Memory Read Strobe Is Generated
[7]	[6]	
0	0	1 bus clock after FRAME# is sampled active-low
0	1	*Not defined!*
1	0	*Not defined!*
1	1	Only after IRDY# is active-low

5 **On-Chip DAC IREF Circuit Power Control:**
When this bit is:

- 0, the power to the on-chip DAC IREF circuit is turned off
- 1, the power to the on-chip DAC IREF circuit is turned on

12.34 SR32: HFA FIFO Threshold in VW / PCI Bus Speed Register *(cont.)*

Bit	Description
4	**Cycle Chaining in Surrounding Graphics Area Enable:** When this bit is 1, it enables cycle chaining for the CRT, frame buffer, and V-Port in the surrounding graphics area. (Cycle chaining prevents CPU cycles from intervening when there is not enough memory bandwidth to complete a cycle for the CRT, frame buffer, or V-Port.)
3	**Cycle Chaining in Video Window Enable:** When this bit is 1, it enables cycle chaining for the CRT, frame buffer, and V-Port in the Video Window. (Cycle chaining prevents CPU cycles from intervening when there is not enough memory bandwidth to complete a cycle for the CRT, frame buffer, or V-Port.)
2:0	**Half-Frame Accelerator FIFO Threshold inside the Video Window:** • This field allows another level of memory bandwidth optimization when using DSTN LCDs with the Video Window. • The value programmed in this field determines the number of CAS# cycles in the half-frame accelerator FIFO cycle in the Video Window.

12.35 SR33: CRT FIFO Request Threshold Register

I/O Port Address: 3CF

Index: 33

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	CPU Stop Enable	0
4	Test Bus #4 Select	0
3	CRT FIFO Request Threshold [3]	0
2	CRT FIFO Request Threshold [2]	0
1	CRT FIFO Request Threshold [1]	0
0	CRT FIFO Request Threshold [0]	0

Bit	Description
7:6	**Reserved**
5	**CPU Stop Enable:** This bit works in combination with SR34[7:4]. If this bit is set to 1, the Extension register bits SR34[7:4] prevent CPU cycles from starting and also terminate any ongoing CPU cycles.
4	**Test Bus #4 Select:** When this bit is 1, in the test mode the test bus TSTBUS4[17:0] is selected. The V-Port and Video Window signals are on this test bus. This bit is for test purposes only.

12.35 SR33: CRT FIFO Request Threshold Register *(cont.)*

Bit	Description
3:0	**CRT FIFO Request Threshold [3:0]:** • If Extension register bits SR20[2] and SRF[5] are both set to 1, then the SR33[3:0] bits can be used to program the CRT FIFO request threshold (that is, when the CRT memory cycle request is generated). • Programming bits SR33[3:0] to: — 0h ('0000') is equivalent to programming Ah ('1010'). Both settings have the result that after every 10 CRT FIFO reads, a CRT memory cycle request is asserted. — Fh ('1111') has the result that after every 15 CRT FIFO reads, a CRT memory cycle request is asserted.

SR20[2]	SRF[5]	SR33 [3]	SR33 [2]	SR33 [1]	SR33 [0]	When CRT FIFO Request Is Generated (Selected Bit Settings)
1	1	0	0	0	0	After every 10 CRT FIFO reads, a CRT memory cycle request is asserted.
		1	0	1	0	After every 10 CRT FIFO reads, a CRT memory cycle request is asserted.
		1	1	0	1	After every 13 CRT FIFO reads, a CRT memory cycle request is asserted.
		1	1	1	1	After every 15 CRT FIFO reads, a CRT memory cycle request is asserted.

12.36 SR34: CPU Stop Control Register

I/O Port Address: 3CF

Index: 34

Bit	Description	Reset State
7	CPU Stop before Half-Frame Accelerator Cycle	0
6	CPU Stop before CRT Cycle [1]	0
5	CPU Stop before CRT Cycle [0]	0
4	CPU Stop before V-Port Cycle	0
3	CPU Stop before VW Cycle [3]	0
2	CPU Stop before VW Cycle [2]	0
1	CPU Stop before VW Cycle [1]	0
0	CPU Stop before VW Cycle [0]	0

This register works in combination with Extension register bit SR33[5].

Bit — **Description**

7 — **CPU Stop before Half-Frame Accelerator Cycle:**
If this bit is 1, a CPU cycle is prevented from starting when (*n*-1) Half-Frame Accelerator FIFO levels are empty. (The *n* value is the threshold value programmed in Extension register SR2F[3:0] and SR32[2:0].)

6:5 — **CPU Stop before CRT Cycle [1:0]:**
If this 2-bit field is set to:

- '00', this field has no effect.
- Anything except '00', a CPU cycle is prevented from starting immediately before the CRT FIFO circuitry generates a cycle request. The following table gives values that determine when the CPU cycle is prevented from starting, in relation to the CRT cycle request.
- For each Graphics mode, this field has an optimum value that uses the display memory bandwidth most efficiently.

NOTE: In the table, *n* refers to the CRT FIFO threshold value programmed in SR33[3:0].

SR34		CPU Stop Before CRT Cycle
[6]	[5]	
0	0	No effect.
0	1	CPU cycle is prevented from starting when (*n* – 1) CRT FIFO levels empty.
1	0	CPU cycle is prevented from starting when (*n* – 2) CRT FIFO levels empty.
1	1	CPU cycle is prevented from starting when (*n* – 3) CRT FIFO levels empty.

12.36 SR34: CPU Stop Control Register *(cont.)*

Bit	Description
4	**CPU Stop before V-Port Cycle:** If this bit is1, a CPU cycle is prevented from starting when (*n*-1) V-Port FIFO levels are filled. (The *n* value is the threshold value programmed in Extension register CR51[7:5] and CR5A[2:0].)
3:0	**CPU Stop before Video Window Cycle [3:0]:** If the CRT generates an interrupt request *and* this 4-bit field is set to: • '0000', this field has no effect. • Anything except '0000': — These bits prevent CPU cycles from starting immediately before Video Window circuitry generates a cycle request and also terminate any ongoing CPU cycles. — The following table gives values that determine when the CPU cycle is prevented from starting, in relation to the Video Window cycle request.

SR34				CPU Early Stop Before VW Cycle
[3]	[2]	[1]	[0]	
0	0	0	0	No effect.
0	0	0	1	CPU is prevented from starting *n* VCLKs before the Video Window circuitry generates a cycle request, where *n* is the number programmed in SR34 [3:0]
to				
1	1	1	1	

12.37 GR9: Offset Register 0

I/O Port Address: 3CF

Index: 9

Bit	Description	Reset State
7	Offset 0 [7]	0
6	Offset 0 [6]	0
5	Offset 0 [5]	0
4	Offset 0 [4]	0
3	Offset 0 [3]	1
2	Offset 0 [2]	1
1	Offset 0 [1]	1
0	Offset 0 [1]	1

This register is used to access up to 2 Mbytes of display memory with up to 16-Kbyte granularity.

Bit	Description
7:0	**Offset Register 0 [7:0]:** • This register is disabled if the PCI bus mode is enabled *and* a dual aperture is used with big-endian PCI bus Base register 14h. • This register is enabled when one of the following conditions is true: — GRB[0] is 0 — GRB[0] is 1 *and* CPU address bit A[15] is 0 • When one of the above conditions is true *and* GRB[5] is 0: — The register's offset value is added to the contents of XA (bus addresses A[19:12]) to provide XMA, an address into display memory. — Access is for 1 Mbyte of display memory with 4-Kbyte granularity. • When one of the above conditions is true *and* GRB[5] is 1: — The register's offset value is added to the contents of XA (bus addresses A[20:14]) to provide XMA, an address into display memory. — Access is for up to 2 Mbytes of display memory with 16-Kbyte granularity. **XMA.** XMA is the display memory address, prior to modification by address wrap controls. XMA = (Bus Address XA) + (value from Offset register GR9 or GRA). **XA.** XA is the address on the bus, with bits [16] and [15] possibly forced to a 0 as indicated in the following table.

12.37 GR9: Offset Register 0 *(cont.)*

Bit	Description
7:0 *(cont.)*	**Offset Register 0 [7:0]** *(cont.)*:

Configuration		Bus Address XA		
If Display Memory is:	**And Register Setting:**	**[16]**	**[15]**	**[14:0]**
128 Kbytes	GR6[3:2] is 00	A[16]	A[15]	A[14:0]
64 Kbytes	GR6[3:2] is 01 *and* GRB[0] is 0 (Offset 1 disabled)	0	A[15]	A[14:0]
64 Kbytes	GR6[3:2] is 01 *or* GRB[0] is 1 (Offset 1 enabled)	0	0	A[14:0]

The XA bus address is summed with the contents of an Offset register with one of three relative alignments, according to the configuration indicated in the three tables that follow:

Bus Address (XA)	0	0	0	XA[16]	XA[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[7]	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]
= Display Memory Address (XMA)	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Bus Address	0	0	0	0	XA[16]	XA[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Bus Address	LA[20]	LA[19]	LA[18]	LA[17]	A[16]	A[15]	A[14]	A[13]	A[12]
+ Offset Value	Offset[6]	Offset[5]	Offset[4]	Offset[3]	Offset[2]	Offset[1]	Offset[0]	0	0
= Display Memory Address	XMA[20]	XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

12.38 GRA: Offset Register 1

I/O Port Address: 3CF

Index: A

Bit	Description	Reset State
7	Offset 1 [7]	0
6	Offset 1 [6]	0
5	Offset 1 [5]	0
4	Offset 1 [4]	0
3	Offset 1 [3]	1
2	Offset 1 [2]	1
1	Offset 1 [1]	1
0	Offset 1 [1]	1

This register is used to access up to 2 Mbytes of display memory with up to 16-Kbyte granularity.

Bit	Description
7:0	**Offset 1 [7:0]:** • This register is disabled: — If the PCI bus mode is enabled *and* a dual aperture is used with big-endian PCI bus Base register 14h. — When Extension register GRB[0] is 0. • This register is enabled if Extension register GRB[0] is set to 1. When GRB[0] is 1 *and*: — CPU bus address bit A[15] is 1, the contents of GRA[7:0] are added to the contents of CPU bus address bits A[19:12] to provide access to up to 1 Mbyte of addresses into display memory, with 4-Kbyte granularity. — GRB[5] is 1, the contents of GRA[6:0] are added to the contents of CPU bus address bits A[20:14] to provide access to up to 2 Mbytes of addresses into display memory, with 16-Kbyte granularity.

12.39 GRB: Graphics Controller Mode Extensions Register

I/O Port Address: 3CF

Index: B

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Offset Granularity	0
4	16-Bit Pixel Enhanced Write Enable	0
3	8-Byte-Wide Display Memory Data Latches Enable	1
2	Extended Write Modes Enable	1
1	By-8 Addressing Enable	1
0	Offset 1 Enable	1

This register is used to enable or disable extended write modes which provide enhanced performance.

Bit	Description
7:6	**Reserved**
5	**Offset Granularity:** When this bit is programmed to 1, the display memory has 16-Kbyte granularity. • Extension register SR7[4] (the least-significant bit of a 1-Mbyte address page) becomes a 'don't care'. • Linear address memory mapping becomes 2 Mbytes on any 2-Mbyte boundary. When this bit is programmed to 0, the display memory has 4-Kbyte granularity.
4	**16-Bit Pixel Enhanced Write Enable:** GRB[2] must be 1 in order to enable this bit. When both GRB[2] and GRB[4] are programmed to 1, the CL-GD7548 executes the following enhanced write modes when Extended Write modes 4 and 5 are enabled and executed: • **By-16 Addressing Enabled:** The system address is shifted by 4, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (16-byte) block in display memory. • **16-Byte Transfer Enabled:** Up to 16 bytes (8 pixels) can be written into display memory for each CPU byte transfer. • **Extension Registers GR10 and GR11 Enabled:** GR10 and GR11 are enabled as foreground and background color extensions. • **Sequencer Register SR2 Doubling Enabled:** Each bit of SR2 is used as a pixel write mask for two bytes (one pixel).

12.39 GRB: Graphics Controller Mode Extensions Register *(cont.)*

Bit	Description
3	**8-Byte-Wide Display Memory Data Latches Enable:** When this bit is 1, display memory data latches are 8 bytes wide rather than the normal 4 bytes.
2	**Extended Write Modes Enable:** When this bit is 1, the CL-GD7548 enables and executes the following extended write modes: • Graphics Controller register GR5[2] is enabled, which also enables Extended Write modes 4 and 5. • Graphics Controller register GR0 is extended from 4 bits to 8 bits. • Graphics Controller register GR1 is extended from 4 bits to 8 bits. • Sequencer register SR2 is extended from 4 bits to 8 bits. • Extension register GRB[4] is enabled, which also enables enhanced writes for 16-bit pixels. • 8-Byte Transfer Enabled: — When GRB[1] is 1 *and* GRB[4] is 0, up to 8 bytes (8 pixels) can be written into display memory for each CPU byte transferred. — When GRB[4] is 1, up to 16 bytes can be written into display memory for color expansion.
1	**By-8 Addressing Enable:** • When this bit is 1, the system address is shifted by 3, relative to true packed-pixel addressing, so that each system byte address points to a different 8-pixel (8-byte) block in display memory. • When GRB[4] is 1, this bit is a 'don't care'.
0	**Offset 1 Enable:** When this bit is programmed to: • 0, the value in system address AD15 is ignored. — As a result, Extension register GR9 (Offset 0) is always selected. — This bit must always be cleared to 0 for 1 Mbyte of linear addressing. • 1, the value in system address AD15 is used to select either Offset 0 (Extension register GR9), or Offset 1 (Extension register GRA). — When system address AD15 is 0, Offset 0 is selected. — When system address AD15 is 1, Offset 1 is selected.

12.40 GRC: Color Key Compare Register

I/O Port Address: 3CF

Index: C

Bit	Description	Reset State
7	Color Key Compare [7]	0
6	Color Key Compare [6]	0
5	Color Key Compare [5]	0
4	Color Key Compare [4]	0
3	Color Key Compare [3]	1
2	Color Key Compare [2]	1
1	Color Key Compare [1]	1
0	Color Key Compare [0]	1

This register contains an 8-bit value that is compared to video data. For more information, refer to the application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.

Bit	Description
7:0	**Color Key Compare [7:0]:** This register contains an 8-bit value that is compared to the video data. When Extension register CR1A[3:2] is either '10' or '11', then if there is a match between this value in GRC[7:0] and the video data value, the video data pixel is replaced with data from the Feature Connector.

12.41 GRD: Color Key Compare Mask Register

I/O Port Address: 3CF

Index: D

Bit	Description	Reset State
7	Color Key Compare Mask [7]	0
6	Color Key Compare Mask [6]	0
5	Color Key Compare Mask [5]	0
4	Color Key Compare Mask [4]	0
3	Color Key Compare Mask [3]	1
2	Color Key Compare Mask [2]	1
1	Color Key Compare Mask [1]	1
0	Color Key Compare Mask [0]	1

This register contains an 8-bit mask under which the color key comparison of GRC is made. For more information, refer to the application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.

Bit	Description
7:0	**Color Key Compare Mask [7:0]:** A bit value of 1 for a GRD bit causes the corresponding video data bit to be masked out and *not* participate in the color comparison.

12.42 GRE: PCI Bus Burst-Write and Green PC Control Register

I/O Port Address: 3CF

Index: E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	PCI Bus Burst-Write Mode Enable	0
3	PCI Bus Extensive Burst-Write Mode Enable	1
2	Display Power Management Signaling (Green PC) Control [1]	1
1	Display Power Management Signaling (Green PC) Control [0]	1
0	DCLK Output Divided By Two	1

Bit	Description
7:5	**Reserved**
4	**PCI Bus Burst-Write Mode Enable:** • When the PCI bus (that is, Extension register SR22[0] = 1) is selected, *and* this bit is 1, the CPU can execute burst writes during vertical non-display time. • When the system BitBLT (bit block transfer) is enabled, the CL-GD7548 automatically disables this burst-write function. • The CL-GD7548 does not support PCI bus burst-read cycles.
3	**PCI Bus Extensive Burst-Write Mode Enable:** When the PCI bus is selected, *and* this bit is 1, the CPU can execute PCI bus burst writes anytime during a frame.
2:1	**Display Power Management Signaling (Green PC) Control [1:0]:** These two bits control the CRT monitor power as specified in the DPMS (Display Power Management Signaling) specification, as shown in the following table:

GRE [2]	GRE [1]	CRT Monitor Power Mode	VSYNC Activity	HSYNC Activity	DAC Power	CL-GD7548 Power Management Mode
0	0	On	Pulsing	Pulsing	On	Active
0	1	Standby	Pulsing	Static at MISC[6] inactive level	Off	Active, Standby, or Suspend
1	0	Suspend	Static at MISC[7] inactive level	Pulsing	Off	Active, Standby, or Suspend
1	1	Off	Static at MISC[7] inactive level	Static at MISC[6] inactive level	Off	Active, Standby, or Suspend

12.42 GRE: PCI Bus Burst-Write and Green-PC Control Register *(cont.)*

Bit	Description
2:1 (*cont.*)	**Display Power Management Signaling (Green PC) Control [1:0]** *(cont.)*: Because the DPMS CRT power-management modes are not related to the CL-GD7548 controller power-management modes, they can be independently programmed, except for the following restrictions: • Suspend mode: — The BIOS can program any DPMS power-saving mode for the CRT, but the BIOS programming must be done prior to placing the CL-GD7548 into Suspend mode. — The 32-kHz input to the CL-GD7548 must be used to provide any synchronization pulse required by the DPMS. • Standby mode: — The CL-GD7548 Standby mode is timer-driven (that is, hardware-controlled). As a result, — The DPMS STANDBY signal must be forced by hardware. — Software control of the DPMS is not allowed. • LCD-only mode: — When the CL-GD7548 is in LCD-only mode, the BIOS must set GRE[2:1] to '11' to power off any CRT that may be connected to the notebook computer. • The inactive static VSYNC and HSYNC signal levels must be determined by the polarity selection in External/General register MISC[7:6]. — When MISC[7] is 1, the inactive level is low for the VSYNC signal. — When MISC[6] is 1, the inactive level is low for the HSYNC signal.
0	**DCLK Output, Divided By Two:** When this bit is: • 0, the CL-GD7548 operates normally. • 1, the CL-GD7548 emulates external DAC clocking mode 1. — The DCLK rising edge can be used to clock a 16-bit data pixel low byte. — The DCLK falling edge can be used to clock a 16-bit data pixel high byte. — The option of setting this bit to 1: — Works only for the CRT-only mode. — Does not work for the LCD or SimulSCAN mode. When this bit is 1, the clock to the LCD section is divided by two, which prevents the LCD from working properly.

12.43 GR10: 16-Bit Pixel Background Color High Register

I/O Port Address: 3CF

Index: 10

Bit	Description	Reset State
7	Background Color [15]	1
6	Background Color [14]	1
5	Background Color [13]	1
4	Background Color [12]	1
3	Background Color [11]	1
2	Background Color [10]	1
1	Background Color [9]	1
0	Background Color [8]	1

This register contains the most-significant 8 bits of the 16-bit background color field for Extended Write mode 5. For more information on color expansion, refer to Appendix D.

Bit	Description
7:0	**Background Color [15:8]:** • The contents of this register are the most-significant 8 bits of the 16-bit background color for Extended Write mode 5. • The contents of Graphics Controller register GR0 are the least-significant 8 bits of the background color for Extended Write mode 5.

12.44 GR11: 16-Bit Pixel Foreground Color High Register

I/O Port Address: 3CF

Index: 11

Bit	Description	Reset State
7	Foreground Color [15]	1
6	Foreground Color [14]	1
5	Foreground Color [13]	1
4	Foreground Color [12]	1
3	Foreground Color [11]	1
2	Foreground Color [10]	1
1	Foreground Color [9]	1
0	Foreground Color [8]	1

This register contains the most-significant 8 bits of the 16-bit foreground color field for Extended Write modes 5 and 4. For more information on color expansion, refer to Appendix D.

Bit	Description
7:0	**Foreground Color [15:8]:** • The contents of this register are the most-significant 8 bits of the 16-bit foreground color for Extended Write modes 5 and 4. • The contents of Graphics Controller register GR1 are the least-significant 8 bits of the foreground color for Extended Write modes 5 and 4.

12.45 GR20: BitBLT Width Low Register

I/O Port Address: 3CF

Index: 20

Bit	Description	Reset State
7	BitBLT Width [7]	1
6	BitBLT Width [6]	1
5	BitBLT Width [5]	1
4	BitBLT Width [4]	1
3	BitBLT Width [3]	1
2	BitBLT Width [2]	1
1	BitBLT Width [1]	1
0	BitBLT Width [0]	1

This register contains the least-significant 8 bits of the 11-bit BitBLT (bit block transfer) width field.

Bit	Description
7:0	**BitBLT Width [7:0]:** • These bits make up the BitBLT Width byte 0, the least-significant 8 bits of the 11-bit value BitBLT width field. • For details refer to Extension register GR21, which contains the most-significant 3 bits.

12.46 GR21: BitBLT Width High Register

I/O Port Address: 3CF

Index: 21

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	BitBLT Width [10]	1
1	BitBLT Width [9]	1
0	BitBLT Width [8]	1

This register contains the most-significant 3 bits of the 11-bit BitBLT width field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:3	**Reserved**
2:0	**BitBLT Width [10:8]:** • These bits make up the BitBLT Width byte 1, the most-significant 3 bits of the 11-bit value specifying in bytes the areas involved in the BitBLT width field. • The least-significant bits are in Extension register GR20.

12.47 GR22: BitBLT Height Low Register

I/O Port Address: 3CF

Index: 22

Bit	Description	Reset State
7	BitBLT Height [7]	0
6	BitBLT Height [6]	0
5	BitBLT Height [5]	0
4	BitBLT Height [4]	0
3	BitBLT Height [3]	1
2	BitBLT Height [2]	1
1	BitBLT Height [1]	1
0	BitBLT Height [0]	1

This register contains the least-significant 8 bits of the 10-bit BitBLT height field.

Bit	Description
7:0	**BitBLT Height [7:0]:** • These bits make up the BitBLT Height byte 0, the least-significant 8 bits of the 10-bit value of the BitBLT height field. • For details refer to Extension register GR23, which contains the most-significant 2 bits.

12.48 GR23: BitBLT Height High Register

I/O Port Address: 3CF

Index: 23

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Reserved	
1	BitBLT Height [9]	1
0	BitBLT Height [8]	1

This register contains the most-significant 2 bits of the 10-bit BitBLT height field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:2	**Reserved**
1:0	**BitBLT Height [9:8]:** • These bits make up the BitBLT Height byte 1, the most-significant 2 bits of the 10-bit value specifying in scanlines the areas involved in the BitBLT height field. • The least-significant bits are in Extension register GR22.

12.49 GR24: BitBLT Destination Pitch Low Register

I/O Port Address: 3CF

Index: 24

Bit	Description	Reset State
7	BitBLT Destination Pitch [7]	0
6	BitBLT Destination Pitch [6]	0
5	BitBLT Destination Pitch [5]	0
4	BitBLT Destination Pitch [4]	0
3	BitBLT Destination Pitch [3]	0
2	BitBLT Destination Pitch [2]	0
1	BitBLT Destination Pitch [1]	1
0	BitBLT Destination Pitch [0]	1

This register contains the least-significant 8 bits of the 12-bit BitBLT destination pitch field.

Bit	Description
7:0	**BitBLT Destination Pitch [7:0]:** • These bits make up the BitBLT Destination Pitch byte 0, the least-significant 8 bits of the 12-bit value BitBLT destination pitch field. • For details refer to Extension register GR25, which contains the most-significant 4 bits.

12.50 GR25: BitBLT Destination Pitch High Register

I/O Port Address: 3CF

Index: 25

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BitBLT Destination Pitch [11]	0
2	BitBLT Destination Pitch [10]	0
1	BitBLT Destination Pitch [9]	1
0	BitBLT Destination Pitch [8]	1

This register contains the most-significant 4 bits of the 12-bit BitBLT destination pitch field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:4	**Reserved**
3:0	**BitBLT Destination Pitch [11:8]:** • These bits make up the BitBLT Destination Pitch byte 1, the most-significant 4 bits of the 12-bit value specifying the destination pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT. • The least-significant bits are in Extension register GR24.

12.51 GR26: BitBLT Source Pitch Low Register

I/O Port Address: 3CF

Index: 26

Bit	Description	Reset State
7	BitBLT Source Pitch [7]	0
6	BitBLT Source Pitch [6]	0
5	BitBLT Source Pitch [5]	0
4	BitBLT Source Pitch [4]	0
3	BitBLT Source Pitch [3]	1
2	BitBLT Source Pitch [2]	1
1	BitBLT Source Pitch [1]	1
0	BitBLT Source Pitch [0]	1

This register contains the least-significant 8 bits of the 12-bit BitBLT source pitch field.

Bit	Description
7:0	**BitBLT Source Pitch [7:0]:** • These bits make up the BitBLT Source Pitch byte 0, the least-significant 8 bits of the BitBLT source pitch field. • For details refer to Extension register GR27, which contains the most-significant 4 bits.

12.52 GR27: BitBLT Source Pitch High Register

I/O Port Address: 3CF

Index: 27

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	BitBLT Source Pitch [11]	1
2	BitBLT Source Pitch [10]	1
1	BitBLT Source Pitch [9]	1
0	BitBLT Source Pitch [8]	1

This register contains the most-significant 4 bits of the 12-bit BitBLT source pitch field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:4	**Reserved**
3:0	**BitBLT Source Pitch [11:8]:** • These bits make up the BitBLT Source Pitch byte 1, the most-significant 4 bits of the 12-bit value specifying the source pitch (that is, the scanline-to-scanline byte address offset) of the areas involved in a BitBLT. • The least-significant bits are in Extension register GR26.

12.53 GR28: BitBLT Destination Start Address Low Register

I/O Port Address: 3CF

Index: 28

Bit	Description	Reset State
7	BitBLT Destination Start Address [7]	1
6	BitBLT Destination Start Address [6]	1
5	BitBLT Destination Start Address [5]	1
4	BitBLT Destination Start Address [4]	1
3	BitBLT Destination Start Address [3]	1
2	BitBLT Destination Start Address [2]	1
1	BitBLT Destination Start Address [1]	1
0	BitBLT Destination Start Address [0]	1

This register contains the least-significant 8 bits of the 21-bit BitBLT destination start field.

Bit	Description
7:0	**BitBLT Destination Start Address [7:0]:** • These bits make up the BitBLT Destination Start Address byte 0, the least-significant 8 bits of the BitBLT destination start field. • The other bits of this field are in Extension registers GR29 and GR2A. • For details on this field, refer to Extension register GR2A.

12.54 GR29: BitBLT Destination Start Address Middle Register

I/O Port Address: 3CF

Index: 29

Bit	Description	Reset State
7	BitBLT Destination Start Address [15]	0
6	BitBLT Destination Start Address [14]	0
5	BitBLT Destination Start Address [13]	0
4	BitBLT Destination Start Address [12]	0
3	BitBLT Destination Start Address [11]	1
2	BitBLT Destination Start Address [10]	1
1	BitBLT Destination Start Address [9]	1
0	BitBLT Destination Start Address [8]	1

This register contains the middle 8 bits of the 21-bit BitBLT destination start field.

Bit	Description
7:0	**BitBLT Destination Start Address [15:8]:** • These bits make up the BitBLT Destination Start Address byte 1, the middle 8 bits of the BitBLT destination start field. • The other bits of this field are in Extension registers GR28 and GR2A. • For details on this field, refer to Extension register GR2A.

12.55 GR2A: BitBLT Destination Start Address High Register

I/O Port Address: 3CF

Index: 2A

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BitBLT Destination Start Address [20]	0
3	BitBLT Destination Start Address [19]	1
2	BitBLT Destination Start Address [18]	1
1	BitBLT Destination Start Address [17]	1
0	BitBLT Destination Start Address [16]	1

This register contains the most-significant 5 bits of the 21-bit BitBLT destination start field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:5	**Reserved**
4:0	**BitBLT Destination Start Address [20:16]:** • These bits make up the BitBLT Destination Start Address byte 2, the most-significant 5 bits of the 21-bit BitBLT destination start value that specifies the byte address of the beginning destination pixel for a BitBLT. • The other bits of this field are in Extension registers GR28 and GR29. • If Extension register GR31[7] is set to 1, a write to this register starts a BitBLT operation. If a BitBLT operation is in progress, the BitBLT that triggers another BitBLT operation as soon as the current BitBLT finishes.

12.56 GR2C: BitBLT Source Start Address Low Register

I/O Port Address: 3CF

Index: 2C

Bit	Description	Reset State
7	BitBLT Source Start Address [7]	0
6	BitBLT Source Start Address [6]	0
5	BitBLT Source Start Address [5]	0
4	BitBLT Source Start Address [4]	0
3	BitBLT Source Start Address [3]	1
2	BitBLT Source Start Address [2]	1
1	BitBLT Source Start Address [1]	1
0	BitBLT Source Start Address [0]	1

This register contains the least-significant 8 bits of the 21-bit BitBLT source start field.

Bit	Description
7:0	**BitBLT Source Start Address [7:0]:** • These bits make up the BitBLT Source Start Address byte 0, the least-significant 8 bits of the BitBLT source start field. • The other bits of this field are in Extension registers GR2D and GR2E. • For details on this field, refer to Extension register GR2E.

12.57 GR2D: BitBLT Source Start Address Middle Register

I/O Port Address: 3CF

Index: 2D

Bit	Description	Reset State
7	BitBLT Source Start Address [15]	0
6	BitBLT Source Start Address [14]	0
5	BitBLT Source Start Address [13]	0
4	BitBLT Source Start Address [12]	0
3	BitBLT Source Start Address [11]	1
2	BitBLT Source Start Address [10]	1
1	BitBLT Source Start Address [9]	1
0	BitBLT Source Start Address [8]	1

This register contains the middle 8 bits of the 21-bit BitBLT source start field.

Bit	Description
7:0	**BitBLT Source Start Address [15:8]:** • These bits make up the BitBLT Source Start Address byte 1, the middle 8 bits of the BitBLT source start field. • The other bits of this field are in Extension registers GR2C and GR2E. • For details on this field, refer to Extension register GR2E.

12.58 GR2E: BitBLT Source Start Address High Register

I/O Port Address: 3CF

Index: 2E

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	BitBLT Source Start Address [20]	0
3	BitBLT Source Start Address [19]	1
2	BitBLT Source Start Address [18]	1
1	BitBLT Source Start Address [17]	1
0	BitBLT Source Start Address [16]	1

This register contains the most-significant 5 bits of the 21-bit BitBLT source start. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:5	**Reserved**
4:0	**BitBLT Source Start Address [20:16]:** • These bits make up the BitBLT Source Start Address byte 2, the most-significant 5 bits of the 21-bit BitBLT source start value that specifies the byte address of the beginning source pixel for a BitBLT. • The other bits of this field are in Extension registers GR2C and GR2D.

12.59 GR30: BitBLT Mode Register

I/O Port Address: 3CF

Index: 30

Bit	Description	Reset State
7	Color Expand Enable	1
6	8 × 8 Source Pattern Copy Enable	1
5	Reserved	
4	Color Expand / Transparency Width	1
3	Transparency Compare Enable	1
2	BitBLT Source Display Memory / System Memory	1
1	BitBLT Destination Display Memory / System Memory	1
0	BitBLT Direction	1

This register contains the bits that specify the BitBLT (bit block transfer) details, but not the BitBLT raster operation. For more information on the BitBLT, refer to Appendix A.

Bit — **Description**

7 — **Color Expand Enable:**
When this bit is programmed to:

- 0, the raster operation source is the pixel data read from the source.
- 1, the raster operation source is the expanded result from the bit-mapped source.
  - — The destination must be screen memory.
  - — The direction must be incremental.
  - — Graphics Controller registers GR0 and GR1 and Extension registers GR10 and GR11 are used for bit-map color-expanded BitBLT operations.
  - — When the source data is expanded, the most-significant bit of the first source byte becomes the first pixel in the screen memory destination.
  - — For color-expanded BitBLTs (the source is system memory or display memory), each logical line must be an even byte.
    - — Source bytes must be completely used. As a result, when a logical line is not an even multiple of eight pixels, 'dummy' bits are used to fill it out to an even byte.
    - — 'Dummy' bits are ignored under control of the BitBLT width setting.
  - — When the source of color-expanded data is display memory, the source starting address must be on a 4-byte boundary, and the addressing is always linear. (The source pitch is ignored.)
  - — For information regarding color expansion, refer to Appendix D.

12.59 GR30: BitBLT Mode Register *(cont.)*

Bit | **Description**

6 — **8 × 8 Source Pattern Copy Enable:**

When this bit is 1, the source pattern is copied repeatedly to the destination area.

- The source pattern must be aligned on a byte boundary.
- The source pattern is linear-addressed data in one of three arrangements as shown in the following table.

Operating Mode	Source Pattern Arrangement
Color Extension Enabled (That is, GR30[7] = 1 *and* GR30[6] = 1.)	8 bytes of monochrome bitmap for the 8 × 8 source pattern
8-bit-pixel	64 bytes of color data for 64 pixels
16-bit-pixel	128 bytes of color data for 64 pixels

5 — **Reserved**

4 — **Color Expand / Transparency Width:**

- When GR30[7] is 1 *and* this bit is:
  - — 0, the bit-mapped source is expanded to 8 bits/pixel.
  - — 1, the bit-mapped source is expanded to 16 bits/pixel.
- When GR30[6] is 1 *and* this bit is:
  - — 0, the color depth is 8 bits/pixel.
  - — 1, the color depth is 16 bits/pixel.
- When GR30[3] is 1 *and* this bit is:
  - — 0, the transparency compare is on 8-bit pixels.
  - — 1, the transparency compare is on 16-bit pixels.

3 — **Transparency Compare Enable:**

When this bit is:

- 0, each pixel data bit is written to the destination without regard to the contents of Extension registers GR34 and GR35.
- 1, for each pixel data bit, the result of the raster operation is compared to the transparent color in Extension registers GR34 and GR35.
  - — When the compare is a match, data bits are not written to the destination.
  - — When the compare is not a match, data bits are written to the destination.
  - — When the color-expand BitBLT is to be used with an opaque foreground and a transparent background (similar to Extended Write mode 4), the transparency feature must be used, and the transparent color must be set to the background color.

12.59 GR30: BitBLT Mode Register *(cont.)*

Bit	Description
2	**BitBLT Source Display Memory / System Memory:** • When this bit is 0, the BitBLT source is display memory. • When this bit is 1, the BitBLT source is system memory. — The CPU performs the system bus transfers, but the CL-GD7548 ignores the address provided with such transfers. — The CPU is required to transfer data in increments of four bytes. When the total number of bytes moved for a BitBLT is not a multiple of four, the CPU must write 'extra' bytes. — System memory-to-system memory BitBLTs are not allowed. • When system memory-to-display memory BitBLTs are being executed: — 16-bit host transfers must be used, or the system becomes non-operative. — If the BitBLTs involve color expansion, Extension registers GR2C, GR2D, and GR2E (the BitBLT Source Start registers) must be cleared to 0.
1	**BitBLT Destination Display Memory / System Memory:** • When this bit is 0, the BitBLT destination is display memory. • When this bit is 1, the BitBLT destination is system memory. — The CPU performs the system bus transfers, but the CL-GD7548 ignores the address provided with such transfers. — The CPU is required to transfer data in increments of four bytes. When the total number of bytes moved for a BitBLT is not a multiple of four, the CPU must read 'extra' bytes. — System memory-to-system memory BitBLTs are not allowed. • When system memory-to-display memory BitBLTs are being executed, 16-bit host transfers must be used, or the system becomes non-operative.
0	**BitBLT Direction:** When this bit is: • 0: — The source and destination addresses are incremented. — The BitBLT proceeds from lower addresses to higher addresses. • 1: — The source and destination addresses are decremented. — The BitBLT proceeds from higher addresses to lower addresses. — The starting address is the highest addressed byte in each area.

12.60 GR31: BitBLT Start / Status Register

I/O Port Address: 3CF

Index: 31

Bit	Description	Reset State
7	BitBLT Automatic Start	1
6	Reserved	
5	Reserved	
4	Buffered Registers Status (Read Only)	1
3	BitBLT Reset Status (Read Only)	1
2	BitBLT Reset	1
1	BitBLT Start	1
0	BitBLT Operation Status (Read Only)	1

This register contains bits for starting a BitBLT and monitoring its status. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7	**BitBLT Automatic Start:** This bit is used in combination with GR2A to allow a fast BitBLT start. When Extension register GR2A is written *and* this bit is: • 0, the BitBLT does not start automatically. In this case, to start the BitBLT, GR31[1] must be set to 1. • 1, the BitBLT starts automatically, using data in the buffered BitBLT registers. — The buffered BitBLT registers are the following: — For BitBLT color expansion, buffered registers are Graphics Controller registers GR0 and GR1 and Extension registers GR10 and GR11. — For BitBLT control, buffered registers are Extension registers GR20:GR2A, GR2C:GR2E, GR30, and GR32. — After the BitBLT starts, GR31[4] is cleared to 0. — If a BitBLT is in progress and GR2A is written, GR31[7] posts a start, which triggers another BitBLT. — In setting up a BitBLT, the GR2A[4:0] bits must be written last.
6:5	**Reserved**

12.60 GR31: BitBLT Start / Status Register *(cont.)*

Bit	Description
4	**Buffered Registers Status (Read Only):** When this bit is: • 0, the CL-GD7548 signals to the software driver that double buffered registers are available, that is, a BitBLT can be programmed. This bit is cleared to 0: — When the BitBLT resets (that is, GR31[2] is set to 1). — After the BitBLT starts in one of the two following ways: — GR31[7] is set to 1 *and* GR2A[4:0] is written. — GR31[1] is set to 1. • 1, the CL-GD7548 signals to the software driver that double buffered registers are not available and cannot be programmed, as they are already loaded with data and waiting for the start of a BitBLT. — For CL-GD7548 AA or AB, this bit is set on the first write to any of the buffered BitBLT registers mentioned in GR31[7]. — For CL-GD7548 BC, this bit is set only when Extension register GR2A is written to.
3	**BitBLT Reset Status (Read Only):** This bit is set to 1 at the start of a BitBLT. • When the BitBLT operation resets (refer to GR32[2]), this bit clears to 0. • When the BitBLT operation suspends (refer to GR31[1]), this bit remains a 1.
2	**BitBLT Reset:** • This bit must be cleared to 0 before any BitBLT operations are attempted. • When this bit is set to 1: — The entire BitBLT engine is immediately reset and any operation in progress is terminated. The operation cannot be restarted. — GR31[3] clears to 0, the GR31[4] is reset.
1	**BitBLT Start:** • When this bit is set to 1, the BitBLT starts with the next available display memory cycle. GR31[0] must be monitored to determine when the BitBLT completes. • This bit clears to 0 when the BitBLT completes. • The BitBLT can be suspended by clearing this bit to 0. In this case, — The BitBLT suspends at the end of the current scanline. — Extension registers GR22 and GR23 (the BitBLT Height registers) reflect the scanline count for the last completed transfer. — Extension register bit GR31[3] remains a 1. — A suspended BitBLT may resume by setting this bit GR31[1] to 1.
0	**BitBLT Operation Status (Read Only):** When this bit is a: • 0, it indicates a BitBLT operation is not in progress or is complete. • 1, it indicates a BitBLT operation is in progress.

12.61 GR32: BitBLT Raster Operation (ROP) Function Register

I/O Port Address: 3CF

Index: 32

Bit	Description	Reset State
7	BitBLT Raster Operation Function [7]	0
6	BitBLT Raster Operation Function [6]	0
5	BitBLT Raster Operation Function [5]	0
4	BitBLT Raster Operation Function [4]	0
3	BitBLT Raster Operation Function [3]	1
2	BitBLT Raster Operation Function [2]	1
1	BitBLT Raster Operation Function [1]	1
0	BitBLT Raster Operation Function [0]	1

This register selects a raster operation function.

Bit **Description**

7:0 **BitBLT Raster Operation Function [7:0]:**
This 8-bit value selects from 1 to 16 two-operand ROP (raster operation) functions, as indicated in the table that follows.

NOTES:

1) Source and Pattern use the same ROP number for the same logical operation.

2) Raster operations that do not use the Source (such as ~D), must not be used when color expansion is selected.

3) S = Source
D = Destination
P = Pattern
+ = OR
• = AND
~ = Inversion (not)
x = Exclusive OR
≠ = Not equal

Logical Function		GR32 [7:0] ROP Number (hex)	Microsoft® Name	Microsoft® ROP
Z (Reverse Polish Notation)	Z (Algebraic Notation)			
0	0	00	BLACKNESS	00000042
1	1	0E	WHITENESS	00FF0062
S	S	0D	SRCCOPY	00CC0020
P	P	0D	PATCOPY	00F00021
D	D	06	–	00AA0029
S~	~S	D0	NOTSRCCOPY	00330008
P~	~P	D0	–	000F0001

12.61 GR32: BitBLT Raster Operation Function Register *(cont.)*

Bit	Description
7:0 *(cont.)*	**Raster Operation Function [7:0]:** *(cont.)*

Logical Function		GR32 [7:0] ROP Number (hex)	Microsoft® Name	Microsoft® ROP
Z (Reverse Polish Notation)	Z (Algebraic Notation)			
D~	~D	0B	DSTINVERT	00550009
DS•	S • D	05	SRCAND	008800C6
DP•	P • D	05	–	00A000C9
SD~•	S • ~D	09	SRCERASE	00440328
PD~•	P • ~D	09	–	00500325
DS~•	~S • D	50	–	00220326
DP~•	~P • D	50	–	000A0329
DS+~	~S • ~D	90	NOTSR-CERASE	001100A6
DP+~	~P • ~D	90	–	000500A9
DS+	S + D	6D	SRCPAINT	00EE0086
DP+	P + D	6D	–	00FF0062
SD~+	S + ~D	AD	–	00DD0228
PD~+	P + ~D	AD	–	00F50225
DS~+	~S + D	D6	MERGEPAINT	00BB0226
DP~+	~P + D	D6		00AF0229
DS•~	~S + ~D	DA	–	007700E6
DP•~	~P + ~D	DA	–	005F00E9
DSx~	S = D	95	–	00990066
DPx~	P = D	95	–	00A50065
DSx	S ≠ D	59	SRCINVERT	00660046
DPx	P ≠ D	59	PATINVERT	005A0049

Examples:

- Reverse Polish notation: (DP+~) means Destination {enter}, Pattern, OR, NOT.
- Algebraic notation: (~P • ~D) means NOT-Pattern AND NOT-Destination.
- DeMorgan's theorem states that these two functions are equivalent: $(\overline{D + P} = \overline{P} \bullet \overline{D})$

12.62 GR34: BitBLT Transparent Color Select Low Register

I/O Port Address: 3CF

Index: 34

Bit	Description	Reset State
7	BitBLT Transparent Color Select [7]	0
6	BitBLT Transparent Color Select [6]	0
5	BitBLT Transparent Color Select [5]	0
4	BitBLT Transparent Color Select [4]	0
3	BitBLT Transparent Color Select [3]	0
2	BitBLT Transparent Color Select [2]	0
1	BitBLT Transparent Color Select [1]	1
0	BitBLT Transparent Color Select [0]	1

This register contains the least-significant 8 bits of the 16-bit Transparent Color Select field.

Bit	Description
7:0	**BitBLT Transparent Color Select [7:0]:** • These bits are the least-significant 8 bits of the BitBLT Transparent Color Select field. • For details refer to Extension register GR35, which contains the most-significant 8 bits.

12.63 GR35: BitBLT Transparent Color Select High Register

I/O Port Address: 3CF

Index: 35

Bit	Description	Reset State
7	BitBLT Transparent Color Select [15]	0
6	BitBLT Transparent Color Select [14]	1
5	BitBLT Transparent Color Select [13]	1
4	BitBLT Transparent Color Select [12]	1
3	BitBLT Transparent Color Select [11]	0
2	BitBLT Transparent Color Select [10]	0
1	BitBLT Transparent Color Select [9]	1
0	BitBLT Transparent Color Select [8]	1

This register contains the most-significant 8 bits of the 16-bit BitBLT Transparent Color Select field For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:0	**BitBLT Transparent Color Select [15:8]:** • These bits are the most-significant 8 bits of the 16-bit BitBLT Transparent Color Select field. • The least-significant 8 bits are in Extension register GR34. • When Extension register GR30[3] is 1, the value of this field is compared with the value that results from the raster operation. If the values are: — Equal, the value that results from the raster operation is not written to the destination. — Not equal, the value that results from the raster operation is written to the destination. • For 8-bit color modes, the contents of this register must be set equal to those of Extension register GR34.

12.64 GR38: BitBLT Transparent Color Mask Low Register

I/O Port Address: 3CF

Index: 38

Bit	Description	Reset State
7	BitBLT Transparent Color Mask [7]	1
6	BitBLT Transparent Color Mask [6]	1
5	BitBLT Transparent Color Mask [5]	1
4	BitBLT Transparent Color Mask [4]	1
3	BitBLT Transparent Color Mask [3]	1
2	BitBLT Transparent Color Mask [2]	1
1	BitBLT Transparent Color Mask [1]	1
0	BitBLT Transparent Color Mask [0]	1

This register contains the least-significant 8 bits of the 16-bit BitBLT Transparent Color Mask field.

Bit	Description
7:0	**BitBLT Transparent Color Mask [7:0]:** • These bits are the least-significant 8 bits of the BitBLT Transparent Color Mask field. • For details refer to Extension register GR39, which contains the most-significant 8 bits of this field.

12.65 GR39: BitBLT Transparent Color Mask High Register

I/O Port Address: 3CF

Index: 39

Bit	Description	Reset State
7	BitBLT Transparent Color Mask [15]	0
6	BitBLT Transparent Color Mask [14]	0
5	BitBLT Transparent Color Mask [13]	0
4	BitBLT Transparent Color Mask [12]	0
3	BitBLT Transparent Color Mask [11]	1
2	BitBLT Transparent Color Mask [10]	1
1	BitBLT Transparent Color Mask [9]	1
0	BitBLT Transparent Color Mask [8]	1

This register contains the most-significant 8 bits of the 16-bit BitBLT Transparent Color Mask field. For more information on the BitBLT, refer to Appendix A.

Bit	Description
7:0	**BitBLT Transparent Color Mask [15:8]:** • These bits are the most-significant 8 bits of the 16-bit BitBLT Transparent Color Mask field. • The least-significant 8 bits are in Extension register GR38. • When Extension register GR30[3] is 1, the value of the transparent color is compared with the value that results from the raster operation under this mask. If the values are: — Equal, the value that results from the raster operation is not written to the destination. — Not equal, the value that results from the raster operation is written to the destination. • For 8-bit color modes, the contents of this register must be set equal to those of register GR38. • A 1 in any bit location of the 16-bit BitBLT Transparent Color Mask field makes the corresponding compare a 'don't care'.

NOTE: The '?' in the I/O port address of the registers in the following sections implies 'B' in Monochrome mode and 'D' in Color mode.

12.66 CR19: Interlace End Register

I/O Port Address: 3?5

Index: 19

Bit	Description	Reset State
7	Interlace End [7]	0
6	Interlace End [6]	1
5	Interlace End [5]	1
4	Interlace End [4]	0
3	Interlace End [3]	0
2	Interlace End [2]	1
1	Interlace End [1]	1
0	Interlace End [0]	0

This register contains the ending horizontal character count for the odd field for VSYNC.

Bit	Description
7:0	**Interlace End:** • In interlaced timing, the value in this field equals the number of characters in the last scanline of the odd field. • To center the scanlines in the odd field, this value can be adjusted half-way between scanlines in the even field. • This register is typically programmed to approximately half the Horizontal Total.

12.67 CR1A: Miscellaneous Control Register

I/O Port Address: 3?5

Index: 1A

Bit	Description	Reset State
7	Vertical Blanking End Extension [9]	0
6	Vertical Blanking End Extension [8]	1
5	Horizontal Blanking End Extension [7]	1
4	Horizontal Blanking End Extension [6]	0
3	DAC Mode Switching / Video Overlay Mode Control [1]	0
2	DAC Mode Switching / Video Overlay Mode Control [0]	1
1	Display Start Address Double Buffer Enable	0
0	Interlaced Timing Enable	1

This register contains timing extension bits as well as some miscellaneous control bits.

Bit	Description
7:6	**Vertical Blanking End Extension [9:8]:** This 2-bit field is used to extend the Vertical Blanking End value to 10 bits. • These bits are enabled only when CR1B[5] is 1 or when CR1B[7] is 1. • The other bits for this field are in CRT Controller register CR16. • For more information on these bits, refer to CRT Controller register CR16.
5:4	**Horizontal Blanking End Extension [7:6]:** This 2-bit field is used to extend the Horizontal Blanking End value to 8 bits. • These bits are enabled only when CR1B[5] is 1 or when CR1B[7] is 1. • The other bits for this field are in CRT Controller registers CR3[4:0] and CR5[7]. • For more information on these bits, refer to CRT Controller register CR3[4:0].

12.67 CR1A: Miscellaneous Control Register *(cont.)*

Bit | **Description**

3:2 **DAC Mode Switching / Video Overlay Mode Control [1:0]:**
This field is used to select DAC Mode Switching and the Video Overlay mode, as summarized in the following table. For more information, refer to the application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.

CR1A		DAC Mode Switching Enabled or Disabled	Video Overlay Mode Control
[3]	[2]		
0	0	Disabled	No Video Overlay. (Normal VGA-compatible operation.)
0	1	Enabled	Video Overlay controlled with FCEVIDEO# only. [a]
1	0	Enabled	Video Overlay controlled with FCEVIDEO# and color key.
1	1	Enabled	Video Overlay controlled with color key only.

[a] FCEVIDEO# is typically generated by OVRW#. For more information, refer to the application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.

1 **Display Start Address Double Buffer Enable:**
When this bit is 1, the Display Start Address is updated on the VSYNC following a write to Start Address Low. This update provides control of display frame switching without the need to explicitly monitor VSYNC.

0 **Interlaced Timing Enable**:
When this bit is 1, it enables interlaced timing.
- In text mode, interlaced synchronization is enabled.
- In graphics mode:
  - — Both interlaced synchronization and video data are enabled.
  - — For both interlaced synchronization and video data, CRT Controller register bit CR9[7] must be 0.
  - — Graphics modes 4h and 6h must always be non-interlaced.
- When this bit is 1, IRQ requests are generated only at the end of odd fields, that is, at the end of a frame.

12.68 CR1B: Extended Display Control Register

I/O Port Address: 3?5

Index: 1B

Bit	Description	Reset State
7	Horizontal and Vertical Blanking End Extension Enable	0
6	Text Mode Fast-Page Enable	1
5	Blanking Control	1
4	Offset [8]	0
3	Screen A Start Address [18]	0
2	Screen A Start Address [17]	1
1	Extended Address Wrap Enable	0
0	Screen A Start Address [16]	0

This register contains miscellaneous bits that control extended display functions.

Bit	Description
7	**Horizontal and Vertical Blanking End Extension Enable**: When this bit is: • 0, *and* CR1B[5] is 0, the Horizontal and Vertical Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are disabled. • 1, the Horizontal and Vertical Blanking End Extension bits of CR1A[7:6] and CR1A[5:4] are enabled, regardless of the CR1B[5] level.
6	**Text Mode Fast-Page Enable**: When Attribute Controller register bit AR10[0] is 0 *and* this bit is: • 0, all text mode fetch cycles take place as random-read cycles. This bit must be 0 for standard VGA operation. • 1, fast-page-mode cycles are used in text modes. — This setting allows for text modes with a VCLK greater than 30 MHz, as is required for 132-column modes. — This bit takes effect when RAS[1:0]# is high to ensure that the change does not occur in the middle of a CPU cycle.

12.68 CR1B: Extended Display Control Register *(cont.)*

Bit	Description
5	**Blanking Control:** • When this bit is 0 (the standard VGA mode): — The blanking signal generated by the CRTC controls the DAC blanking. — The border can be used. (For more information, refer to Attribute Controller register AR11.) • When this bit is 1: — The display enable controls the DAC blanking. — The border cannot be used, as the blanking registers are no longer available to control the border. Instead, the blanking registers are used to generate the OVRW# signal. — The DAC is blanked during the time the border is normally displayed. — The OVRW# pin is an output and follows the blanking signal generated by the CRTC. — The Horizontal and Vertical Blanking End Extension bits in CR1A[7:4] are enabled and used to specify the active portion of the Video Overlay Window. For more information, refer to the application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.
4	**Offset [8]:** This bit is the most-significant bit 9 of the CRT Controller Offset field. For details on this field, refer to CRT Controller register CR13.
3:2	**Screen A Start Address [18:17]:** These bits are the most-significant 2 bits of the CTR Controller Screen A Start Address registers CRC and CRD. Bit 16 is in CR1B[0].

12.68 CR1B: Extended Display Control Register *(cont.)*

Bit	Description
1	**Extended Address Wrap Enable:** • When this bit is 0, VGA compatibility is offered as follows: — The CRTC Character Address Counter is 16 bits wide. — The display memory address wraps at 64K maps (for 256K total memory). • When this bit is 1: — The CL-GD7548 CRT character counter addresses CA[16] and CA[18] provide up to 256K bytes in each bit plane, or one Mbyte of packed-pixel memory. — The CL-GD7548 CRT controller address counter is 19 bits wide. — The display memory address wraps at the total available memory size. • When this bit is 1 *and*: — Chain-4 addressing is selected (Sequencer register SR4[3] is 1): — DRAM addresses MA[0] and MA[1] are supplied from addresses XMA[16] and XMA[17]. — The other DRAM addresses are supplied from addresses XMA[18:12]. These addresses result from the sum of bus addresses XA[16:12] and the contents of either Graphics Controller Offset register 0 (GR9) or Offset register 1 (GRA). — CRTC double-word addressing is selected (CRT Controller register CR14[6] is 1): — DRAM addresses MA[0] and MA[1] are supplied from the internal CL-GD7548 CRT address counter addresses CR[15:14]. (The other DRAM addresses are supplied from addresses XMA[18:12], in the same manner as Chain-4 addressing.) — This action provides four displayable pages in Graphics mode 13h.
0	**Screen A Start Address [16]:** This bit is bit 16 of the Screen A Start Address. Bits 17 and 18 are in CR1B[3:2]. For more information, refer to CRT Controller registers CRC and CRD (the Screen A Start Address registers).

12.69 CR1D: Video Overlay Mode Register

I/O Port Address: 3?5

Index: 1D

Bit	Description	Reset State
7	Reserved	
6	Video Overlay Timing Signal Source	1
5	Reserved	
4	Reserved	
3	Reserved	
2	DAC Mode Switching Control [1]	1
1	DAC Mode Switching Control [0]	0
0	Reserved	

This register contains controls for the extended Video Overlay modes.

Bit **Description**

7 **Reserved**

6 **Video Overlay Timing Signal Source:**

- When this bit is 0, *and* Extension register CR1A[3:2] is 01, the FCEVIDEO# input is used as the timing signal for the Video Overlay modes.
- When this bit is 1, *and* Extension register CR1A[3:2] is 10, the internally generated OVRW# output is the timing signal for the Video Overlay modes. This setting eliminates the need to connect the OVRW# output to the FCEVIDEO# input.

5:3 **Reserved**

2:1 **DAC Mode Switching Control [1:0]:**
This field controls DAC mode switching. CR1A[3:2] selects Video Overlay mode.

CR1D		DAC Mode Switch State and Results		
[2]	[1]	DAC Mode Switch State	Result for Background:	Result for Video Overlay:
0	0	True. Selected Extended DAC mode is enabled.	VGA data from display memory (typically Graphics mode 5Fh)	Live video (typically true color)
0	1	False. Selected Extended DAC mode is enabled.	Live video (typically true color)	VGA data from display memory (typically Graphics mode 5Fh)
1	X	'Don't Care'. Extended DAC mode is disabled.	–	–

0 **Reserved**

12.70 CR1E: LCD Shading Register

I/O Port Address: 3?5

Index: 1E

Bit	Description	Access	Reset State
7	Shade Mapping [1]	R/W	0
6	Shade Mapping [0]	R/W	1
5	Reverse Video for Text Modes	R/W	1
4	Reverse Video for Graphics Modes	R/W	0
3	Dot Clock Duty Cycle Select	R/W	0
2	Horizontal CRTC Register Selection Override	R/W	0
1	Text-Mode Contrast Enhancement	R/W	0
0	Graphics Mode Dithering Enable	R/W	1

Bit **Description**

7:6 **Shade Mapping [1:0]:**
These 2 bits are used to program monochrome grayscale mapping (that is, shading) according to the following table:

CR1E		Shade Map
[7]	[6]	
0	0	Graphics mode. 18-bit output of LUT (Look-up Table) converted to 64 shades, with NTSC weighting.
0	1	LUT output is only the color green. 6-bit output of LUT converted to 64 shades.
1	0	Text mode. Direct display of up to 16 or 64 shades of pixel data (4-bit planar, or lower 6 of 8 bits packed-pixel)
1	1	Reserved

5 **Reverse Video for Text Modes:**
- When this bit is 0, this bit is disabled.
- When this bit is 1, all text modes are displayed in reverse video.

4 **Reverse Video for Graphics Modes:**
- When this bit is 0, this bit is disabled.
- When this bit is 1, all graphics modes are displayed in reverse video.

3 **Dot Clock Duty Cycle Select :**
- This bit controls the DCLK duty cycle and is for test purposes only. It is used to debug DSTN panels that have a problem with a 50% duty cycle.
- This bit can be used only when the CL-GD7548 is using a 2X clock VAFC (VESA Accelerated Feature Connector) mode to drive a panel.
- If the bit is:
  — 0, the DCLK has a 50% duty cycle
  — 1, the DCLK has a 25% duty cycle

12.70 CR1E: LCD Shading Register *(cont.)*

Bit — **Description**

2 — **Horizontal CRTC Register Selection Override:**
If this bit is:

- 0:
  - — *And* if all the following conditions exist:
    - — CR20[5] is 1 (the LCD panel interface is enabled)
    - — R9X[3:2] is '01' (the LCD panel interface is set for a 800 × 600 or a 1024 x 768 panel)
    - — CR2E[5] is 1 (horizontal centering is on)

    then Extension registers RiY and RiZ (i = 0,2,3,4,5) – the horizontal timing shadow registers – are used to control CRT controller horizontal timing.
  - — *But* not all of the conditions above exist:
    then CRT Controller registers CR0, CR2, CR3, CR4, CR5 – the standard VGA horizontal timing registers – are used to control CRT controller horizontal timing.
- 1, then Extension registers RiY or RiZ (i = 0,2,3,4,5) – the horizontal timing shadow registers – are always used to control CRT controller horizontal timing.

1 — **Text-Mode Contrast Enhancement:**
This bit is used along with Extension register R8X[4] to enable text-mode contrast enhancement.

CR1E[1]	R8X[4]	Text-Mode Contrast-Enhancement Characteristics
0	0	No enhancement of text mode.
0	1	Foreground-only enhancement If BG > FG, then BGC = BG and FGC = 0. If BG < FG, then BGC = BG and FGC = 1.
1	0	Contrast enhancement If BG > FG, then BGC = BG and FGC = 0. If BG < FG, then BGC = 0 and FGC = FG.
1	1	Illegal

BG = Background, FG = Foreground, xxC = Color

0 — **Graphics Mode Dithering Enable:**
Program this bit to:

- 0 to disable dithering in graphics mode.
- 1 to enable dithering in graphics mode.

12.71 CR1F: LCD Modulation Control Register

I/O Port Address: 3?5

Index: 1F

Bit	Description	Access	Reset State
7	External / Internal Modulation Control	R/W	0
6	MOD or Retrace LLCLK Control [6]	R/W	1
5	MOD or Retrace LLCLK Control [5]	R/W	1
4	MOD or Retrace LLCLK Control [4]	R/W	0
3	MOD or Retrace LLCLK Control [3]	R/W	0
2	MOD or Retrace LLCLK Control [2]	R/W	0
1	MOD or Retrace LLCLK Control [1]	R/W	0
0	MOD or Retrace LLCLK Control [0]	R/W	0

This register *must* have a programmed value. This register is used for one of two purposes, depending on the state of bit 7.

1) It can control the characteristics of the LCD Modulation (MOD) signal.

2) During vertical blanking, it can generate extra LCD line clocks (LLCLKs), which have two functions:

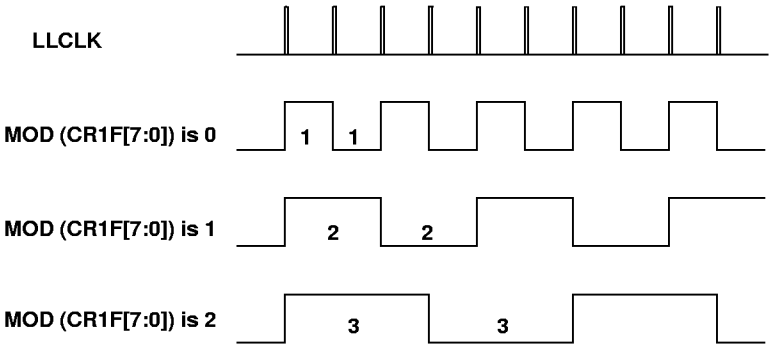
a) They eliminate any 'waterfall motion' (that is, rolling scanlines appearing on the entire LCD).

b) They guarantee the LCD receives a specific number of LLCLKs per frame.

Bit	Description
7	**External or Internal Modulation Control:** This bit controls the source of the modulation (MOD) signal for the LCD. • Clear this bit to 0 when an LCD needs an externally supplied MOD signal. — In this case, CR1F[6:0] can be used to program from 1 to 128 scanlines before MOD changes polarity. — Program CR1F[6:0] to determine the half-period of the square-wave output on the MOD pin, based on the programmed number of LLCLKs. *Continued*

12.71 CR1F: LCD Modulation Control Register *(cont.)*

Bit	Description
7 *(cont.)*	**External or Internal Modulation Control** *(cont.)*: • When CR1F[7] is 0, the resulting value of the MOD signal is one more than the value that is programmed into CR1F[7:0]. — For example, if register bits CR1F[7:0] are programmed to: — 0, the half-period of the square-wave MOD output is 1. — 1, the half-period of the square-wave MOD output is 2. — 2, the half-period of the square-wave MOD output is 3, and so on.



	• Set this bit to 1 when the LCD generates its own internal MOD signal and does not require an externally supplied MOD signal. (In addition, as described below, set CR1F[6:0] for the total number of LLCLKs.)
6:0	**MOD or Retrace LCD Line Clock (LLCLK) Control [6:0]:** • When CR1F[7] is 0: — The contents of CR1F[6:0] can select up to 128 scanlines before the MOD signal changes polarity. • When CR1F[7] is 1: — For dual-scan LCDs, program CR1F[6:0] for the number of LLCLKs that appear for each full frame. (Any extra clocks are seen on every other half-frame of the LCD during CRT vertical retrace.) — For single-scan LCDs, program CR1F[6:0] for the total number of LLCLKs that appear for the entire frame of the LCD. — The contents of CR1F[6:0] are added to 180 hex (384 decimal) to determine the total number of LLCLKs. (The number 180 hex has been predetermined to allow a working range of LLCLKs.) Total number of LLCLKs = 180h + hex value in CR1F[6:0].

12.72 CR20: Power Management Register

I/O Port Address: 3?5

Index: 20

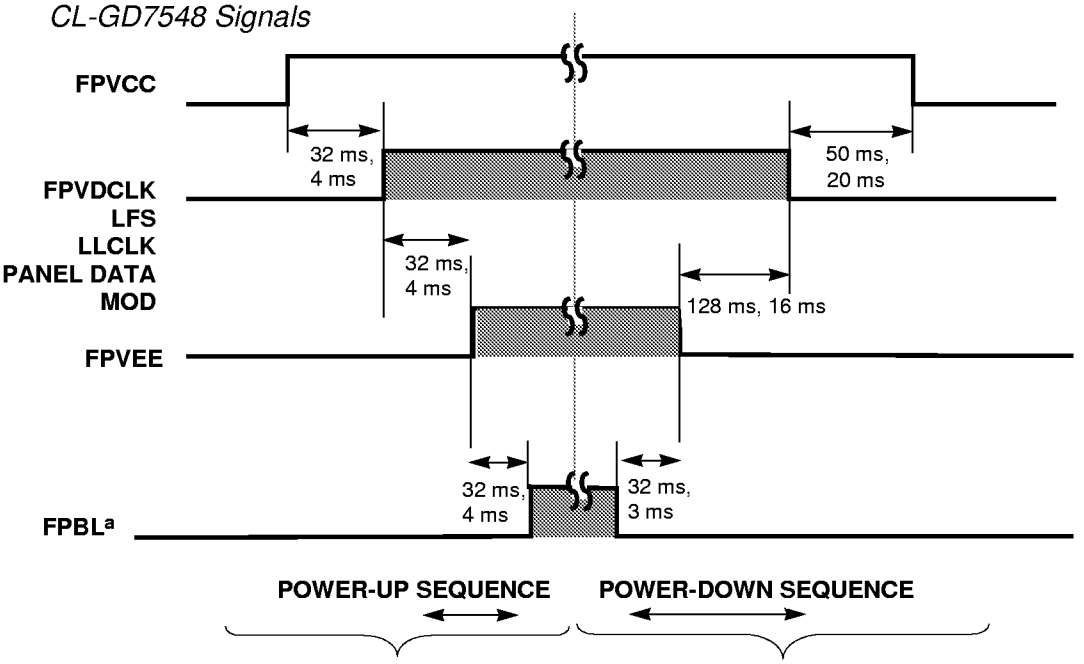
Bit	Description	Access	Reset State
7	SUSPI Pin Debounce Timer Resolution	R/W	0
6	CRT Enable	R/W	1
5	LCD Enable	R/W	0
4	Standby Mode Timer Control Override	R/W	1
3	Suspend Mode Activate	R/W	1
2	Display Memory Refresh Select [1]	R/W	1
1	Display Memory Refresh Select [0]	R/W	1
0	Text Mode Shading Control	R/W	1

This register contains controls for power-management modes. For more information on power management, refer to Appendix H.

Bit	Description
7	**SUSPI Pin Debounce Timer Resolution:** When this bit is: • 0, the SUSPI pin debounce timer resolution = 30 µsec (32-kHz period). • 1, the SUSPI pin debounce timer resolution = 1.0 sec.
6	**CRT Enable**: Setting this bit to 1 enables the analog CRT output from the video DAC.

12.72 CR20: Power Management Register *(cont.)*

Bit	Description
5	**LCD Enable:** To enable the LCD interface, set this bit to 1. As shown in Figure 12-1, when this bit has a: • Low-to-high transition, the CL-GD7548 LCD power-up sequence occurs, which enables the following signals in the proper sequence: the FPVCC signal, the drive signals (FPVDCLK, LFS, LLCLK, Panel Data, and MOD), the logic supply signal (FPVEE), and the backlight signal (FPBL). • High-to-low transition, the CL-GD7548 LCD power-down sequence occurs, which disables in the proper sequence the backlight signal (FPBL) and logic supply signal (FPVEE), the drive signals, and the FPVCC signal.



[a] This timing diagram applies to FPBL only if FPBL is enabled.

NOTE: In the above diagram, the first measurements are for 32-ms LCD power sequence, and the second measurements are for 4-ms LCD power sequence.

Figure 12-1. Normal Power-Up/Power-Down Sequence

NOTES:

1) The LCD power-up sequence begins when any of the following occur:
   a) When the LCD is powered on and CR20[5] = 1
   b) When Standby or Suspend modes are terminated, and the LCD was on prior to entering the Standby or Suspend mode
   c) When switching from CRT-only mode to an LCD or SimulSCAN mode

12.72 CR20: Power Management Register *(cont.)*

Bit	Description
	2) The LCD power-down sequence begins when any of the following occur: a) When the LCD is powered off and CR20[5] = 0 b) When Standby or Suspend modes are entered, and the LCD was previously on c) When switching from an LCD or SimulSCAN mode to a CRT-only mode • Extension register bits CR2C[7:6], SR21[6], R8X[5], and R9X[1:0] are among the registers that determine the type of LCD selected.
4	**Standby Mode Timer Control Override:** When this bit is: • 0, the current internal Standby mode timer setting of CR21[3:0] controls when the CL-GD7548 is placed into Standby mode. • 1, the current internal Standby mode timer setting of CR21[3:0] is overridden, and immediately the CL-GD7548 is placed into Standby mode.
3	**Suspend Mode Activate:** This bit takes effect only when no hardware-controlled Suspend mode is in effect. When this bit is: • 0, the input on the SUSPI pin controls when the CL-GD7548 is placed into Suspend mode. • 1, a software-controlled Suspend mode is initiated. As a result, the power-down sequence blanks the LCD screen. (If a CRT is on, the CRT is blanked as well.)
2:1	**Display Memory Refresh Select:** The programming of these 2 bits control the type of refresh applied to the display memory during Suspend mode as follows.
0	**Text Mode Shading Control**: When this bit is: • 0, text shades are derived directly from foreground/background data. • 1, text shades are derived the same way as graphics, with CR1E[7:6].

CR20		Display Memory Refresh Type
[2]	[1]	
0	0	Refresh cycle is 8 ms, CAS*-before-RAS*.
0	1	Refresh cycle is 64 ms, CAS*-before-RAS*.
1	0	Self-refresh. CAS* and RAS* are driven low.
1	1	No refresh. All clock inputs are disabled. All outputs to display memory are high-impedance.

12.73 CR21: Power-Down Timer Control Register

I/O Port Address: 3?5

Index: 21

Bit	Description	Access	Reset State
7	Backlight Timer Control [3]	R/W	0
6	Backlight Timer Control [2]	R/W	1
5	Backlight Timer Control [1]	R/W	0
4	Backlight Timer Control [0]	R/W	1
3	Standby Mode Timer Control [3]	R/W	1
2	Standby Mode Timer Control [2]	R/W	1
1	Standby Mode Timer Control [1]	R/W	1
0	Standby Mode Timer Control [0]	R/W	0

This register has two timers, and each controls the time at which power to the LCD is switched off.

- Programming CR21[7:4] controls the time it takes for the LCD backlight to switch off.
- Programming CR21[3:0] controls the time it takes for the Standby mode to be entered and power to the LCD to be switched off.

The timers operate as follows.

- Both timers may be set for times from 1 to 15 minutes.
- A programmed value of zero disables the timer.
- Instead of 60 seconds, the timers use 64 seconds for each 'minute' programmed.
- The timers subtract a correcting factor of 32 seconds from the timed subtotal.
- For example, a setting of 15 'minutes' (Fh) results in:
  [(15 counts × 64 seconds) – correcting factor of 32 seconds] =
  [(960 seconds) – 32 seconds] =
  928 seconds, or an actual time of (928 ÷ 60) = 15.5 minutes.

For typical power-down timer settings, refer to the table shown on the following page.

Bit	Description
7:4	**Backlight Timer Control [3:0]:** These bits program the value for the internal flat panel backlight timer, FPBL, as shown in the table that follows the description of bits CR21[3:0].

12.73 CR21: Power-Down Timer Control Register *(cont.)*

Bit	Description
3:0	**Standby Mode Timer Control [3:0]:** These bits program the value for the internal Standby mode timer as shown in the table that follows.

CR21 Backlight Timer Control Bits				Hex Code	Actual Seconds Programmed for Delay Time (Seconds)	Approximate Corresponding Delay Time (Minutes)
[7]	[6]	[5]	[4]			
CR21 Standby Mode Timer Control Bits						
[3]	[2]	[1]	[0]			
0	0	0	0	0h	Disabled	Disabled
0	0	0	1	1h	32	0.5
0	1	0	1	5h	288	4.8
0	1	1	1	7h	416	6.9
1	0	1	0	Ah	608	10.1
1	1	1	1	Fh	928	15.5

12.74 CR23: SUSPI Pin Debounce Timer Register

I/O Port Address: 3?5

Index: 23

Bit	Description	Access	Reset State
7	SUSPI Pin Debounce Timer [3]	R/W	0
6	SUSPI Pin Debounce Timer [2]	R/W	1
5	SUSPI Pin Debounce Timer [1]	R/W	0
4	SUSPI Pin Debounce Timer [0]	R/W	1
3	FPBL Control Override	R/W	1
2	FPBL Output State	R/W	1
1	FPVCC Control Override	R/W	0
0	FPVCC Output State	R/W	0

Bit **Description**

7:4 **SUSPI Pin Debounce Timer [3:0]:**
These bits define the number of seconds the input to the SUSPI (Suspend Input) pin must remain high and stable before the CL-GD7548 enters Suspend mode.

- The SUSPI debounce timer may be set for 1 to 15 seconds or 30 to 450 µs.
- A setting of 0000 disables the SUSPI debounce timer.

CR23				CR20	
[3]	[2]	[1]	[0]	CR20[7] is 1: Resolution for SUSPI Debounce Timer = 1.0 sec	CR20[7] is 0: Resolution for SUSPI Debounce Timer = 30 µs
0	0	0	0	0 (SUSPI debounce timer disabled)	
0	0	0	1	1 second	30 µs
0	0	1	0	2 seconds	60 µs
0	0	1	1	3 seconds	90 µs
0	1	0	0	4 seconds	120 µs
0	1	0	1	5 seconds	150 µs
0	1	1	0	6 seconds	180 µs
0	1	1	1	7 seconds	210 µs
1	0	0	0	8 seconds	240 µs
1	0	0	1	9 seconds	270 µs
1	0	1	0	10 seconds	300 µs
1	0	1	1	11 seconds	330 µs
1	1	0	0	12 seconds	360 µs
1	1	0	1	13 seconds	390 µs
1	1	1	0	14 seconds	420 µs
1	1	1	1	15 seconds	450 µs

12.74 CR23: SUSPI Pin Debounce Timer Register *(cont.)*

Bit	Description
3	**FPBL Control Override**: Setting this bit to 1: • Overrides the state of the flat panel backlight (FPBL) output pin. • Enables CR23[2] to directly control the output state of the flat panel backlight FPBL pin.
2	**FPBL Output State:** When CR23[3] is 1, *and* this bit is: • 0, the output state of the flat panel backlight FPBL pin is 0. • 1, the output state of the flat panel backlight FPBL pin is 1.
1	**FPVCC Control Override**: Setting this bit to 1: • Overrides the state of the flat panel VCC (FPVCC) output pin. • Enables CR23[0] to directly control the output state of the flat panel VCC (FPVCC) pin. **CAUTION:** Setting this bit to 1 can cause excessive power consumption and damage the flat panel. It is strongly recommended that this bit be left in the 0 state.
0	**FPVCC Output State:** When CR23[1] is 1, *and* this bit is: • 0, the output state of the flat panel VCC (FPVCC) pin is 0. • 1, the output state of the flat panel VCC (FPVCC) pin is 1.

12.75 CR25: Manufacturing Revision Identification Register

I/O Port Address: 3?5

Index: 25

Bit	Description	Reset State
7	Manufacturing Revision Identification [7]	'MFG revision'
6	Manufacturing Revision Identification [6]	'MFG revision'
5	Manufacturing Revision Identification [5]	'MFG revision'
4	Manufacturing Revision Identification [4]	'MFG revision'
3	Manufacturing Revision Identification [3]	'MFG revision'
2	Manufacturing Revision Identification [2]	'MFG revision'
1	Manufacturing Revision Identification [1]	'MFG revision'
0	Manufacturing Revision Identification [0]	'MFG revision'

This register contains the least-significant 8 bits of the 10-bit Manufacturing Revision Identification field.

Bit	Description
7:0	**Manufacturing Revision Identification [7:0]:** • These bits are the least-significant 8 bits of the 10-bit read-only Manufacturing Revision Identification field that uniquely identifies the CL-GD7548 manufacturing revision level. • This read-only Identification field is used for factory testing and internal tracking purposes only. Application programs must not use this field, which is listed here only for completeness. • The most-significant 2 bits are in Extension register CR27[1:0].

12.76 CR27: Device ID and Manufacturing Revision Identification Register

I/O Port Address: 3?5

Index: 27

Bit	Description	Reset State
7	Device ID [5]	0
6	Device ID [4]	0
5	Device ID [3]	1
4	Device ID [2]	1
3	Device ID [1]	1
2	Device ID [0]	0
1	Manufacturing Revision Identification [9]	'MFG revision'
0	Manufacturing Revision Identification [8]	'MFG revision'

This read-only register returns in bits [7:2] a value that uniquely identifies the CL-GD7548. Application programs have no requirement to read this register if a Cirrus Logic BIOS is being used.

Bit	Description
7:2	**Device ID [5:0]:** This 6-bit field contains a unique value that identifies the CL-GD7548 as a Cirrus Logic product.
1:0	**Manufacturing Revision ID [9:8]:** • These bits are the most-significant 2 bits of the 10-bit Manufacturing Revision ID field. • For details refer to Extension register CR25[7:0], which contains the least-significant 8 bits of this field.

12.77 CR29: Status Register

I/O Port Address: 3?5

Index: 29

Bit	Description	Reset State
7	Suspend Mode Status	0
6	32-kHz Clock Status	0
5	LCD Power Sequence Status	0
4	Standby Mode Status	0
3	V-Port Field Status	1
2	LCD Expansiion Status	0
1	Reserved	
0	Reserved	

This read-only register gives the status of various CL-GD7548 modes and processes.

Bit	Description
7	**Suspend Mode Status:** • This bit is 1 when the CL-GD7548 is in Suspend mode. This bit remains 1 (high) from the time the clocks are stopped until 32 ms after the clocks are restarted, that is, until power-up sequencing is started. • While this bit is 1, the SUSPST# pin output remains low. • This bit is used with software-controlled Suspend mode.
6	**32-kHz Clock Status:** This bit reflects the status of the 32-kHz clock. • This bit is 0 when the 32-KHz clock signal is low. • This bit is 1 when the 32-kHz clock signal is high. • This bit can be used to create a software timer.
5	**LCD Power Sequence Status:** • This bit is 1 while the CL-GD7548 is going through a power-up or power-down sequence. • This bit can be read in all modes except hardware-controlled Suspend mode, which locks out access to all registers.
4	**Standby Mode Status:** • This bit is 1 when the CL-GD7548 is in Standby mode. This bit remains 1 (high) from the time the clocks are stopped until 32 ms after the clocks are restarted, that is, until power-up sequencing is started. • While this bit is 1, the SBYST# pin output remains low.
3	**V-Port FieldStatus:** • This bit toggles on every falling (trailing) edge of the VSYNC signal. • This bit can be used by software to switch between two V-Port capture windows, on a frame-by-frame basis.
2	**LCD Expansion Status:** When the LCD panel is 800 x 600 or 1024 x 768, a 1 in this bit indicates that expansion is enabled.
1:0	**Reserved**

12.78 CR2C: LCD Interface Register

I/O Port Address: 3?5

Index: 2C

Bit	Description	Reset State
7	LCD Class Select [1]	0
6	LCD Class Select [0]	0
5	Horizontal Timing Shadow Registers Write Protect	0
4	Horizontal Timing Shadow Registers Select	0
3	CRT Controller Registers for LCD Vertical Timing Write Protect	0
2	CRT Controller Registers for LCD Horizontal Timing Write Protect	0
1	LLCLK Invert	0
0	LFS Invert	0

Bit **Description**

7:6 **LCD Class Select [1:0]:**
These 2 bits select the class of LCD to be connected. The following table lists available choices:

CR2C		LCD Class Selected
[7]	[6]	
0	0	Dual-scan monochrome LCD selected if CR2C[7:6] is 00 *and* R8X[5] is 0. Single-scan monochrome LCD selected if CR2C[7:6] is 00 *and* R8X[5] is 1.
0	1	Reserved
1	0	Dual-scan color STN LCD selected if CR2C[7:6] is 10 *and* SR21[6] is 1. Single-scan color STN LCD selected if CR2C[7:6] is 10 *and* SR21[6] is 0.
1	1	TFT-color LCDs selected. R9X[1:0] selects the pixel data format: 9-, 12-, 18- or 24-bit width.

12.78 CR2C: LCD Interface Register *(cont.)*

Bit	Description
5	**Horizontal Timing Shadow Registers Write Protect:** • When this bit is 0: — Extension registers RiY and RiZ (i = 0,2,3,4,5) – the horizontal timing shadow registers – are write-protected and cannot be accessed. — Writing and reading applies only to CRT Controller registers CR0 through CR5 – the standard VGA horizontal timing registers. • When this bit is 1: — *And* CRT Controller register bit CR11[7] is a 0, writing is done to only the horizontal timing shadow registers, Extension registers RiY and RiZ (i = 0,2,3,4,5). — *And* CRT Controller register bit CR11[7] is a 1, writing is done to both the standard VGA horizontal timing registers CR0 through CR5 and the horizontal timing shadow registers, Extension registers RiY and RiZ (i = 0,2,3,4,5). — Reading is done only from the horizontal timing shadow registers. • For write accesses to standard VGA horizontal timing registers, this bit is a 'don't care'.
4	**Horizontal Timing Shadow Registers Select:** This bit selects which set of horizontal timing shadow registers the CL-GD7548 uses. When CR2C[5] is 1 *and* this bit is: • 0, it selects Extension registers R0Y to R5Y, used with the normal DCLK. • 1, it selects Extension registers R0Z to R5Z, used with DCLK ÷ 2. (For information on DCLK ÷ 2, refer to Sequencer register SR1[3].)

12.78 CR2C: LCD Interface Register *(cont.)*

Bit | **Description**

3 — **CRT Controller Registers for LCD Vertical Timing Write Protect:**

- For LCD operation, some CRT controller registers must be write protected, that is, the last data bits written are used for CRT controller timing control, and a read/write shadow register is enabled for any subsequent I/O.
- When this bit is 0, the value that is written is the same as the value that is read.
- When this bit is 1, the value that is written is *not* the same as the value that is read and which takes effect.
  - — In this case, the CRT Controller registers in the table below are write-protected for LCD timing.
  - — The value that does take effect is not a standard VGA value, because it is used to control the LCD (and not the CRT).

CRT Controller Register / Bits	Description of CRT Controller Registers That Are Write Protected for LCD Timing
CR6 [7:0]	Vertical Total (protected value is used)
CR7 [7, 5, 2, 0]	Vertical Overflow bIts for total and synchronization start
CR10 [7:0]	Vertical Retrace Start (protected value is used for CRT VSYNC)
CR11 [3:0]	Vertical Retrace End (protected value is used for CRT VSYNC)
CR15 [7:0]	Vertical Blanking Start
CR16 [7:0]	Vertical Blanking End

2 — **CRT Controller Registers for LCD Vertical Timing Write Protect:**
When the LCD is enabled and this bit is 1, CRT Controller registers CR0, CR2, CR3, CR4 and CR5 are write protected.

1 — **LLCLK Invert:**
When this bit is 1, the LLCLK output is inverted.

0 — **LFS Invert:**
When this bit is 1, the LFS output is inverted.

Continued on next page.

12.78 CR2C: LCD Interface Register *(cont.)*

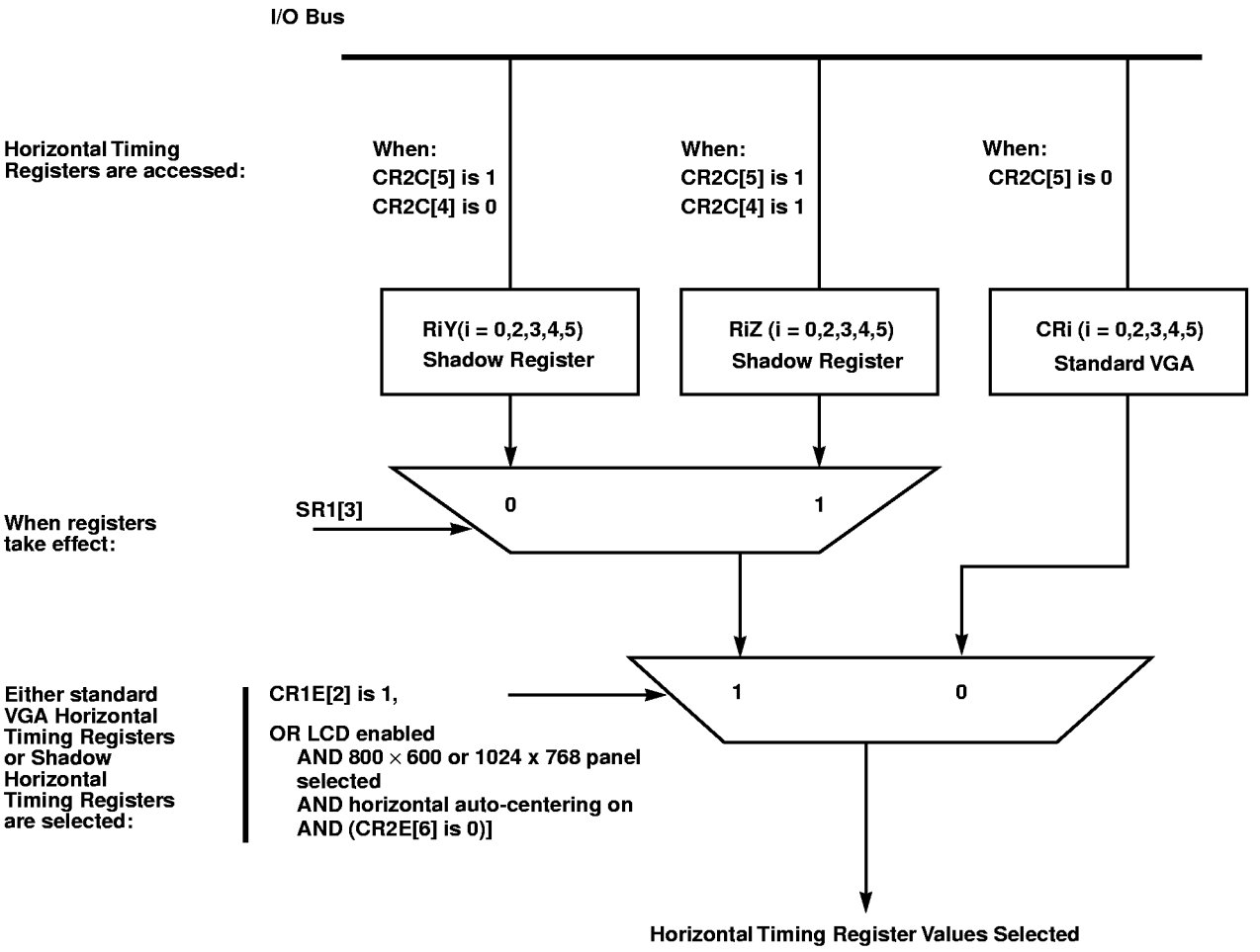


Figure 12-2. Horizontal Timing Register Values Selection

Table 12-1. Horizontal Timing Register References

CRi (Standard VGA) Horizontal (H) Timing Registers		Horizontal (H) Timing Shadow Registers			
		RiY Registers		RiZ Registers	
CR0	H Total	R0Y	H Total	R0Z	H Total
CR2	H Blanking Start	R2Y	H Blanking Start	R2Z	H Blanking Start
CR3	H Blanking End	R3Y	H Blanking End	R3Z	H Blanking End
CR4	H Sync Start	R4Y	H Sync Start	R4Z	H Sync Start
CR5	H Sync End	R5Y	H Sync End	R5Z	H Sync End

12.79 CR2D: LCD Display Controls Register

I/O Port Address: 3?5

Index: 2D

Bit	Description	Reset State
7	LCD Timing Registers Enable	0
6	Standby Mode Timer Reset by ACTI	0
5	Standby Mode Timer Reset by VGA Access	0
4	Suspend Mode Clock Source	0
3	Backlight Timer Reset by ACTI	0
2	Backlight Timer Reset by VGA Access	0
1	Automatic Vertical Expansion for 640 × 480 LCDs	0
0	Automatic Centering Enable	0

Bit	Description
7	**LCD Timing Registers Enable:** • The CRT Controller Index register (CRX) does not have bits to index the LCD timing registers (Extension registers R2X to REX). Instead, CR2D[7] acts as an extra CRT Controller Index register bit to enable registers R2X to REX. • When this bit is 1, it enables read/write of Extension registers R2X to REX, which are mapped at the standard CRTC locations. These special timing control registers are used to control LLCLK, LFS, and other LCD control signals.
6	**Standby Mode Timer Reset by ACTI:** When this bit is set to 1, activity on the ACTI pin resets the internal Standby Timer.
5	**Standby Mode Timer Reset by VGA Access:** When this bit is set to 1, any valid VGA memory access resets the internal Standby Timer.
4	**Suspend Mode Clock Source**: This bit selects the source for the clock used during Suspend mode. • When this bit is 0, a 32-kHz clock must be connected to the 32-kHz pin. • When this bit is 0, *and* when the CL-GD7548 is in Suspend mode, the OSC input pin is disabled. • When this bit is set to 1, the 14-MHz clock required on the OSC input pin is divided by 432 to derive the 32-kHz clock.
3	**Backlight Timer Reset by ACTI:** When this bit is set to 1, activity on the ACTI pin resets the Backlight control timer.
2	**Backlight Timer Reset by VGA Access:** When this bit is set to 1, any valid VGA memory access resets the Backlight control timer.

12.79 CR2D: LCD Display Controls Register *(cont.)*

Bit **Description**

1 **Automatic Vertical Expansion of Graphics and Text for 640 × 480 LCDs:**
When this bit is 1, it enables automatic vertical expansion of graphics and text for 640 × 480 LCDs, as controlled by the synchronization polarity bits in External/General register MISC[7:6].

Automatic Vertical Expansion Enable

MISC [7]	MISC [6]	Automatic Vertical Expansion of Graphics and Text Modes	
0	0	More than 480 scanlines on a 800 × 600 LCD. Reserved in standard VGA.	
0	1	400-scanline or 200-scanline mode	400-scanline mode is for text only. 200-scanline mode is for double-scanned graphics only.
1	0	350-scanline mode	
1	1	480-scanline mode	

Vertical Expansion Method For Graphics Modes:

Original Scanlines	Vertical Expansion Method for Graphics Modes
200	Pattern used is double-scan and triple-scan: 2,2,3,2,2,3,2,3. Pattern expands 200 scanlines to 475 by expanding every 8 scanlines to 19.
350	Pattern used is single-scan and double-scan: 1,1,2,1,1,2,1,2,1,1,2,1,1,2. Pattern expands 350 scanlines to 475 by expanding every 14 scanlines to 19.

Vertical Expansion Method For Text Modes:

Original Scanlines / Text	Vertical Expansion Method for Text Modes
200 scanlines, 8 × 8 text	Normal double-scan is applied. Extra scanlines (1 top and 2 bottom) are added to each character row (only when maximum row scan is set for 7 scanlines).
350 scanlines, 8 × 14 text	Extra scanlines (2 top and 3 bottom) are added to each character row (only when maximum row scan is set for 14 scanlines).
400 scanlines, 8 × 16 text	Extra scanlines (1 top and 2 bottom) are added to each character row (only when maximum row scan is set for 16 scanlines).

0 **Automatic Centering Enable:**
When this bit is:

- 0, automatic centering is disabled.
- 1, *and* when automatic expansion bit CR2D[1] is 0 (based on synchronization polarities), it enables LCD automatic centering. This action uses alternate LFS (line-frame start) timing as programmed in the LCD Timing registers, Extension registers R2X, R3X, R4X, R5X, R6X, RCX, RDX, and REX.

12.80 CR2E: LCD High-Resolution Control Register

I/O Port Address: 3?5

Index: 2E

Bit	Description	Reset State
7	Vertical Centering Enable for 1024 x 768 LCDs	0
6	Low Resolution Expansioin Disable for 1024 x 768 LCDs	0
5	Horizontal Centering Enable for LCDs	0
4	10-Dot True-Font Text Select	0
3	Horizontal Graphics Expansion for 800 × 600 and 1024 x 768 LCDs	0
2	Horizontal Text Expansion for 800 × 600 and 1024 x 768 LCDs	0
1	Vertical Graphics Expansion for 800 × 600 and 1024 x 768 LCDs	0
0	Vertical Text Expansion for 800 × 600 and 1024 x 768 LCDs	0

Bit	Description
7	**Vertical Centering Enable for 1024 x 768 LCDs:** When this bit is set to 1, vertical centering is enabled for 1024 x 768 LCDs.
6	**Low Resolution Expansioin Disable for 1024 x 768 LCDs:** When this bit is set to 1, and the LCD is in low-resolution mode (SR1[3] = 1), expansion for 1024 x 768 LCDs is disabled.
5	**Horizontal Centering Enable for LCDs:** A 1 in this bit enables horizontal centering for 800 × 600 and 1024 × 768 LCDs.
4	**10-Dot True-Font Text Select:** When this bit is 1 *and* a text mode is selected, 10-dot true-font text is selected.
3	**Horizontal Graphics Expansion for 800 × 600 and 1024 x 768 LCDs:** When this bit is 1 *and* a graphics mode is selected, horizontal graphics expansion is enabled, which replicates every fourth pixel. • For an 800 × 600 LCD, this bit is used to expand 640-pixel data of each scan-line to 800-pixel data. • This bit does not work in 16-bit/pixel and 24-bit/pixel modes.
2	**Horizontal Text Expansion for 800 × 600 and 1024 x 768 LCDs:** When this bit is 1 *and* a text mode is selected, 8- and 9-dot-wide text is expanded to 10-dot-wide text.
1	**Vertical Graphics Expansion for 800 × 600 and 1024 x 768 LCDs:** When this bit is 1 *and* a graphics mode is selected, vertical graphics on 800 × 600 LCDs are expanded by: • Doubling every odd scanline in 350-scanline and 400-scanline modes • Replicating every fourth scanline in 480-scanline mode
0	**Vertical Text Expansion for 800 × 600 and 1024 x 768 LCDs:** When this bit is 1 *and* a text mode is selected, the text is expanded by: • Doubling every odd scanline for 9 × 14 text or 8 × 16 text • Tripling every scanline for 8 × 8 text

12.81 CR2F: Driver and BIOS Revision Register

I/O Port Address: 3?5

Index: 2F

Bit	Description	Reset State
7	Driver Revision [3]	'Driver Revision'
6	Driver Revision [2]	'Driver Revision'
5	Driver Revision [1]	'Driver Revision'
4	Driver Revision [0]	'Driver Revision'
3	BIOS Revision [3]	'BIOS Revision'
2	BIOS Revision [2]	'BIOS Revision'
1	BIOS Revision [1]	'BIOS Revision'
0	BIOS Revision [0]	'BIOS Revision'

This read-only register returns two 4-bit codes that uniquely identify the CL-GD7548 to drivers and to the BIOS.

Bit	Description
7:4	**Driver Revision [3:0]:** This 4-bit field contains a value identifying the CL-GD7548 to various software drivers.
3:0	**BIOS Revision [3:0]:** This 4-bit field contains a value identifying the CL-GD7548 to the video BIOS.

12.82 CR30: TV-OUT Control Register

I/O Port Address: 3?5

Index: 30

Bit	Description	Reset State
7	PROG Pin-Level Control	0
6	Reserved	
5	Horizontal Total Dot Clock Delay Control [1]	0
4	Horizontal Total Dot Clock Delay Control [0]	0
3	TV-OUT Mode Enable	0
2	NTSC / PAL Output Control	0
1	CSYNC Dot Clock Delay Control [1]	0
0	CSYNC Dot Clock Delay Control [0]	0

Bit — **Description**

7 — **PROG Pin-Level Control:**
This bit controls the logic level on the PROG output pin. When this bit is a:
- 0, the CL-GD7548 PROG pin level is low.
- 1, the CL-GD7548 PROG pin level is high.

6 — **Reserved**

5:4 — **Horizontal Total Dot Clock Delay Control [1:0]:**
The value in these bits control the dot clock delay for the horizontal total signal according to the following table:

CR30		Dot-Clock Delay for Horizontal Total
[5]	[4]	
0	0	No delay
0	1	Delay is 2 dot clocks.
1	0	Delay is 4 dot clocks.
1	1	Delay is 6 dot clocks.

12.82 CR30: TV-OUT Control Register *(cont.)*

Bit	Description
3	**TV-OUT Mode Enable:** • When this bit is 0: — The TV-OUT mode is disabled, and the TVON output is forced low. — CR30[2] is disabled, and NTSC/PAL and CSYNC outputs are forced low. • When this bit is 1: — The TV-OUT mode is enabled, and the TVON output is high. — CR30[2] is enabled, and depending on the CR30[2] bit setting, CSYNC timing is generated in accordance with either PAL or NTSC timing requirements. • When Extension register SR25[6] is 1, the TVON pin is not controlled by CR30[3]. However, the TV-OUT feature can still be used without a power-down feature on CR30[3].
2	**NTSC / PAL Output Control:** This bit is programmed to reflect required input levels to the NTSC/PAL encoder. • When CR30[3] is 0, this bit is disabled. • When CR30[3] is 1, *and* this bit is: — 0, this bit creates a low on the NTSC/PAL output pin. As a result, CSYNC timing is generated in accordance with PAL timing requirements. — 1, this bit creates a high on the NTSC/PAL output pin. As a result, CSYNC timing is generated in accordance with NTSC timing requirements.
1:0	**CSYNC Dot Clock Delay Control [1:0]:** The value in these bits control the dot clock delay for the generation of a composite synchronization signal (CSYNC) according to the following table.

CR30		Dot Clock Delay for CSYNC Start
[1]	[0]	
0	0	No delay
0	1	Delay is 2 dot clocks.
1	0	Delay is 4 dot clocks.
1	1	Delay is 6 dot clocks.

12.83 CR31: VW Horizontal Upscaling Coefficient Low Register

I/O Port Address: 3?5

Index: 31

Bit	Description	Reset State
7	VW Horizontal Upscaling Coefficient [7]	0
6	VW Horizontal Upscaling Coefficient [6]	0
5	VW Horizontal Upscaling Coefficient [5]	0
4	VW Horizontal Upscaling Coefficient [4]	0
3	VW Horizontal Upscaling Coefficient [3]	0
2	VW Horizontal Upscaling Coefficient [2]	0
1	VW Horizontal Upscaling Coefficient [1]	0
0	VW Horizontal Upscaling Coefficient [0]	0

This register controls the horizontal upscaling of the Video Window.

Bit	Description
7:0	**Video Window Horizontal Upscaling Coefficient [7:0]:** • These bits are the least-significant 8 bits of the 12-bit field for the VW HU (Video Window Horizontal Upscaling) Coefficient. • The most-significant 4 bits are in Extension register CR5D[3:0]. • The VW HU range that the CL-GD7548 supports is from 1x to 4x. • The VW HU is calculated as follows: $\text{VW HU} = \frac{\text{4096 (The VW HU field is 12 bits and } 2^{12} = 4096.)}{\text{Value programmed in CR31[7:0] / CR5D[3:0] (Range is 1024–4095.)}}$ • If the value programmed for the VW HU coefficient is: — 0h (the default, and an exception), the horizontal upscaling coefficient is 1x. [The horizontal upscaling coefficient is (4096 ÷ 4096) = 1x, and the resulting VW image is unchanged from the image source.] — 400h (1024 decimal), the horizontal upscaling coefficient is 4x. [The horizontal upscaling coefficient is (4096 ÷ 1024) = 4x, and the resulting VW image is four times as large as the image source.] — 800h (2048 decimal), the horizontal upscaling coefficient is 2x. [The horizontal upscaling coefficient is (4096 ÷ 2048) = 2x, and the resulting VW image is two times as large as the image source.] • If horizontal upscaling of greater than 1x is chosen: — Some pixels are generated by horizontal interpolation of source image pixels. — As a result of this generation, the VW includes the extra pixels and is wider than it would be if upscaling was not enabled. That is, horizontal upscaling is accomplished by making the VW physically wider rather than by keeping the VW width constant and displaying fewer source pixels.

12.84 CR32: VW Vertical Upscaling Coefficient Low Register

I/O Port Address: 3?5

Index: 32

Bit	Description	Reset State
7	VW Vertical Upscaling Coefficient [7]	0
6	VW Vertical Upscaling Coefficient [6]	0
5	VW Vertical Upscaling Coefficient [5]	0
4	VW Vertical Upscaling Coefficient [4]	0
3	VW Vertical Upscaling Coefficient [3]	0
2	VW Vertical Upscaling Coefficient [2]	0
1	VW Vertical Upscaling Coefficient [1]	0
0	VW Vertical Upscaling Coefficient [0]	0

This register controls the vertical upscaling of the Video Window.

Bit **Description**

7:0 **Video Window Vertical Upscaling Coefficient [7:0]:**

- These bits are the least-significant 8 bits of the 12-bit field for the VW VU (Video Window Vertical Upscaling) Coefficient.
- The most-significant 4 bits are in Extension register CR5D[7:4].
- The VW VU range that the CL-GD7548 supports is from 1x to 4x.
- The VW VU is calculated as follows:

$$\text{VW VU} = \frac{\text{4096 (The VW VU field is 12 bits and } 2^{12} = 4096.)}{\text{Value programmed in CR32[7:0] / CR5D[7:4] (Range is 1024–4095.)}}$$

- If the value programmed for the VW VU is:
  - — 0h (the default, and an exception), the vertical upscaling coefficient is 1x. [The vertical upscaling coefficient is 4096 ÷ 4096) = 1x, and the resulting VW image is unchanged from the image source.]
  - — 400h (1024 decimal), the vertical upscaling coefficient is 4x. [The vertical upscaling coefficient is (4096 ÷ 1024) = 4x, and the resulting VW image is four times as large as the image source.]
  - — 800h (2048 decimal), the vertical upscaling coefficient is 2x. [The vertical upscaling coefficient is (4096 ÷ 2048) = 2x, and the resulting VW image is two times as large as the image source.]
- If vertical upscaling of greater than 1x is chosen:
  - — Some scanlines are generated by vertical replication of source image scanlines.
  - — As a result of this generation, since the physical height of the VW is fixed by the Vertical Start and Vertical End values, some scanlines at the bottom of the source image do not display. In contrast to horizontal upscaling, with vertical upscaling, the VW dimension (in this case, height) is kept constant and the extra source scanlines are not displayed.

12.85 CR33: VW Horizontal Start (XS) / Width (XW) Extension Register

I/O Port Address: 3?5

Index: 33

Bit	Description	Reset State
7	VW Surrounding Address Offset [0]	0
6	VW Horizontal Start (XS) [9]	0
5	VW Horizontal Start (XS) [8]	0
4	VW (AccuPak Data Format) Dithering Disable	0
3	VW Horizontal Width (XW) [9]	0
2	VW Horizontal Width (XW) [8]	0
1	VW Memory Bandwidth Improvement	0
0	VW Fast FIFO Request Enable	0

In the Video Window, the horizontal start position is programmed using the number of memory cycles used by the surrounding pixel-depth resolution.

Bit	Description
7	**VW Surrounding Address Offset [0]:** • This bit is the least-significant of the 9-bit VW Surrounding Address Offset field. • For details refer to Extension register CR39, which contains the most-significant 8 bits of this field.
6:5	**VW Horizontal Start (XS) [9:8]:** • These bits are the most-significant 2 bits of a 10-bit field that defines the horizontal starting position of the Video Window. • For details refer to Extension register CR34, which contains the least-significant 8 bits of this field.
4	**VW (AccuPak Data Format) Dithering Disable:** This bit is used to control dithering within the Video Window when it is in the AccuPak data format. (This bit applies to both CRTs and LCDs.) When the VW is active and this bit is: • 0, dithering is enabled for the VW, resulting in a smoother VW appearance. • 1, dithering is disabled for the VW.
3:2	**VW Horizontal Width (XW) [9:8]:** • These bits are the most-significant 2 bits of a 10-bit field that defines the horizontal width of the Video Window. • For details refer to Extension register CR35, which contains the least-significant 8 bits of this field.

12.85 CR33: VW Horizontal Start (XS) / Width (XW) Extension Register *(cont.)*

Bit	Description
1	**VW Display Memory Bandwidth Improvement:** When this bit is: • 0: — The CPU cannot access the display memory during the VW refresh. — Clear this bit if there is not enough display memory bandwidth because: — The VW has a high pixel depth. — The dot clock has a high frequency. • 1, the CPU can access the display memory during the VW refresh.
0	**VW Fast FIFO Request Enable:** This bit enables bypassing the synchronizer in the VW circuitry to fill the FIFO faster.

12.86 CR34: VW Horizontal Start (XS) Register

I/O Port Address: 3?5

Index: 34

Bit	Description	Reset State
7	VW Horizontal Start (XS) [7]	0
6	VW Horizontal Start (XS) [6]	0
5	VW Horizontal Start (XS) [5]	0
4	VW Horizontal Start (XS) [4]	0
3	VW Horizontal Start (XS) [3]	0
2	VW Horizontal Start (XS) [2]	0
1	VW Horizontal Start (XS) [1]	0
0	VW Horizontal Start (XS) [0]	0

This register contains the least-significant 8 bits of the 10-bit VW (Video Window) horizontal start position field. In the VW, the horizontal start position is programmed by using the number of memory fetch cycles in the surrounding pixel-depth resolution.

Bit	Description
7:0	**VW Horizontal Start (XS) [7:0]:** • These are the least-significant 8 bits of the VW horizontal start position field. • The most-significant 2 bits are in Extension register CR33[6:5]. To program XS (the horizontal coordinate to start the VW on the screen): 1. Determine the number of the pixel at which the VW must start. 2. Determine the surrounding pixel-depth resolution, in bits per pixel. 3. Determine the size of the memory bus, which determines how many bits each memory fetch cycle transfers. 4. Obtain the number of pixels per memory fetch cycle by dividing the size of the memory bus by the number of bits in the surrounding pixel-depth resolution. (If the memory bus is 32 bits wide and 4 bits per pixel is used for the surrounding pixel-depth resolution, the number of pixels per memory fetch cycle is 8.) 5. Divide the number of the pixel at which the VW must start by the number of pixels per memory fetch cycle. 6. Program the resulting value into CR34[7:0]. For example, If: A VW is to start at pixel 16. The surrounding pixel-depth resolution is 4 bits per pixel. The memory bus transfers 32 bits (32-bit memory fetch cycle). Then: The number of pixels per memory fetch cycle is 32 ÷ 4 = 8. The number of memory fetch cycles needed for a MWV starting at pixel 16 is 2. (A starting VW value pixel number of 16 ÷ 8 pixels per memory fetch cycle = 2 memory fetch cycles.) Program: Into CR34[7:0] the value 2 as the number of memory fetch cycles needed for a VW starting at pixel 16.

12.87 CR35: VW Horizontal Width (XW) Register

I/O Port Address: 3?5

Index: 35

Bit	Description	Reset State
7	VW Horizontal Width (XW) [7]	0
6	VW Horizontal Width (XW) [6]	0
5	VW Horizontal Width (XW) [5]	0
4	VW Horizontal Width (XW) [4]	0
3	VW Horizontal Width (XW) [3]	0
2	VW Horizontal Width (XW) [2]	0
1	VW Horizontal Width (XW) [1]	0
0	VW Horizontal Width (XW) [0]	0

This register contains the least-significant 8 bits of the 10-bit VW horizontal width field, which is calculated in video resolution memory fetch cycles as explained below.

Bit **Description**

7:0 **VW Horizontal Width (XW) [7:0]:**

- These are the least-significant 8 bits of the 10-bit VW horizontal width field.
- The most-significant 2 bits are in Extension register CR33[3:2].
- For the VW, this field must be programmed , even when the VW is displayed on the full screen.
- This 10-bit field can define a VW that is 1024 pixels wide, even with a 32-bpp VW pixel depth.

To program the number of memory fetch cycles needed for the value of XW (the horizontal width of the Video Window):

1. Determine the width of the VW in increments of 8 pixels, up to 1024 pixels.
   a. To determine VW width, use the width of the VW *before* upscaling occurs.
   b. For example, if the VW width in display memory is 320 pixels x 240 scan-lines, use the 320 value as the VW width.
2. Determine the color depth of the VW display, in bits per pixel.
3. Determine the size of the memory bus, which determines how many bits each memory fetch cycle transfers.
4. Multiply the VW width (in pixels) times the VW depth (in bits per pixel).
5. Divide the above quantity by how many bits each memory fetch cycle transfers.
6. Program the resulting value.

For example,

If:	A VW is 320 pixels wide. The VW display has a color depth of 16 bits per pixel. The memory bus transfers 32 bits wide (a 32-bit fetch cycle).
Then:	Multiply the VW width (320 pixels) × VW depth (16 bits/pixel). Divide the above quantity by the number of bits each memory fetch cycle transfers (32).
Program:	Into CR35[7:0] the resulting value of 160 memory fetch cycles.

12.88 CR36: VW Vertical Position Extension Register

I/O Port Address: 3?5

Index: 36

Bit	Description	Reset State
7	Force Linear Display Memory Map	0
6	VW Live Video Gamma Reduction Enable	0
5	Excess 128 Data Format Select	1
4	VW Memory Address Offset [8]	0
3	VW Vertical Height (YH) [9]	0
2	VW Vertical Height (YH) [8]	0
1	VW Vertical Start (YS) Position [9]	0
0	VW Vertical Start (YS) Position [8]	0

Bit	Description
7	**Force Linear Display Memory Map:** This bit is used to simplify the use of drivers for the VW by providing a unique way of accessing the memory for VW, that is, from the CPU side. **NOTE:** The BitBLT engine can always be used with this mode of operation, which speeds up VW accesses. This bit must be programmed to: • 0 by the Windows driver after writes to the VW memory are executed. • 1 when the CPU is writing to VW memory and running Microsoft® Windows in 4-bpp planar mode, to ensure that the CPU writes to VW memory execute independently of surrounding graphics. (When this bit is 1, the CPU writes data to the VW memory in a linear memory map, the same as in extended 8-bpp packed-pixel modes.) • Any value (that is, this bit is a 'don't care') when the CPU is writing to VW memory and running Microsoft® Windows in a 4-, 8-, or 16-bpp packed-pixel mode.
6	**VW Live Video Gamma Reduction Enable:** When the VW is enabled, live video is displayed, and this bit is 1, live video gamma is reduced. (Live video quality is further improved for LCDs and CRTs if brightness and contrast are also properly adjusted.)
5	**Excess 128 Data Format Select:** When this bit is: • 0, the selected data format is 2's complement. • 1, the selected data format is excess 128 data format.

12.88 CR36: VW Vertical Position Extension Register *(cont.)*

Bit	Description
4	**VW Memory Address Offset [8]:** • This is the most-significant bit of the 9-bit VW Memory Address Offset field. • For details refer to Extension register CR3B, which contains the 8 least significant bits.
3:2	**VW Vertical Height (YH)[9:8]:** • These are the most-significant 2 bits of the 10-bit VW Vertical Height field. • For details refer to Extension register CR38, which contains the 8 least significant bits.
1:0	**VW Vertical Start (YS) [9:8]:** • These are the most-significant 2 bits of the 10-bit VW Vertical Start field. • For details refer to Extension register CR37, which contains the 8 least significant bits.

12.89 CR37: VW Vertical Start (YS) Register

I/O Port Address: 3?5

Index: 37

Bit	Description	Reset State
7	VW Vertical Start (YS) [7]	0
6	VW Vertical Start (YS) [6]	0
5	VW Vertical Start (YS) [5]	0
4	VW Vertical Start (YS) [4]	0
3	VW Vertical Start (YS) [3]	0
2	VW Vertical Start (YS) [2]	0
1	VW Vertical Start (YS) [1]	0
0	VW Vertical Start (YS) [0]	0

Bit	Description
7:0	**VW Vertical Start (YS) [7:0]:** • These bits are the least-significant 8 bits of the 10-bit field for the VW Vertical Start (YS). • The 10 bits of this field: — Define the first scanline of the VW — Are not affected by scanline doubling or LCD vertical expansion • The most-significant 2 bits are in Extension register CR36[1:0].

12.90 CR38: VW Vertical Height (YH) Register

I/O Port Address: 3?5

Index: 38

Bit	Description	Reset State
7	VW Vertical Height (YH) [7]	0
6	VW Vertical Height (YH) [6]	0
5	VW Vertical Height (YH) [5]	0
4	VW Vertical Height (YH) [4]	0
3	VW Vertical Height (YH) [3]	0
2	VW Vertical Height (YH) [2]	0
1	VW Vertical Height (YH) [1]	0
0	VW Vertical Height (YH) [0]	0

Bit	Description
7:0	**VW Vertical Height (YH) [7:0]:** • These bits are the least-significant 8 bits of the 10-bit field for the VW Vertical Height (YH). • The 10 bits of this field: — Define the height of the Video Window — Are not affected by scanline doubling or LCD vertical expansion — Are programmed before upscaling the VW vertically, based on the size of the image in memory that is to be displayed • The most-significant 2 bits are in Extension register CR36[3:2].

12.91 CR39: VW Surrounding Address Offset Register

I/O Port Address: 3?5

Index: 39

Bit	Description	Reset State
7	VW Surrounding Address Offset [8]	0
6	VW Surrounding Address Offset [7]	0
5	VW Surrounding Address Offset [6]	0
4	VW Surrounding Address Offset [5]	0
3	VW Surrounding Address Offset [4]	0
2	VW Surrounding Address Offset [3]	0
1	VW Surrounding Address Offset [2]	0
0	VW Surrounding Address Offset [1]	0

This register defines an offset value used when the VW width is less than the screen maximum.

Bit	Description
7:0	**VW Surrounding Address Offset [8:1]:** • These bits are the most-significant 8 bits of the 9-bit field for the VW Surrounding Address Offset. This field is used when the VW width is less than the screen maximum. • The least-significant bit is in Extension register CR33[7]. • The address offset value in this register is added to the address in the CRT address counter to allow the counter to skip over the area for the VW. • As a result, a restart address for the surrounding area can be defined without having to count through the VW. • This address offset value depends on the resolution of the surrounding mode. To program this register for the surrounding address offset: 1. For the VW, determine its width in pixels. 2. For the surrounding area, determine: a. The number of bits/pixel. b. The number of pixels/memory access. 3. Determine the address offset for the VW by dividing its width by the number of pixels in a memory fetch cycle. 4. Program into this register one-half the resulting value. For example, If: The VW is 320 pixels wide. The surrounding area has 4 bits/pixel. Therefore the number of pixels/memory access is 8. (The 32-bit width of the memory bus divided by 4 = 8 pixels/memory access.) Then: The offset is 320 ÷ 8 pixels/address = a 40-address offset. One-half of 40 is 20 decimal (14 hex). Program: Into CR39[7:0] the resulting value of 14h.

12.92 CR3A: VW Memory Start Address High Register

I/O Port Address: 3?5

Index: 3A

Bit	Description	Reset State
7	Reserved	
6	VW Memory Start Address [18]	0
5	VW Memory Start Address [17]	0
4	VW Memory Start Address [16]	0
3	VW Memory Start Address [15]	0
2	VW Memory Start Address [14]	0
1	VW Memory Start Address [13]	0
0	VW Memory Start Address [12]	0

Bit	Description
7	**Reserved**
6:0	**VW Memory Start Address [18:12]:** These bits are the 7 most-significant bits of the 19-bit field for the VW Memory Start Address field. • This address is programmed in increments of double-words, or on 32-bit boundaries. • As an example of how to program this field, for: — 1 Mbyte, the physical address is 00000:3FFF F from the display memory start. — 2 Mbytes, the physical address is 00000:7FFF F from the display memory start. • The other bits of this field are in Extension registers CR3E[7:0] and CR3F[3:0]. • If only this register is written, the VW is aligned at a 16-Kbyte boundary in the CPU host address space.

12.93 CR3B: VW Memory Address Offset Register

I/O Port Address: 3?5

Index: 3B

Bit	Description	Reset State
7	VW Memory Address Offset [7]	0
6	VW Memory Address Offset [6]	0
5	VW Memory Address Offset [5]	0
4	VW Memory Address Offset [4]	0
3	VW Memory Address Offset [3]	0
2	VW Memory Address Offset [2]	0
1	VW Memory Address Offset [1]	0
0	VW Memory Address Offset [0]	0

This register, along with the most-significant bit in CR36[4], defines an offset value.

Bit	Description
7:0	**VW Memory Address Offset [7:0]:** • These bits are the least-significant 8 bits of the 9-bit VW memory address offset value. This offset value is expressed as a double-word, and is added to the present VW Memory Start Address to obtain the next VW Memory Start Address. ADD: Present VW Memory Start Address TO: + VW Memory Address Offset (9-bit value) × 2 TO OBTAIN: = Next VW Memory Start Address • Using the VW Memory Address Offset to define the next memory-start address of the VW allows panning through a large area of the VW. The actual image stored in memory may be as large as 2K pixels at 16 bits/pixel. • The most-significant bit is in Extension register CR36[4].

12.94 CR3C: VW Horizontal Pixel Width, Enable, and Encoding Format Register

I/O Port Address: 3?5

Index: 3C

Bit	Description	Reset State
7	VW Horizontal Pixel Width [10]	0
6	VW Horizontal Pixel Width [9]	0
5	VW Live-Video Full-Screen Enable	0
4	VW Enable	0
3	VW Data Encoding Format [3]	0
2	VW Data Encoding Format [2]	0
1	VW Data Encoding Format [1]	0
0	VW Data Encoding Format [0]	0

Bit **Description**

7:6 **VW Horizontal Pixel Width [10:9]:**

- These bits are the most-significant 2 bits of the 11-bit VW Horizontal Pixel Width field.
- For details refer to Extension register CR3D[7:0], which contains the least-significant 8 bits of this field.

5 **VW Live Video Full-Screen Enable:**
When this bit is 1, through the MotionVideo Acceleration architecture, the VW uses the entire screen to display live video from off-screen display memory.

4 **VW Enable:**
When this bit is 1, the VW is enabled to fetch data from off-screen display memory and display it on the screen based on current programming for VW registers.

3:0 **VW Data Encoding Format [3:0]:**
These bits define in which data format the VW data is encoded.

NOTE: Reserved bits must not be programmed, as results cannot be guaranteed.

CR3C[3:0]		Encoding Format for VW
0h	0000	VW power-down (default)
1h	0001	15-bit RGB 5-5-5
2h	0010	AccuPak
3h	0011	4:2:2 YUV Y0UY1V (On the CPU bus, this encoding format appears as UY0 VY1.)
4h:7h	0100 to 0111	Reserved
8h	1000	24-bit RGB 8-8-8 (mapped through the Video Window)
9h–15h	1001 to 1111	Reserved

12.95 CR3D: VW Horizontal Pixel Width Register

I/O Port Address: 3?5

Index: 3D

Bit	Description	Reset State
7	VW Horizontal Pixel Width [8]	0
6	VW Horizontal Pixel Width [7]	0
5	VW Horizontal Pixel Width [6]	0
4	VW Horizontal Pixel Width [5]	0
3	VW Horizontal Pixel Width [4]	0
2	VW Horizontal Pixel Width [3]	0
1	VW Horizontal Pixel Width [2]	0
0	VW Horizontal Pixel Width [1]	0

Bit **Description**

7:0 **VW Horizontal Pixel Width [8:1]:**

- These 8 bits are the least-significant bits of an 11-bit field that contains a hex value used to define the VW width for each scanline the VW is enabled. (Refer to Figure 12-3.) The hex value represents the VW width as it is to be displayed, before on-chip upscaling.
- VW Horizontal Pixel Width bit 0 is always 0 and is not specified by a register.
- The most-significant 2 bits are in Extension register CR3C[7:6].

To calculate the value:

1. Determine the desired width of the VW. The VW width:
   a. Is expressed in 2-pixel pairs and is incremented with a 2-pixel granularity
   b. Must be at least 32 pixels wide and:
      — A multiple of 4 pixels if the VW data format is 8 bpp
      — A multiple of 2 pixels if the VW data format is 16 bpp

   NOTE: The 8-bpp and 16-bpp VW data formats provide a double-word pixel alignment, which is consistent with DCI requirements.
2. Divide the desired width by 2-pixel increments.
3. Translate the resulting decimal number into a hex number.
4. Program a hex number that is 1 hex number less than the result from the previous step.

12.95 CR3D: VW Horizontal Pixel Width Register *(cont.)*

Bit	Description
7:0 *(cont.)*	For example, to calculate the hex value for a 320-pixel-wide VW when the data format is 8 bpp: DIVIDE: The desired width (320 pixels) BY: ÷ 2-pixel increments TO OBTAIN: = Value for a 320-pixel-wide VW, where 160 (decimal) = A0h Program: A hex value that is one hex number less than the result (that is, program 9Fh).

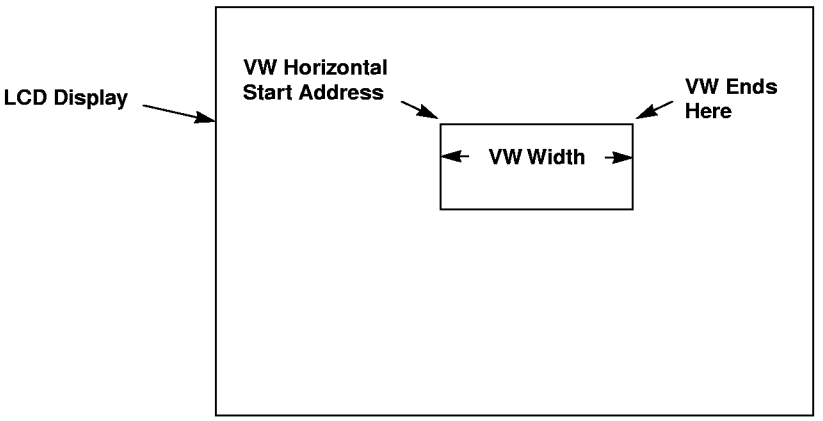


Figure 12-3. LCD Display with Video Window

12.96 CR3E: VW Memory Start Address Middle Register

I/O Port Address: 3?5

Index: 3E

Bit	Description	Reset State
7	VW Memory Start Address [11]	0
6	VW Memory Start Address [10]	0
5	VW Memory Start Address [9]	0
4	VW Memory Start Address [8]	0
3	VW Memory Start Address [7]	0
2	VW Memory Start Address [6]	0
1	VW Memory Start Address [5]	0
0	VW Memory Start Address [4]	0

Bit	Description
7:0	**VW Memory Start Address [11:4]:** • These bits are the middle 8 bits of the VW Memory Start Address field. • The other bits of this field are in Extension registers CR3A and CR3F. • For details on this field, refer to Extension register CR3A.

12.97 CR3F: VW Memory Start Address Low Register

I/O Port Address: 3?5

Index: 3F

Bit	Description	Reset State
7	VW Horizontal Pixel Interpolation Enable	0
6	Reserved	
5	Reserved	
4	Reserved	
3	VW Memory Start Address [3]	0
2	VW Memory Start Address [2]	0
1	VW Memory Start Address [1]	0
0	VW Memory Start Address [0]	0

Bit	Description
7	**VW Horizontal Pixel Interpolation Enable:** When this bit is: • 0 *and* Extension register CR31[7:0] is not programmed to 0, this bit enables the VW upscaling engine to horizontally replicate pixels selectively, based on the coefficient programmed in Extension register CR31. • 1, horizontal upscaling is done by pixel interpolation.
6:4	**Reserved**
3:0	**VW Memory Start Address [3:0]:** • These are the least-significant 4 bits of the VW Memory Start Address field. • The other bits of this field are in Extension registers CR3A and CR3E. • For details on this field, refer to Extension register CR3A.

12.98 CR40: LCD Horizontal-Display-Enable Start Register – No Centering

I/O Port Address: 3?5

Index: 40

Bit	Description	Reset State
7	LCD HDE Start (No Centering) [7]	0
6	LCD HDE Start (No Centering) [6]	0
5	LCD HDE Start (No Centering) [5]	0
4	LCD HDE Start (No Centering) [4]	0
3	LCD HDE Start (No Centering) [3]	0
2	LCD HDE Start (No Centering) [2]	0
1	LCD HDE Start (No Centering) [1]	0
0	LCD HDE Start (No Centering) [0]	0

This register is one of four Extension registers – CR40, CR41, CR42, and CR43 – that are used both to generate LCD horizontal timing and to center the image that appears on the LCD display.

Three of these registers – CR40, CR41, and CR42 – are complementary and mutually exclusive. Although they store the same timing-signal parameters, the values for the timing-signal parameters are usually different.

- Only one of these registers is enabled at any time.
- The selection of which of these registers control the LCD is done automatically, based on the conditions explained for each register.
- These registers are generally programmed only once at power-on self-test or when switching to LCD mode.

The 8 least-significant bits in CR40 and the ninth most-significant bit of Extension register CR46[4] make up a field that is used for non-centering cases for the following LCDs:

- 640 x 480 LCDs
- 800 x 600 LCDs
- 1024 x 768 LCDs

The CL-GD7548 *automatically* selects register CR40 as the default LCD horizontal-display-enable (HDE) start register if:

- Either CR41 or CR42 *are not* selected, or
- Horizontal expansion *is* selected

In normal 24-bit LCD modes, the CL-GD7548 starts to send data to the LCD immediately after HDE start, which may cause problems for some graphics modes. These three registers can be programmed to avoid the problems.

For typical timing relationships, refer to Figure 12-4.

12.98 CR40: LCD Horizontal-Display-Enable Start Register – No Centering *(cont.)*

Bit	Description
7:0	**LCD HDE Start (No Centering) [7:0]:** When no horizontal centering is needed, this register defines LCD HDE start (that is, the rising edge of the LCD horizontal display enable signal), relative to the previous CRT HDE start. • The value in this register defines both the LCD Line Clock start and the LCD HDE start. • For this register, a fine adjustment in 1-DCLK dot clock units is in CR43[1:0]. The LCD HDE start is expressed in 4-DCLK units. To calculate LCD HDE start: DIVIDE: [(Number of CRT Horizontal Total pixels) minus 32 pixels] BY: ÷ 4 (Number of 4-DCLK units) TO OBTAIN: = LCD HDE Start Where: Horizontal Total = CRT horizontal total in DCLK units. For example, If: A panel is 640 × 480 with a Horizontal Total of 800. Then: The CRT Horizontal Total, minus 32 is (800 – 32) = 768. The quantity 768 expressed in 4-DCLK units is (768 ÷ 4) = 192 decimal. Program: Into CR40 the hex value of 192 decimal, which is C0h.

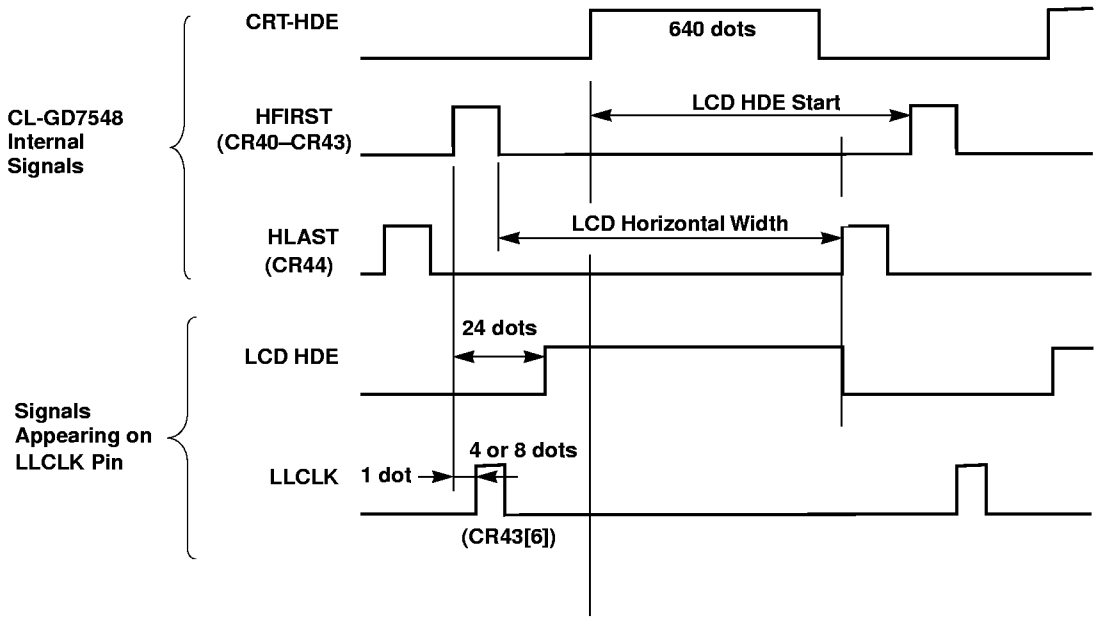


Figure 12-4. Horizontal Position for STN LCD Displaying 640 × 480 Image

12.99 CR41: LCD Horizontal-Display-Enable Start to Center 720-Dot Image

I/O Port Address: 3?5

Index: 41

Bit	Description	Reset State
7	LCD HDE Start to Center 720-Dot Image [7]	0
6	LCD HDE Start to Center 720-Dot Image [6]	0
5	LCD HDE Start to Center 720-Dot Image [5]	0
4	LCD HDE Start to Center 720-Dot Image [4]	0
3	LCD HDE Start to Center 720-Dot Image [3]	0
2	LCD HDE Start to Center 720-Dot Image [2]	0
1	LCD HDE Start to Center 720-Dot Image [1]	0
0	LCD HDE Start to Center 720-Dot Image [0]	0

This register is one of four Extension registers – CR40, CR41, CR42, and CR43 – that are used both to generate LCD horizontal timing and to center the image that appears on the LCD display.

The 8 least-significant bits in CR41 and the ninth most-significant bit of Extension register CR46[3] make up a field that is used for centering 720-dot images for the following LCDs:

- 800 x 600 LCDs
- 1024 x 768 LCDs

NOTE: For a description of all four registers and the LCD Horizontal Display Enable signal, and for the formula to calculate the LCD Horizontal Display Enable signal, refer to Extension register CR40.

The CL-GD7548 *automatically* uses this register to provide centering of a 720-dot image (text or graphics) when all the following conditions are met:

- The LCD is an 800 × 600.
- The LCD is not using 800 × 600 graphics modes.
- The LCD is using a character clock of 9-DCLK cycles (in text mode), or CRT HDE > 50h (in graphics mode).
- The LCD is not using horizontal expansion.

Bit	Description
7:0	**LCD HDE Start to Center 720-Dot Image [7:0]:** This register provides centering of a 720-dot image on a 800 × 600 LCD by defining the present LCD HDE start signal. • This register defines the present HDE start signal, relative to the previous HDE start signal, in 4-DCLK increments. (The DCLK is never divided by two.) • The value programmed in this register is in 4-DCLK increments, and this value is one less than the HDE start parameter. • On a 800 × 600 LCD, the value in this register defines both the LCD line-clock start and the LCD HDE start signals. A fine adjustment for this register is in Extension register CR43[3:2]. • When horizontal expansion is enabled, instead of using this register to define the LCD HDE start signal, the value in CR40 is used to define the LCD HDE start signal.

12.100 CR42: LCD Horizontal-Display-Enable Start to Center 640-Dot Image

I/O Port Address: 3?5

Index: 42

Bit	Description	Reset State
7	LCD HDE Start to Center 640-Dot Image [7]	0
6	LCD HDE Start to Center 640-Dot Image [6]	0
5	LCD HDE Start to Center 640-Dot Image [5]	0
4	LCD HDE Start to Center 640-Dot Image [4]	0
3	LCD HDE Start to Center 640-Dot Image [3]	0
2	LCD HDE Start to Center 640-Dot Image [2]	0
1	LCD HDE Start to Center 640-Dot Image [1]	0
0	LCD HDE Start to Center 640-Dot Image [0]	0

This register is one of four Extension registers – CR40, CR41, CR42, and CR43 – that are used both to generate LCD horizontal timing and to center the image that appears on the LCD display.

The 8 least-significant bits in CR42 and the ninth most-significant bit of Extension register CR46[2] make up a field that is used for centering 640-dot images for the following LCDs:

- 800 x 600 LCDs
- 1024 x 768 LCDs

NOTE: For a description of all four registers and the LCD Horizontal Display Enable signal, and for the formula to calculate the LCD Horizontal Display Enable signal, refer to Extension register CR40.

The CL-GD7548 *automatically* uses this register to provide centering of a 640-dot image (text or graphics) when all the following conditions are met:

- The LCD is an 800 × 600.
- The LCD is not using 800 × 600 graphics modes.
- The LCD is using a character clock of 8-DCLK cycles, and CRT HDE ≤ 50h.
- The LCD is not using horizontal expansion.

Bit	Description
7:0	**LCD HDE Start to Center 640-Dot Image [7:0]:** This register provides centering of a 640-dot image on a 800 × 600 LCD by defining the present LCD HDE start signal. • This register defines the present HDE start signal, relative to the previous HDE start signal, in 4-DCLK increments. (The DCLK is never divided by two.) • The value programmed in this register is in 4-DCLK increments, and this value is one less than the HDE start parameter. • On a 800 × 600 LCD, the value in this register defines both the LCD line-clock start and the LCD HDE start signals. A fine adjustment for this register is in Extension register CR43[5:4]. • When horizontal expansion is enabled, instead of using this register to define the LCD HDE start signal, the value in CR40 is used to define the LCD HDE start signal.

12.101 CR43: LCD Dot Clock Delay Control Register

I/O Port Address: 3?5

Index: 43

Bit	Description	Reset State
7	LCD HSYNC Width Control Enable	0
6	LCD Line Clock Width	0
5	CR42 Fine Dot Clock Delay [1]	0
4	CR42 Fine Dot Clock Delay [0]	0
3	CR41 Fine Dot Clock Delay [1]	0
2	CR41 Fine Dot Clock Delay [0]	0
1	CR40 Fine Dot Clock Delay [1]	0
0	CR40 Fine Dot Clock Delay [0]	0

This register is one of four Extension registers – CR40, CR41, CR42, and CR43 – that are used both to generate LCD horizontal timing and to center the image that appears on the LCD display. This register centers the image for the following LCDs:

- 640 x 480 LCDs
- 800 x 600 LCDs
- 1024 x 768 LCDs

NOTE: For a description of all four registers and the LCD Horizontal Display Enable signal, and for the formula to calculate the LCD Horizontal Display Enable signal, refer to Extension register CR40.

Bits [5:0] apply only to 800 x 600 LCDs. These bits make up three fields that when required, compensate for CL-GD7548 internal delays of the LCD horizontal display enable (HDE) start signal.

- For the different types of LCDs, these three fields make it possible to change the LCD horizontal display enable (HDE) start by adjusting the fine dot clock delay in 1-DCLK units.
- When it is necessary to change the LCD horizontal display enable (HDE) start, automatic switching takes place between these three fields. The switching is based on the following:
  — Values in the CRT controller registers
  — Values in the Sequencer registers
  — The type of LCD used (that is, 640 × 480 or 800 × 600)

Bit	Description
7	**LCD HSYNC Width Control Enable:** When this bit is 1, it enables the LCD HSYNC Width Control bits in Extension register R1X[4:0] to be used with any LCD panel, including non-TFT LCDs.
6	**LCD Line Clock Width:** This bit selects the width of the LLCLK, the LCD scanline clock. When this bit is: • 0, the LLCLK width is 4 dot clocks. • 1, the LLCLK width is 8 dot clocks.

12.101 CR43: LCD Dot Clock Delay Control Register *(cont.)*

Bit	Description
5:4	**CR42 Fine Dot Clock Delay [1:0]:** To program the LCD HDE start signal for a dot clock delay, refer to Table 12-2.
3:2	**CR41 Fine Dot Clock Delay [1:0]:** To program the LCD HDE start signal for a dot clock delay, refer to Table 12-2.
1:0	**CR40 Fine Dot Clock Delay [1:0]:** To program the LCD HDE start signal for a dot clock delay, refer to Table 12-2.

Table 12-2. Fine Dot Clock Delay Options for LCD HDE Start Signals

CR43		Fine Dot Clock Delay for:
[5]	[4]	CR42
[3]	[2]	CR41
[1]	[0]	CR40
0	0	No delay
0	1	Delay LCD HDE start by 1 DCLK
1	0	Delay LCD HDE start by 2 DCLKs
1	1	Delay LCD HDE start by 3 DCLKs

12.102 CR44: LCD Horizontal Width Register

I/O Port Address: 3?5

Index: 44

Bit	Description	Reset State
7	LCD Horizontal Width [7]	0
6	LCD Horizontal Width [6]	0
5	LCD Horizontal Width [5]	0
4	LCD Horizontal Width [4]	0
3	LCD Horizontal Width [3]	0
2	LCD Horizontal Width [2]	0
1	LCD Horizontal Width [1]	0
0	LCD Horizontal Width [0]	0

This register defines the horizontal width for the following LCDs:

- 640 x 480 LCDs
- 800 x 600 LCDs
- 1024 x 768 LCDs

Bit	Description
7:0	**LCD Horizontal Width [7:0]:** • These bits are the least-significant 8 bits of a 9-bit field that defines the LCD horizontal width. If an LCD: — Is an XGA LCD (1024 x 768), these 8 bits are used in combination with the most-significant ninth bit, in Extension register CR46[0]. — Is not an XGA LCD, only these 8 bits are used. • The value programmed in this register: — Defines the LCD horizontal width. This width can be different from the width of the image, stored in display memory, that is to be displayed. — Is never expressed in units of DCLK ÷ 2. — Must be the desired width (expressed in 4 DCLK increments), plus five, all expressed in hex. For example, If: An LCD panel is 800 (horizontal) x 600 (vertical). Then: The desired width is 800 pixels. The desired width, when expressed in 4 DCLK increments, is 800 ÷ 4 = 200. The desired 4-DCLK width of 200, plus 5 = 205 decimal. Program: Into the LCD horizontal width field the hex equivalent of 205 decimal, which is CDh.

12.103 CR46: LCD Shift Clock Delay Control Register

I/O Port Address: 3?5

Index: 46

Bit	Description	Reset State
7	LCD Programmable Shift Clock Delay [2]	0
6	LCD Programmable Shift Clock Delay [1]	0
5	LCD Programmable Shift Clock Delay [0]	0
4	LCD HDE Start (No Centering) [8]	0
3	LCD HDE Start to Center 720-Dot Image [8]	0
2	LCD HDE Start to Center 640-Dot Image [8]	0
1	TFT HSYNC Horizontal Start [8]	0
0	LCD Horizontal Width [8]	0

Bit	Description
7:5	**LCD Programmable Shift Clock Delay [2:0]** This 3-bit field controls the shift clock delay, which can be from 0 to 7 ns.
4	**LCD Horizontal-Display-Enable Start (No Centering) [8]:** • This bit is the most-significant bit of a 9-bit field that is used for non-centering of XGA (1024 x 768) TFT LCDs. • This ninth bit is required only for XGA TFT LCDs. • For details refer to CR40, which contains the 8 least-significant bits.
3	**LCD Horizontal-Display-Enable Start to Center 720-Dot Image [8]:** • This bit is the most-significant bit of a 9-bit field that defines the present HDE start signal to center a 720-dot image on an XGA (1024 x 768) TFT LCD. • This ninth bit is required only for XGA TFT LCDs. • For details refer to CR41, which contains the 8 least-significant bits.
2	**LCD Horizontal-Display-Enable Start to Center 640-Dot Image [8]:** • This bit is the most-significant bit of a 9-bit field that defines the present HDE start signal to center a 640-dot image on an XGA (1024 x 768) TFT LCD. • This ninth bit is required only for XGA TFT LCDs. • For details refer to CR42, which contains the 8 least-significant bits.
1	**TFT HSYNC Horizontal Start [8]:** • This bit is the most-significant bit of a 9-bit field that defines the exact starting position of the TFT HSYNC signal. • This ninth bit is required only for XGA TFT LCDs. • For details refer to CR47, which contains the 8 least-significant bits.
0	**LCD Horizontal Width [8]:** • This bit is the most-significant bit of a 9-bit field that defines the LCD horizontal width. • This ninth bit is required only for XGA TFT LCDs. • For details refer to CR44, which contains the 8 least-significant bits.

12.104 CR47: TFT HSYNC Horizontal Start Register

I/O Port Address: 3?5

Index: 47

Bit	Description	Reset State
7	TFT HSYNC Horizontal Start [7]	0
6	TFT HSYNC Horizontal Start [6]	0
5	TFT HSYNC Horizontal Start [5]	0
4	TFT HSYNC Horizontal Start [4]	0
3	TFT HSYNC Horizontal Start [3]	0
2	TFT HSYNC Horizontal Start [2]	0
1	TFT HSYNC Horizontal Start [1]	0
0	TFT HSYNC Horizontal Start [0]	0

The bits in this register are part of a 9-bit field that defines the start of the TFT HSYNC signal. This field is not dependent on character-clock width or DCLK/2 control.

Bit	Description
7:0	**TFT HSYNC Horizontal Start [7:0]:** • These bits are the least-significant bits of a 9-bit field that defines the exact starting position of the TFT HSYNC horizontal start signal. If an LCD: — Is an XGA LCD (1024 x 768), these 8 bits are used in combination with the most-significant ninth bit, in Extension register CR46[1]. — Is not an XGA LCD, only these 8 bits are used. The TFT HSYNC Horizontal Start position is: • Relative to the previous LCD CRT horizontal display enable (HDE) start, in DCLK/4 increments. • Positioned about 144 dot clocks before the start of the LCD HDE start signal, which is also relative to the CRT HDE start. • Adjustable in 1-DCLK increments with CR48[1:0]. When Extension register R7X[2] = 1: • The TFT HSYNC signal, instead of the LLCLK signal, appears on the LLCLK pin. (The LLCLK signal always starts 1 DCLK after the LCD HDE start.) • This setup is needed to support TFT LCDs that require 144 dot clocks between LLCLK and the first shift clock on a scanline. **NOTE:** Some LCD manufacturers call the LLCLK signal HSYNC. Cirrus Logic calls this signal TFT HSYNC, to differentiate it from the CRT HSYNC signal.

12.105 CR48: TFT HSYNC and Vertical Size for LCD Extension Register

I/O Port Address: 3?5

Index: 48

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Vertical Size for LCDs [9]	0
4	Vertical Size for LCDs [8]	0
3	Reserved	
2	Vertical Size for Upper Half of Dual-Scan STN LCDs [8]	0
1	TFT HSYNC Dot-Clock Delay [1]	0
0	TFT HSYNC Dot-Clock Delay [0]	0

Bit — **Description**

7:6 — **Reserved**

5:4 — **Vertical Size for LCDs [9:8]:**

- These bits are the most-significant 2 bits of a 10-bit field that defines in scanlines the vertical size of an LCD (either STN or TFT).
- For details refer to Extension register CR4A[7:0], which contains the least-significant 8 bits.

3 — **Reserved**

2 — **Vertical Size for Upper Half of Dual-Scan STN LCDs [8]:**

- This bit is the most-significant bit of a 9-bit field that defines in scanlines the vertical size for the upper half of a dual-scan STN LCD.
- For details refer to Extension register CR49[7:0], which contains the least-significant 8 bits.

1:0 — **TFT HSYNC Dot Clock Delay [1:0]:**

- These bits provide further control, in 1-DCLK increments, for the TFT HSYNC horizontal start position that is defined in CR47 in 4-DCLK increments.
- These bits control the dot clock delay in 1-DCLK increments, according to the following table:

CR48		Dot-Clock Delay
[1]	[0]	
0	0	No delay
0	1	Delay is 1 dot clock.
1	0	Delay is 2 dot clocks.
1	1	Delay is 3 dot clocks.

12.106 CR49: Vertical Size for Upper Half of Dual-Scan STN LCDs

I/O Port Address: 3?5

Index: 49

Bit	Description	Reset State
7	Vertical Size for Upper Half of Dual-Scan STN LCDs [7]	0
6	Vertical Size for Upper Half of Dual-Scan STN LCDs [6]	0
5	Vertical Size for Upper Half of Dual-Scan STN LCDs [5]	0
4	Vertical Size for Upper Half of Dual-Scan STN LCDs [4]	0
3	Vertical Size for Upper Half of Dual-Scan STN LCDs [3]	0
2	Vertical Size for Upper Half of Dual-Scan STN LCDs [2]	0
1	Vertical Size for Upper Half of Dual-Scan STN LCDs [1]	0
0	Vertical Size for Upper Half of Dual-Scan STN LCDs [0]	0

Bit	Description
7:0	**Vertical Size for Upper Half of Dual-Scan STN LCDs [7:0]:** • These bits are the least-significant 8 bits of a 9-bit field that defines the vertical size in scanlines for the upper half of a dual-scan STN LCD. • The most-significant ninth bit of this field is in CR48[2]. • This vertical display position is relative to the start of the first vertical pulse, which is ahead of the actual vertical display when the centering feature is enabled (using Extension registers CR40 through CR43). • Up to 511 scanlines can be defined for display on the upper half of a dual-scan STN LCD. • The actual value in this register is one less than the lines displayed on the upper half of the LCD. For example, for an LCD using a: — 480-scanline mode, program 239, which is obtained as follows: (480 ÷ 2) = 240 scanlines being displayed on upper half of LCD display. Therefore, 240 - 1 = 239. — 600-scanline mode, program 299, which is obtained as follows: (600 ÷ 2) = 300 scanlines being displayed for upper half of LCD display. Therefore, 300 - 1 = 299. **NOTE:** The number of scanlines programmed in this register represents actual displayed scanlines for the upper half of a dual-scan STN LCD. (In contrast, Extension register CR4A programs a value that represents two less scanlines than the actual displayed scanlines.)

12.107 CR4A: Vertical Size for LCDs

I/O Port Address: 3?5

Index: 4A

Bit	Description	Reset State
7	Vertical Size for LCDs [7]	0
6	Vertical Size for LCDs [6]	0
5	Vertical Size for LCDs [5]	0
4	Vertical Size for LCDs [4]	0
3	Vertical Size for LCDs [3]	0
2	Vertical Size for LCDs [2]	0
1	Vertical Size for LCDs [1]	0
0	Vertical Size for LCDs [0]	0

Bit	Description
7:0	**Vertical Size for LCDs [7:0]:** • These bits are the least-significant 8 bits of a 10-bit field that defines in scanlines the total vertical size of an LCD, either STN or TFT. • The vertical display position is relative to the first vertical pulse on LCDs. • The actual value in this register is two scanlines less than the total scanlines being displayed. (For example, for a 480-scanline display, program 478 scanlines.) • Dual-scan LCDs normally have the same amount of scanlines in both the upper and lower halves of the LCD. • The most-significant 2 bits of this field are in CR48[5:4].

12.108 CR4B: Reserved — Scratchpad Register

I/O Port Address: 3?5

Index: 4B

Bit	Description	Reset State
7	R/W Data [7]	0
6	R/W Data [6]	0
5	R/W Data [5]	0
4	R/W Data [4]	0
3	R/W Data [3]	0
2	R/W Data [2]	0
1	R/W Data [1]	0
0	R/W Data [0]	0

This register is reserved for the exclusive use of the CL-GD7548 BIOS and must never be written by any application program. It is listed here only for completeness.

Bit	Description
7:0	**Reserved:** These bits are reserved for the Cirrus Logic BIOS.

12.109 CR4C: Graphics Input-Resolution Override for Dithering

I/O Port Address: 3?5

Index: 4C

Bit	Description	Reset State
7	Graphics Input-Resolution Override Enable	0
6	Reserved	
5	Reserved	
4	Reserved	
3	Graphics Input-Resolution Override [3]	0
2	Graphics Input-Resolution Override [2]	0
1	Graphics Input-Resolution Override [1]	0
0	Graphics Input-Resolution Override [0]	0

This register, which is used with both TFT and STN LCDs, is used to change the CL-GD7548 default input resolution settings for graphics data sent to the dither block. (For input resolution for VW and the Video Overlay, refer to Extension register CR4E.)

- When the VW is enabled, this override register affects only the surrounding area.
- The VW display is controlled by independent input and output resolution control bits.
- This register supports a maximum of 6 × 6 dithering.
- STILL NEED TO INVESTIgATE 5-5-5 and 5-5-6???

Bit **Description**

7 **Graphics Input-Resolution Override Enable:**

- When this bit is 0:
  - — The CL-GD7548 has default input resolution settings for dithering that maximize the number of colors displayed on an LCD.
  - — The settings from Extension register HDR (the Hidden DAC register) apply, including the default input resolution settings shown in the table below:

Dithering Matrix	Default Input Resolution Settings
8 bits/color	8-8-8 true-color mode
6 bits/color	All VGA-compatibility color modes
	All extended color modes that go through the palette RAMDAC
	5-6-5 high-color mode (Video Overlay mode only, and not VW)
5 bits/color	5-5-5 direct-color mode
3 bits/color	3-3-2 color mode (does not go through the palette RAMDAC)

12.109 CR4C: Graphics Input-Resolution Override for Dithering *(cont.)*

Bit	Description
7 *(cont.)*	**Graphics Input-Resolution Override Enable** *(cont.)*: • When this bit is 1: — The default input resolution settings are overridden, and new input resolution values are defined in CR4C[3:0]. — If the default input resolution settings are not desired, the BIOS can override them by programming any number between 0h and Fh. As a result, the CL-GD7548 can dither more or less than the default case. — As long as the dithering matrix is smaller than or equal to 6 × 6, the CL-GD7548 supports a combination of input and output resolutions.
6:4	**Reserved**
3:0	**Graphics Input-Resolution Override [3:0]:** • When the CR4C[7] override enable bit is 1, as shown in the table that follows, the CR4C[3:0] bits define the new input-resolution values for data sent to the dithering block. • The hex value programmed in these bits define the number of bits per color that the CL-GD7548 uses to control the dithering on an LCD, independent of the following: — The output resolution — The dithering state (enabled vs. disabled) — The CL-GD7548 mode (graphics vs. text)

CR4C				Dithering Result for LCD
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/color
0	1	0	0	4 bits/color
0	1	0	1	5 bits/color
0	1	1	0	6 bits/color
0	1	1	1	7 bits/color
1	0	0	0	8 bits/color

12.109 CR4C: Graphics Input-Resolution Override for Dithering *(cont.)*

Bit	Description
3:0 *(cont.)*	**Graphics Input-Resolution Override [3:0]** *(cont.)*:

Example 1:

When the given conditions are:

- Data comes from the 18-bit palette DAC CLUT as 6 bits/color.
- Colors displayed are 256.
- There are 8 bits/pixel.
- LCD is a 3 bits/color TFT.

Then:

- The CL-GD7548 default input resolution is 6 bits/color.
- The CL-GD7548 output resolution is 3 bits/color.
- When 2 × 2 dithering is enough:
  - The 6 bits/color default input resolution is overridden with one of 5 bits/color.
  - Since 5 bits/color – 3 bits/color = 2 bits/color, this leads to a 2 × 2 dithering and the equivalent of 5 bits/color (2^5 = 32 colors per color, or 32K colors).
- When 256K colors is not enough and a better effect is desired:
  - More dithering is possible by programming an input resolution of 7 bits/color.
  - Since 7 bits/color – 3 bits/color = 4 bits/color, this leads to a 4 × 4 dithering and the equivalent of 7 bits/color (2^7 = 128 colors per color, or 2M colors).

Example 2:

When the given conditions are:

- Colors displayed are 16.
- There are 8 bits/pixel.
- LCD is a color STN.
- The output resolution is programmed as 4 bits/color (2^4 = 16).

Then:

- The CL-GD7548 default input resolution is 6 bits/color. (Combining 2^4 = 16 colors with 2^2 = 4 color dithering results in 2^4 x 2^2 = 2^6 = 6 bits/color.
- By changing the output resolution to 3 bits/color, the CL-GD7548 generates 2^3 = 8 colors.
- When the input resolution is 6 bits/color, the CL-GD7548 does more dithering to get 6 bits/color.
- When the input resolution is 4 bits/color, the CL-GD7548 needs only 1 × 1 dithering to get a total of 16 equivalent colors per color.

12.110 CR4D: Output Resolution for Dithering

I/O Port Address: 3?5

Index: 4D

Bit	Description	Reset State
7	VW / Video Overlay Output Resolution for Dithering [3]	0
6	VW / Video Overlay Output Resolution for Dithering [2]	0
5	VW / Video Overlay Output Resolution for Dithering [1]	0
4	VW / Video Overlay Output Resolution for Dithering [0]	0
3	Output Resolution for Dithering [3]	0
2	Output Resolution for Dithering [2]	0
1	Output Resolution for Dithering [1]	0
0	Output Resolution for Dithering [0]	0

Bit **Description**

7:4 **VW and Video Overlay Output Resolution for Dithering [3:0]:**
These bits define the output resolution value for dithering exactly in the same way as CR4D[3:0], except they apply to the VW and/or to the Feature Connector Video Overlay.

3:0 **Output Resolution for Dithering [3:0]:**
These bits define typical output resolution values for dithering various LCDs. The hex value programmed in these bits define the number of bits per color used by the CL-GD7548.

CR4D				Output Resolution for Dithering LCDs:	
[3]	[2]	[1]	[0]	TFT LCDs (No Frame-Rate Modulation)	STN LCDs (Frame-Rate Modulation Occurs)
0	0	0	1	Not applicable	2-shade STN LCDs: 1 bit/color
0	0	1	0	Not applicable	4-shade STN LCDs: 2 bits/color
0	0	1	1	3 bits/color	8-shade STN LCDs: 3 bits/color
0	1	0	0	4 bits/color	16-shade STN LCDs: 4 bits/color
0	1	1	0	6 bits/color	Not applicable
1	0	0	0	8 bits/color	Not applicable

NOTE: Programming values other than the ones specified in the above table may have unpredictable results. Also, the system reset value of zero is not a valid value. Therefore, **this register must be programmed at start-up with the correct output resolution for the LCD used (TFT or STN).**

12.111 CR4E: VW/Video Overlay Input-Resolution Override

I/O Port Address: 3?5

Index: 4E

Bit	Description	Reset State
7	VW / Video Overlay Input-Resolution Override Enable	0
6	VW Dithering Enable for LCDs	0
5	Video Overlay Dithering Enable	0
4	Reserved	
3	VW/Video Overlay Input-Resolution Override [3]	0
2	VW/Video Overlay Input-Resolution Override [2]	0
1	VW/Video Overlay Input-Resolution Override [1]	0
0	VW/Video Overlay Input-Resolution Override [0]	0

This register is used to change the CL-GD7548 default resolution settings for the video data sent to the dither block, either for the VW only, or for when the VW fills the entire screen.

Bit **Description**

7 **VW/Video Overlay Input-Resolution Override Enable:**

- When this bit is 0:
  - — The input resolution for video data is controlled by Extension register HDR (the Hidden DAC register).
  - — The default input resolution settings shown in the table below apply.

Dithering Matrix	Default Input Resolution Settings
8 bits/color	8-8-8 true-color mode
6 bits/color	All VGA-compatibility color modes
	All extended color modes that go through the palette RAMDAC
5 bits/color	5-5-5 direct-color mode
3 bits/color	3-3-2 color mode (does not go through the palette RAMDAC)

- When this bit is 1:
  - — The default input resolution settings for the VW are overridden, and new values are defined in bits CR4E[3:0] of this register.

12.111 CR4E: VW/Video Overlay Input-Resolution Override *(cont.)*

Bit	Description
6	**VW Dithering Enable for LCDs:** • When this bit is: — 0, VW dithering is disabled. — 1, VW dithering is enabled. • This bit applies only to LCDs, and not CRTs.
5	**Video Overlay Dithering Enable:** When this bit is: • 0, the Video Overlay Window is dithered exactly as in graphics modes. The color key and the OVRW# signal define the Video Overlay Window. • 1, Video Overlay dithering is enabled. — Feature Connector Video Overlay data is dithered, based on the input resolution in CR4E[3:0] and the output resolution in CR4D[7:4]. — Unlike VW and graphics modes, Video Overlay does not have an override for input resolution. Instead, the input resolution is always the one in CR4E[3:0].
4	**Reserved**
3:0	**VW/Video Overlay Input-Resolution Override [3:0]:** When the CR4E[7] override enable bit is 1, the CR4E[3:0] bits define the new input-resolution values for data sent to the dithering block, so that the amount of colors in VW can differ from the surrounding area. • The hex value programmed can be any number between 1h and Fh. • There is no default value for the Video Overlay input resolution. Instead, it is always defined by these bits. • The value programmed in these bits define the number of bits per color that the CL-GD7548 uses to control the dithering on an LCD, independent of: — The output resolution — The dithering state (enabled vs. disabled) — The CL-GD7548 mode (graphics vs. text)

CR4E				Dithering Result for LCD
[3]	[2]	[1]	[0]	
0	0	1	1	3 bits/color (RGB 3-3-2)
0	1	0	1	5 bits/color (RGB 5-5-5)
0	1	1	0	6 bits/color (all palettized modes)
0	1	1	1	7 bits/color
1	0	0	0	8 bits/color. Includes: RGB 5-5-5 mode and 4:2:2 YUV

12.112 CR50: V-Port Control Register

I/O Port Address: 3?5

Index: 50

Bit	Description	Access	Reset State
7	Reserved		
6	V-Port Non-Interlaced Mode Enable	R/W	0
5	V-Port Data Latch Control	R/W	0
4	V-Port Data Bus Width Control	R/W	0
3	DDCC / DDCD Pinout Configuration	R/W	0
2	V-Port Pinout and Hardware Configuration [2]	R/W	0
1	V-Port Pinout and Hardware Configuration [1]	R/W	0
0	V-Port Pinout and Hardware Configuration [0]	R/W	0

This register is used to configure the CL-GD7548 hardware and V-Port pins for specifed port configurations. However, the V-Port operation does not become enabled until CR51[3] is set to 1.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7	**Reserved**
6	**V-Port Non-Interlaced Mode Enable:** When the FCPU pin is low *and* this bit is: • 0, the V-Port is in the interlaced mode. • 1, the V-Port is in the non-interlaced mode.
5	**V-Port Data Latch Control:** When the FCPU pin is low *and* this bit is: • 0, the V-Port latches data on the rising edge of ZVPCLKI. • 1, the V-Port latches data on the falling edge of ZVPCLKI.
4	**V-Port Data Bus Width Control:** When the FCPU pin is low *and* this bit is: • 0, the V-Port is 8 bits wide. (When the CL-GD7548 is configured for the VESA VL-Bus, this bit setting *must* be used.) • 1, *and* the CL-GD7548 is configured for PCI bus, the V-Port is 16 bits wide.

12.112 CR50: V-Port Control Register *(cont.)*

Bit	Description
3	**DDCC / DDCD Pinout Configuration:** When the FCPU pin is low *and* this bit is: • 0: — The DDCC / FCDCLK / VCLK pin is configured for either FCDCLK or VCLK, depending on the settings described under Extension register bits SR23[4] and SR24[4]. — The ACTI / DDCD / FCEVIDEO# / SBYI is configured for ACTI, FCEVIDEO#, or SBYI, depending on the settings described under Extension register bit SR23[6]. • 1 (*or* when Extension register bit SR8[6] is 1): — The DDCC / FCDCLK / VCLK pin is configured for DDCC. — The ACTI / DDCD / FCEVIDEO# / SBYI pin is configured for DDCD.
2:0	**V-Port Pinout and Hardware Configuration:** When Extension register CR51[3] is set to 1, (that is, the V-Port operation is enabled), the V-Port data and control pins are configured as shown in the table below:

CR50			Configuration
[2]	[1]	[0]	
0	0	0	V-Port disabled
0	0	1	V-Port enabled
0	1	0	Reserved
to			
1	1	1	

NOTE: The DDC pinout configuration (that is, the configuration for the DDCC / FCDCLK / VCLK and ACTI / DCDD / FCEVIDEO# / SBYI pins) is not affected by these bits.

12.113 CR51: V-Port Data Format Register

I/O Port Address: 3?5

Index: 51

Bit	Description	Reset State
7	V-Port FIFO Threshold in VW [2]	0
6	V-Port FIFO Threshold in VW [1]	0
5	V-Port FIFO Threshold in VW [0]	0
4	V-Port Downscaling Enable	0
3	V-Port Operation Enable	0
2	V-Port Data Format Select [2]	0
1	V-Port Data Format Select [1]	0
0	V-Port Data Format Select [0]	0

This register is used to configure the CL-GD7548 V-Port data format.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:5	**V-Port FIFO Threshold in VW [2:0]:** When the FCPU pin is low, the value programmed in these bits determines the number of CAS# cycles in each V-Port FIFO fill cycle within the Capture Window, except for V-Port FIFO flush cycles.
4	**V-Port Downscaling Enable:** When the FCPU pin is low *and* this bit is: • 0, the V-Port downscaler is disabled. • 1, the V-Port downscaler is enabled, and the following color space formats can be downscaled: — 4:2:2 YUV — 4:2:2 YUV compressed to AccuPak — RGB 5-5-5 **NOTE:** Video data from AccuPak cannot be downscaled within the V-Port. Instead, the data must be scaled down within the original source of the video data.
3	**V-Port Operation Enable:** This bit enables the V-Port operations. When the FCPU pin is low, *and* this bit is: • 0, the V-Port is disabled, even if the the CL-GD7548 hardware and V-Port pins are configured for the V-Port. • 1, the V-Port memory cycles occur based on the current V-Port configuration, and the V-Port data is displayed. — The V-Port configuration bits in CR50[2:0] must be set before this bit can be enabled. — This bit takes effect on the falling edge of the V-Port VSYNC signal.

12.113 CR51: V-Port Data Format Register *(cont.)*

Bit	Description
2:0	**V-Port Data Format Select:** These bits select the format of the V-Port data, according to the following table.

CR51			V-Port Data Format
[2]	[1]	[0]	
0	0	0	4:2:2 YUV
0	0	1	RGB 5-5-5
0	1	0	AccuPak
0	1	1	4:2:2 YUV, compressed to AccuPak by the CL-GD7548 before being stored in frame buffers
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

12.114 CR52: V-Port Horizontal Downscaling Coefficient Register

I/O Port Address: 3?5

Index: 52

Bit	Description	Reset State
7	V-Port Horizontal Downscaling Coefficient [7]	0
6	V-Port Horizontal Downscaling Coefficient [6]	0
5	V-Port Horizontal Downscaling Coefficient [5]	0
4	V-Port Horizontal Downscaling Coefficient [4]	0
3	V-Port Horizontal Downscaling Coefficient [3]	0
2	V-Port Horizontal Downscaling Coefficient [2]	0
1	V-Port Horizontal Downscaling Coefficient [1]	0
0	V-Port Horizontal Downscaling Coefficient [0]	0

This register is used to set the coefficient for the V-Port horizontal downscaling.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:0	**V-Port Horizontal Downscaling Coefficient:** These bits determine the coefficient for V-Port horizontal downscaling, which is done through pixel decimation. To calculate the V-Port horizontal downscaling coefficient: DIVIDE: The value in CR52[7:0] (in its decimal form) BY: ÷ 256 (This register is an 8-bit register, and $2^8 = 256$.) TO OBTAIN: = V-Port Horizontal Downscaling Coefficient When the value in CR52[7:0] is 0h, no downscaling can occur.

12.115 CR53: V-Port Vertical Downscaling Coefficient Register

I/O Port Address: 3?5

Index: 53

Bit	Description	Reset State
7	V-Port Vertical Downscaling Coefficient [7]	0
6	V-Port Vertical Downscaling Coefficient [6]	0
5	V-Port Vertical Downscaling Coefficient [5]	0
4	V-Port Vertical Downscaling Coefficient [4]	0
3	V-Port Vertical Downscaling Coefficient [3]	0
2	V-Port Vertical Downscaling Coefficient [2]	0
1	V-Port Vertical Downscaling Coefficient [1]	0
0	V-Port Vertical Downscaling Coefficient [0]	0

This register is used to set the coefficient for the V-Port vertical downscaling.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:0	**V-Port Vertical Downscaling Coefficient:** These bits determine the coefficient for V-Port vertical downscaling, which is done through scanline decimation. To calculate the V-Port vertical downscaling coefficient: DIVIDE: The value in CR53[7:0] (in its decimal form) BY: ÷ 256 (This register is an 8-bit register, and $2^8 = 256$.) TO OBTAIN: = V-Port Vertical Downscaling Coefficient When the value in CR53[7:0] is 0h, no downscaling can occur.

12.116 CR54: V-Port Capture Window Horizontal Start Register

I/O Port Address: 3?5

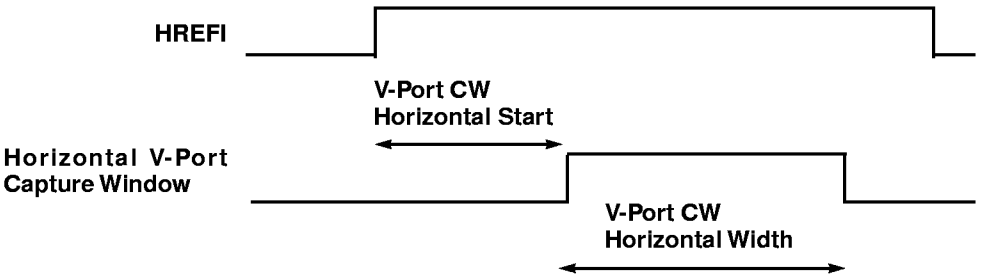
Index: 54

Bit	Description	Reset State
7	V-Port Capture Window Horizontal Start [7]	0
6	V-Port Capture Window Horizontal Start [6]	0
5	V-Port Capture Window Horizontal Start [5]	0
4	V-Port Capture Window Horizontal Start [4]	0
3	V-Port Capture Window Horizontal Start [3]	0
2	V-Port Capture Window Horizontal Start [2]	0
1	V-Port Capture Window Horizontal Start [1]	0
0	V-Port Capture Window Horizontal Start [0]	0

This register is used to set the delay for the horizontal start of the V-Port Capture Window.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:0	**V-Port Capture Window Horizontal Start [7:0]:** • These bits are the least-significant 8 bits of a 10-bit field that expresses a value for the position of the horizontal start of the V-Port Capture Window. • The start value: — In contrast to CR55 (the V-Port Capture Window Horizontal Width register) is expressed in pixels *before* the video data is scaled down. — Must always be a multiple of two. • The most-significant 2 bits of this field are in CR58[1:0]. • The following timing diagram shows the relationship of the V-Port Capture Window horizontal start signal to the HREFI signal (which is generated by the decoder).



12.117 CR55: V-Port Capture Window Horizontal Width Register

I/O Port Address: 3?5

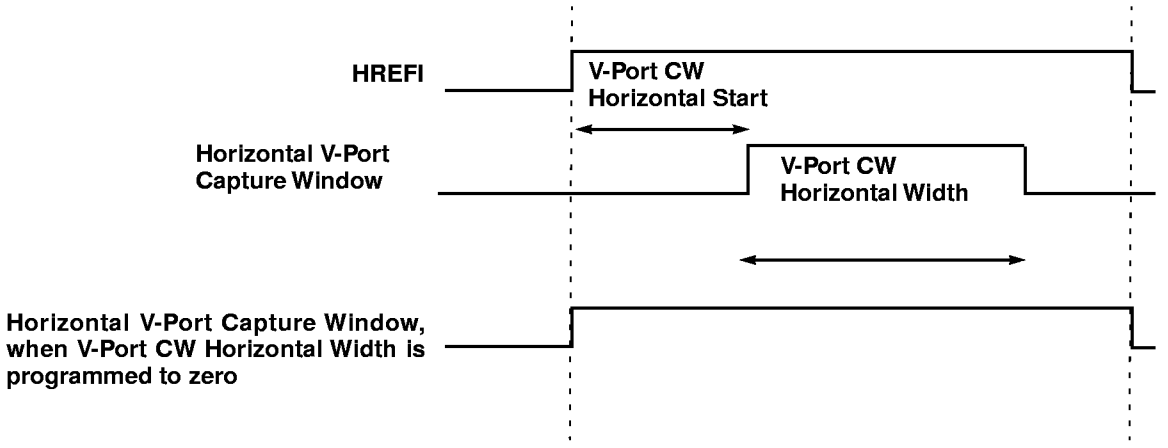
Index: 55

Bit	Description	Reset State
7	V-Port Capture Window Horizontal Width [7]	0
6	V-Port Capture Window Horizontal Width [6]	0
5	V-Port Capture Window Horizontal Width [5]	0
4	V-Port Capture Window Horizontal Width [4]	0
3	V-Port Capture Window Horizontal Width [3]	0
2	V-Port Capture Window Horizontal Width [2]	0
1	V-Port Capture Window Horizontal Width [1]	0
0	V-Port Capture Window Horizontal Width [0]	0

This register is used to set the horizontal width of the V-Port Capture Window.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:0	**V-Port Capture Window Horizontal Width [7:0]:** • These bits are the least-significant 8 bits of a 10-bit field that expresses a value for the horizontal width of the V-Port Capture Window. • The width value: — In contrast to CR54 (the V-Port Capture Window Horizontal Start register) is expressed in pixels *after* the video data is scaled down. — Must always be a multiple of two. • If the value in this field is zero, then the HREFI signal defines the horizontal width of the V-Port Capture Window. • The most-significant 2 bits of this field are in CR58[3:2]. • The following timing diagram shows the relationship of the V-Port Capture Window horizontal width signal to the horizontal start signal.



12.118 CR56: V-Port Capture Window Vertical Start Register

I/O Port Address: 3?5

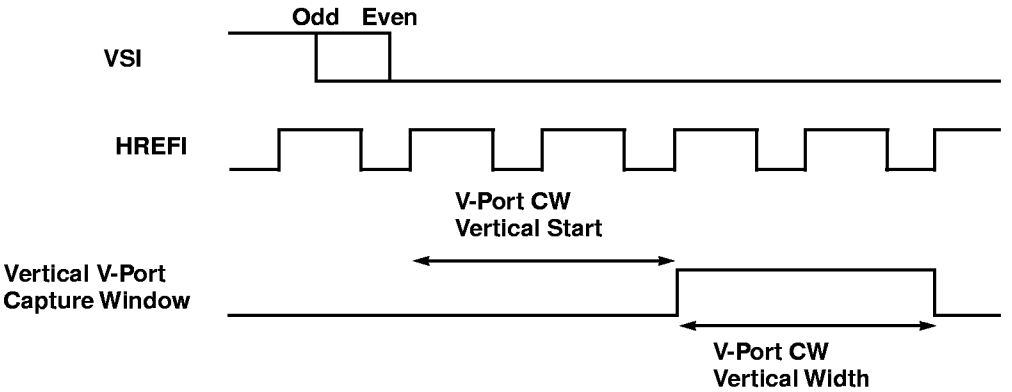
Index: 56

Bit	Description	Reset State
7	V-Port Capture Window Vertical Start [7]	0
6	V-Port Capture Window Vertical Start [6]	0
5	V-Port Capture Window Vertical Start [5]	0
4	V-Port Capture Window Vertical Start [4]	0
3	V-Port Capture Window Vertical Start [3]	0
2	V-Port Capture Window Vertical Start [2]	0
1	V-Port Capture Window Vertical Start [1]	0
0	V-Port Capture Window Vertical Start [0]	0

This register is used to set the delay for the vertical start of the V-Port Capture Window.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:0	**V-Port Capture Window Vertical Start [7:0]:** • These bits are the least-significant 8 bits of a 9-bit field that expresses a value for the vertical start of the V-Port Capture Window. • This value, based on the falling (trailing) edge of the VSI (vertical sync) signal, shows how many HREFI pulses are skipped until the beginning of the Capture Window. — The value for this field is expressed in the number of scanlines *before* the video lines have been scaled down. — The value for this field is programmed as *n*, where *n* is the number of full HREFI signals to be skipped. • The most-significant bit of this field is in CR58[4]. • The following timing diagram shows the relationship of the vertical start signal to the HREFI and the trailing edge of the VSI signal.



12.119 CR57: V-Port Capture Window Vertical Height Register

I/O Port Address: 3?5

Index: 57

Bit	Description	Reset State
7	V-Port Capture Window Vertical Height [7]	0
6	V-Port Capture Window Vertical Height [6]	0
5	V-Port Capture Window Vertical Height [5]	0
4	V-Port Capture Window Vertical Height [4]	0
3	V-Port Capture Window Vertical Height [3]	0
2	V-Port Capture Window Vertical Height [2]	0
1	V-Port Capture Window Vertical Height [1]	0
0	V-Port Capture Window Vertical Height [0]	0

This register is used to set the delay for the vertical height of the V-Port Capture Window.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:0	**V-Port Capture Window Vertical Height [7:0]:** • These bits are the least-significant 8 bits of a 9-bit field that expresses a value for the vertical height of the V-Port Capture Window. • This value controls how many scanlines of V-Port data are captured in display memory. — The value for this field is expressed in the number of scanlines *after* the video data has been scaled down. — Program this register for the hex quantity ($n - 1$), in which n is the number of scanlines to be captured. — If the value for this field is programmed as '0', the result is 1 HREFI capture window. • The most-significant bit of this field is in CR58[5].

12.120 CR58: V-Port Capture Window Extension Register

I/O Port Address: 3?5

Index: 58

Bit	Description	Reset State
7	V-Port Cycle Skip for VW Enable	0
6	V-Port Interlaced Mode Odd/Even Meaning Invert	0
5	V-Port Capture Window Vertical Height [8]	0
4	V-Port Capture Window Vertical Start [8]	0
3	V-Port Capture Window Horizontal Width [9]	0
2	V-Port Capture Window Horizontal Width [8]	0
1	V-Port Capture Window Horizontal Start [9]	0
0	V-Port Capture Window Horizontal Start [8]	0

This register contains extension bits for other V-Port Capture Window registers.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7	**V-Port Cycle Skip for VW Enable:** On each scanline, this bit allows the V-Port cycle to be skipped immediately after each VW period.
6	**V-Port Interlaced Mode Odd/Even Meaning Invert:** When the VSYNC falling edge occurs when HREFI is high *and* this bit is: • 0, this condition indicates an odd field. • 1, this condition indicates an even field.
5	**V-Port Capture Window Vertical Height [8]:** • This bit is the most-significant bit of a 9-bit field. • For details refer to Extension register CR57, which contains the 8 least-significant bits of this field.
4	**V-Port Capture Window Vertical Start [8]:** • This bit is the most-significant bit of a 9-bit field. • For details refer to Extension register CR56, which contains the 8 least-significant bits of this field.
3:2	**V-Port Capture Window Horizontal Width [9:8]:** • These bits are the most-significant 2 bits of a 10-bit field. • For details refer to Extension register CR55, which contains the 8 least-significant bits of this field.
1:0	**V-Port Capture Window Horizontal Start [9:8]:** • These bits are the most-significant 2 bits of a 10-bit field. • For details refer to Extension register CR54, which contains the 8 least-significant bits of this field.

12.121 CR59: V-Port Capture Window Start Address High Register

I/O Port Address: 3?5

Index: 59

Bit	Description	Reset State
7	V-Port Capture Window Start Address [18]	0
6	V-Port Capture Window Start Address [17]	0
5	V-Port Capture Window Start Address [16]	0
4	V-Port Capture Window Start Address [15]	0
3	V-Port Capture Window Start Address [14]	0
2	V-Port Capture Window Start Address [13]	0
1	V-Port Capture Window Start Address [12]	0
0	V-Port Capture Window Start Address [11]	0

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:0	**V-Port Capture Window Start Address [18:11]:** These bits are the 8 most-significant bits of the 19-bit field for the V-Port Capture Window Start Address field. • The value programmed in the entire 19-bit field gives the value for the address start for the V-Port Capture Window. — This address start value can be changed to a new value at any time. — New address start values take effect in the following vertical retrace VSYNC period of the V-Port. • The other bits of this field are in Extension register CR5E and CR5F.

12.122 CR5A: V-Port Cycle and FIFO Control Register

I/O Port Address: 3?5

Index: 5A

Bit	Description	Reset State
7	V-Port Cycle Control after Non-Aligned VW FIFO Cycle [1]	0
6	V-Port Cycle Control after Non-Aligned VW FIFO Cycle [0]	0
5	V-Port Cycle Control after Non-Aligned CRT FIFO Cycle [1]	0
4	V-Port Cycle Control after Non-Aligned CRT FIFO Cycle [0]	0
3	V-Port FIFO Underrun Status	0
2	V-Port FIFO Threshold in Surrounding Graphics [2]	0
1	V-Port FIFO Threshold in Surrounding Graphics [1]	0
0	V-Port FIFO Threshold in Surrounding Graphics [0]	0

This register controls V-Port cycles after non-aligned VW/CRT FIFO cycles and the V-Port FIFO threshold in the surrounding graphics.

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit **Description**

7:6 **V-Port Cycle Control After Non-Aligned VW FIFO Cycle [1:0]:**
This 2-bit field controls the number of V-Port CAS# cycles that occur after the Video Window FIFO cycle in which a display memory page miss occurred, as indicated in the following table.

CR5A		Number of Completed V-Port Cycles Before Video Window FIFO Sequence Stops
[7]	[6]	
0	0	V-Port cycle is skipped.
0	1	1 V-Port CAS# cycle occurs.
1	0	2 V-Port CAS# cycles occur.
1	1	3 V-Port CAS# cycles occur.

12.122 CR5A: V-Port FIFO Control Register *(cont.)*

Bit | **Description**

5:4 **V-Port Cycle Control After Non-Aligned CRT FIFO Cycle [1:0]:**
This 2-bit field controls the number of V-Port CAS# cycles that occur after the CRT FIFO cycle in which a display memory page miss occurred, as indicated in the following table.

CR5A		Number of Completed V-Port Cycles Before CRT FIFO Sequence Stops
[5]	[4]	
0	0	V-Port cycle is skipped.
0	1	1 V-Port CAS# cycle occurs.
1	0	2 V-Port CAS# cycles occur.
1	1	3 V-Port CAS# cycles occur.

3 **V-Port FIFO Underrun Status:**
This bit reflects the V-Port FIFO underrun status. When this bit is:

- 0, the V-Port FIFO does not have an underrun. (When this bit is read, it is cleared to 0.)
- 1, the V-Port FIFO had an underrun. (That is, the V-Port did not obtain sufficient cycles to empty the V-Port FIFO to the display memory.)

2:0 **V-Port FIFO Threshold in Surrounding Graphics:**
These bits program a value that, within each V-Port cycle, specifies the number of V-Port CAS# cycles in the surrounding graphics.

12.123 CR5B: VW YUV Data Format Brightness Control Register

I/O Port Address: 3?5

Index: 5B

Bit	Description	Reset State
7	VW YUV Data Format Brightness Control [7]	0
6	VW YUV Data Format Brightness Control [6]	0
5	VW YUV Data Format Brightness Control [5]	0
4	VW YUV Data Format Brightness Control [4]	0
3	VW YUV Data Format Brightness Control [3]	0
2	VW YUV Data Format Brightness Control [2]	0
1	VW YUV Data Format Brightness Control [1]	0
0	VW YUV Data Format Brightness Control [0]	0

Bit	Description
7:0	**VW YUV Data Format Brightness Control [7:0]:** The value in this register: • Is added to the luminance value of each data pixel to enhance the brightness quality of an image within the VW. • Is expressed in terms of 2's complement. • When positive (such as Ah), increases the luminance value of each pixel. • When negative (such as –Ah), decreases the luminance value of each pixel.

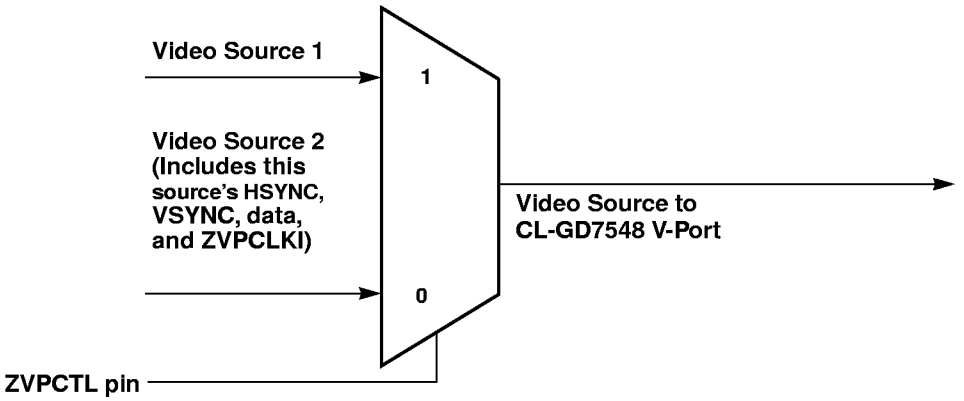
12.124 CR5C: V-Port/ CRT FIFO CAS# Cycle Control at VW Period End

I/O Port Address: 3?5

Index: 5C

Bit	Description	Reset State
7	ZVPCTL Pin Programmable Output	0
6	V-Port Capture Window Odd-Field Enable for MPEG Fields	0
5	V-Port Capture Window Two-Field Enable	0
4	VW Right Side Transition Threshold Enable	0
3	VW Right Side Transition Threshold [3]	0
2	VW Right Side Transition Threshold [2]	0
1	VW Right Side Transition Threshold [1]	0
0	VW Right Side Transition Threshold [0]	0

Bit	Description
7	**ZVPCTL Pin Programmable Output:** • This bit can be used if Extension register SR22[4] is 0, to allow the V-Port to synchronize with a second video source when the external video source is changed. • The value programmed into this bit affects the ZVPCTL pin when SR22[4] is 0 (that is, no external pull-up is on MD[20] / SLEEPPU). • When SR22[4] is a 0 *and* this bit is programmed to: — 0, the value on the ZVPCTL pin is a low and is updated on the V-Port VSYNC falling (trailing) edge. — 1, the value on the ZVPCTL pin is a high and is updated on the V-Port VSYNC falling (trailing) edge.



12.124 CR5C: V-Port/ CRT FIFO CAS# Cycle Control at VW Period End *(cont.)*

Bit	Description
6	**V-Port Capture Window Odd-Field Enable for MPEG Fields:** This bit enables high-quality MPEG field capture. When this bit is: • 0, both the odd and even MPEG fields are captured. • 1, *and* Extension register CR58[6] is: — 0, this bit enables only an odd MPEG field capture. — 1, this bit enables only an even MPEG field capture.
5	**V-Port Capture Window Two-Field Enable:** • This bit can be used in conjunction with CR5C[7] for tele-conferencing from two sources of video. Software controls how many frames of each video source are displayed, relative to the other. (That is, software controls the interleaving ratio between the two sources of video.) • If Extension register CR51[3] is 0 *and* this bit is 1, it enables a V-Port Capture Window for two full fields (one frame). • This bit remains set to 1 for two full V-Port fields after it is initially set by I/O. • At the end of the two full fields of video capture, this bit automatically clears to 0, and the V-Port is disabled.
4	**VW Right Side Transition Threshold Enable:** When this bit is 1, at the end of each VW period for each scanline, this bit enables the V-Port FIFO CAS# cycle and the CRT FIFO CAS# cycle control feature.
3:0	**VW Right Side Transition Threshold [3:0]:** When CR5C[4] is 1, the value programmed in these bits determines the total number of the Video Window FIFO CAS# and CRT FIFO CAS# cycles at the end of each VW period for each scanline. (That is, the total equals the number of the VW FIFO CAS# cycles plus the number of the CRT FIFO CAS# cycles.)

12.125 CR5D: VW Horizontal/Vertical Upscaling Coefficients High Register

I/O Port Address: 3?5

Index: 5D

Bit	Description	Reset State
7	VW Horizontal Upscaling Coefficient [11]	0
6	VW Horizontal Upscaling Coefficient [10]	0
5	VW Horizontal Upscaling Coefficient [9]	0
4	VW Horizontal Upscaling Coefficient [8]	0
3	VW Vertical Upscaling Coefficient [11]	0
2	VW Vertical Upscaling Coefficient [10]	0
1	VW Vertical Upscaling Coefficient [9]	0
0	VW Vertical Upscaling Coefficient [8]	0

Bit	Description
7:4	**VW Horizontal Upscaling Coefficient [11:8]:** • These bits are the most-significant 4 bits of the 12-bit field for the VW HU (the Video Window Horizontal Upscaling Coefficient). • For details refer to Extension register CR31, which contains the least-significant 8 bits.
3:0	**VW Vertical Upscaling Coefficient [11:8]:** • These bits are the most-significant 4 bits of the 12-bit field for the VW VU (the Video Window Vertical Upscaling Coefficient). • For details refer to Extension register CR32, which contains the least-significant 8 bits.

12.126 CR5E: V-Port Capture Window Start Address Middle Register

I/O Port Address: 3?5

Index: 5E

Bit	Description	Reset State
7	V-Port Capture Window Start Address [10]	0
6	V-Port Capture Window Start Address [9]	0
5	V-Port Capture Window Start Address [8]	0
4	V-Port Capture Window Start Address [7]	0
3	V-Port Capture Window Start Address [6]	0
2	V-Port Capture Window Start Address [5]	0
1	V-Port Capture Window Start Address [4]	0
0	V-Port Capture Window Start Address [3]	0

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:0	**V-Port Capture Window Start Address [10:3]:** • These bits are the middle 8 bits of the V-Port Capture Window Start Address field. • The other bits of this field are in Extension registers CR59 and CR5F. • For details on this field, refer to Extension register CR59.

12.127 CR5F: V-Port Capture Window Start Address Low Register

I/O Port Address: 3?5

Index: 5F

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	V-Port Capture Window Start Address [2]	0
3	V-Port Capture Window Start Address [1]	0
2	V-Port Capture Window Start Address [0]	0
1	Reserved	
0	AccuPak Dithering Enable	0

NOTE: The FCPU pin must be pulled low for the V-Port configuration.

Bit	Description
7:5	**Reserved**
4:2	**V-Port Capture Window Start Address [2:0]:** • These bits are the least-significant 3 bits of the V-Port Capture Window Start Address field. • The other bits of this field are in Extension registers CR59 and CR5E. • For details on this field, refer to Extension register CR59.
1	**Reserved**
0	**AccuPak Dithering Enable:** When this VW is in the AccuPak data format *and* this bit is 1, on the data compression side of the VW, this bit enables dithering.

12.128 HDR: Hidden DAC Register

I/O Port Address: 3C6

Index: (n/a)

Bit	Description	Reset State
7	5-5-5 Extended Color Mode Enable	0
6	Extended Color Mode Select Enable	0
5	Clocking Mode	0
4	32K Extended Color Mode Control	0
3	Extended Color Mode Select [3]	0
2	Extended Color Mode Select [2]	0
1	Extended Color Mode Select [1]	0
0	Extended Color Mode Select [0]	0

The Hidden DAC register (HDR) is 'hidden' because it shares its I/O address with External/General register 3C6. The HDR:

- Is used to enable extended color modes, including the following:
  - — 15-bit/pixel extended color mode
  - — 16-bit/pixel extended color mode
  - — 24-bit/pixel extended color mode
- Is accessed by reading four times in succession External/General register 3C6 (the Pixel Mask register). The next write or read of the 3C6 register then accesses the HDR.
  - — A *write* to the HDR resets the internal counter, and the four dummy reads of the 3C6 register must be executed again.
  - — A *read* from the HDR resets the internal counter, and the four dummy reads of the 3C6 register must be executed again.
  - — Reads from the 3C6 register do not lock the HDR.
- Is cleared to all zeroes at reset, putting the CL-GD7548 in VGA-compatibility mode.
- Does not affect Video Window modes.

Bit	Description
7	**5-5-5 Extended Color Mode Enable:** • When this bit is 0: — The extended color modes are disabled. — The palette DAC is VGA-compatible. • When this bit is 1: — It enables the extended color modes (including the RGB 5-5-5 extended color mode), as chosen by bit [6] and bits [3:0] of this register.
6	**Extended Color Mode Select Enable:** When bit [7] is 1, and this bit is: • 0, the extended color mode select bits [3:0] of this register are ignored, and the extended color mode is the RGB 5-5-5 mode. • 1, the extended color mode select bits [3:0] of this register are enabled to select an extended color mode (other than the RGB 5-5-5 mode).

12.128 HDR: Hidden DAC Register *(cont.)*

Bit	Description
5	**Clocking Mode:** When this bit is: • 0, Clocking mode 1 is chosen. In Clocking mode 1: — The 16-bit/pixel modes use both edges of DCLK to latch data. — The rising edge of DCLK latches the least-significant byte. — The falling edge of DCLK latches the most-significant byte. • 1, Clocking mode 2 is chosen. In Clocking mode 2: — The 16-bit/pixel modes use only the rising edge of DCLK to latch data. — The DCLK must be supplied at twice the pixel rate. — The first rising edge of DCLK latches the least-significant byte. — The second rising edge of DCLK latches the most-significant byte. **NOTE:** All modes other than 16-bit/pixel use only the rising DCLK edge, regardless of this bit setting.
4	**32K Extended Color Mode Control:** When this bit is: • 0, an RGB 5-5-5 extended color mode operation takes place normally. • 1 *and* the 15th pixel data bit of the RGB 5-5-5 operation is: — 0, then the RGB 5-5-5 extended color mode operation that is chosen allows RGB 5-5-5 data to overlay 256-color images on a pixel-by-pixel basis. — 1, then the first 8 pixel data bits of the RGB 5-5-5 operation choose a palette entry and the last 7 pixel data bits are ignored.
3:0	**Extended Color Mode Select [3:0]:** When HDR[7:6] is '11', this 4-bit field selects an extended color mode according to the following table:

HDR						Color Mode	
[7]	[6]	[3]	[2]	[1]	[0]		
0	X	X	X	X	X	VGA compatibility color mode	
1	0	X	X	X	X	Extended color modes	RGB 5-5-5
1	1	0	0	0	1		RGB 5-6-5 (XGA)
1	1	0	1	0	1		RGB 8-8-8 (16M color)
1	1	0	1	1	X		DAC power-down
1	1	1	0	0	0		8-bit grayscale
1	1	1	0	0	1		RGB 3-3-2

NOTE: Any undefined settings are reserved.

12.129 R1X: LCD HSYNC Width Control Register

I/O Port Address: 3?5

Index: 2 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Reset State
7	CRT VSYNC on LFS Select	0
6	CRT HSYNC on LLCLK Select	0
5	TFT LCD High-Resolution Select	0
4	LCD HSYNC Width Control [4]	0
3	LCD HSYNC Width Control [3]	0
2	LCD HSYNC Width Control [2]	0
1	LCD HSYNC Width Control [1]	0
0	LCD HSYNC Width Control [0]	0

Bit	Description
7	**CRT VSYNC on LFS Select:** When this bit is 1, the LFS pin outputs a CRT VSYNC signal controlled by the LCD power-up/down sequencing. • When the LCD powers: — Up, the LFS outputs a high CRT VSYNC signal. — Down, the LFS outputs a low CRT VSYNC signal. • This bit can be used with any LCD that has timing similar to a CRT.
6	**CRT HSYNC on LLCLK Select:** When this bit is 1, the LLCLK pin outputs a CRT HSYNC signal controlled by the LCD power-up/down sequencing. • When the LCD powers: — Up, the LLCLK outputs a high CRT HSYNC signal. — Down, the LLCLK outputs a low CRT HSYNC signal. • This bit can be used with any LCD that has timing similar to a CRT.
5	**TFT LCD High-Resolution Select:** This bit configures a TFT LCD data path. When this bit is: • 0, the TFT LCD is configured for the same data path as for the CL-GD7541, CL-GD7542, and CL-GD7543 Super VGA controllers. • 1, the TFT LCD is configured for a higher resolution with a high-frequency dot clock, and another video pipeline stage is included for the LCD only.

12.129 R1X: LCD HSYNC Width Control Register *(cont.)*

Bit	Description
4:0	**LCD HSYNC Width Control [4:0]:** When Extension register CR43[7] is a 1, this field controls the width of the LCD HSYNC signals. The width of the signals can be increased in increments of 4 dot clocks (also called 'pixel clocks'), according to the following table.

R1X					Resulting Widths of LCD HSYNC Signals (In dot clocks)
[4]	[3]	[2]	[1]	[0]	
0	0	0	0	0	LCD HSYNC signal width is 4 dot clocks.
0	0	0	0	1	LCD HSYNC signal width is 8 dot clocks.
0	0	0	1	0	LCD HSYNC signal width is 12 dot clocks.
0	0	0	1	1	LCD HSYNC signal width is 16 dot clocks.
0	0	1	0	0	LCD HSYNC signal width is 20 dot clocks.
0	0	1	0	1	LCD HSYNC signal width is 24 dot clocks.
Selected Resulting Widths of LCD HSYNC Signals					
0	1	0	0	0	LCD HSYNC signal width is 36 dot clocks.
1	0	0	0	0	LCD HSYNC signal width is 68 dot clocks.
1	1	1	1	1	LCD HSYNC signal width is 128 dot clocks.

12.130 R2X: LCD Timing Register — LFS Vertical Position #1 (MISC[7:6] Is 11)

I/O Port Address: 3?5

Index: 2 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	LFS Vertical Position #1 [7]	R/W	0
6	LFS Vertical Position #1 [6]	R/W	0
5	LFS Vertical Position #1 [5]	R/W	0
4	LFS Vertical Position #1 [4]	R/W	0
3	LFS Vertical Position #1 [3]	R/W	0
2	LFS Vertical Position #1 [2]	R/W	0
1	LFS Vertical Position #1 [1]	R/W	0
0	LFS Vertical Position #1 [0]	R/W	0

Register R2X (and registers R3X, R4X, R5X, and RCX, with extra bits in R6X and REX) define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal.

- At power-on self-test, these registers are programmed according to the size of LCD used.
- As explained in Table 12-3, which registers are automatically selected depends upon the following:
  - — The expansion and centering options selected.
  - — The setting of MISC[7:6].
  - — The resolution modes selected.

Bit	Description
7:0	**LFS Vertical Position #1 [7:0]:** • These bits are the least-significant 8 bits of a 10-bit field. The field's value defines in scanlines the vertical position of the line frame start (LFS) signal, relative to the CRT frame start signal. • The most-significant 2 bits of this field are stored in register R6X[7:6]. • The R2X fields (and fields R3X through R6X) are used according to Table 12-3. • For LFS vertical position selection logic diagrams, refer to Figure 12-5.

12.130 R2X: LCD Timing Register — LFS Vertical Position #1 (MISC[7:6] Is 11) *(cont.)*

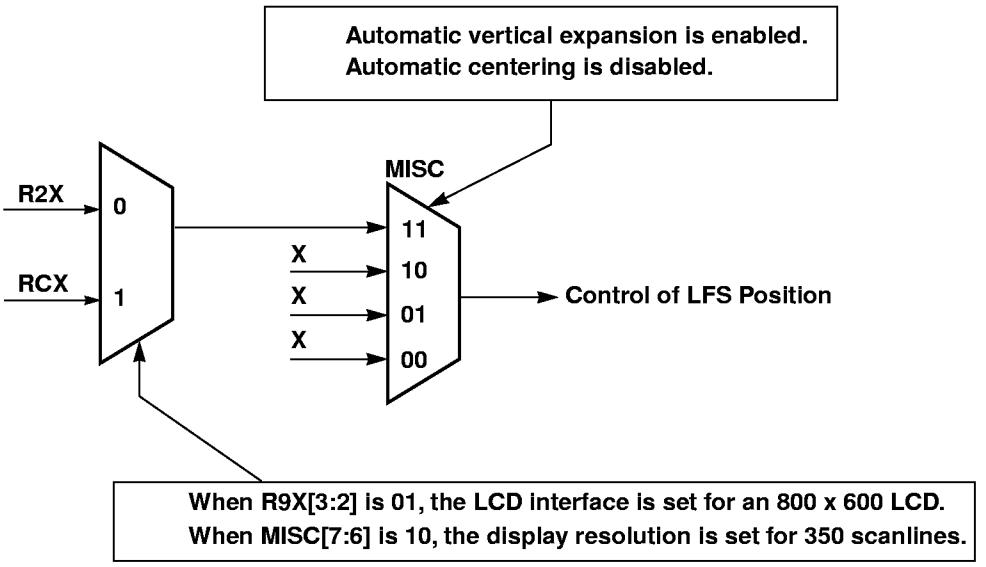
Table 12-3. LFS Register Selection Options

Conditions:					Result:
LCD Size Is:	**Automatic Vertical Expansion[a] Is:**	**Automatic Centering Is:**	**MISC [7:6] =**	**Selected Display Resolution Modes (in Scanlines)**	**LFS Vertical Position Registers Selected**
640 × 480	Off (That is, CR2D[1] is 0)	On (That is, CR2D[0] is 1)	'11'	480 scanlines	R2X[7:0] and R6X[7:6]
640 × 480	On (That is, CR2D[1] is 1)	Off (That is, CR2D[0] is 0)	XX	All display resolution modes	R2X[7:0] and R6X[7:6]
800 × 600	Off (That is, CR2D[1] is 0)	On (That is, CR2D[0] is 1)	'01'	400 scanlines	R4X[7:0] and R6X[3:2]
800 × 600	Off (That is, CR2D[1] is 0)	On (That is, CR2D[0] is 1)	'00'	600 scanlines	R5X[7:0] and R6X[1:0]
800 × 600	On [That is, CR2D[1] is 1, *and* one of the following is true: • CR2E[1] is 1 (that is, graphics expansion is enabled and the LCD is in graphics mode) • CR2E[0] is 1 (that is, text expansion is enabled and the LCD is in text mode)]	'Don't care'	'11' '01' '00'	All display resolution modes *except* for 350 scanlines	R2X[7:0] and R6X[7:6]
800 × 600	On [That is, CR2D[1] is 1, *and* one of the following is true: • CR2E[1] is 1 (that is, graphics expansion is enabled and the LCD is in graphics mode) • CR2E[0] is 1 (that is, text expansion is enabled and the LCD is in text mode)]	'Don't care'	'10'	350 scanlines	RCX[7:0] and REX[1:0]
640 × 480 or 800 × 600	Off (That is, CR2D[1] is 0)	On (That is, CR2D[0] is 1)	'10'	350 scanlines	R3X[7:0] and R6X[5:4]
640 × 480 or 800 × 600	Off (That is, CR2D[1] is 0)	On (That is, CR2D[0] is 1)	'01'	400 scanlines	R4X[7:0] and R6X[3:2]

[a] Depending on the LCD size selected, automatic vertical expansion is controlled by different registers.

12.130 R2X: LCD Timing Register — LFS Vertical Position #1 (MISC[7:6] Is 11) *(cont.)*

The logic diagrams of Figure 12-5 apply to registers R2X–R5X and RCX.



NOTE: For 800 x 600 and 640 x 480 LCDs, the vertical expansions are controlled by different bits, and the expansion algorithms are different.

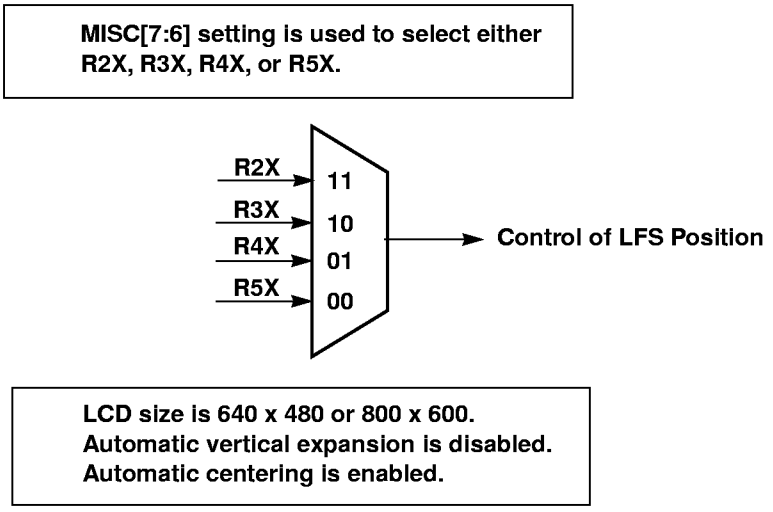


Figure 12-5. Logic Diagrams for LFS Vertical Position Selection

12.131 R3X: LCD Timing Register — LFS Vertical Position #2 (MISC[7:6] Is 10)

I/O Port Address: 3?5

Index: 3 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	LFS Vertical Position #2 [7]	R/W	0
6	LFS Vertical Position #2 [6]	R/W	0
5	LFS Vertical Position #2 [5]	R/W	0
4	LFS Vertical Position #2 [4]	R/W	0
3	LFS Vertical Position #2 [3]	R/W	0
2	LFS Vertical Position #2 [2]	R/W	0
1	LFS Vertical Position #2 [1]	R/W	0
0	LFS Vertical Position #2 [0]	R/W	0

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #2 [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General register MISC[7:6] is '10' (350 scanlines are displayed). — Extension register CR2D[1] is 0 (automatic vertical expansion is disabled). — Extension register CR2D[0] is 1 (automatic centering is enabled, when CR2D[1] is 0). • The most-significant 2 bits are stored in Extension register R6X[5:4]. • For selection options, refer to Table 12-3.

12.132 R4X: LCD Timing Register — LFS Vertical Position #3 (MISC[7:6] Is 01)

I/O Port Address: 3?5

Index: 4 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	LFS Vertical Position #3 [7]	R/W	0
6	LFS Vertical Position #3 [6]	R/W	0
5	LFS Vertical Position #3 [5]	R/W	0
4	LFS Vertical Position #3 [4]	R/W	0
3	LFS Vertical Position #3 [3]	R/W	0
2	LFS Vertical Position #3 [2]	R/W	0
1	LFS Vertical Position #3 [1]	R/W	0
0	LFS Vertical Position #3 [0]	R/W	0

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #3 [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General Register MISC[7:6] is '01' (400 scanlines are displayed). — Extension Register CR2D[1] is 0 (automatic vertical expansion is disabled). — Extension Register CR2D[0] is 1 (automatic centering is enabled, when CR2D[1] is 0). • The most-significant 2 bits are stored in Extension register R6X[3:2]. • For selection options, refer to Table 12-3.

12.133 R5X: LCD Timing Register — LFS Vertical Position #4 (MISC[7:6] Is 00)

I/O Port Address: 3?5

Index: 5 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	LFS Vertical Position #4 [7]	R/W	0
6	LFS Vertical Position #4 [6]	R/W	0
5	LFS Vertical Position #4 [5]	R/W	0
4	LFS Vertical Position #4 [4]	R/W	0
3	LFS Vertical Position #4 [3]	R/W	0
2	LFS Vertical Position #4 [2]	R/W	0
1	LFS Vertical Position #4 [1]	R/W	0
0	LFS Vertical Position #4 [0]	R/W	0

This register defines in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #4 [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General register MISC[7:6] is '00'. — Extension register CR2D[1] is 0 (automatic vertical expansion is disabled). — Extension register CR2D[0] is 1 (automatic centering is enabled, when CR2D[1] is 0). • The most-significant 2 bits are stored in Extension register R6X[1:0]. • For selection options, refer to Table 12-3.

12.134 R6X: LCD Timing — Extension Bits for LFS Signal Compare

I/O Port Address: 3?5

Index: 6 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	R2X LFS Vertical Position #1 [9]	R/W	0
6	R2X LFS Vertical Position #1 [8]	R/W	0
5	R3X LFS Vertical Position #2 [9]	R/W	0
4	R3X LFS Vertical Position #2 [8]	R/W	0
3	R4X LFS Vertical Position #3 [9]	R/W	0
2	R4X LFS Vertical Position #3 [8]	R/W	0
1	R5X LFS Vertical Position #4 [9]	R/W	0
0	R5X LFS Vertical Position #4 [8]	R/W	0

This register defines the two most-significant extension bits for the LFS vertical position registers R2X, R3X, R4X, and R5X.

Bit	Description
7:6	**R2X LFS Vertical Position #1 [9:8]**: When External/General register MISC[7:6] is programmed to '11', these bits are the most-significant 2 bits of Extension register R2X, creating a 10-bit value.
5:4	**R3X LFS Vertical Position #2 [9:8]**: When External/General register MISC[7:6] is programmed to '10', these are the most-significant 2 bits of Extension register R3X, creating a 10-bit value.
3:2	**R4X LFS Vertical Position #3 [9:8]**: When External/General register MISC[7:6] is programmed to '01', these are the most-significant 2 bits of Extension register R4X, creating a 10-bit value.
1:0	**R5X LFS Vertical Position #4 [9:8]**: When External/General register MISC[7:6] is programmed to '00', these are the most-significant 2 bits of Extension register R5X, creating a 10-bit value.

12.135 R7X: LCD Timing Register — Signal Control for Color TFT LCDs

I/O Port Address: 3?5

Index: 7 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	LCD Short Power Sequence Enable	R/W	0
6	FPVDCLK Delay Control	R/W	0
5	LCD Line-clock Control	R/W	0
4	Force 8-Dot Clock for LCD	R/W	0
3	LFS Output	R/W	0
2	LLCLK Output	R/W	0
1	FPVDCLK Inversion	R/W	0
0	FPVDCLK Free-Running Enable for TFT LCDs	R/W	0

Bit	Description
7	**LCD Short Power Sequence Enable**: If this bit is: • 0, the LCD power sequence is 32 msec. • 1, the LCD power sequence is 4 msec. This bit setting is used with special LCDs that require a maximum of 10 msec between the LCD power sequencing signals [that is, the FPVCC signal, the drive signals (FPVDCLK, LFS, LLCLK, Panel Data, and MOD), the logic supply signal (FPVEE), and the backlight signal (FPBL)].
6	**FPVDCLK Delay Control**: If this bit is 1, FPVDCLK (the LCD panel shift clock), is delayed by 4 more nsec relative to the LCD Panel Data signals, than is the case in which this bit is 0.
5	**LCD Line-clock Control:** When this bit is set to 1, the total number of LLCLKs = 200h + hex value in CR1F[6:0].
4	**Force 8-Dot Clock for LCD:** When the LCD is enabled and this bit is set to 1, the character clock for Text modes is forced to 8-dots per clock.
3	**LFS Output:** In both of the following cases, the line frame start signal (LFS) output is controlled by the first vertical pulse, which marks the beginning of the LCD display. • When this bit is 0: — The LFS output pin drives both STN and DE-type TFT LCDs. — The LFS output (which may also be called FLM) is one line wide and is programmable. • When this bit is 1: — The LFS output pin drives the VSYNC input for non-DE-type TFT LCDs. — The LFS output (which may also be called TFT-VSYNC) is two lines wide and can support only single-scan LCDs. • Set this bit to 1 for any TFT LCDs that require a VSYNC input wider than one line.

12.135 R7X: LCD Timing Register — Signal Control for Color TFT LCDs *(cont.)*

Bit	Description
2	**LLCLK Output:** • When this bit is 0: — The LLCLK output pin drives both STN LCDs and those TFT LCDs that have a 'display enable' signal. — The LLCLK signal position is controlled by 'LCD Horizontal Display Enable Start' values stored in Extension registers CR40 to CR42, and Extension register CR43 is used for fine positioning. — The LLCLK signal starts with the HFirst pulse. (Refer to the timing diagram within the description of Extension register CR40.) — The LLCLK signal is always 25 dot clocks before the LCD display enable start signal. • When this bit is 1: — Connect LFS to VSYNC. (Refer to Extension register R7X[3].) • This bit *must* be set to 1 for: — Those TFT LCDs that do not have a 'display enable' signal. — LCDs that require an offset different than 25 dot clocks between the LLCLK (or LCD HSYNC) signal and the LCD display enable start signal. For example, some LCDs require an offset of 144 dot clocks between LLCLK and the first LCD shift clock. In this case, set R7X[2] to 1, which places the LLCLK output under the control of Extension register CR47[7:0].
1	**FPVDCLK Inversion:** This bit can be used with all LCDs. • When this bit is: — 0, LCD data are latched on the high-to-low transition of the internal CL-GD7548 FPVDCLK signal. — 1, LCD data are latched on the low-to-high transition of the internal CL-GD7548 FPVDCLK signal. • During Suspend mode, FPVDCLK is forced low, independent of this bit polarity.
0	**FPVDCLK Free-Running Enable for TFT LCDs:** Set this bit to: • 0 for the type of TFT LCDs that cannot accept a free-running FPVDCLK. — When this bit is 0, FPVDCLK is gated by the display enable signal and remains active only during display time. — This setting is generally not required. • 1 only for the type of TFT LCDs that require a free-running FPVDCLK (that is, a clock that constantly toggles). — When this bit is 1 *and* when the LCD power sequence is on, FPVDCLK is always active (free-running) for TFT LCDs. — This setting is the usual setting.

12.136 R8X: LCD Timing Register — Shift Clock and Data Format Select for STN LCDs

I/O Port Address: 3?5

Index: 8 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	Horizontal Cross-Talk Reduction Enable	R/W	0
6	Vertical Cross-Talk Reduction Disable	R/W	0
5	Dual-/Single-Scan Monochrome LCD Select	R/W	0
4	Foreground-Only Text Enhancement	R/W	0
3	Reserved		
2	Cross-Talk Reduction Option Enable	R/W	0
1	Dual-/Single- Shift Clock Select for STN LCDs	R/W	0
0	16-Bit / 8-Bit Data Interface Select for STN LCDs	R/W	0

Bit	Description
7	**Horizontal Cross-Talk Reduction Enable:** • When this bit is 1, horizontal cross-talk reduction is enabled. • This bit is a test bit, and it must never be written by any application program. It is listed here only for completeness.
6	**Vertical Cross-Talk Reduction Disable:** • When this bit is 1, vertical cross-talk reduction is disabled. • This bit is a test bit, and it must never be written by any application program. It is listed here only for completeness.
5	**Dual-/Single-Scan Monochrome LCD Select:** When Extension register CR2C[7:6] is programmed to '00' *and* this bit is: • 0, dual-scan monochrome LCDs are selected. • 1, single-scan monochrome LCDs are selected.
4	**Foreground-Only Text Enhancement:** When this bit is: • 0, normal text is displayed. • 1, *and* Extension register CR1E[1] is 1, the foreground-only text enhancement is enabled.
3	**Reserved**
2	**Cross-Talk Reduction Option Enable:** Depending on the LCD display quality, one of the following options is used. When this bit is: • 0, the cross-talk reduction operation uses Line Counter bits [1:0]. • 1, the cross-talk reduction operation uses Line Counter bits [5:4].

12.136 R8X: LCD Timing Register — Shift Clock and Data Format Select for STN LCDs *(cont.)*

Bit	Description
1	**Dual-/Single-Shift Clock Select for STN LCDs:** On an STN LCD, when this bit is: • 0, a single-shift clock is supplied to the FPVDCLK pin. • 1, a dual-shift clock is supplied to the FPVDCLK and FPDE / XCLKU pins.
0	**16-Bit / 8-Bit Data Interface Select for STN LCDs:** On an STN LCD, when this bit is: • 0, a 16-bit data STN LCD interface is selected. • 1, an 8-bit data STN LCD interface is selected. **NOTE:** For 8-bit STN LCDs that are dual-clock, single-scan, and interleaved, only R8X[0] needs to be programmed, and not R8X[1].

12.137 R9X: LCD Size and TFT LCD Data Format Register

I/O Port Address: 3?5

Index: 9 — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	LCD Size Select [1]	R/W	0
2	LCD Size Select [0]	R/W	0
1	TFT LCD Data Format [1]	R/W	0
0	TFT LCD Data Format [0]	R/W	0

Bit **Description**

7:4 **Reserved**

3:2 **LCD Size Select [1:0]:**
These 2 bits select an LCD size as shown in the table below. For details on specific LCD types and connection information, refer to the "Panel Interface Guide" in the *CL-GD754X Application Book*.

R9X		LCD Size	LCD Types to Which LCD Size Can Be Applied
[3]	[2]		
0	0	640 × 480	STN and TFT
0	1	800 × 600	STN and TFT
1	0	1024 × 768	STN and TFT
1	1	Reserved	–

1:0 **TFT LCD Data Format [1:0]**:
These 2 bits select the data format for TFT LCDs as shown in the table below. For information on specific LCD types and for detailed connection information, refer to the "Panel Interface Guide" in the *CL-GD754X Application Book*.

R9X		TFT LCD Data Format	Corresponding Cirrus Logic Abbreviation for TFT LCD Data Format
[1]	[0]		
0	0	9-bit (3-3-3)	C512SS-9
0	1	12-bit (4-4-4)	C4KSS-12
1	0	18-bit (6-6-6)	C256K-18
1	1	24-bit (8-8-8)	C16MSS-24

12.138 RBX: Shade Conversion and Extra LCD Line Clock Insertion Register

I/O Port Address: 3?5

Index: B — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	Reserved		
6	LCD Data Test Options		0
5	LCD Data Test Options		0
4	Shades 7 and 9 Convert	R/W	0
3	Shades 5 and 11 Convert	R/W	0
2	Reserved		
1	XGA LCD Panel Width Override Disable		0
0	XGA LCD Shift Clock Option Select		0

Bit — **Description**

7 — **Reserved**

6:5 — **LCD Data Test Options:**
These bits control LCD data test options, according to the following table:

RBX [6]	RBX [5]	LCD Data Test Options
0	0	Normal operation
0	1	Direct data is blanked.
1	0	Indirect data is blanked.
1	1	LCD scanline counter bits [3:0] use an indirect path to frame buffer.

NOTES:

1) Direct data is data that does not go through a frame buffer before it is displayed.
2) Indirect data is data that goes through a frame buffer before it is displayed.

4 — **Shades 7 and 9 Convert:**
When this bit is 1:
- Shade 7 is converted to shade 6.
- Shade 9 is converted to shade 8.

3 — **Shades 5 and 11 Convert:**
When this bit is 1:
- Shade 5 is converted to shade 4.
- Shade 11 is converted to shade 10.

2 — **Reserved**

12.138 RBX: Shade Conversion and Extra LCD Line Clock Insertion Register *(cont.)*

Bit	Description
1	**XGA LCD Panel Width Override Disable:** For an XGA LCD, this bit must be 1.
0	**XGA LCD Shift Clock Option Select:** This bit selects timing for FPVDCLK, which drives the shift clock. When this bit is: • 0, the FPVDCLK is not divided by 2, resulting in only 1 pixel being displayed during each shift clock. This setting is used for most 1024 x 768 LCDs. • 1, the FPVDCLK is divided by 2, resulting in 2 pixels being displayed during each shift clock. For this bit setting, the falling (trailing) edge of the FPVDCLK signal is used for the divide-down.

12.139 RCX: LCD Timing Register — LFS Vertical Position for 525-Scanline Modes

I/O Port Address: 3?5

Index: C — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Reset State
7	LFS Vertical Position for 525-Scanline Modes [7]	0
6	LFS Vertical Position for 525-Scanline Modes [6]	0
5	LFS Vertical Position for 525-Scanline Modes [5]	0
4	LFS Vertical Position for 525-Scanline Modes [4]	0
3	LFS Vertical Position for 525-Scanline Modes [3]	0
2	LFS Vertical Position for 525-Scanline Modes [2]	0
1	LFS Vertical Position for 525-Scanline Modes [1]	0
0	LFS Vertical Position for 525-Scanline Modes [0]	0

For 800 × 600 LCDs, this register is used to:

- Expand the 350 scanlines that result from a 350-scanline mode to 525 scanlines and then to center the 525 scanlines.
- Define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position for 525-Scanline Modes [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — External/General register MISC[7:6] is '10'. (The vertical size is 350 scanlines, before expansion.) — Graphics modes 10h or Fh are being used. (These modes display 350 scanlines.) — Extension register CR2D[1] is 1. (Automatic vertical expansion is enabled.) • The most-significant 2 bits of this field are in REX[1:0]. • For selection options refer to Table 12-3.

12.140 RDX: LCD Timing Register — LFS Vertical Position #6

I/O Port Address: 3?5

Index: D — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	LFS Vertical Position #6 [7]	R/W	0
6	LFS Vertical Position #6 [6]	R/W	0
5	LFS Vertical Position #6 [5]	R/W	0
4	LFS Vertical Position #6 [4]	R/W	0
3	LFS Vertical Position #6 [3]	R/W	0
2	LFS Vertical Position #6 [2]	R/W	0
1	LFS Vertical Position #6 [1]	R/W	0
0	LFS Vertical Position #6 [0]	R/W	0

For 800 × 600 LCDs, this register is used to define in scanlines the vertical position of the line frame start signal (LFS), relative to the CRT frame start signal, under the conditions explained below.

Bit	Description
7:0	**LFS Vertical Position #6 [7:0]:** • These bits are the least-significant 8 bits of a 10-bit value that defines in scanlines the vertical position of the LFS signal, relative to the CRT frame start signal, when: — The LCD is an 800 × 600 LCD. — External/General register MISC[7:6] is 11. — Extension register CR2D[1] is 0 (automatic vertical expansion is disabled). — Extension register CR2D[0] is 1 (automatic centering is enabled). • The most-significant 2 bits are stored in REX[3:2]. • For selection options refer to Table 12-3.

12.141 REX: RDX and RCX Extension Register

I/O Port Address: 3?5

Index: E — This register is accessible only when Extension register CR2D[7] is 1.

Bit	Description	Access	Reset State
7	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	RDX: LFS Vertical Position #6 [9]	R/W	0
2	RDX: LFS Vertical Position #6 [8]	R/W	0
1	RCX: LFS Vertical Position for 525-Scanline Modes [9]	R/W	0
0	RCX: LFS Vertical Position for 525-Scanline Modes [8]	R/W	0

Bit	Description
7:4	**Reserved**
3:2	**RDX LFS Vertical Position #6 [9:8]:** • These extension bits are the most-significant 2 bits of a 10-bit field, LFS Vertical Position #6. • For more information, refer to Extension register RDX[7:0], which contains the least-significant bits for this field.
1:0	**RCX LFS Vertical Position for 525-Scanline Modes [9:8]:** • These extension bits are the most-significant 2 bits of a 10-bit field, LFS Vertical Position for 525-scanline modes. • For more information, refer to Extension register RCX[7:0], which contains the least-significant bits for this field.

12.142 R0Y: Horizontal Total Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension Register CR2C[5:4] is 10.

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

The RiY (i = 0,2,3,4,5) Extension registers are horizontal timing shadow registers.

- These registers are used to automatically control the CRT controller on 640 × 480 and 800 × 600 LCDs.
- These registers control LCD timing independent of VGA modes.

Bit	Description
7:0	**Horizontal Total [7:0]:** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR0[7:0]).

12.143 R2Y: Horizontal Blanking Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 10.

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR2[7:0].

12.144 R3Y: Horizontal Blanking End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 10.

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

Bit	Description
7:5	**Reserved**
4:0	**Horizontal Blanking End [4:0]:** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR3[4:0]. • These bits are the least-significant 5 bits of a 6-bit field controlling the horizontal blanking end signal. • The most-significant bit that controls the horizontal blanking end signal is in Extension register R5Y[7].

12.145 R4Y: Horizontal Sync Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 10.

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR4[7:0].

12.146 R5Y: Horizontal Sync End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 10.

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Reserved	
5	Reserved	
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

Bit	Description
7	**Horizontal Blanking End [5]:** • This bit is the most-significant bit for the 6-bit horizontal blanking end signal. • The least-significant 5 bits of the horizontal blanking end signal are in Extension register R3Y[4:0].
6:5	**Reserved**
4:0	**Horizontal Sync End [4:0]:** When Sequencer register SR1[3] is 0 (the DCLK signal is the same signal as VCLK), this register performs the same function as CRT Controller register CR5[4:0].

12.147 R0Z: Horizontal Total Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset State
7	Horizontal Total [7]	0
6	Horizontal Total [6]	0
5	Horizontal Total [5]	0
4	Horizontal Total [4]	0
3	Horizontal Total [3]	0
2	Horizontal Total [2]	0
1	Horizontal Total [1]	0
0	Horizontal Total [0]	0

The RiZ (i = 0,2,3,4,5) Extension registers are horizontal timing shadow registers.

- These registers are used to automatically control the CRT controller on 640 × 480 and 800 × 600 LCDs.
- These registers control LCD timing independent of VGA modes.

Bit	Description
7:0	**Horizontal Total [7:0]:** When Sequencer register SR1[3] is 1 (the DCLK signal is derived by dividing VCLK by 2), this register performs the same function as CRT Controller register CR0[7:0].

12.148 R2Z: Horizontal Blanking Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset State
7	Horizontal Blanking Start [7]	0
6	Horizontal Blanking Start [6]	0
5	Horizontal Blanking Start [5]	0
4	Horizontal Blanking Start [4]	0
3	Horizontal Blanking Start [3]	0
2	Horizontal Blanking Start [2]	0
1	Horizontal Blanking Start [1]	0
0	Horizontal Blanking Start [0]	0

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** When Sequencer register SR1[3] is 1 (the DCLK signal is derived by dividing VCLK by 2), this register performs the same function as CRT Controller register CR2[7:0].

12.149 R3Z: Horizontal Blanking End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Horizontal Blanking End [4]	0
3	Horizontal Blanking End [3]	0
2	Horizontal Blanking End [2]	0
1	Horizontal Blanking End [1]	0
0	Horizontal Blanking End [0]	0

Bit	Description
7:5	**Reserved**
4:0	**Horizontal Blanking End [4:0]:** When Sequencer register SR1[3] is 1 (the DCLK signal is derived by dividing VCLK by 2), these bits perform the same function as CRT Controller register CR3[4:0]. • These bits are the least-significant 5 bits of a 6-bit field controlling the horizontal blanking end signal. • The most-significant sixth bit that controls the horizontal blanking end signal is in Extension register R5Z[7].

12.150 R4Z: Horizontal Sync Start Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset State
7	Horizontal Sync Start [7]	0
6	Horizontal Sync Start [6]	0
5	Horizontal Sync Start [5]	0
4	Horizontal Sync Start [4]	0
3	Horizontal Sync Start [3]	0
2	Horizontal Sync Start [2]	0
1	Horizontal Sync Start [1]	0
0	Horizontal Sync Start [0]	0

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** When Sequencer register SR1[3] is 1 (the DCLK signal is derived by dividing VCLK by 2), this register performs the same function as CRT Controller register CR4[7:0].

12.151 R5Z: Horizontal Sync End Shadow Register

I/O Port Address: 3?5

Index: This register is accessible only when Extension register CR2C[5:4] is 11.

Bit	Description	Reset State
7	Horizontal Blanking End [5]	0
6	Reserved	
5	Reserved	
4	Horizontal Sync End [4]	0
3	Horizontal Sync End [3]	0
2	Horizontal Sync End [2]	0
1	Horizontal Sync End [1]	0
0	Horizontal Sync End [0]	0

Bit	Description
7	**Horizontal Blanking End [5]:** • This bit is the most-significant bit of the 6-bit horizontal blanking end signal. • The least-significant 5 bits of the horizontal blanking end signal are in Extension register R3Z[4:0].
6:5	**Reserved**
4:0	**Horizontal Sync End [4:0]:** When Sequencer register SR1[3] is 1 (the DCLK signal is derived by dividing VCLK by 2), this register performs the same function as CRT Controller register CR5[4:0].

13. ELECTRICAL SPECIFICATIONS

13.1 Absolute Maximum Ratings

Specification	Maximum Rating
Ambient temperature while operating (T_A)	0°C to 70°C
Storage temperature	–65°C to 150°C
Voltage on any pin	V_{SS} – 0.5 V to V_{DD} + 0.5 V
Operating power dissipation	2 W (watts)
Power supply voltage	7.0 V
Injection current (latch-up testing)	100 mA

NOTES:

1) System components must be operated within the limits of the absolute maximum ratings. If system components are run at conditions at or outside these limits, the system components can be permanently damaged.
2) Functional operation at or outside any of the conditions indicated in the absolute maximum ratings is not implied.
3) Exposure to absolute maximum rating conditions for extended periods can affect system reliability.

13.2 DC Specifications

13.2.1 DC Specifications — Digital Values

In the table below, V_{DD} = 5.0 ± 0.25 V [or V_{DD} = 3.3 (+ 0.30 V or – 0.15 V)] and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Conditions	Note
V_{DD} (5 V)	Power Supply Voltage (TTL)	4.75 Volts	5.25 Volts	Normal Operation	
V_{DD} (3.3 V)	Power Supply Voltage (CMOS)	3.15 Volts	3.6 Volts	Normal Operation	
V_{IL}	Input Low Voltage (TTL)	0 Volts	0.8 Volts	3.15 V < V_{DD} < 5.25 V	
V_{IH}	Input High Voltage (TTL)	2.0 Volts	V_{DD} + 5% V_{DD} (Volts)	3.15 V < V_{DD} < 5.25 V	
V_{IHC}	Input High Voltage (CMOS)	0.7 V_{DD} (Volts)	V_{DD} + 5% V_{DD} (Volts)	3.15 V < V_{DD} < 5.25 V	
V_{ILC}	Input Low Voltage (CMOS)	–0.5 Volts	0.3V_{DD} (Volts)	3.15 V < V_{DD} < 5.25 V	
V_{OL}	Output Low Voltage (TTL)		0.4 Volts	I_{OL} = (Refer to Section 13.2.2.)	1
V_{OH}	Output High Voltage (TTL)	2.4 Volts		I_{OH} = (Refer to Section 13.2.2.)	2
V_{OHC}	Output High Voltage (CMOS)	0.9 V_{DD} (Volts)		I_{OHC} = –200 µA	
V_{OLC}	Output Low Voltage (CMOS)		0.1V_{DD} (Volts)	I_{OLC} = 3.2 mA	
I_{CC1}	Power Supply Current		150 mA	CRT-only Operation	3
I_{CC2}	Power Supply Current		100 mA	LCD-only Operation	3
I_{CC3}	Power Supply Current		100 µA	Hardware-Controlled Suspend mode	3
I_{IL}	Input Low Current		–10 µA	V_{IN} = 0.0 V	
I_{IH}	Input High Current		10 µA	V_{IN} = V_{DD}	
I_{OZ}	Output Leakage Current	–10 µA	10 µA	0 < V_{OUT} < V_{DD}	4
C_{IN}	Input Capacitance		10 pF		5
C_{OUT}	Output Capacitance		10 pF		5

NOTES:

1) When V_{DD} = 5.0 V, data outputs D31:0 rated at I_{OL} = 8 mA at V_{OL} = 0.5 V sink I_{OL} = 20 mA at V_{OL} = 0.6 V.
When V_{DD} = 3.3 V, data outputs D31:0 rated at I_{OL} = 4 mA at V_{OL} = 0.3 V sink I_{OL} = 12 mA at V_{OL} = 0.6 V.
2) When V_{DD} = 5.0 V, data outputs D31:0 rated at I_{OH} = –6.0 mA at V_{OH} = 4.5 V source I_{OH} = –15 mA at V_{OH} = 4.0 V.
When V_{DD} = 3.3 V, data outputs D31:0 rated at I_{OH} = –3.0 mA at V_{OH} = 3.0 V source I_{OH} = –12 mA at V_{OH} = 2.0 V.
3) These current values occur when V_{DD} = 3.3 V, FPVDCLK = 28 MHz, and MCLK = 45 MHz.
4) This current is a measure of tristate output leakage current when in high-impedance (high-Z) mode.
5) This capacitance is periodically sampled and tested.

13.2.2 DC Specifications — Output Loading Values

CL-GD7548 Pin Number	CL-GD7548 Pin Name	I_{OH} (mA) When $V_{OH} = 0.9V_{DD}$		I_{OL} (mA) When $V_{OL} = 0.1V_{DD}$		Load (pF)
		V_{DD} = 3.3 V	V_{DD} = 5.0 V	V_{DD}= 3.3 V	V_{DD}= 5.0 V	
3	DEVSEL / LDEV#	–6	–10	10.0	20.0	200
4	RDY# / TRDY#	–6	–10	10.0	20.0	200
5	INTR / INTR#	–4	–8	6	12	200
22	A7 / STOP#	–4	–8	10	16	200
23	A8 / PAR	–4	–8	10	16	200
43:46, 48:51, 53:61, 63:66, 68:72, 74:79	AD[31:0] / D[31:0]	–3	–6	2	4	240
81	SLEEP# / ZVPCTL	–4	–8	6	12	50
91	HSYNC	–4	–8	6	12	50
93	VSYNC	–4	–8	6	12	50
94	NTSC / PAL	–4	–8	6	12	50
140:133, 131:125, 123:122, 120:114	FP[23:0]	–3	–6	6	12	50
95	CSYNC	–4	–8	6	12	50
144:141,134:133,125,123	FCP[7:0]	–3	–6	6	12	50
101	FCBLANK# / HREFI	–3	–6	4	8	50
102	FPVEE	–3	–6	6	12	35
103	DDCC / FCDCLK / VCLK	–3	–6	6	12	35
106	FPVCC	–3	–6	6	12	35
108	FPDE / XCLKU	–3	–6	6	12	50
110	LFS	–3	–6	6	12	50
112	LLCLK[a]	–4	–8	6	12	50
113	FPVDCLK	–4	–8	6	12	50
115	FP[1] / OVRW# / VACTI	–3	–6	6	12	35
117	FP[3] / MOD	–3	–6	6	12	20
123	FCP[0] / FP[8] / SBYST#	–4	–8	6	12	35
125	FCP[1] / FP[9] / SUSPST#	–4	–8	6	12	35
146	TVON / XRDACCS	–3	–6	6	12	50
148	PROG	–3	–6	6	12	35
151:161,163:167,186:191,193, 196, 202:204, 206:208,1,2	MD[31:0]	–3	–6	4	8	50
169, 170, 195, 194	CAS[3:0]#	–3	–6	4	8	50
169, 170, 195, 194	WE[3:0]#	–3	–6	4	8	50
171:180	MA[9:0]	–3	–6	4	8	50
181	CAS# / WE#	–3	–6	4	8	50
182	OE#	–3	–6	4	8	50
184:183	RAS[1:0]#	–3	–6	4	8	50

[a] The LLCLK and FPVDCLK values depend on the bit setting of Extension register SR2B[7].
When this bit = 0, the values for these pins are: I_{OH} = –8 mA, I_{OL} = 12 mA, and the load is 50 pF.
When this bit = 1, the values for these pins are: I_{OH} = –16mA, I_{OL} = 24 mA, and the load remains 50 pF.

13.2.3 DC Specifications — Palette DAC

In the table below, V_{DD} = 5.0 ± 0.25 V [or V_{DD} = 3.3 (+ 0.30 V or – 0.15 V)] and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Conditions
DACVDD (5.0 V)	DAC Supply Voltage	4.75 Volts	5.25 Volts	Normal Operation
DACVDD (3.3 V)	DAC Supply Voltage	3.15 Volts	3.6 Volts	Normal Operation
$AI_{DD2,3}$ (5.0 V)	Analog Supply Current		tbd[a]	$AV_{DD2,3}$ = 5.25 V
$AI_{DD2,3}$ (3.3 V)	Analog Supply Current		tbd	$AV_{DD2,3}$ = 3.45 V
I_{REF}[b]	DAC Reference Current (Nominal)	6.20 mA	7.14 mA	6.67 mA ± 7%

[a] 'tbd' = to be determined

[b] Refer to the detailed pin description in Chapter 2 for information regarding nominal I_{REF}.

13.2.4 DC Specifications — Frequency Synthesizer

In the table below, V_{DD} = 5.0 ± 0.25 V [or V_{DD} = 3.3 (+ 0.30 V or – 0.15 V)] and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Conditions
MAVDD VAVDD	Synthesizer Supply Voltage	3.15 Volts	3.6 Volts	V_{DD} = 3.3 (+ 0.30 V or – 0.15 V)
MAVDD VAVDD	Synthesizer Supply Voltage	4.75 Volts	5.25 Volts	V_{DD} = 5.5 ± 0.25 V

13.3 DAC Characteristics

In the table below, V_{DD} = 5.0 ± 0.25 V [or V_{DD} = 3.3 (+ 0.30 V or – 0.15 V)] and T_A = 0°C to 70°C, unless otherwise specified.

Symbol	Parameter	MIN	MAX	Notes
Res.	Resolution		8 bits	
I_O	Output Current		30 mA	Note 1
t_D	Analog Output Delay		tbd[9]	Notes 2, 3, 4
t_r, t_f	Analog Output Rise/Fall Time		8 ns	Notes 3, 4, 5
t_s	Analog Output Settling Time		15 ns	Notes 3, 4, 6
t_{SK}	Analog Output Skew		tbd	Notes 3, 4, 7
FT	Clock and Data Feed-Through		tbd	Notes 3, 4, 7
DT	DAC-to-DAC Correlation		tbd	Notes 7, 8
GI	Glitch Impulse		tbd	Notes 3, 4, 7
CT	DAC-to-DAC Crosstalk		tbd	Notes 3, 4, 5

NOTES:

1) Output current measure occurs under the condition V_O < 1 volt.
2) t_D is measured from the 50% point of VCLK to 50% point of full-scale transition.
3) Load is 50 Ω and 30 pF per analog output.
4) I_{REF} = value to be determined from measures taken according to the application note “IREF Current Source” in the *CL-GD754X Application Book*.
5) t_r and t_f are measured from 10% to 90% full-scale.
6) t_s is measured from 50% of full-scale transition to output remaining within 2% of final value.
7) Outputs loaded identically.
8) About the mid-point of the distribution of the three DACs measured at full-scale output.
9) ‘tbd’ = to be determined.

13.4 AC Parameters — List of Timing Relationships

NOTES: In the following diagrams:

1) High-Z is high-impedance.
2) 'tbd' is to be determined.
3) 'MCLK' is the period for MCLK, a clock that is internal to the CL-GD7548.

13.5 Bus Configuration — System Reset Timing

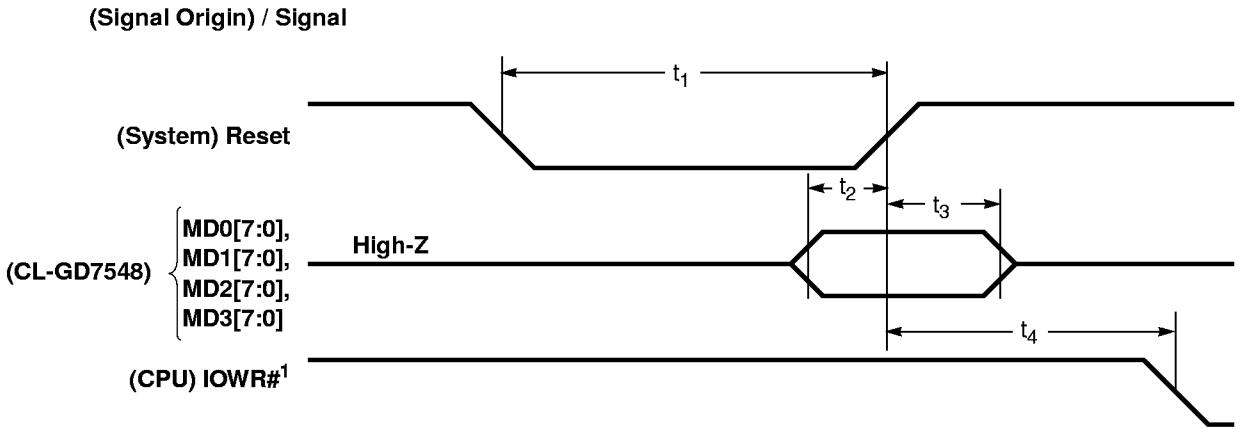
The timing diagram in this section is for the bus configuration, which takes place during system reset.

Table 13-1 and Figure 13-1 refer to information from the SW0, SW1, and SW2 pins, which are read by Extension register bits SR24[2:0] and used by the memory data lines to configure the CL-GD7548.

Table 13-1. Bus Configuration — System Reset Timing

Symbol	Parameter	MIN	MAX
t_1 [a]	System reset pulse width	12 MCLK	–
t_2	Memory data setup time to system reset rising edge	2 ns	–
t_3	Memory data hold time from system reset rising edge	5 ns	–
t_4	System reset high to first I/O Read/Write command	12 MCLK	–

[a] 'MCLK' is the period for MCLK, a clock that is internal to the CL-GD7548.



1. This signal name depends on the bus interface that is being used.

Figure 13-1. Bus Configuration — System Reset Timing

13.6 Timing Diagrams — Local Bus

The timing diagrams in this section apply to the '486 local bus and VESA VL-Bus interfaces to the CL-GD7548.

Table 13-2. Local Bus — LCLK Timing

Symbol	Parameter	CLK1X	
		MIN	MAX
t_1	Input clock rise time	0.5 ns	4.0 ns
t_2	Input clock fall time	0.5 ns	4.0 ns
t_3	Input clock high pulse width	40% t_5	60% t_5
t_4	Input clock low pulse width	40% t_5	60% t_5
t_5	Input clock period	30 ns	tbd[a]

[a] 'tbd' = to be determined

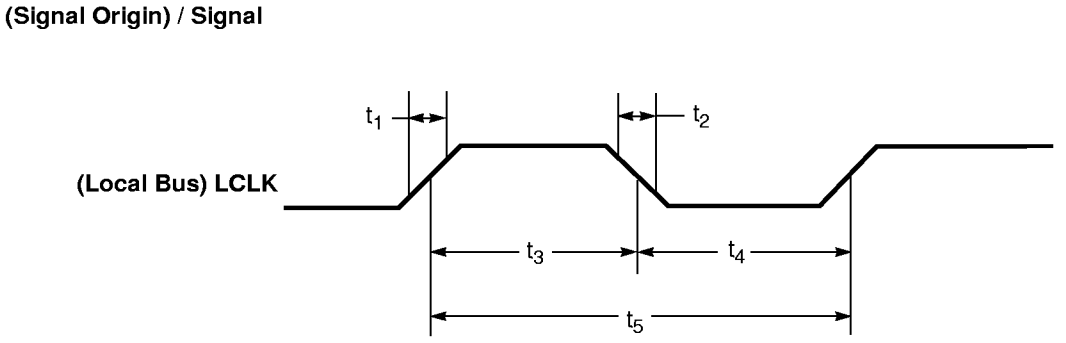


Figure 13-2. Local Bus — LCLK Timing

Table 13-3. Local Bus — ADS# and LDEV# Timing

Symbol	Parameter	MIN	MAX
t_1	Address, Status, ADS# setup to LCLK	5 ns	–
t_2	LDEV# low delay from Address, Status (20-pF loading)	–	15 ns
t_3	LDEV# high delay from Address, Status	–	18 ns

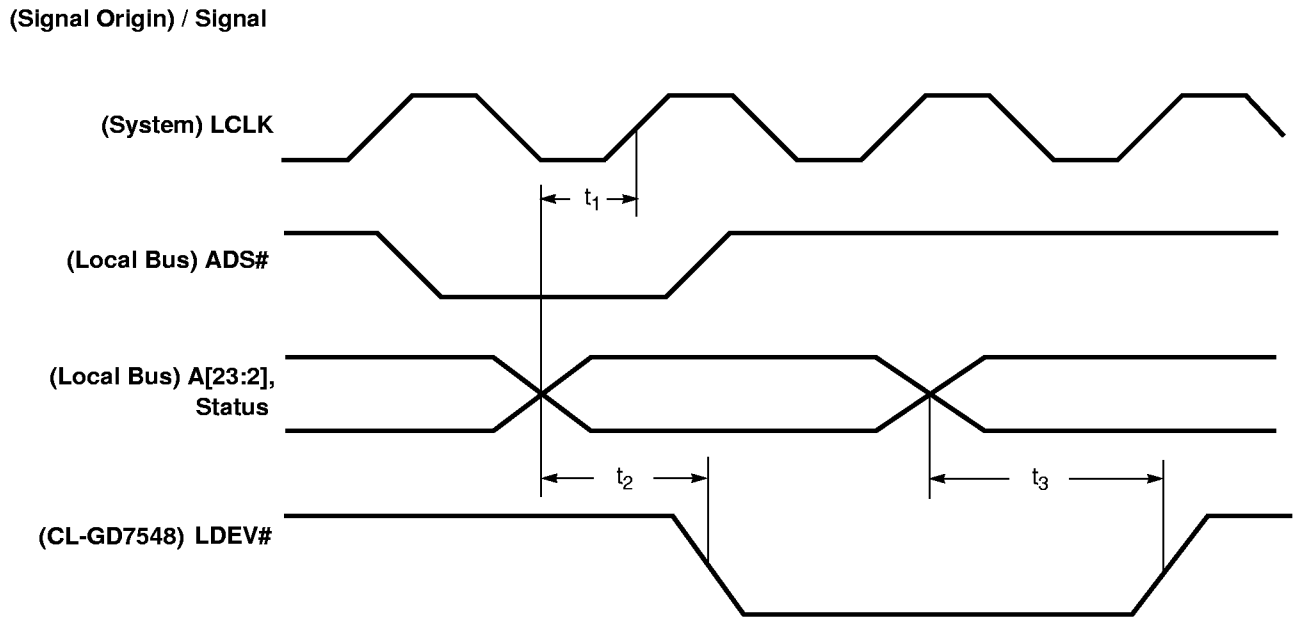


Figure 13-3. Local Bus — ADS# and LDEV# Timing

Table 13-4. Local Bus — RDY# and Read-Data Timing

Symbol	Parameter	MIN	MAX
t_1	RDY# low delay from LCLK	0	12 ns
t_2	RDY# high delay from LCLK	0	12 ns
t_3	RDY# high pulse width before high-Z	1/2 LCLK	–
t_4	Read data setup to RDY# low	0 ns	–
t_5	Read data hold from RDYRTN# high	12 ns	tbd[a]

[a] 'tbd' = to be determined

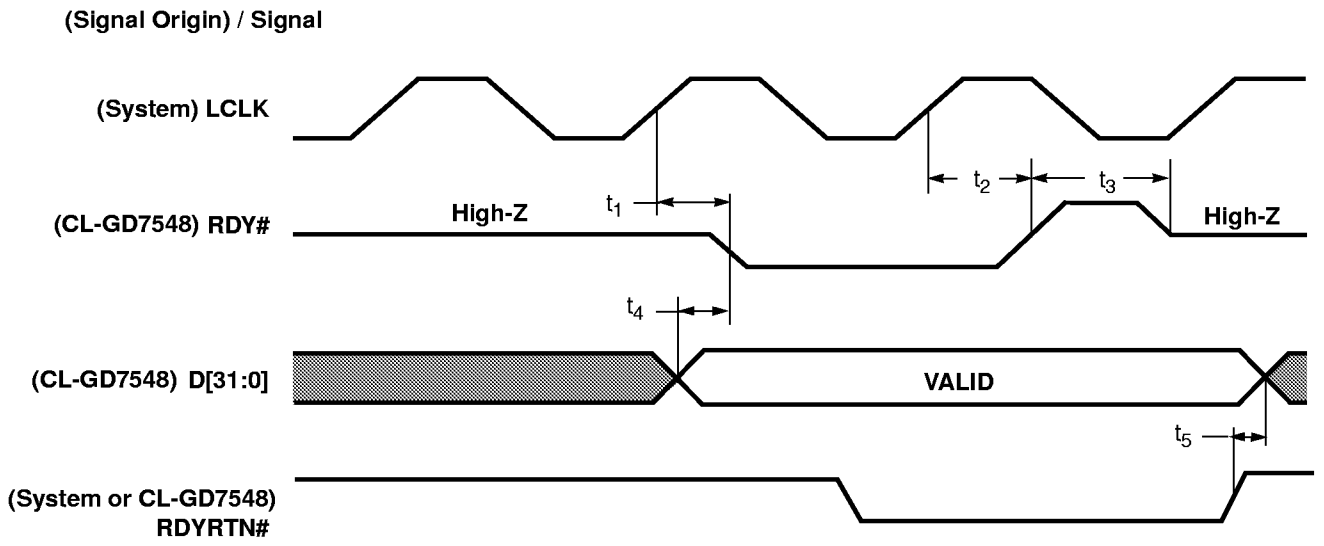


Figure 13-4. Local Bus — RDY# and Read-Data Timing

Table 13-5. Local Bus — RDYRTN# Timing

Symbol	Parameter	MIN	MAX
t_1	RDYRTN# setup time to LCLK	5 ns	–
t_2	RDYRTN# hold time from LCLK	2 ns	–

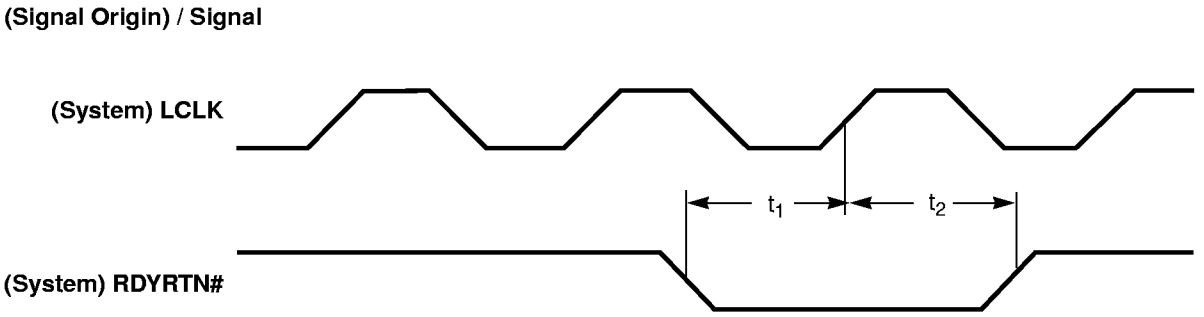


Figure 13-5. Local Bus: RDYRTN# Timing

Table 13-6. Local Bus — Write Data Timing

Symbol	Parameter	MIN	MAX
t_1	Data setup time to LCLK	7 ns	–
t_2	Data hold time from LCLK	2 ns	–

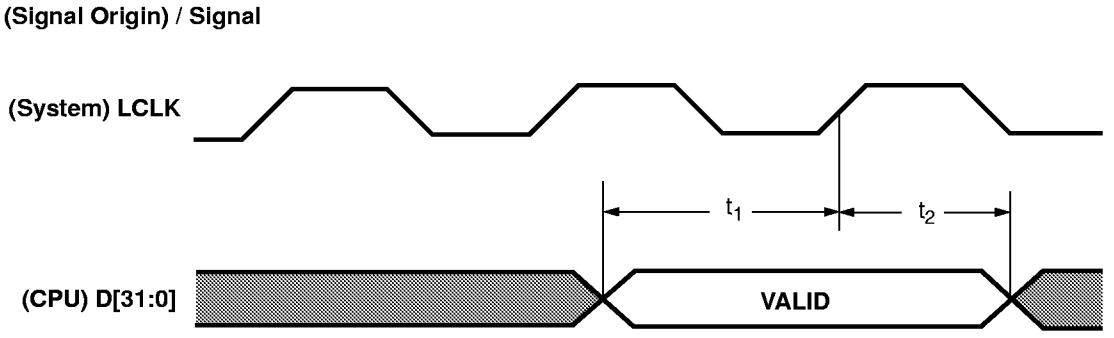


Figure 13-6. Local Bus — Write Data Timing

13.7 Timing Diagrams — PCI Bus

The timing diagrams in this section apply to a PCI bus interface to the CL-GD7548.

Table 13-7. PCI Bus — FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# Timing (Write)

Symbol	Parameter	MIN	MAX
t_1	FRAME# setup to CLK	7 ns	–
t_2	AD[31:0] (Address) setup to CLK	7 ns	–
t_3	AD[31:0] (Address) hold from CLK	0 ns	–
t_4	AD[31:0] (Data) setup to CLK (write)	7 ns	–
t_5	AD[31:0] (Data) hold from CLK (write)	0 ns	–
t_6	C/BE[3:0]# (Bus CMD) setup to CLK	7 ns	–
t_7	C/BE[3:0]# (Bus CMD) hold from CLK	0 ns	–
t_8	C/BE[3:0]# (Byte Enable) setup to CLK	7 ns	–
t_9	DEVSEL# delay from CLK	0 ns	11
t_{10}	DEVSEL# high before high-Z	1 CLK	–

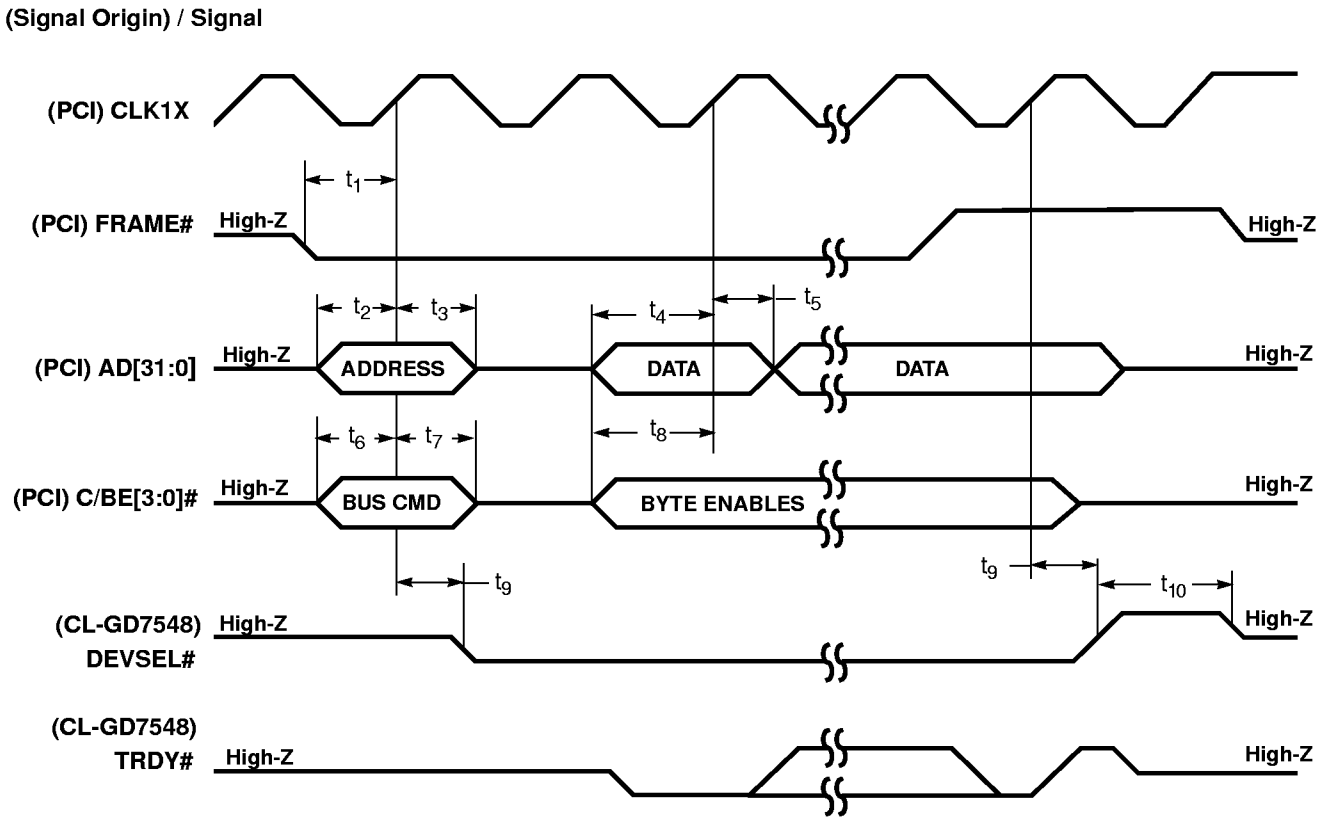


Figure 13-7. PCI Bus — FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# Timing (Write)

Table 13-8. PCI Bus — FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# Timing (Read)

Symbol	Parameter	MIN	MAX
t_1	FRAME# setup to CLK	7 ns	–
t_2	AD[31:0] (Address) setup to CLK	7 ns	–
t_3	AD[31:0] (Address) hold from CLK	0 ns	–
t_4	AD[31:0], C/BE[3:0]# high-Z from CLK (read)	0 ns	28 ns
t_5	C/BE[3:0]# (Bus CMD) setup to CLK	7 ns	–
t_6	C/BE[3:0]# (Bus CMD) hold from CLK	0 ns	–
t_7	C/BE[3:0]# (Byte Enable) setup to CLK	7 ns	–
t_8	DEVSEL# delay from CLK	0 ns	11
t_9	DEVSEL# high before high-Z	1 CLK	–
t_{10}	Data delay from CLK (read)	2 ns	11 ns
t_{11}	Data hold from CLK (read)	0 ns	tbd

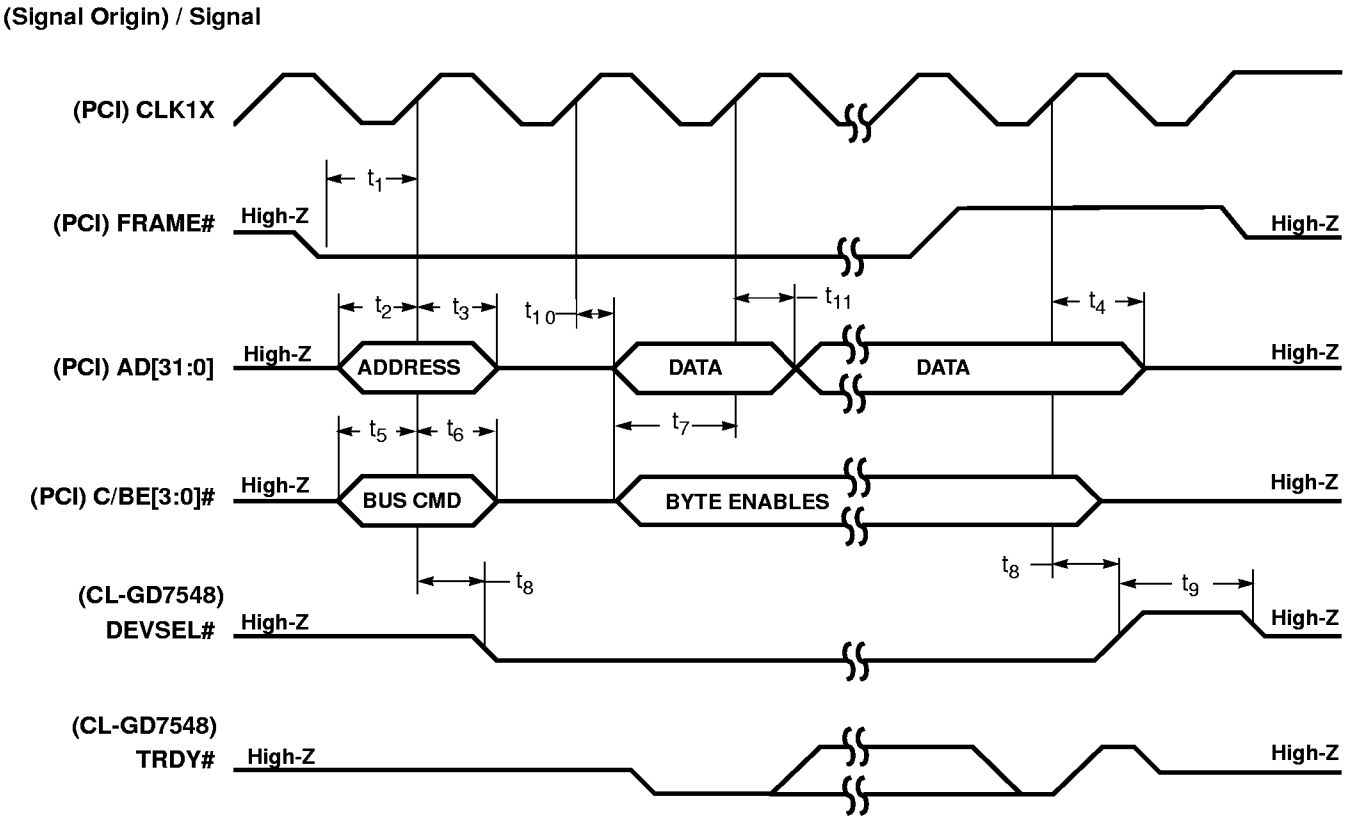


Figure 13-8. PCI Bus — FRAME#, DEVSEL#, AD[31:0], and C/BE[3:0]# Timing (Read)

Table 13-9. PCI Bus — TRDY# Delay Timing

Symbol	Parameter	MIN	MAX
t_1	TRDY# low delay from CLK	0 ns	11 ns
t_2	TRDY# high delay from CLK	0 ns	11 ns
t_3	TRDY# high pulse before high-Z	1 CLK	–

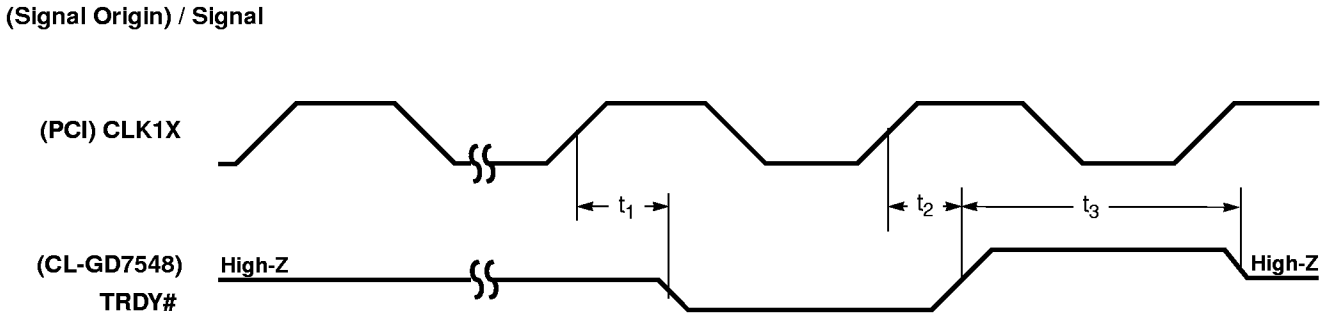


Figure 13-9. PCI Bus — TRDY# Delay Timing

Table 13-10. PCI Bus — Read Data / IRDY# Timing

Symbol	Parameter	MIN	MAX
t_1	IRDY# setup to CLK	7 ns	–
t_2	IRDY# hold from CLK	0 ns	–

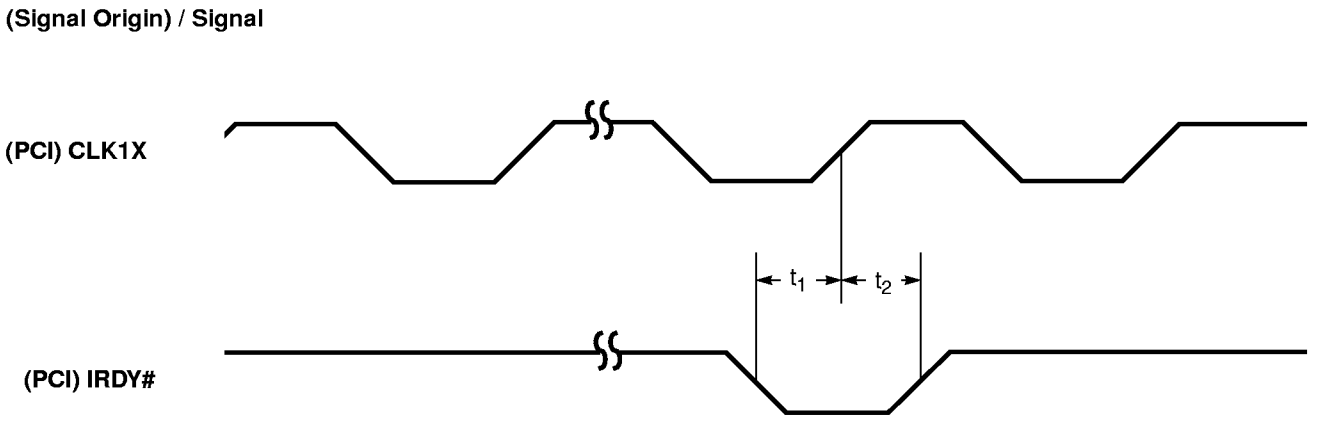


Figure 13-10. PCI Bus — Read Data / IRDY# Timing

Table 13-11. PCI Bus — STOP# Delay Timing

Symbol	Parameter	MIN	MAX
t_1	STOP# low delay from CLK	2 ns	11 ns
t_2	STOP# high delay from CLK	2 ns	11 ns
t_3	STOP# high pulse before high-Z	1 CLK	–

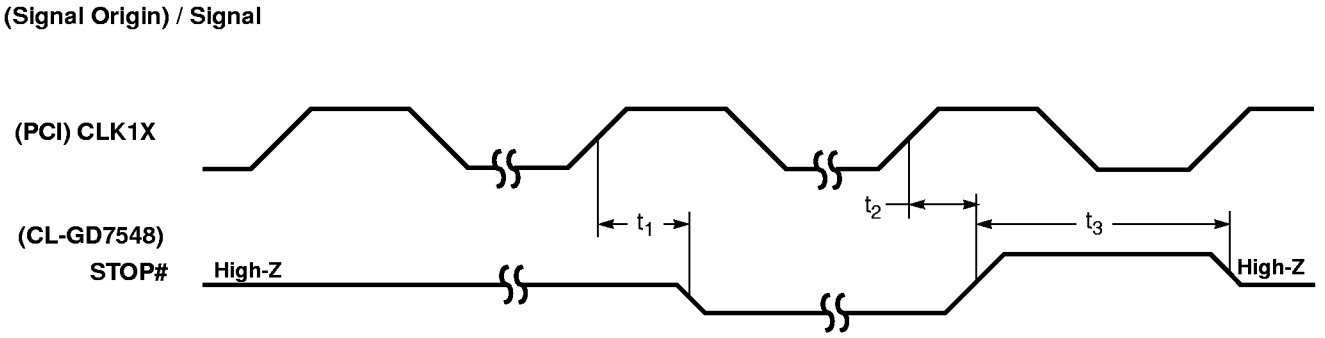


Figure 13-11. PCI Bus — STOP# Delay Timing

Table 13-12. PCI Bus — IDSEL Timing

Symbol	Parameter	MIN	MAX
t_1	IDSEL setup to CLK	7 ns	–
t_2	IDSEL hold	0 ns	–

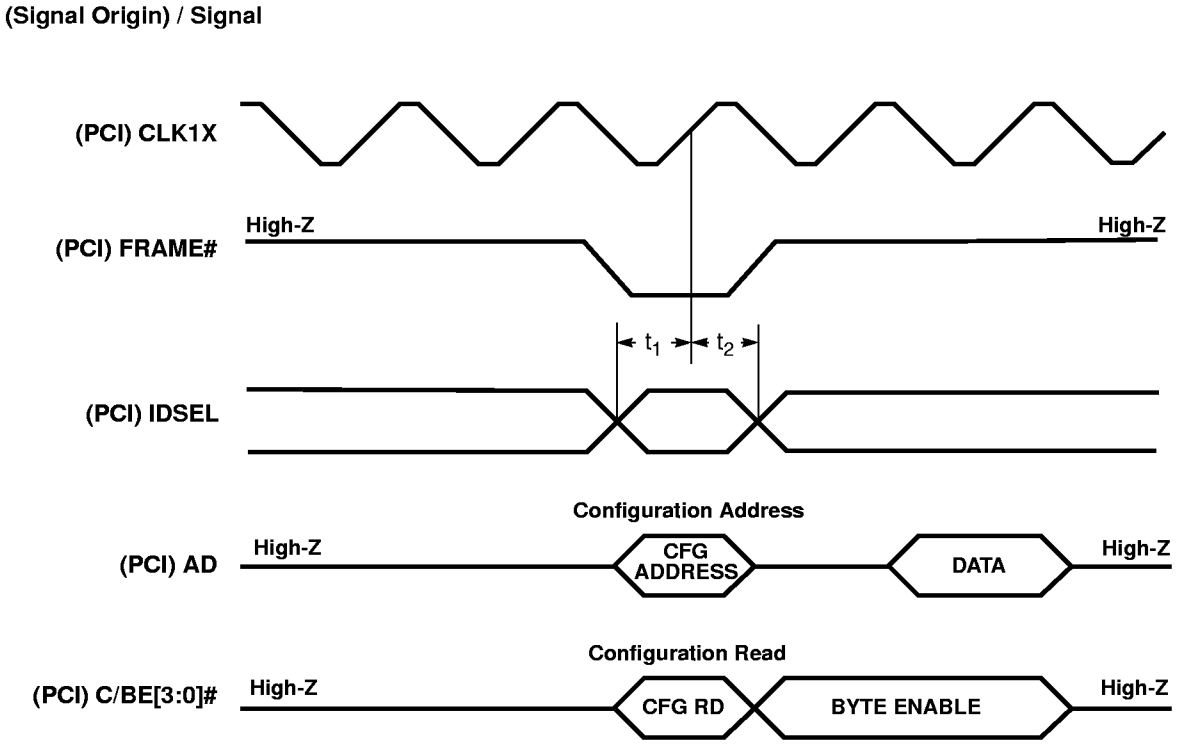


Figure 13-12. PCI Bus — IDSEL Timing

Table 13-13. PCI Bus — PAR Timing (Write)

Symbol	Parameter	MIN	MAX
t_1	Address PAR setup from CLK (input to CL-GD7548)	7 ns	–
t_2	Address PAR hold from CLK (input to CL-GD7548)	0 ns	–
t_3	Data PAR setup from CLK (input to CL-GD7548)	7 ns	–
t_4	Data PAR hold from CLK (input to CL-GD7548)	0 ns	–

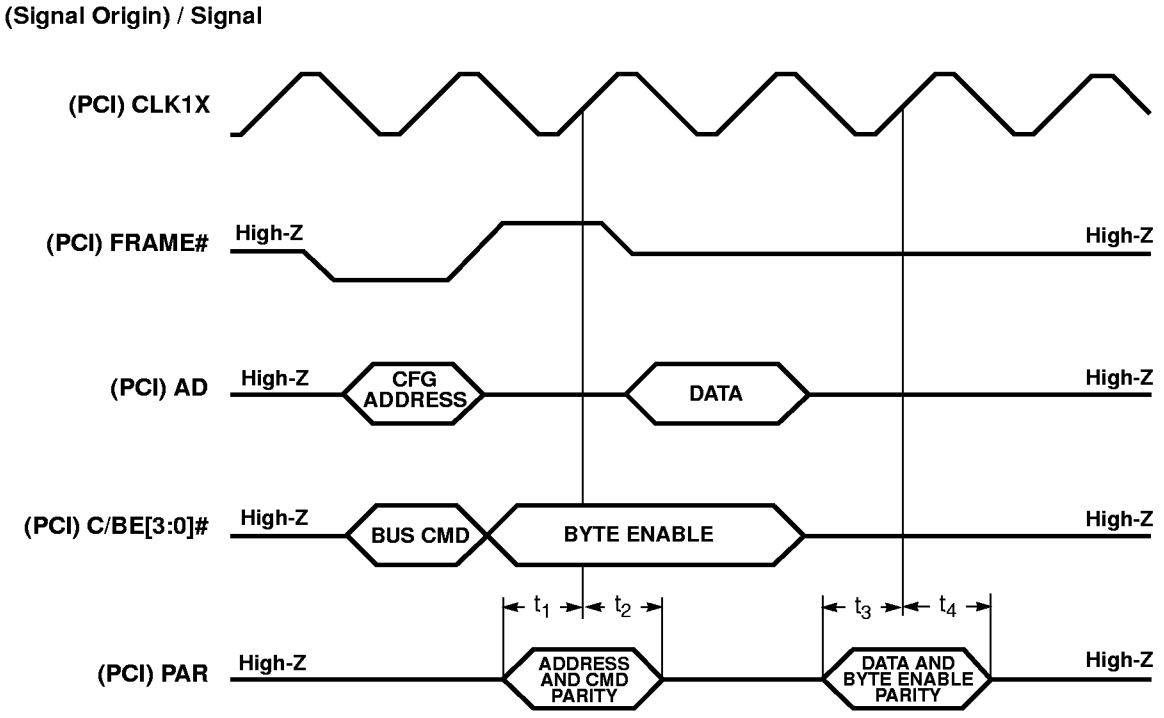


Figure 13-13. PCI Bus — PAR Timing (Write)

Table 13-14. PCI Bus — PAR Timing (Read)

Symbol	Parameter	MIN	MAX
t_1	PAR setup from CLK (input to CL-GD7548)	7 ns	–
t_2	PAR hold from CLK (input to CL-GD7548)	0 ns	–
t_3	PAR delay from CLK (output to CL-GD7548)	2 ns	11 ns
t_4	PAR off delay from CLK (output to CL-GD7548)	–	28 ns

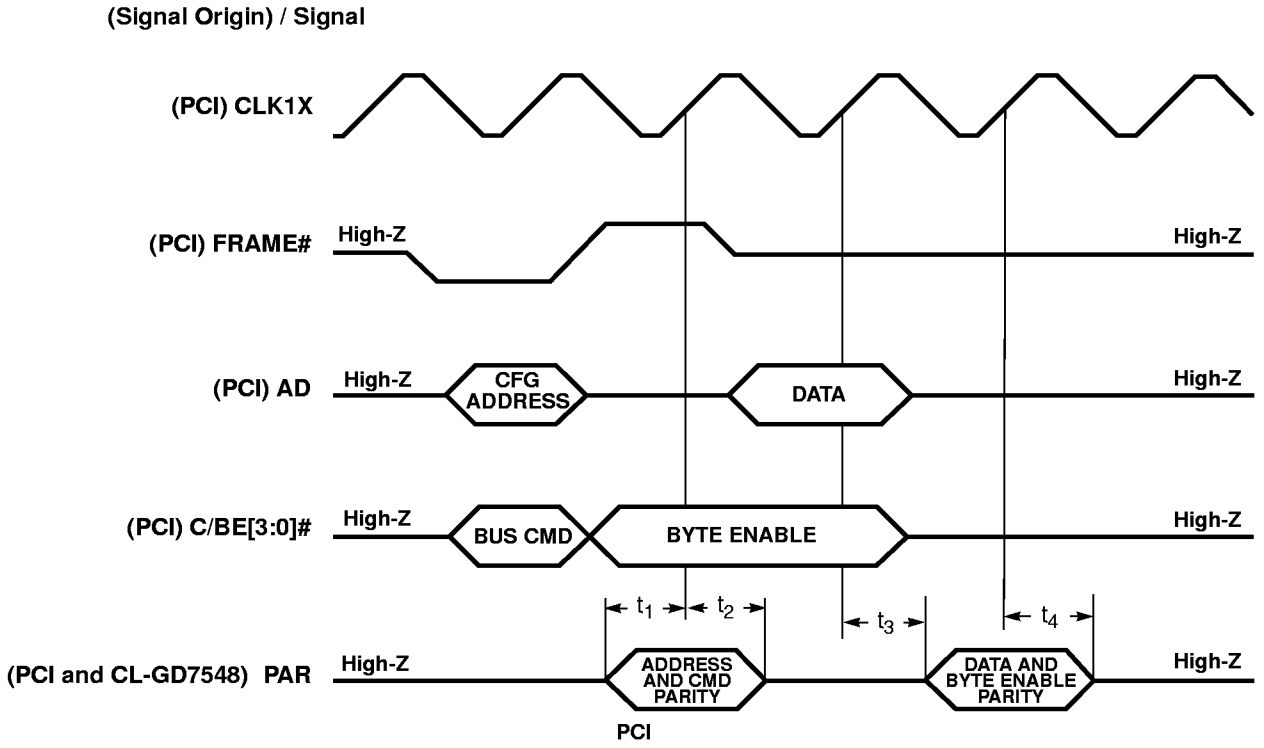


Figure 13-14. PCI Bus — PAR Timing (Read)

13.8 Timing Diagrams — Display Memory Bus

The timing diagrams in this section apply to the CL-GD7548 bus interface to the display memory.

Table 13-15. Display Memory Bus — Read Timing (t = 1-MCLK cycle)

Symbol	Parameter	MIN	MAX
t_1	Address setup to RAS# low	1.0t – 2 ns	
t_2	Address setup to CAS# low	1.0t – 3 ns	
t_3	RAS# low to CAS# low delay	2.5t – 2 ns at t_{RAC} = 6t/8t 3.0t – 7 ns at t_{RAC} = 7t/9t	
t_4	Row address hold from RAS# low	1.5t – 2 ns	
t_5	Column address hold from CAS# low	1.0t – 2 ns	
t_6	RAS# precharge	2.5t – 4 ns at t_{RAC} = 6t 3.0t at t_{RAC} = 7t 3.5t – 4 ns at t_{RAC} = 8t 4.0t at t_{RAC} = 9t	
t_7	t_{RAC}, read cycle time (depends on DRAM type)	6t, 7t, 8t or 9t	
t_8	Read command hold from CAS# high	1.0t + 3 ns at SR23[3] = 1 1.5t – 3 ns MIN at SR23[3] = 0	
t_9	CAS# precharge	1.0t-6ns	1.0t – 2 ns
t_{10}	RAS# low pulse width	3.5t at t_{RAC} = 6t 4.0t at t_{RAC} = 7t 4.5t at t_{RAC} = 8t 5.0t at t_{RAC} = 9t	
t_{11}	CAS# low pulse width	1.0t + 2 ns	1.0t + 6 ns
t_{12}	CAS# cycle time	2.0t	
t_{13}	RAS# hold time	1.0t + 2 ns at t_{RAC} = 6t/7t 2.0t at t_{RAC} = 8t or 9t	
t_{14}	Read command setup to CAS# low	3.0t – 3 ns at t_{RAC} = 6t 4.0t – 3 ns at t_{RAC} = 7t 5.0t – 3 ns at t_{RAC} = 8t 6.0t – 3 ns at t_{RAC} = 9t	
t_{15}	CAS# low to data latch	1.0t + 2 ns at SR20[7] = 0 2.0t – 5 ns at SR20[7] = 1	
t_{16}	Column address to data latch	2.0t – 1 ns at SR20[7] = 0 3.0t – 8 ns at SR20[7] = 1	

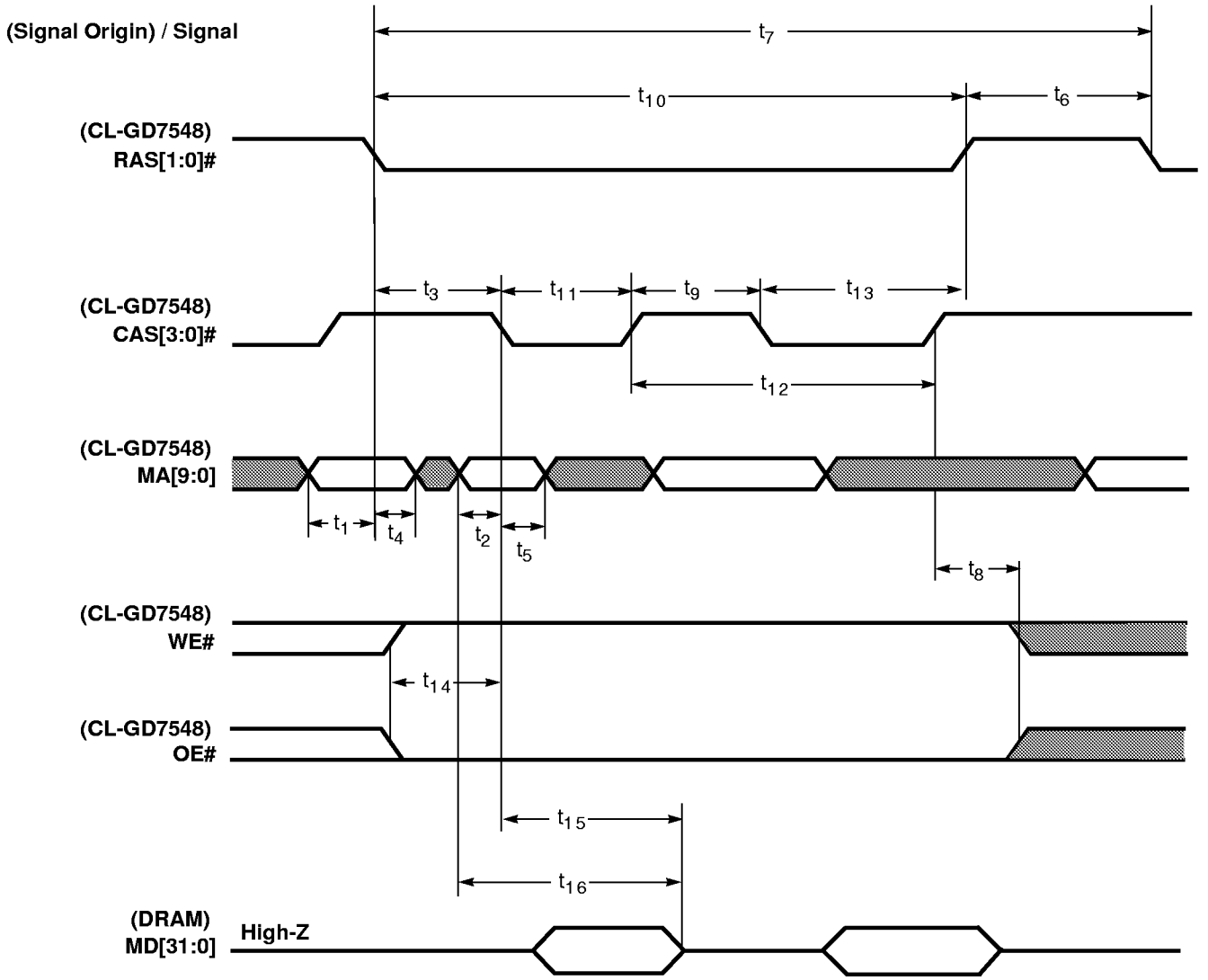


Figure 13-15. Display Memory Bus — Read Timing

Table 13-16. Display Memory Bus — Write Timing (t = 1-MCLK cycle)

Symbol	Parameter	MIN	MAX
t_1	Address setup to RAS# low	1.0t – 2 ns	
t_2	Address setup to CAS# low	1.0t – 3 ns	
t_3	RAS# low to CAS# low delay	2.5t – 2 ns at t_{RAC} = 6t/8t 3.0t – 7 ns at t_{RAC} = 7t/9t	
t_4	Row address hold from RAS# low	1.5t – 2 ns	
t_5	Column address hold from CAS# low	1.0t – 2 ns	
t_6	RAS# precharge	2.5t at t_{RAC} = 6t 3.0t at t_{RAC} = 7t 3.5t at t_{RAC} = 8t 4.0t at t_{RAC} = 9t	
t_7	t_{RAC}, write cycle time (depends on DRAM type)	6t, 7t, 8t or 9t	
t_8	CAS# precharge	1.0t – 6 ns	1.0t – 2 ns
t_9	CAS# cycle time	2.0t	
t_{10}	CAS# low pulse width	1.0t + 2 ns	1.0t + 6 ns
t_{11}	RAS# low pulse width	3.5t at t_{RAC} = 6t 4.0t at t_{RAC} = 7t 4.5t at t_{RAC} = 8t 5.0t at t_{RAC} = 9t	
t_{12}	WE# low setup to CAS# low	2.0t – 5 ns when SR23[3] = 1 0.5t – 2 ns when SR23[3] = 0	
t_{13}	WE# low hold from CAS# low	1.5t – 4 ns	
t_{14}	Write data setup to CAS# low	1.0t – 4 ns	
t_{15}	Write data hold from CAS# low	1.0t + 1 ns	
t_{16}	RAS# hold time	1.0t + 2 ns at t_{RAC} = 6t or 7t 2.0t at t_{RAC} = 8t or 9t	

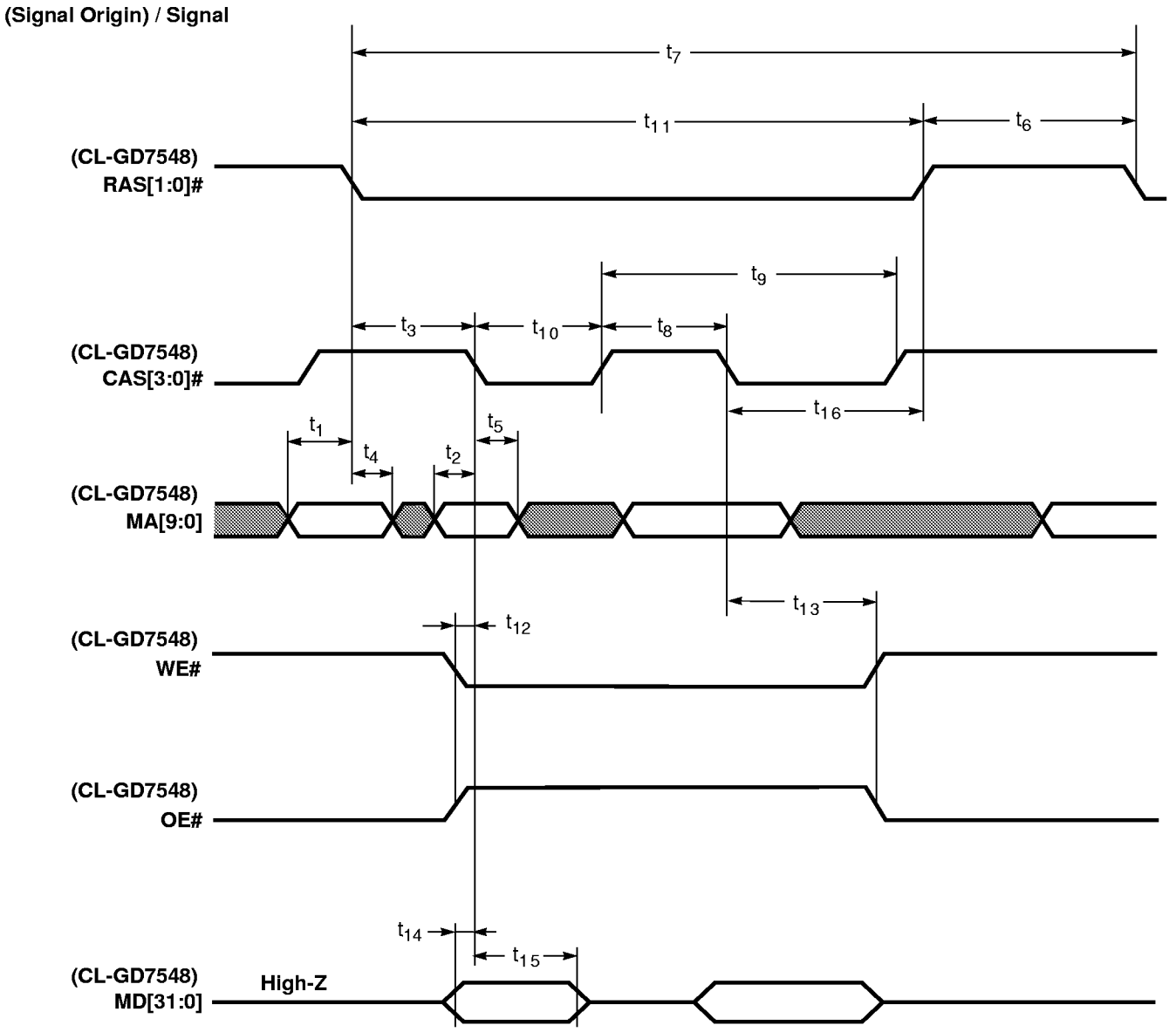


Figure 13-16. Display Memory Bus — Write Timing

Table 13-17. Display Memory Bus — CAS#-Before-RAS# Refresh Timing (t = 1-MCLK Cycle)

Symbol	Parameter	MIN	MAX
t_1	CAS# low setup to RAS# low[a]	1.5t – 2 ns	
t_2	RAS# low pulse width	3.5t	
t_3	RAS# high pulse width	2.5t – 4 ns	
t_4	CAS# hold time for refresh	2.5t – 4 ns	
t_5	Refresh cycle period	10.0t	
t_6	CAS# high pulse width	5.0t	
t_7	RAS# high to CAS# low	5.0t	

[a] There are one, three, or five RAS# pulses while CAS# remains low.

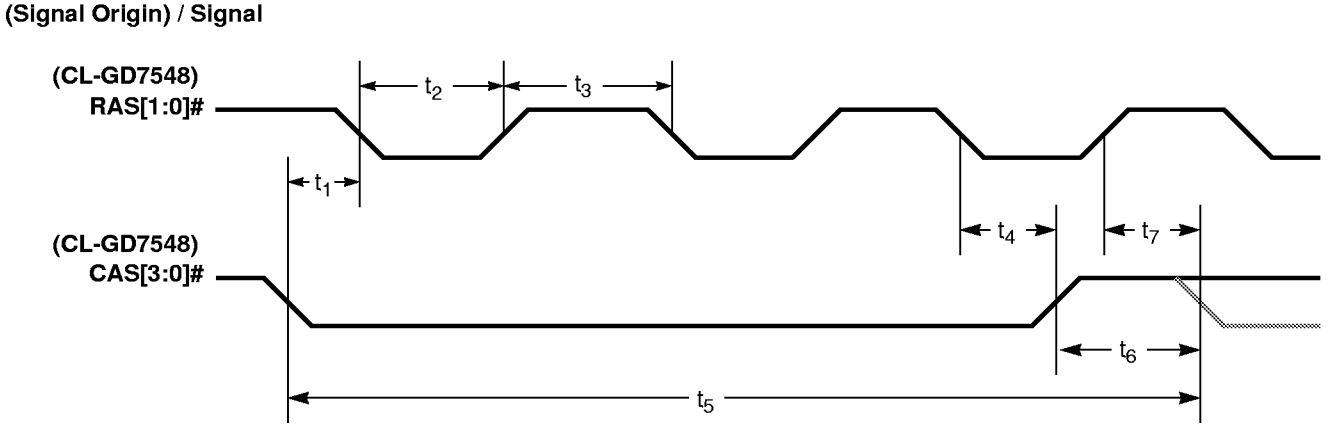


Figure 13-17. Display Memory Bus — CAS#-Before-RAS# Refresh Timing

13.9 Timing Diagrams — Feature Connector

The timing diagrams in this section apply to the CL-GD7548 interface to the Feature Connector (FC). For more information, refer to application note "The 8-Bit Dynamic Video Overlay" in the *CL-GD754X Application Book*.

Table 13-18. Feature Connector — Timing with Clock and Data Driven Externally

Symbol	Parameter	MIN	MAX
t_1	FCP[7:0] setup to FCVCLK	6 ns	–
t_2	FCP[7:0] hold from FCVCLK	6 ns	–

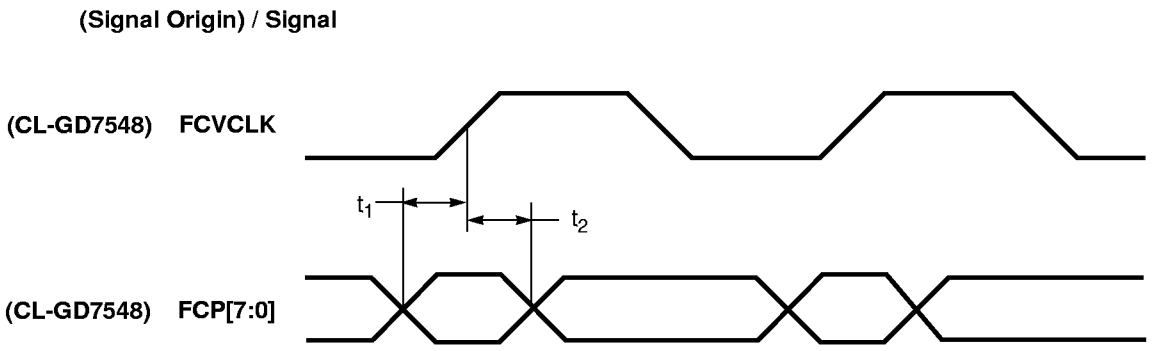


Figure 13-18. Feature Connector — Timing with Clock and Data Driven Externally

Table 13-19. Feature Connector — FCVCLK Input Timing Requirements

Symbol	Parameter	MIN	MAX
t_1	Rise time (FCVCLK)	–	3 ns
t_2	Fall time (FCVCLK)	–	3 ns
t_3	Clock high pulse width (FCVCLK)	40% of t_5	60% of t_5
t_4	Clock low pulse width (FCVCLK)	40% of t_5	60% of t_5
t_5	Clock period (FCVCLK)	20 ns	–

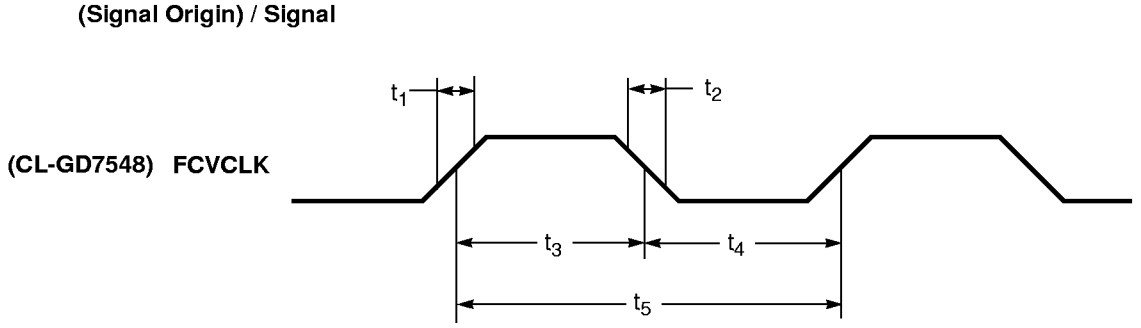


Figure 13-19. Feature Connector — FCVCLK Input Timing Requirements

13.10 Timing Diagrams — LCD Interface

The timing diagrams in this section apply to the CL-GD7548 interface to LCD flat panels.

NOTES:

C8DD-16 is:	color	8-color	dual-scan	16-bit data interface
C8DD-8 is:	color	8-color	dual-scan	8-bit data interface
C8SS-16 is:	color	8-color	single-scan	16-bit data interface
C512SS is:	color	512 colors	single-scan	
C4KSS is:	color	4K colors	single-scan	
C256KSS is:	color	256K colors	single-scan	
C16MSS is:	color	16M colors	single-scan	

Table 13-20. LCD Interface: High-Resolution Color-Passive STN LCD Timing[a]

Symbol	Parameter	C8DD-16	C8DD-8	C8SS-16
		Color	Color	Color
t_1	FPVDCLK period	$2.5t_1$[b]	t_1	$5t_1$
t_2	FPVDCLK high time	t_1 – 6 ns	$0.5t_1$ – 6 ns	$2t_1$ – 6 ns
t_3	FPVDCLK low time	t_1 – 6 ns	$0.5t_1$ – 6 ns	$2t_1$ – 6 ns
t_4	FPVDCLK rise and fall time (maximum)	6 ns	6 ns	6 ns
t_5	Data setup time	t_1 – 6 ns	$0.5t_1$ – 6 ns	$2t_1$ – 10 ns
t_6	Data hold time	t_1 – 6 ns	$0.5t_1$ – 6 ns	$2t_1$ – 10 ns
t_7	FPVDCLK low to LLCLK low	t_1 – 6 ns	$2t_1$ – 10 ns	$4t_1$ – 10 ns
t_8	FPVDCLK low from LLCLK low	t_1 – 6 ns	$2t_1$ – 10 ns	$4t_1$ – 10 ns
t_9	LLCLK high time	$4t_1$ – 6 ns	$4t_1$ – 6 ns	$4t_1$ – 6 ns
t_{10}	LFS high setup to LLCLK low (typical)	$2t_1$	$2t_1$	$2t_1$
t_{11}	LFS high hold time from LLCLK low (typical)	$2t_1$	$2t_1$	$2t_1$
t_{12}	MOD delay from FPVDCLK high (maximum)	300 ns	300 ns	300 ns

[a] Values are *minimum* unless otherwise specified.
[b] 't_1' is the period for the FPVDCLK.

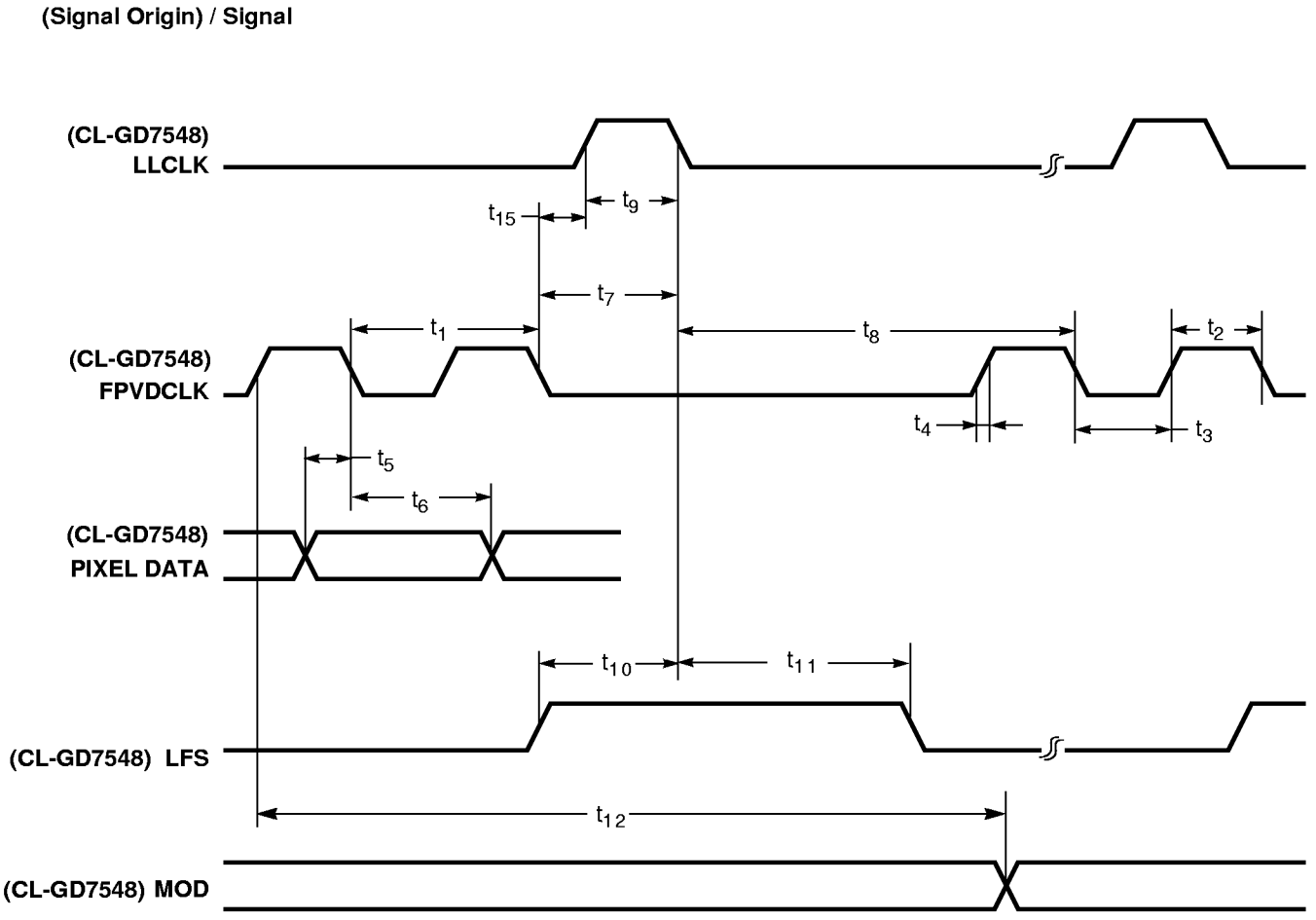
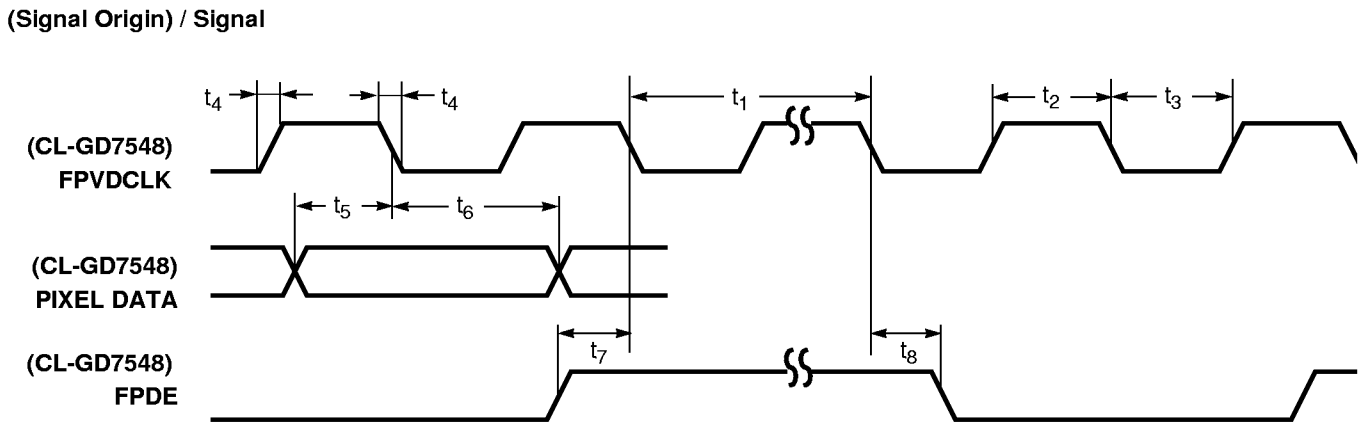


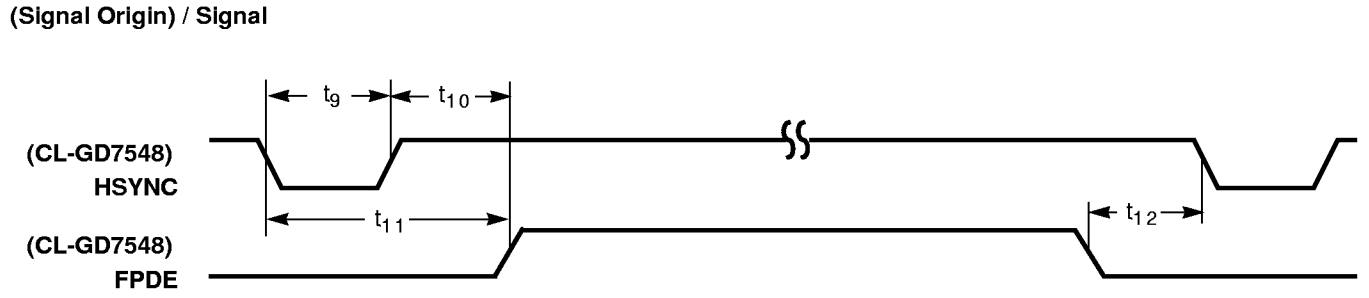
Figure 13-20. LCD Interface — Timing for High-Resolution Monochrome and Color-Passive STNs

Table 13-21. LCD Interface: Color TFT LCD Timing

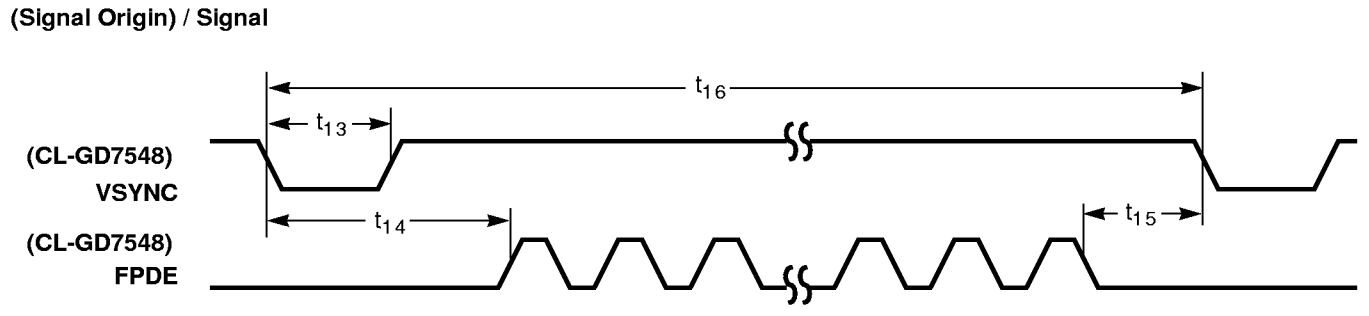
Symbol	Parameter	TFT — C512SS / C4KSS / C256KSS / C16MSS	
		MIN	MAX
t_1	FPVDCLK period	FPVDCLK	
t_2	FPVDCLK high pulse width	$0.5t_1$ – 6 ns	
t_3	FPVDCLK low pulse width	$0.5t_1$ – 6 ns	
t_4	FPVDCLK rise and fall time		10 ns
t_5	Data setup time	$0.5t_1$ – 6 ns	
t_6	Data hold time	$0.5t_1$ – 6 ns	
t_7	FPDE setup to FPVDCLK	$0.5t_1$ – 6 ns	
t_8	FPDE hold to FPVDCLK	$0.5t_1$ – 6 ns	
t_9	HSYNC width	$4t_1$	$128t_2$
t_{10}	HSYNC inactive to FPDE	0 ns	
t_{11}	Horizontal front porch	$16t_1$	$192t_1$
t_{12}	Horizontal back porch	0 ns	$192t_2$
t_{13}	VSYNC width	1 scanline	2 scanlines
t_{14}	Vertical front porch	0 scanline	1 scanlines
t_{15}	Vertical back porch		31 scanlines
t_{16}	VSYNC period (typical)	60 Hz	



TFT Pixel Data Timing



TFT HSYNC Timing



TFT VSYNC Timing

Figure 13-21. LCD Interface — Timing for Single-Scan Color TFT LCD

Table 13-22. V-Port™ Timing

Symbol	Parameter	MIN	MAX
t1	HREFI setup time for odd field	50 ns	
t2	HREFI hold time for odd field	50 ns	
t3	HREFI setup time for even field	50 ns	
t4	HREFI hold time for even field	50 ns	
t5	ZVPCLKI rise time		4 ns
t6	ZVPCLKI fall time		4 ns
t7	ZVPCLKI high period	20 ns	
t8	ZVPCLKI low period	20 ns	
t9	Data, VACT setup time	10 ns	
t10	Data, VACT hold time	2 ns	

NOTE: At 20 MHz, the maximum time for the PCLK period is 50 ns.

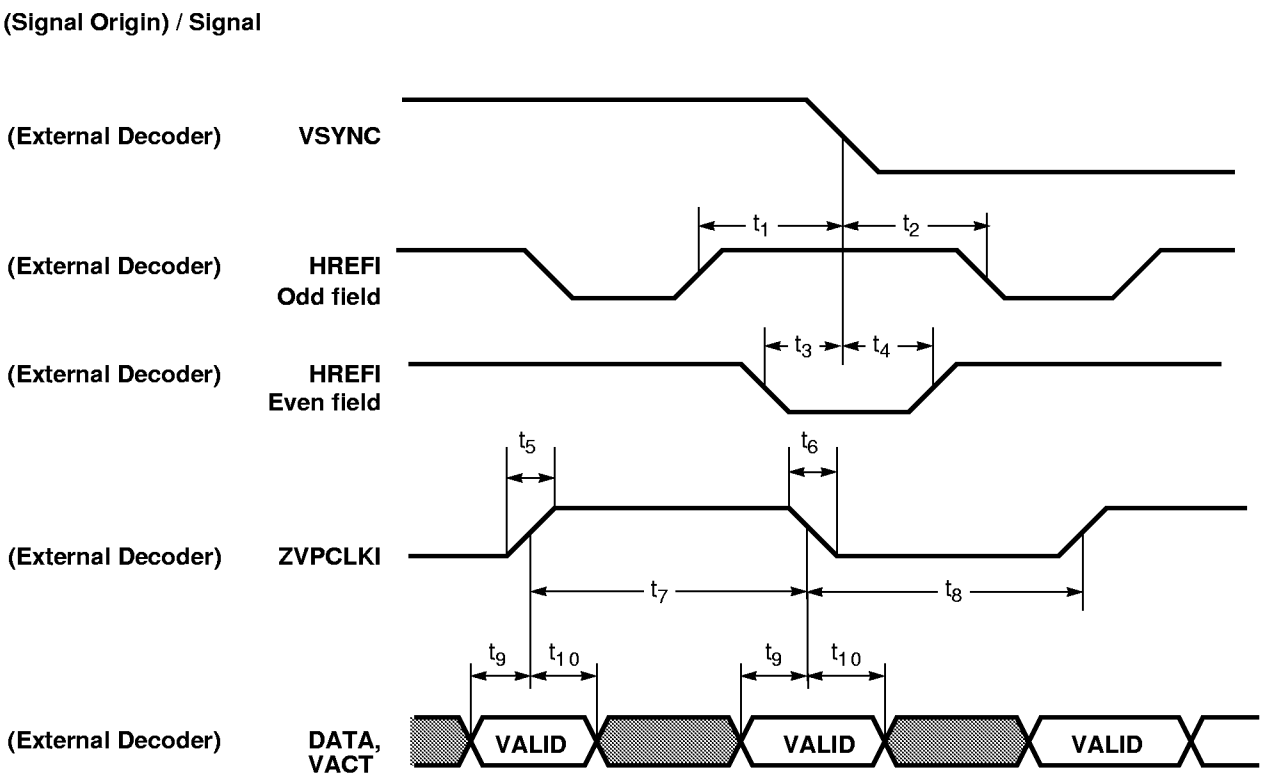


Figure 13-22. V-Port™ Timing

13.11 Frequency Synthesizer — Input Timing

The timing diagram in this section applies to the inputs to the frequency synthesizer. The nominal frequency of the frequency synthesizer is 14.318 MHz, and the nominal period is 69.84 ns.

Table 13-23. Input Timing — Frequency Synthesizer (14.318 MHz)

Symbol	Parameter	3.3 V		5.0 V	
		MIN	MAX	MIN	MAX
t_1	Input clock rise time	1 ns	7 ns	1 ns	7 ns
t_2	Input clock fall time	1 ns	7 ns	1 ns	7 ns
t_3	Input clock low period	$[t_5 \div 2]$ – 10% (t_5)	$[t_5 \div 2]$ + 10% (t_5)	t_5 – 10% (t_5)	t_5 + 10% (t_5)
t_4	Input clock high period	$[t_5 \div 2]$ – 10% (t_5)	$[t_5 \div 2]$ + 10% (t_5)	t_5 – 10% (t_5)	t_5 + 10% (t_5)
t_5	Input clock period	69.84 ns – [0.1% of 69.84 ns] = 69.77 ns	69.84 ns + [0.1% of 69.84 ns] = 69.9 ns	69.84 ns – [0.1% of 69.84 ns] = 69.77 ns	69.84 ns + [0.1% of 69.84 ns] = 69.9 ns
V_{IH}	Input high voltage	2.0 V	Vcc	2.0 V	Vcc
V_{IL}	Input low voltage	GND	0.5 V	GND	0.8 V

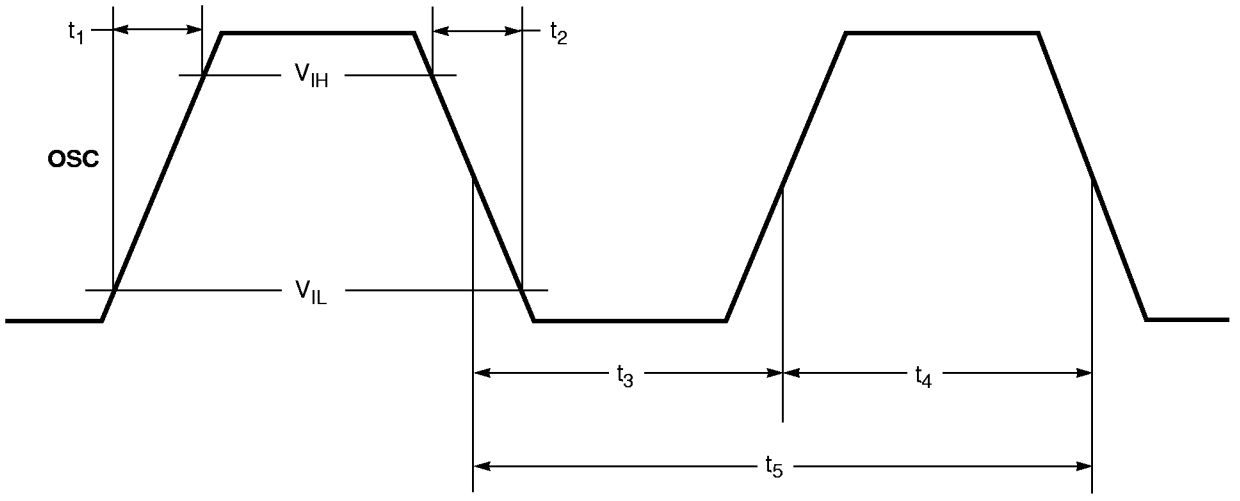
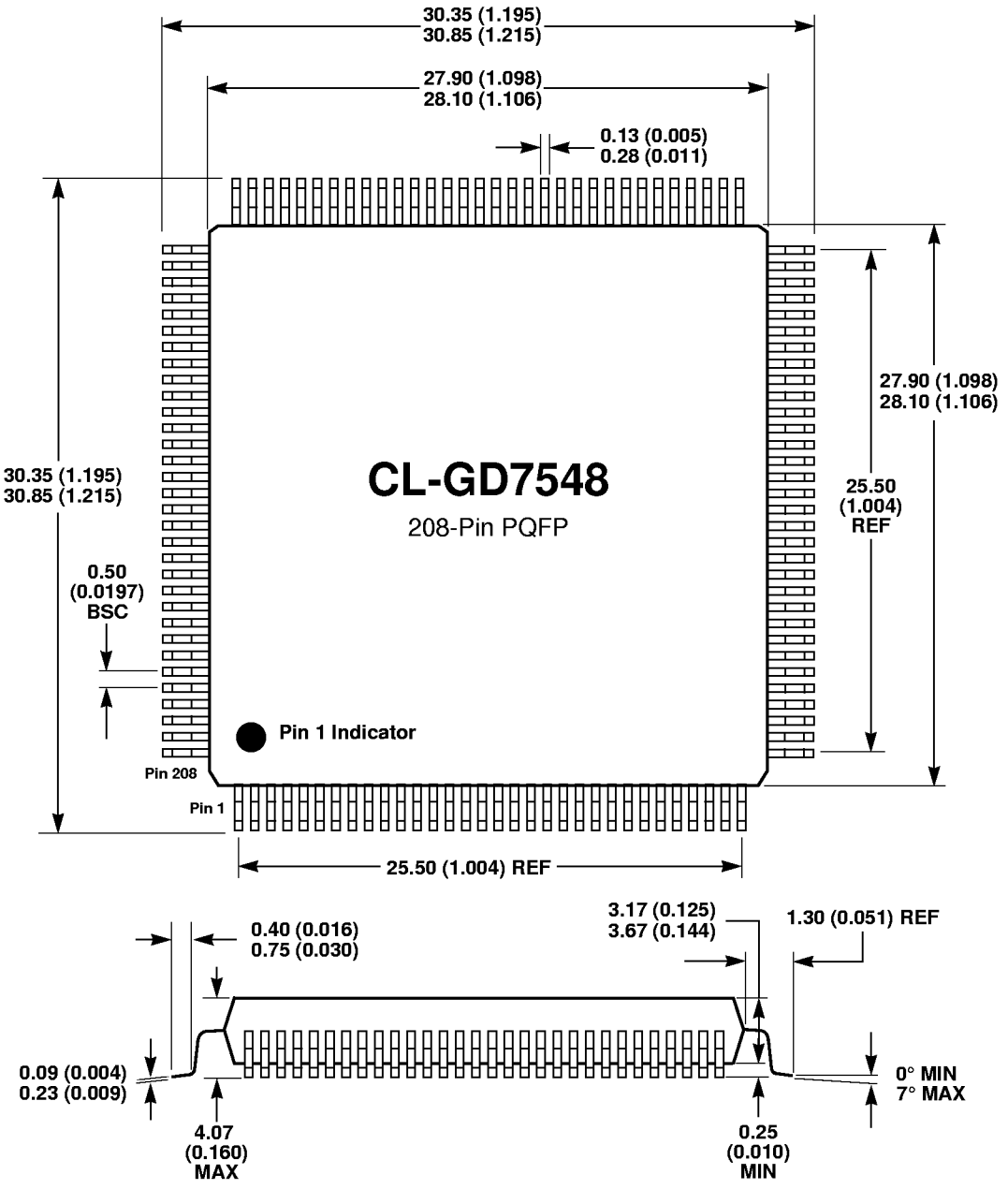


Figure 13-23. Frequency Synthesizer — Input Timing

14. PACKAGE SPECIFICATIONS

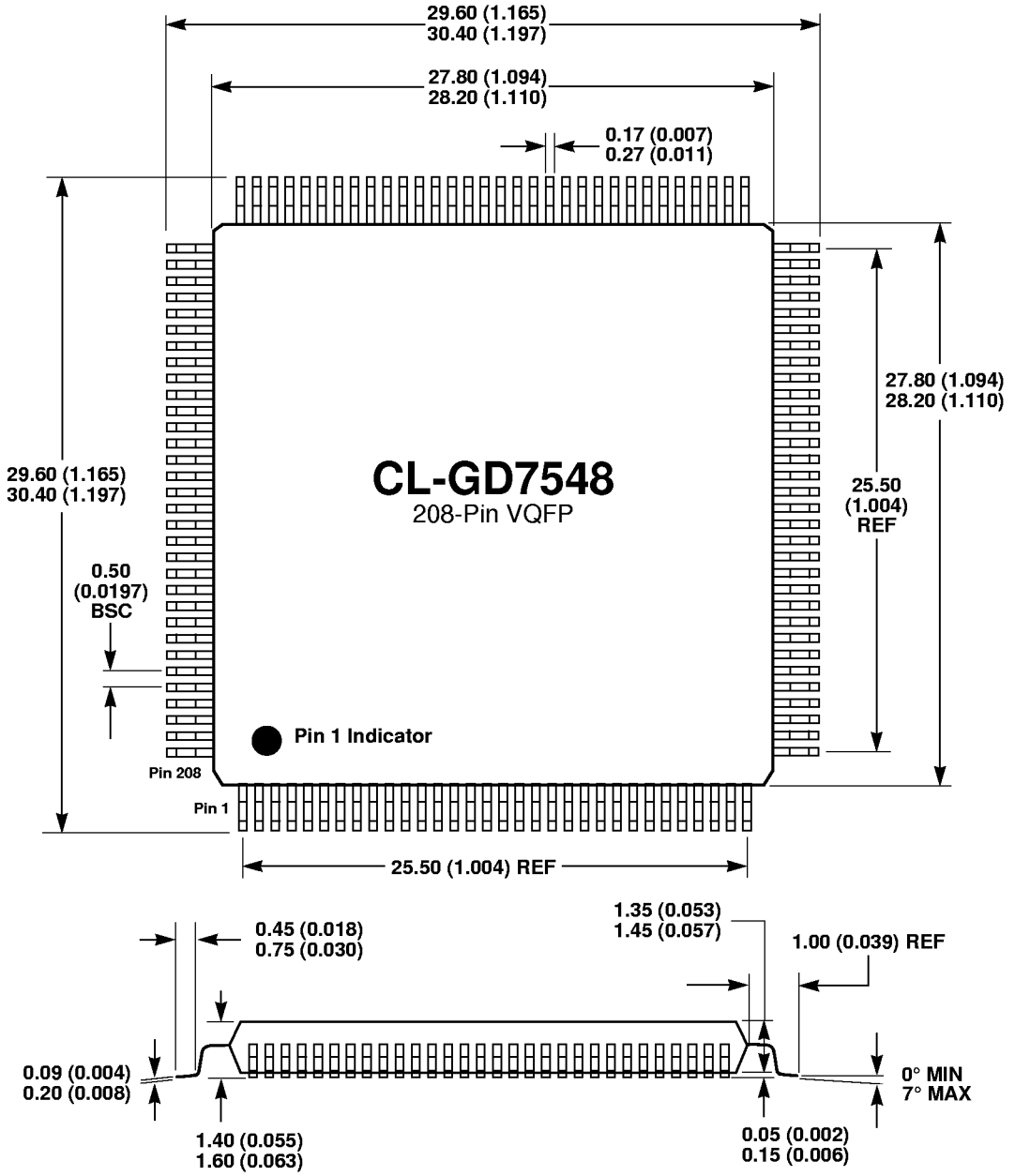
14.1 Plastic Quad Flat-Package (PQFP) Dimensions



NOTES:

1) Dimensions are in millimeters (inches), and the controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

14.2 Very-thin Plastic Quad Flat-Package (VQFP) Dimensions



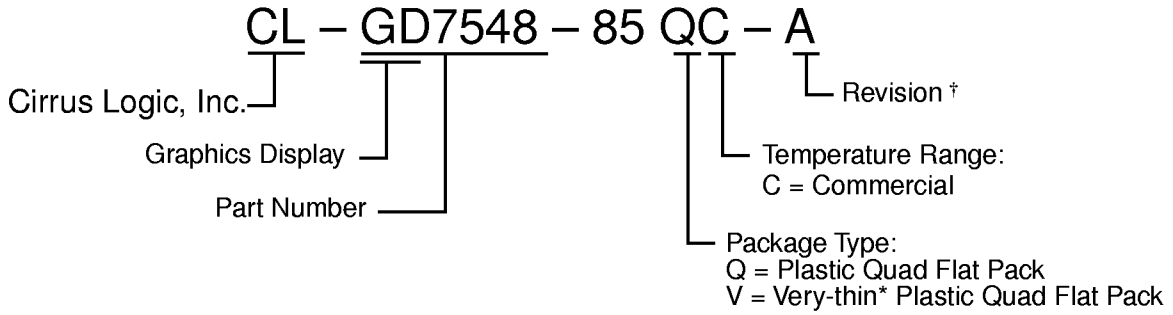
NOTES:

4) Dimensions are in millimeters (inches), and the controlling dimension is millimeter.

5) Drawing above does not reflect exact package pin count.

6) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.

15. ORDERING INFORMATION EXAMPLE



† Contact Cirrus Logic for up-to-date information on revisions.
*V = Very-tight-pitch in Cirrus Logic Package Information Guide

Appendix A

BitBLT Engine

A.1 Introduction

BitBLT (bit block transfer) is an operation in which data can be copied:

- From one area of display memory to either of the following:
  - — Another area of display memory
  - — An area of system memory
- From one area of system memory to an area of display memory

NOTE: Data cannot be copied from one area of system memory to another area of system memory.

The CL-GD7548 BitBLT engine moves data bytes from the source area to the destination area, and it performs 16 logical raster operations to combine the source bytes with the destination bytes. In addition, it can expand a monochrome image into a color image and replicate a single 8-pixel × 8-pixel pattern to fill a large area. These operations are done with minimum CPU intervention.

A.2 BitBLT Definitions

A.2.1 BitBLT Source Area

The BitBLT source area is the area from which data are copied. The source area is never written to except in those special cases in which both the source area and the destination area overlap in display memory. The BitBLT source area has the following characteristics:

- Located either in display memory or system memory, depending on the source area address
- Can be a monochrome image which is expanded into a color image
- Can be a single 8-pixel-by-8-pixel pattern that is replicated to fill a larger area

A.2.2 BitBLT Destination Area

The BitBLT destination area is the area into which data are written. The destination area can be in either display memory or system memory.

A.2.3 BitBLT Width

For an illustration and explanation of the BitBLT width, refer to Table A-1 and Figure A-1.

- The BitBLT 'width' refers to the number of bytes (not pixels) in the destination area that are processed before adding BitBLT pitch values to the address values.
- The 11-bit BitBLT width is specified in Extension register pair GR20/GR21 and has a maximum width of 2048 bytes.
- The number written into this register pair is 1 byte less than the actual desired width.

Table A-1. BitBLT Width

Source Area Conditions	Destination Area Conditions	Other Conditions	Resulting BitBLT Width
Source area is a rasterized area that is displayed on the active display screen.	Destination area is a rasterized area that is displayed on the active display screen.	None.	BitBLT width is the number of bytes (not necessarily pixels) in each scanline.
Source area is a rasterized area that is displayed on the active display screen.	Destination area is off-screen or in system memory.	There is no pattern copy or color expansion.	BitBLT width is the number of bytes per scanline of the source.
Source area is not a rasterized area. (That is, instead, the source area is a non-rasterized, vector-based area that is off the display screen.)	Destination area is not a rasterized area. (That is, instead, the destination area is a non-rasterized, vector-based area that is off the display screen.)	None.	BitBLT width is the number of bytes processed before pitch values are added to the address values (that is, BitBLT width has no special meaning.).

A.2.4 BitBLT Height

For an illustration and explanation of the BitBLT height, refer to Table A-1 and Figure A-1.

- The BitBLT 'height' refers to the number of times the pitch values are added to the address values.
- The 10-bit BitBLT height is specified in the Extension register pair GR22/GR23 and has a maximum height of 1024 scanlines.
- The number written into this register pair is 1 scanline less than the actual desired height..

Table A-2. BitBLT Height

Source and Destination Area Conditions	Resulting BitBLT Height
Either the source area, or the destination area, or both are a rasterized area that is displayed on the active display screen.	BitBLT height is the number of scanlines in that area.
Both the source area and the destination area are off-screen.	BitBLT height is the number of times pitch values are added to the address values (that is, BitBLT height has no special meaning.) In this case, both width and height are two numbers that are multiplied together to define the number of bytes in the destination are.

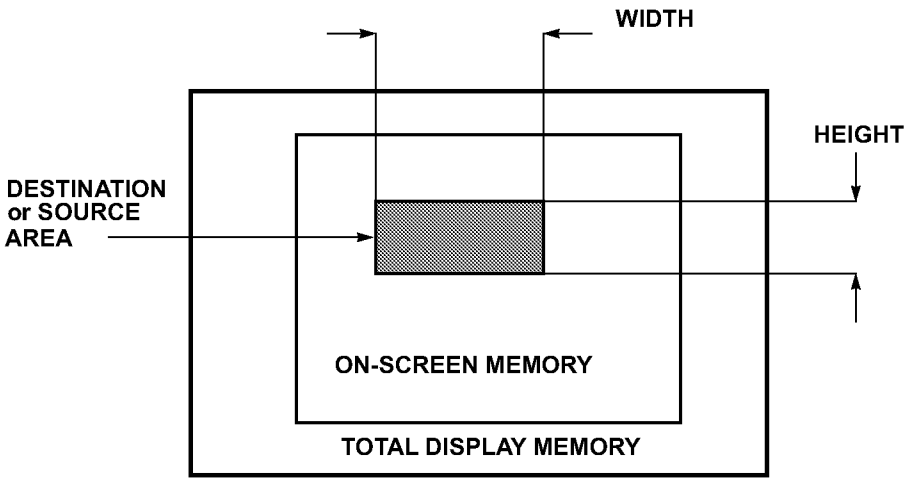


Figure A-1. Width and Height

A.2.5 BitBLT Source Pitch and Destination Pitch

After the bytes of each scanline in a destination area have been processed:

- The BitBLT 'source pitch' is a value added to the source area address.
- The BitBLT 'destination pitch' is a value added to the destination area address.

For the case of a rasterized image, refer to Figure A-3.

- When a source area or destination area is a rasterized image, the respective pitch is the number of bytes between vertically adjacent pixels. This value is the number of bytes between the (first) pixels of scanline 'n' and scanline 'n+1', that is, the number that is added to the area address to get from one scanline to the next.
- When a source area or destination area is in off-screen display memory, data pertaining to each of the scanlines are often stored in contiguous locations, which minimizes fragmentation. In this case, the respective pitch would be set equal to (width + 1).
- When an area is in system memory, the respective pitch is unused and is a 'don't care'.

When executing BitBLTs with pattern copy or color expansion, the source area is assumed to be linear, and the source pitch is a 'don't care'.

For the CL-GD7548, both register pairs are 12-bit values, allowing a pitch of 4095 bytes.

A.2.6 BitBLT Start

For an illustration of the BitBLT start, refer to Figure A-3. The BitBLT 'start' refers to the address of the first byte of a source area or destination area. This first byte is a byte offset from the beginning of display memory.

- The source area start address is specified in Extension register triplet GR2C/GR2D/GR2E.
- The destination area start address is specified in Extension register triplet GR28/GR29/GR2A.

Each start address is a 21-bit value, allowing up to 2 Mbytes of display memory. The destination-start address is shown in Figure A-3.

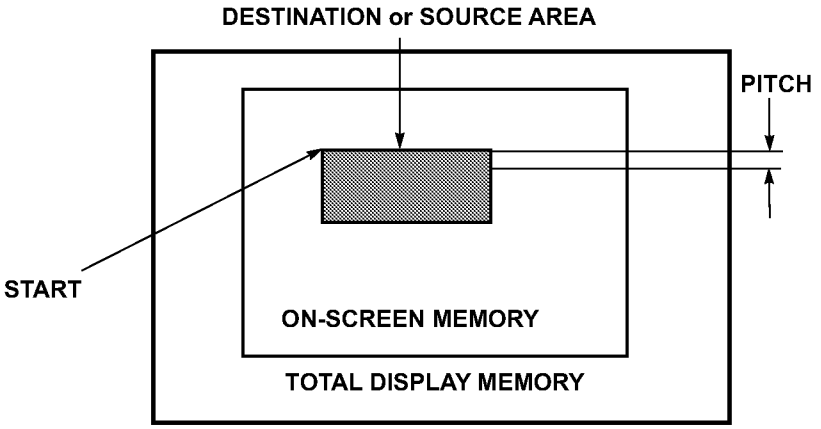


Figure A-2. Pitch and Start

A.3 BitBLT Display Memory-to-Display Memory Example

For a BitBLT operation that copies source data of 128 bytes × 64 scanlines from one area of display memory into another part of display memory, Table A-3 shows how the BitBLT registers must be programmed.

In this example, the CL-GD7548 is assumed to be programmed in display mode 65h (that is, 800 × 600, 16 bits per pixel). Therefore, each 128-byte scanline represents 64 pixels. The source area of this operation begins at address 0. The destination area begins at 160,200 (that is, 100 scanlines from the top of the screen, and 100 pixels from the left edge).

Table A-3. Typical Register Settings for Source Copy BitBLT Operation

Field	Graphics Controller Registers	Extension Registers	Field Contents	How Field Contents Are Calculated
Background Color	GR0	GR10	'Don't care'	Not applicable
Foreground Color	GR1	GR11	'Don't care'	Not applicable
Width		GR20, GR21	127	(64 pixels × 2) – 1 pixel = 127 pixels
Height		GR22, GR23	63	64 scanlines – 1 scanline = 63 scanlines
Destination Pitch		GR24, GR25	1,600	800 pixels × 2 bytes/pixel = 1600 bytes
Source Pitch		GR26, GR27	1,600	800 pixels × 2 bytes/pixel = 1600 bytes
Destination Start		GR28, GR29, GR2A	160,200	(100 scanlines × 1600 bytes/scanline) + (100 pixels × 2 bytes/pixel) = 160,200 bytes
Source Start		GR2C, GR2D, GR2E	0	(From the beginning of display memory)
BitBLT Mode		GR30	00 (hex)	From display screen to display screen. No color expansion. No pattern copy.
Start		GR31	02 (hex)	Set GR31[1] to 1.
Raster Operation		GR32	0D (hex)	Source copy

This BitBLT is executed as indicated in the following fragment of pseudo-code:

```
sourceAdrs = sourceStartAdrs;
destAdrs = destStartAdrs;
for (i = 0; i < Height; i++)                    /*For each scanline*/
    {
    workingSourceAdrs = sourceAdrs
    workingDestAdrs = destAdrs
    for (j =0; j < Width; j++)                  /*For each byte*/
         {
         Process one byte of Destination;
         workingDestAdrs++;                     /*to next byte*/
         workingSourceAdrs++;
         }
    sourceAdrs = sourceAdrs + sourcePitch; /*Next scanline*/
    destAdrs = destAdrs + destPitch;
    }
```

The BitBLT engine processes the bytes of a scanline in a destination area, incrementing temporary source and destination addresses after each byte of the scanline. Multiple scanline bytes are processed in parallel.

At the end of each scanline, the source pitch value is added to the source address as it was at the beginning of the scanline, and the destination pitch value is added to the destination address as it was at the beginning of the scanline. The BitBLT engine then moves on to the next scanline, and the process continues. This BitBLT loop iterates these additions (that is, the number of times the pitch values are added to the address values) until the specified height is reached.

All BitBLTs are processed in this general manner. However, some variations include the following:

- For color expansion, the source address is incremented as a bit address rather than as a byte address.
- Pattern fill occurs as explained in Section A.7.
- As discussed in Section A.8, when there is an overlap of the source area and the destination area, the BitBLT direction bit (that is, Extension register bit GR30[0]) must be set to 1 to decrement the source and destination addresses, which reverses the direction in which the BitBLT operation progresses.

A.4 Raster Operations

In addition to moving bytes from the source area to the destination area, the CL-GD7548 BitBLT engine can use logical ROPs (Raster OPerations) to combine either source bytes or pattern bytes with destination bytes. Also, the ROPs can be used to ignore bytes in the source area, the destination area, or both.

Table A-4 enumerates the 16 ROPs of Extension register GR32, for logically combining either a source bit (S) or a pattern bit (P) with a destination bit (D). Regardless of whether the ROP uses either a source bit or a pattern bit to combine with a destination bit, the same values of Extension register bits GR32[7:0] are used for the combinations.

The CL-GD7548 BitBLT engine directly implements all 16 ways of logically combining two operands. However, in the unusual cases for which three operands need to be combined, the CL-GD7548 BitBLT engine can use the operands of Table A-4 to synthesize an indirect way to logically combine the three operands.

Table A-4. Logical Combinations of Bits Using the BitBLT Engine

GR32[7:0] Setting (hex)	Resulting Source ROP: Source Bit Combined with Destination Bit	Microsoft® Name for Source ROP	Resulting Pattern ROP: Pattern Bit Combined with Destination Bit	Microsoft® Name for Pattern ROP
00	0	BLACKNESS 00000042	0	BLACKNESS 00000042
90	~S.~D	NOTSRCERASE 001100A6	~P.~D	– 000500A9
50	~S.D	– 00220326	~P.D	– 000A0329
D0	~S	NOTSRCCOPY 00330008	~P	– 000F0001
09	S.~D	SRCERASE 00440328	P.~D	– 00500325
0B	~D	DSTINVERT 00550009	~D	DSTINVERT 00550009
59	S~=D	SRCINVERT 00660046	P~=D	PATINVERT 005A0049
DA	~S+~D	– 007700E6	~P+~D	– 005F00E9
05	S.D	SRCAND 008800C6	P.D	– 00A000C9
95	S=D	– 00990066	P=D	– 00A50065
06	D	– 00AA0029	D	– 00AA0029
D6	~S+D	MERGEPAINT 00BB0226	~P+D	– 00AF0229
0D	S	SRCCOPY 00CC0020	S	PATCOPY 00F00021
AD	S+~D	– 00DD0228	P+~D	– 00F50225
6D	S+D	SRCPAINT 00EE0086	P+D	– 00FA0089
0E	1	WHITENESS 00FF0062	1	WHITENESS 00FF0062

A.5 BitBLT Color Expansion of Graphics Data

When Extension register bit GR30[7] is 1, the source input to the ROPS of Extension register GR32 is not actual data from the source area, but instead is data that has been color-expanded. Since the source area is a monochrome image that has a single bit per pixel, substantial performance benefits are possible, especially when the source image is expanded to 16 bits. Color expansion can be used when what appears in a destination is either of the following:

- A single foreground color by itself
- A single foreground color along with a single background color

The CL-GD7548 supports color expansion of data that is in either 8- or 16-bit-per-pixel display modes. The source can be monochrome data from either display memory or system memory. When the source data is in:

- Display memory, the starting address of the data must be located on a 4-byte boundary.
- A pattern of 8-pixels × 8-pixels, the starting address of the data must be on an 8-byte boundary.

When the data in the source area is a:

- 0, the result is the background color is written into corresponding byte(s) of the destination area. Also, no change takes place to the destination area (that is, the data written to the destination area is transparent).
- 1, the result is the foreground color is written into corresponding byte(s) of the destination area.

For color expansion, the destination must be in the display memory that is displayed and the direction must be incremental. Any ROP can be used, although SRCCOPY is most common when using color expansion.

The most-significant bit of the first source byte is expanded into the ROP source data for the first pixel of the destination. Depending on the contents of GR30[4], it is expanded to 1or 2 bytes. Table A-5 indicates the registers that contain the expansion colors.

Table A-5. Color Expansion Registers

GR30[4]	Width	Background Expansion (0 in Source Area)		Foreground Expansion (1 in Source Area)	
		GR0	GR10	GR1	GR11
0	8-bit	Color	Don't care	Color	Don't care
1	16-bit	Low byte	High byte	Low byte	High byte

The next bit of source data is processed for the next 1 or 2 bytes of destination, and so on, until the bytes of the scanline in the destination area have been processed. Unused source bits are discarded.

The destination address is modified by the destination pitch. The source pitch is ignored since the source is taken to be a linear string of bytes. The next byte of source is the first 8 pixels for the next scanline.

A.6 BitBLT Color Expansion of Graphics Data (with Transparency)

When GR30[3] is '1', a color expansion with transparency comparison is enabled. For each pixel, results of a ROP are compared to the contents of the Transparent Color registers (Extension registers GR34 and GR35). When the results are compared in all bit positions for which the Transparent Compare Mask registers (Extension registers GR38 and GR39) are 0, the results are *not* written to display memory. In 8 bits/pixel modes (that is, Extension register GR30[4] = '0'), registers GR34 and GR35 *must* be programmed identically, as must GR38 and GR39.

When color expansion is used with an opaque foreground and a transparent background (analogous to Extended Write mode 4), the transparency feature must be used, and the transparent color must be set to the background color. The registers used for foreground color expansion with transparency are the same as the color expansion registers with '1' in the source.

A.7 BitBLT Pattern Fills

The CL-GD7548 BitBLT engine has provisions for filling a destination area with a repeating pattern. The pattern fill size is 8 pixels × 8 pixels, chosen for compatibility with Microsoft Windows. Pattern fill replication can be done either with or without color expansion, as explained in Section A.5.

When Extension register bit GR30[6] is 1, data in the source area is defined as an array of 8 × 8 pixels. This source area data array is copied repeatedly to the destination area, with color expansion if necessary. For the same scanline, the same 8 pixels of source data are used repeatedly. The source pitch is ignored.

As indicated in Table A-6, the operating mode determines the number of data bytes in the source area pattern. The starting address boundary of a source pattern is equal to the number of bytes in the source pattern.

For pattern fill, the source address is incremented until the pattern fill completes and the address returns to the source start address, so that the pattern is used over and over.

Table A-6. Pattern-Fill Data Size

Operating Mode	Number of Data Bytes in Source Area Pattern	Starting Address Boundary
Color Expansion Enabled (That is, Extension registers GR30[7] = 1 *and* GR30[6] = 1.)	8 bytes of monochrome data for 64 pixels	8 bytes
8-bit pixels	64 bytes of color data for 64 pixels	64 bytes
16-bit pixels	128 bytes of color data for 64 pixels	128 bytes

A.8 BitBLT Direction

The direction of the progression of the BitBLT operation must be properly programmed when, as shown in Figure A-3, the source area and destination area overlap in display memory. In this situation, if a BitBLT operation were to start at the upper-left corner of the source and at the upper-left corner of the destination, then the source area data that is within the overlap area would be overwritten before being used.

To ensure that source area data are not overwritten prior to being used, Extension register bit GR30[0] must be set to 1. This setting decrements the source and destination addresses, which reverses the direction in which the BitBLT operation progresses. As a result, processing of data bytes for both the source and the destination starts at the lower-right corner, with data bytes processed right to left and bottom to top. This setting therefore guarantees that data bytes of the source are used prior to being changed. (With this setting, the start addresses in the source and destinations areas are the highest addressess, and not the lowest.)

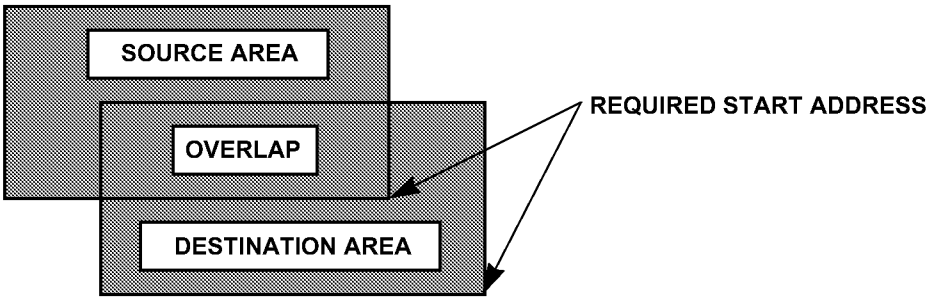


Figure A-3. Required Start Address When Source and Destination Area Overlap in Display Memory (Extension Register GR30[0] = 1)

A.9 BitBLT Source Area or Destination Area in System Memory

For a BitBLT, either the source area can be in system memory, or the destination area can be in system memory. However, the source area and the destination area cannot both be in the system memory at the same time.

If either the source area or the destination area of a BitBLT is in system memory, the host CPU must perform the transfers because the CL-GD7548 is never a bus master. For such transfers, the address provided by the host CPU is ignored (except the address must be in the range being decoded as display memory). The host CPU *must* execute double-word data transfers.

- When Extension register bit GR30[2] is a 1, the source of the BitBLT is system memory.
  - — For system memory-to-screen BitBLTs, up to 3 bytes of the last transfer for each scanline are ignored (depending on the width of the source and the destination areas). The next scanline begins with the next double-word transfer.
- When Extension register bit GR30[1] is a 1, the destination of the BitBLT is system memory.
  - — The CL-GD7548 pads each scanline with up to 3 indeterminate bytes (depending on the width of the source and the destination areas). BitBLTs involving color expansion or pattern copy cannot use this mode.

A.10 BitBLT Start and Reset Controls

Once the parameters have been loaded into the registers, the BitBLT can be started. It is also possible to unconditionally reset the BitBLT engine. These functions are controlled by bits in Extension register GR31.

A.10.1 BitBLT Start

To start a BitBLT, program Extension register bit GR31[1] to 1. As long as the BitBLT is in progress, bit GR31[0] is 1. When the BitBLT has completed, bit GR31[0] changes to 0.

Monitoring bit GR31[0] is the most straightforward way to synchronize the host CPU operation with the BitBLT engine. While the BitBLT is in progress, the CL-GD7548 display memory and BitBLT registers (except GR31) must not be accessed for read or write.

A.10.2 BitBLT Reset

To unconditionally stop the current operation and reset the entire BitBLT engine, program Extension register GR31[2] to 1, which forces bits GR31[3] and GR31[0] to 0 and stops the operation after the next write. This operation can result in partial pixels being written.

NOTE: A BitBLT operation that is reset *cannot* be resumed.

A.11 BitBLT Automatic Start

The CL-GD7548 has an automatic start capability for the BitBLT engine. By using double-buffering registers, the CL-GD7548 allows the parameters for BitBLT (*n + 1*) to be loaded while BitBLT *n* is taking place. Consequently, when BitBLT *n* completes, BitBLT (*n + 1*) can begin without host CPU intervention. As a result, this action allows for a high degree of parallelism between the host CPU and the CL-GD7548.

The automatic start for the BitBLT engine occurs as follows.

1. The automatic start is enabled by programming Extension register bit GR31[7] to a 1.
2. While bit GR31[7] is a 1, a BitBLT starts automatically when both of the following conditions are true:
   - The BitBLT engine is not busy.
   - A set of parameters, consisting of the BitBLT engine registers of Table A-7, is available. (A set of parameters is 'available' if, since the last time a BitBLT started, the destination address has been written and Extension register GR31[4] is a 0.)
3. To determine when the double-buffered registers are available to be loaded with a new set of parameters for the next BitBLT, the host CPU must monitor bit GR31[4] .
   - When bit GR31[4] is a 0, the double-buffered registers can be loaded. (To avoid starting a BitBLT with an incomplete set of parameters, the last address to be written must be the destination address of Extension registers GR28, GR29, and GR2A.)
   - Those registers that have not changed their contents from the previous set of parameters do not need to be rewritten.
4. When bit GR31[7] is programmed to a 0, the automatic start for the BitBLT engine is disabled. In this case, to start the BitBLT manually, bit GR31[1] must be set to 1.

A.12 Complete BitBLT Register Field Listing

Table A-7 lists every register associated with the BitBLT engine. Except for Extension register GR31, Sequencer register SR2, and the reserved registers, all registers in Table A-7 are double buffered.

Table A-7. Listing of BitBLT Enginer Register Fields

Location of BitBLT Register			Memory-Mapped I/O Offset for BitBLT (hex)	How BitBLT Register Is Used	BitBLT Register Size (bits)	Register Modified During BitBLT?
Sequencer Register	Graphics Controller Register	Extension Register				
	GR0		00	Background Color byte 0	8	No
	GR1		04	Foreground Color byte 0	8	No
		GR10	01	Background Color byte 1	8	No
		GR11	05	Foreground Color byte 1	8	No
		GR20	08	Width byte 0	8	–
		GR21	09	Width byte 1	3	–
		GR22	0A	Height byte 0	8	Yes
		GR23	0B	Height byte 1	2	Yes
		GR24	0C	Destination Pitch byte 0	8	No
		GR25	0D	Destination Pitch byte 1	4	No
		GR26	0E	Source Pitch byte 0	8	No
		GR27	0F	Source Pitch byte 1	4	No
		GR28	10	Destination Start byte 0	8	Yes
		GR29	11	Destination Start byte 1	8	Yes
		GR2A	12	Destination Start byte 2	5	Yes
		GR2B	13	Reserved	–	–
		GR2C	14	Source Start byte 0	8	Yes
		GR2D	15	Source Start byte 1	8	Yes
		GR2E	16	Source Start byte 2	5	Yes
		GR2F	17	Reserved	–	–
		GR30	18	BitBLT mode	8	No
		GR31	40	Start / Status	6	–
		GR32	1A	Raster Operation	8	No
		GR34	1C	Transparent Color byte 0	8	No
		GR35	1D	Transparent Color byte 1	8	No
		GR38	20	Transparent Color Mask byte 0	8	No
		GR39	21	Transparent Color Mask byte 1	8	No
SR2			–	Plane Mask	8	No

A.13 BitBLT Color Expansion of Text Data in Graphics Write Modes

With non-color-expanded graphics write modes, each individual character that makes up a text string is copied from system memory, and desired color attributes are applied to each individual character. The monochrome image of the text string is arranged in system memory by scanlines.

In contrast, with color-expanded graphics write modes, an entire text string is copied from system memory, and desired color attributes are applied to the entire string, resulting in faster text-write operations.

For example, assume a destination area is 150 pixels × 25 scanlines, with 8 bits per pixel, and the destination pitch is 1024 pixels. In this case, the registers must be programmed as indicated in Table A-8.

NOTES:

1) The following example shows register settings for a BitBLT operation that transfers data (which in this case, is a bitmap) from system memory to the display screen. In this case, after registers are programmed, data must be transferred from system memory by the host CPU.
   a) The first double-word write transfers the image for pixels 0 to 31.
   b) The second double-word write transfers the image for pixels 32 to 63.
   c) The third double-word transfers the image for pixels 64 to 95.
   d) The fourth double-word transfers the image for pixels 96 to 127.
   e) The data sent in the fifth double-word transfer is shown in Figure A-4
2) When background pixels are not to be written, Extension register GR30[3] must be set to '1'.

Table A-8. Typical Register Settings for Color Text Expansion

Field	Graphics Controller Registers	Extension Registers	Field Contents	How Field Contents Are Calculated
Background Color	GR0	GR10	'Don't care'	Not applicable
Foreground Color	GR1	GR11	'Don't care'	Not applicable
Width		GR20, GR21	149	150 pixels – 1 pixel = 149 pixels
Height		GR22, GR23	24	25 scanlines – 1 scanline = 24 scanlines
Destination Pitch		GR24, GR25	1024	Not applicable
Source Pitch		GR26, GR27	Not applicable	(System memory)
Destination Start		GR28, GR29, GR2A	'Don't care'	Not applicable
Source Start		GR2C, GR2D, GR2E	Not applicable	(System memory)
BitBLT Mode		GR30	84 (hex)	Color Expansion, Source = System memory
Start		GR31	02 (hex)	Set bit GR31[1] to 1
Raster Operation		GR32	0D (hex)	Source copy. (Refer to information on 0Dh in Table A-4.)

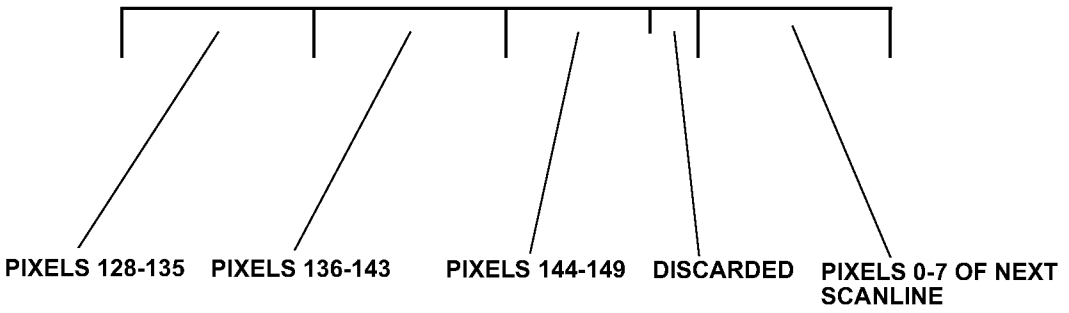


Figure A-4. Color Expand Transfer

A total of 119 double-word transfers are required. The last 1 byte of the last transfer is discarded.

Appendix B

Hardware Cursor

B.1 Introduction

The CL-GD7548 is capable of supporting a 32 × 32 or 64 × 64 hardware-driven cursor in either16-color planar display modes or in 256-, 32K-, or 64K-color packed-pixel graphics display modes.The hardware cursor (also called a 'mouse pointer') replaces a software mouse pointer commonly used by GUI (graphics user interface) applications. The hardware cursor eliminates the need for application software to save and restore the screen data as the on-screen cursor position changes.

After the application software initializes the hardware cursor, the application software needs only to update the cursor position (X,Y) to move the cursor on the screen. Compared to a software cursor, the hardware cursor offers a smooth-moving mouse pointer with improved performance.

B.2 Hardware Cursor Operation

Multiple hardware cursor patterns can be loaded in the top 8 Kbytes of display memory area. The number of cursor patterns that can be loaded in the display memory at one time is either 32 (for 32 × 32-bit cursors) or 8 (for 64 × 64-bit cursors). Of the cursor patterns that are loaded in display memory, application programs select one as the active cursor pattern by programming Extension register SR13.

Each pixel in the hardware cursor consists of 2 bits: bit 0 and bit 1. The following table shows how the 2 bits determine the displayed data of each hardware cursor pixel.

Table B-1. Hardware Cursor Bits

Bit 0	Bit 1	Displayed Data of Hardware Cursor Pixel
0	0	Transparent cursor pixel
0	1	VGA display data inverted
1	0	Cursor color 0
1	1	Cursor color 1

Cursor color 0 and Cursor color 1 are supplied by the CL-GD7548 internal palette DAC two extra LUT (Lookup Table) locations, which are mapped into the existing LUT indexes 00h and 0Fh, respectively. As a result, the hardware cursor colors are independent of the existing LUT indexes 00h through FFh.

Extension register SR12 can be programmed:

- To enable or disable the cursor (SR12[0])
- To enable access to the palette DAC cursor colors (SR12[1])
- To select the cursor size (SR12[2])
- To enable cursor movement (SR12[3])

The hardware cursor position is controlled by programming the hardware cursor horizontal (X) position and hardware cursor vertical (Y) position. The 11-bit cursor X-location and Y-location values are programmed by writing two 16-bit I/O writes each to:

- Sequencer register SRX (3C4h) and Extension register SR10 (3C5h), for the horizontal position
- Sequencer register SRX (3C4h) and Extension register SR11 (3C5h), for the vertical position

The SRX[4:0] bits of the Sequencer Index register are the index into the horizontal and vertical position registers. The SRX[7:5] bits of the Sequencer Index register are the least-significant 3 bits of the 11-bit (horizontal or vertical) value. The SR10[7:0] bits are the most-significant 8 bits of the 11-bit horizontal value, and the SR11[7:0] bits are the most-significant 8 bits of the 11-bit vertical value.

Moving the cursor always requires writing to both the horizontal and vertical position registers. The horizontal position is written first, but it does not take effect until the vertical position is updated.

NOTE: For expanded graphics display modes (for example, if a 640 × 480 graphics display mode is expanded for use on an 800 × 600, or if an expanded graphics display mode uses 10-dot character clocks) an additional bit in Extension register bit SR2E[0] must be used to control the fine horizontal position of the hardware cursor. This SR2E[0] bit is appended to Sequencer register index bits SRX[7:5].

For standard non-expanded graphics display modes, Extension register bit SR2E[0] is always cleared to 0 and can be ignored when moving the hardware cursor.

The following table shows CL-GD7548 registers that must be programmed for the hardware cursor:

Table B-2. Registers for Programming Hardware Cursor

To:	Program:			
	Register	I/O Port Address	Register Bits	Value
Enable the hardware cursor	SR12	3C5h	[0]	1
Enable CPU access to DAC extended colors	SR12	3C5h	[1]	1
Select a hardware cursor size of 32 × 32[a]	SR12	3C5h	[2]	0
Select a hardware cursor size of 64 × 64[a]	SR12	3C5h	[2]	1
Enable hardware cursor movement	SR12	3C5h	[3]	0
Select a hardware cursor pattern of 32 × 32	SR13	3C5h	[4:0]	31...0
Select a hardware cursor pattern of 64 × 64	SR13	3C5h	[4:2]	7...0
Select the hardware cursor horizontal position	SRX / SR10, 30, 50, 70, 90, B0, D0, F0	3C4h / 3C5h	[7:5] / [7:0]	2047...0
Select the hardware cursor horizontal position fine-position extension (most-significant bit) for expanded graphics	SR2E	3C5h	[0]	0: Non-Expanded 1: Expanded
Select hardware cursor vertical position	SRX / SR11, 31, 51, 71, 91, B1, D1, F1	3C4h / 3C5h	[7:5] / [7:0]	2047...0
Enable a hardware cursor size of 32 × 32[a]	SR21	3C5h	[4]	0
Enable a hardware cursor size of 64 × 64[a]	SR21	3C5h	[4]	1

[a] Extension register bits SR12[2] and SR21[4] must both be programmed to the same binary value.

B.3 The 32 × 32 Hardware Cursor Pattern

Each 32 × 32 hardware cursor pattern requires 256 bytes (128 bytes per cursor pixel bit × 2 cursor pixel bits), which allows for 32 cursor patterns to be loaded into the upper 8 Kbytes of display memory. The hardware cursor pattern that is active is selected by programming Extension register bits SR13[4:0].

The 32 × 32 hardware cursor pattern data for cursor pixel bit 0 and cursor pixel bit 1 is stored into the display memory as shown in the following figure:

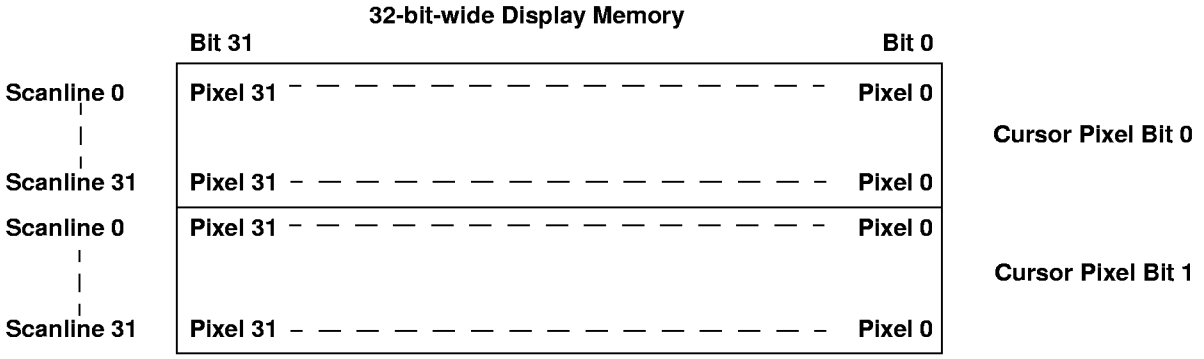


Figure B-1. Mapping of 32 × 32 Hardware Cursor

B.4 The 64 × 64 Hardware Cursor

Each 64 × 64 cursor pattern requires 1024 bytes (512 bytes per cursor pixel bit × 2 cursor pixel bits), which allows for 8 cursor patterns to be loaded into the upper 8 Kbytes of the display memory. The hardware cursor pattern that is active is selected by programming Extension register bits SR13[4:2].

The 64 × 64 hardware cursor pattern data from cursor pixel bit 0 and cursor pixel bit 1 is loaded into display memory one cursor scanline at a time. The same action occurs until all 64 scanlines from cursor pixel bit 0 and cursor pixel bit 1 are loaded into the system memory, as shown in the following figure:

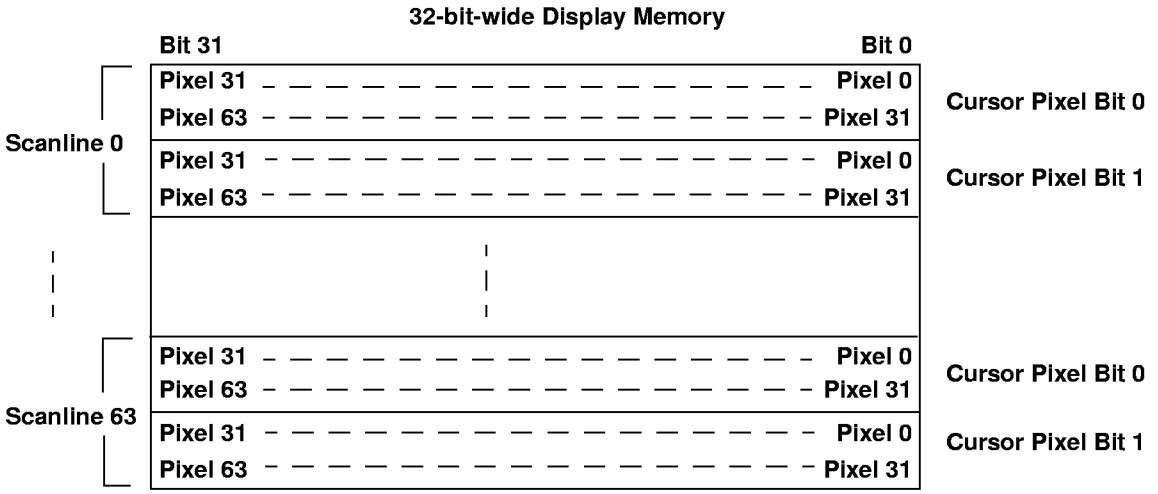


Figure B-2. Mapping of 64 × 64 Hardware Cursor

NOTE: To obtain proper 64 × 64 hardware cursor mapping, Extension register bit SR21[4] must be set to 1.

The following table shows the location of the hardware cursor memory map within the display memory.

Table B-3. Hardware Cursor Memory Map in 1-Mbyte Display Memory

Address	32 × 32 Hardware Cursor	64 × 64 Hardware Cursor
3FF00–3FFFF	Cursor Map #28 — Cursor Map #31	Cursor Map #7
3FE00–3FEFF	Cursor Map #24 — Cursor Map #27	Cursor Map #6
3FD00–3FDFF	Cursor Map #20 — Cursor Map #23	Cursor Map #5
3FC00–3FCFF	Cursor Map #16 — Cursor Map #19	Cursor Map #4
3FB00–3FBFF	Cursor Map #12 — Cursor Map #15	Cursor Map #3
3FA00–3FAFF	Cursor Map #8 — Cursor Map #11	Cursor Map #2
3F900–3F9FF	Cursor Map #4 — Cursor Map #7	Cursor Map #1
3F800–3F8FF	Cursor Map #0 — Cursor Map #3	Cursor Map #0

NOTE: For the 32 × 32 hardware cursor, four hardware cursor data patterns occupy 3Fx00 through 3FxFF. Their respective addresses (in which x = 8 – F) are:

3Fx00–3Fx3F
3Fx40–3Fx7F
3Fx80–3FxBF
3FxC0–3FxFF

The addresses in the table above assume that each location is 32 bits wide.

Appendix C

Hardware Icon

C.1 Introduction

A hardware icon (that is, a hardware-driven icon window), as compared to a software icon, eliminates the need for application software to save and restore the screen data as the icon position changes.

In various operational modes, the CL-GD7548 is capable of supporting four hardware icons with the following features:

- One to four icons displayed simultaneously on the screen.
- The default icon size of 64 × 64 pixels can be doubled vertically and/or horizontally to the following sizes:
  - 64 × 128 pixels
  - 128 × 64 pixels
  - 128 × 128 pixels
- Up to eight icon maps may be defined in display memory for use and are associated with the displayed icons in two ways:
  - Two icon maps are used for each hardware icon.
  - All eight icon maps are used with the first hardware icon.
- A single location, known as a 'hot spot', is used to define the screen position of all of the icons. The hot spot defines the upper left-hand corner of the first icon. All subsequent icons are left-aligned vertically down from the first icon. The hot spot is positioned at a resolution of one pixel.
- Each icon independently controls the following:
  - Display Enable
  - Display Mode: either 4-color display mode, or 3-colors-and-transparency display mode
  - Blink Enable: one-half the text cursor blink rate
  - Horizontal Pixel Doubling
  - Vertical Pixel Doubling
  - Memory Map Selection
- The hardware icons have the second-most display priority in the video sub-system. Only the hardware cursor appears on top of the hardware icon.

The hardware icon memory model and programming model are very similar in usage to that of the hardware cursor. The memory used to define the icon maps is located just below the hardware cursor area (which is at the top of the available display memory space), and the icon memory map is fixed by the CL-GD7548.

C.2 Hardware Icon Operation

The CL-GD7548 Video Data Path Control register (Extension register SR12), and Hardware Icon Control registers (Extension registers SR2A/SR2B/SR2C/SR2D) can be programmed for the following:

- To enable/disable the icon
- To select the icon size
- To enable access to the palette DAC icon colors
- To enable icon movement.

The hardware icon data is located in the bottom 8 Kbytes of the of the top 16 Kbytes of available display memory. The number of icon patterns that can be loaded in the display memory at one time is eight 64 × 64-bit icons (of which four can be simultaneously displayed). These patterns can be defined as either two patterns per icon, or all eight patterns can be displayed on the first icon, allowing all of the patterns to be displayed at the same location without having to update the icon hot spot.

C.2.1 Icon Color

Each hardware icon pixel consists of 2 bits, icon pixel bit 0 and icon pixel bit 1. Table C-1 shows how these 2 bits determine the displayed state of each icon pixel.

Table C-1. Hardware Icon Pixel Bits

Icon Pixel Bit 0	Icon Pixel Bit 1	Displayed Data of Hardware Icon Pixel
0	0	Icon color 0 (Transparent)
0	1	Icon color 1
1	0	Icon color 2
1	1	Icon color 3

The icon colors 0 and 3 are supplied by the internal palette DAC's four extra lookup table (LUT) locations, which are mapped into the existing LUT indexes 03h, 04h, 05h, and 06h, respectively. As a result, the hardware cursor colors are independent of the existing LUT indexes 00h through FFh.

- When Extension register SR12[1] is set to '1', these four additional palette locations are enabled and are accessible the same way as their standard VGA counterparts.
- Clearing Extension register SR12[1] to '0' restores standard VGA operation to the palette locations.

C.2.2 Icon Position

The hardware icon position is controlled by programming the Graphics Icon Horizontal (X) position and Graphics Icon Vertical (Y) position. The position of the hardware icon is programmed in the same way as for the hardware cursor, using the same I/O addresses. The CL-GD7548 distinguishes the difference between the two operations by the state of Extension register bit SR12[3].

- When SR12 [3] = '0', writing X and Y position data controls the position of the hardware cursor.
- When SR12 [3] = '1', writing X and Y position data controls the position of the hot spot of the hardware icons.

The 11-bit icon X-and Y-location values are programmed by initiating two 16-bit I/O writes to:

- SRX (3C4h) and SR10 (3C5h): Horizontal position
- SRX (3C4h) and SR11 (3C5h): Vertical position

where SRX[7:5] of the Index register are the least-significant bits of the 11-bit value, and SRX[4:0] is the index into the horizontal and vertical position registers. Moving the icon always requires writing to both the horizontal and vertical position registers. The horizontal position is written first, but it does not take effect until the vertical position is updated.

NOTE: The horizontal fine-position control requires one more bit for those expanded graphics display modes that use 10-dot character clocks. For these special cases (for example, 640 × 480 graphics expanded for 800 × 600 panels), the most-significant bit for the fine-position adjustment is in SR2A[6], which is appended to the index bits SRX[7:5]. For standard non-expanded graphics display modes, SR2A[6] is always '0' and can be ignored when moving the icon.

Figure C-1 shows the hot spot and vertical alignment of the icons as they appear on the display.

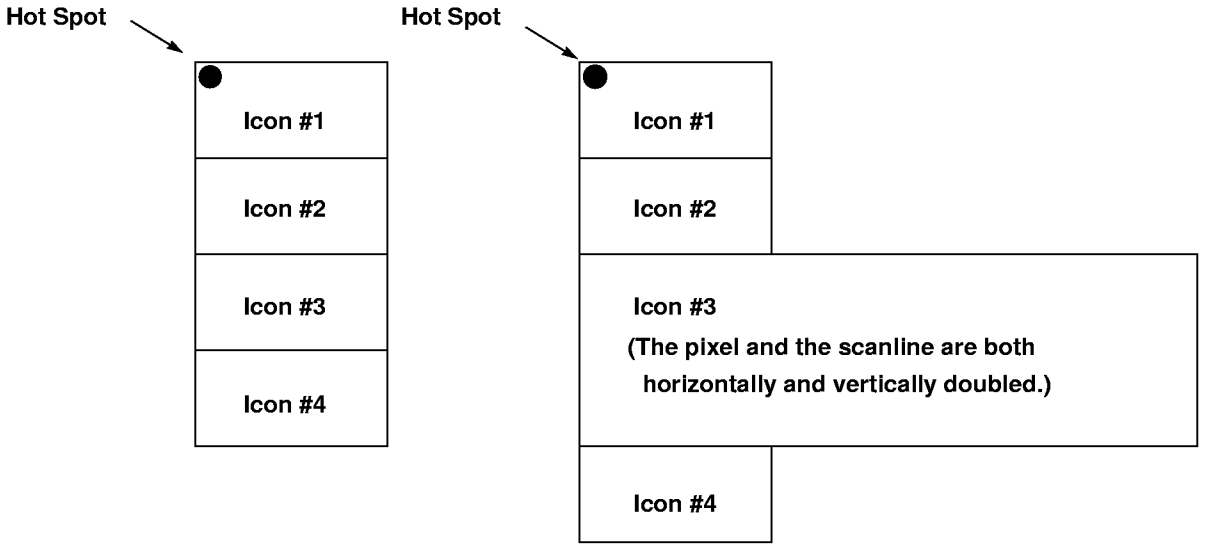


Figure C-1. Hot Spot and Vertical Alignment of the Icons

Table C-2 shows the CL-GD7548 Extension register bits for programming the hardware icon.

Table C-2. Extension Register Bits for Programming Hardware Icon

To:	Program:			
	Register	I/O Port Address	Register Bits	Value
Enable hardware icon	SR2x[a]	3C5h	[0]	1
Display 3-colors-and-transparency display modes	SR2x[a]	3C5h	[1]	1
Display 4-color display modes	SR2x[a]	3C5h	[1]	0
Enable blink	SR2x[a]	3C5h	[2]	1
Double horizontal pixel	SR2x[a]	3C5h	[3]	1
Double vertical scanline	SR2x[a]	3C5h	[4]	1
Select memory map	SR2x[a]	3C5h	[5]	0 or 1
Select icon #0 eight memory maps option	SR2E	3C5h	[2:1]	11, 10, 01, 00
Set hardware icon horizontal position[b]	SRX/SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]/[7:0]	2047...0
Set icon horizontal position fine-position extension (most-significant bit) for expanded graphics	SR2A	3C5h	[6]	0: Non-Expanded 1: Expanded
Set hardware icon vertical position[b]	SRX/SR11, 31, 51, 71, 91, B1, D1, F1	3C4h / 3C5h	[7:5] / [7:0]	2047...0

[a] The x represents the four available icon programming registers; 2Ah, 2Bh, 2Ch, and 2Dh, which correspond to the four hardware icons of the CL-GD7548.

[b] The icon position is programmed the same way as the hardware cursor, using the same I/O addresses. The state of SR12[3] determines whether the icon position or the cursor position are to be updated.

C.2.3 Memory Map Option

According to the setting of Extension register SR2E[2:1], the eight CL-GD7548 icon maps can be configured in two ways:

- Two maps per icon
- All eight maps available to icon #0

Extension register SR2E[2:1] controls this configuration option as follows:

- When this field is zero, the corresponding map pair that is displayed is icon #0.
- When this field is non-zero:
  - — Only icon #0 can be used, and it has accesses to all eight memory maps. The non-zero number points to the corresponding map pair that is displayed as icon #0.
  - — Icons #1, #2, and #3 must be disabled.

The member of the map pair that is actually displayed is selected by the state of SR2A[5]. For example, if SR2E[2:1] = '11' and SR2A[5] = '0', then map #6 is displayed as icon #0. For memory map details, refer to Table C-3.

C.3 Hardware Icon Memory Map and Data Format

Table C-3 shows the location of the hardware icon memory maps within the display memory.

Table C-3. Hardware Icon Memory Map in 1-Mbyte Display Memory

Address	Hardware Icon Memory Map
3F700–3F7FF	Icon #3 Map #1 or Icon #0 Map #7
3F600–3F6FF	Icon #3 Map #0 or Icon #0 Map #6
3F500–3F5FF	Icon #2 Map #1 or Icon #0 Map #5
3F400–3F4FF	Icon #2 Map #0 or Icon #0 Map #4
3F300–3F3FF	Icon #1 Map #1 or Icon #0 Map #3
3F200–3F2FF	Icon #1 Map #0 or Icon #0 Map #2
3F100–3F1FF	Icon #0 Map #1
3F000–3F0FF	Icon #0 Map #0

NOTE: The above addresses assume each location is 32 bits wide.

The actual data that is stored in display memory to define the icon is written with two bits of data per pixel, as defined in Section C.2.1. The following figure shows how the 64-pixel-by-64-pixel icon is stored in 32-bit-wide display memory.

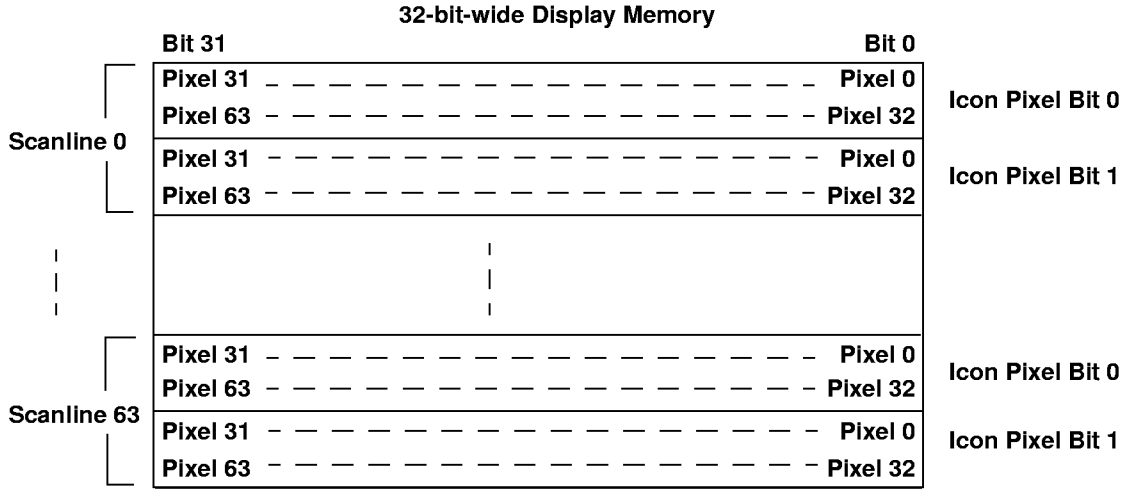


Figure C-2. Icon (64 Pixels × 64 Pixels) Stored in the Display Memory

Appendix D

Color Expansion and Extended Write Modes

D.1 Introduction

The CL-GD7548 supports color expansion, which uses extended write modes for faster CPU write performance. In graphics modes, Extended Write modes can be used for the following operations: faster text write, pattern fill, and block move operations. In 8- or 16-bit-per-pixel graphics modes with packed-pixel addressing, these Extended Write modes operate on 8 pixels at a time.

D.2 Color Expansion

Color expansion is the automatic conversion of a monochrome bitmap, typically defining a character, icon, or pattern into foreground and background color values that are written into display memory. The foreground and background color values are held in the CL-GD7548, and only the monochrome bit maps need to be transmitted across the bus. Each bit of the monochrome map is converted into an 8-bit or 16-bit pixel value: The bus traffic is reduced accordingly.

D.3 Registers Involved in Color Expansion

The following registers are involved in color expansion.

Table D-1. Color Expansion Registers

Register Bit	Function
SR2[7:0]	Enable writing pixels
GRB[2]	'1' enables Extended Write modes
GRB[4]	'1' enhances Extended Write modes to 16-bit pixels
GR5[2:0]	'100' chooses Extended Write mode 4 '101' chooses Extended Write mode 5
GR0[7:0]	Extended Write mode 5, background-color low byte
GR1[7:0]	Extended Write mode 4/5, foreground-color low byte
GR10[7:0]	Extended Write mode 5, background-color high byte
GR11[7:0]	Extended Write mode 4/5, foreground-color high byte

D.4 Extended Write Modes

The CL-GD7548 supports two extended write modes: Extended Write modes 4 and 5. These extended write modes can selectively update up to 8 pixels of 8 or 16 bits each. For more information, refer to Section D.8 and Section D.9.

Extension register GRB, the Graphics Controller Mode Extensions register, bits [4:1] are used in combination to enable the CL-GD7548 Extended Write modes.

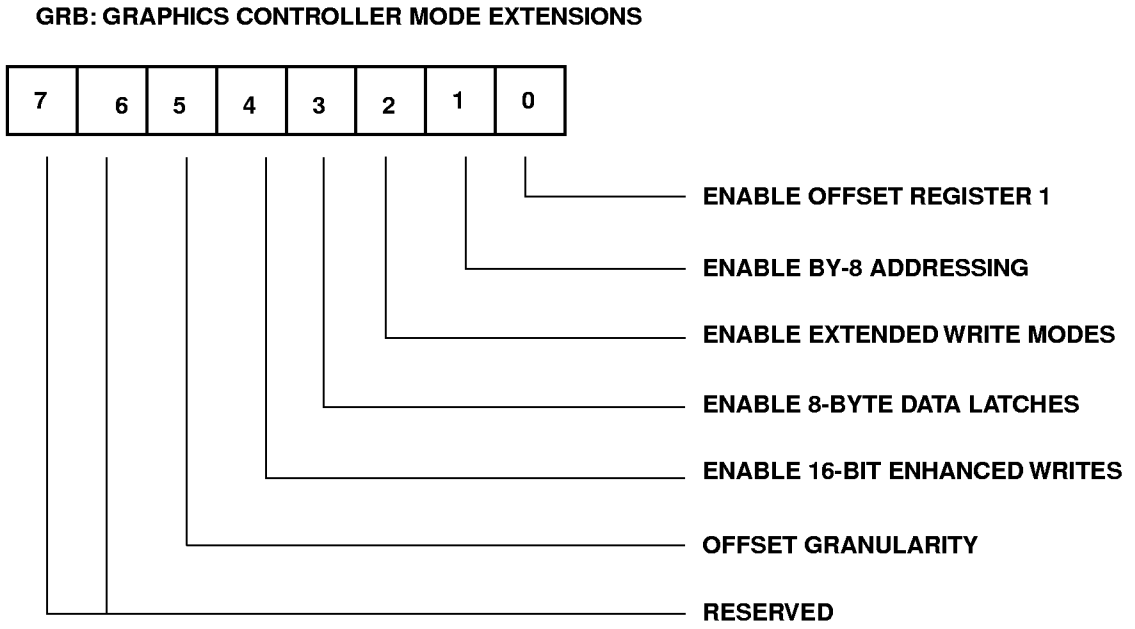


Figure D-1. Extension Register GRB

When Extended Write modes are enabled by setting GRB[2] to '1':

- Up to 8 bytes can be transferred to display memory for every CPU byte transfer.
- Graphics Controller register GR0[7:0] extends read/write values for Extended Write mode 5, the background color.
- Graphics Controller register GR1[7:0] extends read/write values for Write mode 4/5, the foreground color.
- Graphics Controller register GR5[2] is enabled to select Extended Write modes 4 and 5.
- Graphics Controller register GRB[4] is enabled to select enhanced writes for Write modes 4 and 5.
- Sequencer register SR2[3:0] extends to SR2[7:0] for Write modes 4 and 5.

D.5 By-8 Addressing

GRB[1], when set to '1', selects By-8 addressing for 8-bit-per-pixel (256-color) graphics modes. The system address is shifted left by 3 bits relative to packed-pixel addressing so that each system byte address points to a different 8-pixel (8 bytes) block in display memory.

This GRB[1] bit, in combination with GRB[2], is used for selecting Extended Write modes. This bit is a 'don't care' when GRB[4] is '1'.

D.6 By-16 Addressing

GRB[4], in combination with GRB[2], is used to select Write mode 4 and 5 for 16-bits-per-pixel graphics modes (RGB 555 or 565). The system address is shifted left by 4 bits relative to packed-pixel addressing so each system byte address points to a different 8 pixels (16-byte block) in display memory. GRB[4] and GRB[2], when set to '1', select the following Write mode operation:

- Enables By-16 addressing.
- Enables up to 16 bytes (8 pixels) to be transferred for each CPU byte cycle.
- Enables GR10 and GR11 as high-byte data for foreground and background color extensions. (GR0 and GR1 contain the low-byte data.)
- Enables each bit of SR2 to be used as pixel write mask for 2 bytes.

D.7 Data Latches

When GRB[3] is set to '1', the memory read latches are 8 bytes wide, instead of the normal 4. Eight-byte-wide memory read latches can be used in Write mode 1 to write 8 latched bytes back into display memory. This action allows either 8 pixels in 256-color modes or 4 pixels in 16-bits-per-pixel modes to be updated in a single CPU byte cycle.

D.8 Extended Write Mode 4

The CL-GD7548 supports Extended Write mode 4, which is used in combination with By-8 or By-16 addressing modes to operate on 8 pixels of data at a time (8 or 16 bytes, depending on 8- or 16-bit-per-pixel mode).

- In 8-bits-per-pixel mode:
  - — The Foreground Color bits GR1[7:0] are used to update each pixel byte in display memory.
  - — The 8-bit value is written as the foreground color when the corresponding CPU data is a '1', and the corresponding Map Mask register bit in SR2 is also set to a '1'.
  - — When the CPU Data bit is a '0', the corresponding pixel in display memory is not changed by the write.
- In 16-bits-per-pixel mode:
  - — The Foreground Color register bits GR11[7:0] (foreground-color high byte) and GR1[7:0] (foreground-color low byte) are used to update each pixel word in display memory.
  - — When the corresponding CPU data is '1' and the corresponding Map Mask register bit in SR2 is also '1', the 16-bit value is written as the foreground color.
  - — When the CPU Data bit is '0', the corresponding pixel in display memory is not changed by the write.

This mode, for example, can be used to write text to display memory with the foreground color while preserving the background color. This action allows 8 pixels of display data to be updated with a single CPU byte cycle.

D.9 Extended Write Mode 5

The CL-GD7548 supports Write mode 5, which is used in combination with By-8 or By-16 addressing mode to operate on 8 pixels of data at a time (8 or 16 bytes, based on 8- or 16-bit-per-pixel mode). This mode can be used to write text to display memory with a selected foreground color and a background color. This action allows 8 pixels of display data to be updated with a single CPU byte cycle.

- In 8-bit-per-pixel mode:
  - — The Foreground Color bits GR1[7:0] or the Background Color bits GR0[7:0] are used to update each pixel byte in display memory.
  - — When the corresponding CPU data bit is '1', the 8-bit value is written as the foreground color.
  - — When the corresponding CPU data bit is '0', the corresponding pixel in display memory is written with the background color.
  - — The corresponding Map-Mask register, SR2[7:0], also inhibits writes to selected pixel in display memory.
- In 16-bit-per-pixel mode:
  - — The Foreground-Color bits GR11[7:0] (foreground-color high byte) and GR1[7:0] (foreground-color low byte), or the Background Color bits GR10[7:0] (background-color high byte) and GR0[7:0] (background-color low byte), are used to update each pixel word in display memory.
  - — When the corresponding CPU data is '1', the 16-bit value is written with the foreground color.
  - — When the corresponding CPU data bit is '0', the corresponding pixel in display memory is written with the background color.
  - — The corresponding Map-Mask register, SR2[7:0], also inhibits the corresponding pixel value (2 bytes) to be written to display memory.

Appendix E

True-Color Modes

E.1 Introduction

The CL-GD7548 has a built-in true-color multi-mode palette DAC that supports the following modes:

- 8 bits per pixel (VGA-standard 256-Color Palette mode)
- 15 bits per pixel (32K color, the RGB 5-5-5 mode)
- 16 bits per pixel (64K color, the RGB 5-6-5 XGA™ mode)
- 24 bits per pixel (16.8-million color, the RGB 8-8-8 True-Color mode)

In the 256-Color Palette mode, the palette DAC is VGA-compatible and provides 256 simultaneous colors from a palette of 256K on the display screen.

E.2 Programming for a True-Color Multi-Mode Palette DAC

Extended Color modes are enabled by the Hidden DAC register (Extension register HDR at I/O Port 3C6h). At reset, the HDR is loaded with 00h, which programs the palette DAC in a VGA-compatible mode. In this mode, the palette DAC is functionally equivalent to the industry-standard Brooktree® BT476 RAM-DAC. By writing code to the HDR, the palette DAC can be programmed in one of the modes mentioned above. The following method is used to write to the HDR:

1. Read from the Pixel-Mask register (3C6h) four times in succession.

   No other reads/writes must be directed to that address. After the fourth read, the Pixel-Mask register points to the HDR.

2. Program the HDR by writing to it at Port 3C6h.

   Any read from or write to any address (other than the Pixel-Mask register) resets an internal counter, which 'hides' the HDR again. To continue, repeat Step 1.

Table E-1. Extended Color Mode Selected with the Hidden DAC Register

HDR								Function
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0	X	X	X	X	X	X	X	Standard VGA-compatible 256-color mode
1	1	1/0	0	0	0	0	0	RGB 5-5-5 mode (32K colors)
1	1	1/0	1	0	0	0	0	Reserved (RGB 5-5-5 and 256-Color Mix mode)
1	1	1/0	0	0	0	0	1	RGB 5-6-5 mode (64K colors, XGA™)
1	1	X	0	0	1	0	1	RGB 8-8-8 mode (16.8-million color, True-Color mode)

NOTE: In RGB 5-5-5 mode, programming HDR[5] to '0' chooses Clocking mode 1 and programming HDR[5] to '1' chooses Clocking mode 2. When using a video overlay feature of the CL-GD7548, choose Clocking mode 1.

E.2.1 RGB 5-5-5 Mode with 32K Colors

This mode supports the industry-standard RGB 5-5-5 mode with 32,768 colors. Each pixel is represented by 15 bits containing 5 bits of red, green, and blue color information. The input sequence for each pixel is the low byte first, followed by the high byte.

The first low byte is taken on the first rising edge of clock occurring after BLANK# has gone inactive (high).

- In Clocking mode 2 (HDR[5] = '1'), all subsequent bytes are clocked in on the rising edge of the clock.
- In Clocking mode 1 (HDR[5] = '0'), the low bytes are clocked in on the rising edge of the clock and the high bytes are clocked in on the falling edge of the clock.

This mode ignores the palette DAC lookup table.

Table E-2. Pixel Data Format in RGB 5-5-5 Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
X	RED					GREEN					BLUE				

E.2.2 RGB 8-8-8 Mode with 16.8 Million Colors (True Color Mode)

This mode supports the industry-standard RGB 8-8-8 mode with 16,777,216 colors. Each pixel is represented by 24 bits containing one byte each of red, green, and blue color information. The input sequence for each pixel is the low byte (blue) first, followed by the middle byte (green), followed by the high byte (red).

This mode uses Clocking mode 2 (HDR[5] = '1'). The first low-byte is taken on the first rising edge of clock occurring, after BLANK# has gone inactive (high). All subsequent bytes are clocked in on the rising edge of clock. This mode ignores the palette DAC lookup table.

Table E-3. Pixel Data Format in RGB 8-8-8 Mode with 16.8 Million Colors

MSB HIGH BYTE								MIDDLE BYTE								LOW BYTE							LSB
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
RED								GREEN								BLUE							

E.2.3 Mix Mode

When Extension register HDR[4] is set to '1', pixel data bit [15] is used to select between RGB 5-5-5 mode and the standard VGA-compatible, 256-color mode.

Table E-4. Pixel Data Format in RGB 5-5-5 Mode of the Mix Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	4	3	2	1	0	4	3	2	1	0	4	3	2	1	0
RGB 5-5-5	RED					GREEN					BLUE				

Table E-5. Pixel Data Format in 256-Color Mode of the Mix Mode

MSB HIGH BYTE								LOW BYTE							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	7	6	5	4	3	2	1	0
256-Color mode	Ignored							Palette DAC lookup-table input							

Appendix F

Memory Configurations

F.1 Introduction

The CL-GD7548 supports scalable 32-bit-wide display-memory configurations, from 1 to 2 Mbytes, using the following types of DRAMs.

- 512K × 8
- 256K × 16 — multiple-CAS#
- 256K × 16 — multiple-WE#

F.2 Possible Memory Configurations

Table F-1 shows the possible memory configurations that the CL-GD7548 supports.

For 256K × 16 DRAM configurations, the total display memory can be expanded from 1 to 2 Mbytes. The 512K × 8 DRAM configuration must be 2 Mbytes. Some signals of the CL-GD7548 change functions according to the DRAM organization that is used.

For optimum performance, choose multiple-CAS# configurations over multiple-WE# configurations.

Table F-1. CL-GD7548 Memory Configurations

Total Display Memory Size	Memory Bus Width	DRAMs	
		Number	Type
1 Mbyte	32 bits	2	256 Kbytes × 16
2 Mbytes[a]	32 bits	4	512 Kbytes × 8
2 Mbytes[b]	32 bits	4	256 Kbytes × 16

[a] The Extension register SRF[7] = '0'.
[b] The Extension register SRF[7] = '1'.

F.3 Control Signals for Various Memory Configurations

The following five tables indicate how the CL-GD7548 and the DRAMs must be connected.

Table F-2. 2-Mbyte Display Memory: Four 512K × 8 DRAMs

DRAM Pins Connected to CL-GD7548 Pins	CL-GD7548 Pins Connected to the DRAM Pins			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
OE#	OE#	OE#	OE#	OE#
WE#	WE#	WE#	WE#	WE#
CAS#	CAS0#	CAS1#	CAS2#	CAS3#
RAS#	RAS0#	RAS0#	RAS0#	RAS0#
ADDR[9:0]	MA[9:0]	MA[9:0]	MA[9:0]	MA[9:0]
DATA	MD[7:0]	MD[15:8]	MD[23:16]	MD[31:24]
Bit planes stored in each DRAM	3	2	1	0

NOTE: This configuration is multiple-CAS#, common-WE# (SRF[0] = '1').

Table F-3. 1-Mbyte Display Memory: Two 256K × 16 Multiple-CAS# DRAMs

DRAM Pins Connected to CL-GD7548 Pins	CL-GD7548 Pins Connected to the DRAM Pins	
	To DRAM #1	To DRAM #2
LCAS#	CAS2#	CAS0#
UCAS#	CAS3#	CAS1#
OE#	OE#	OE#
RAS#	RAS0#	RAS0#
WE#	WE#	WE#
ADDR[8:0]	MA[8:0]	MA[8:0]
ADDR[9]	Not valid	Not valid
DATA	MD[31:16]	MD[15:0]
Bit planes stored in each DRAM	0,1	2,3

Table F-4. 1-Mbyte Display Memory: Two 256K × 16 Multiple-WE# DRAMs

DRAM Pins Connected to CL-GD7548 Pins	CL-GD7548 Pins Connected to the DRAM Pins	
	To DRAM #1	To DRAM #2
LWE#	WE2#	WE0#
UWE#	WE3#	WE1#
OE#	OE#	OE#
RAS#	RAS0#	RAS0#
CAS#	CAS#	CAS#
ADDR[8:0]	MA[8:0]	MA[8:0]
ADDR[9]	Not valid	Not valid
DATA	MD[31:16]	MD[15:0]
Bit planes stored in each DRAM	0,1	2,3

Table F-5. 2-Mbyte Display Memory: Four 256K × 16 Multiple-CAS# DRAMs

DRAM Pins Connected to CL-GD7548 Pins	CL-GD7548 Pins Connected to the DRAM Pins			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
LCAS	CAS2#	CAS0#	CAS2#	CAS0#
UCAS	CAS3#	CAS1#	CAS3#	CAS1#
OE#	OE#	OE#	OE#	OE#
RAS#	RAS0#	RAS0#	RAS1#	RAS1#
WE#	WE#	WE#	WE#	WE#
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
Bit planes stored in each DRAM	0,1	2,3	0,1	2,3

Table F-6. 2-Mbyte Display Memory: Four 256K × 16 Multiple-WE# DRAMs

DRAM Pins Connected to CL-GD7548 Pins	CL-GD7548 Pins Connected to the DRAM Pins			
	To DRAM #1	To DRAM #2	To DRAM #3	To DRAM #4
LWE#	WE2#	WE0#	WE2#	WE0#
UWE#	WE3#	WE1#	WE3#	WE1#
OE#	OE#	OE#	OE#	OE#
RAS#	RAS0#	RAS0#	RAS1	RAS1
CAS#	CAS#	CAS#	CAS#	CAS#
ADDR[8:0]	MA[8:0]	MA[8:0]	MA[8:0]	MA[8:0]
DATA	MD[31:16]	MD[15:0]	MD[31:16]	MD[15:0]
Bit planes stored in each DRAM	0,1	2,3	0,1	2,3

Appendix G

Clock Options

G.1 Introduction

The dual-frequency synthesizer in the CL-GD7548 generates all the clocks needed for the memory timing (for example, RAS#, CAS#), as well as the video clock timing. To derive these internal clock signals, an external reference clock must be provided to the OSC input of the CL-GD7548. For all calculations in this document, the external reference clock used is 14.318 MHz ± 0.01% with a duty cycle of 50 ± 10%.

G.2 Memory Clock

MCLK (the memory clock) is used to generate all memory timing signals (for example, RAS# and CAS#).

G.2.1 Default MCLK (Memory Clock)

The CL-GD7548 default memory clock frequency is 42.955 MHz. For the equation in the next section, this frequency is equivalent to 18h (24 decimal). For information regarding CL-GD7548 configuration, refer to Appendix L.

G.2.2 MCLK Programming

For higher performance, the CL-GD7548 has a programmable memory clock. The desired MCLK frequency is programmed directly into SR1F[5:0], by using the equation below. The MCLK selected at system reset (18h) is valid until SR1F is written.

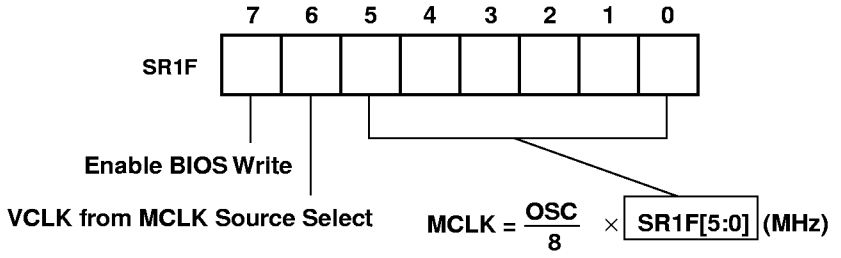


Figure G-1. Programmable Memory Clock

Examples of valid MCLK frequencies are shown in Table G-1:

Table G-1. Examples of Valid MCLK Frequencies

SR1F[5:0] (decimal)	SR1F[5:0] (hex)	MCLK Frequency (MHz)
21	15h	37.585
23	17h	41.165
25	19h	44.744
28	1Ch	50.114

G.3 Video Clock

The VCLK (video clock) is the fundamental video timing clock in the system. The CRT monitor timing signals (HSYNC and VSYNC), as well as the LCD clocks, are derived from VCLK.

G.3.1 Default Video Clock Source

The VCLK source is determined by a number of factors as indicated in Table G-2. For a default VCLK, either MCLK or MCLK/2 (one-half the frequency of MCLK), as well as four VCLKs, can be used.

Table G-2. VCLK Sources and Frequencies

Extension Register SR1F[6]	Extension Register SR1E[0]	External/General Register MISC 3C2[3:2]	Video Clock (Defaults)	
			Source	Frequency (MHz)
0	X	00	VCLK0	25.180
0	X	01	VCLK1	28.325
0	X	10	VCLK2	41.165
0	X	11	VCLK3	36.082
1	0	XX	MCLK	42.955
1	1	XX	MCLK/2	21.477

G.3.2 VCLK Programming

As indicated in Table G-3, the VCLK sources can be programmed with two registers each.

Table G-3. Internal VCLK Sources

Video Clock Source	Default Frequency (MHz)	Numerator			Denominator			Post-scalar
		Extension Register	Decimal	Hex	Extension Register	Decimal	Hex	
VCLK0	25.180	SRB[6:0]	102	66h	SR1B[5:1]	29	3Bh	1
VCLK1	28.325	SRC[6:0]	91	5Bh	SR1C[5:1]	23	2Fh	1
VCLK2	41.165	SRD[6:0]	69	45h	SR1D[5:1]	24	30h	0
VCLK3	36.082	SRE[6:0]	126	7Eh	SR1E[5:1]	25	19h	1

For each VCLK, a 7-bit numerator (N), 5-bit denominator (D), and 1-bit post-scalar (P) determines the frequency according to the equation shown in Figure G-2:

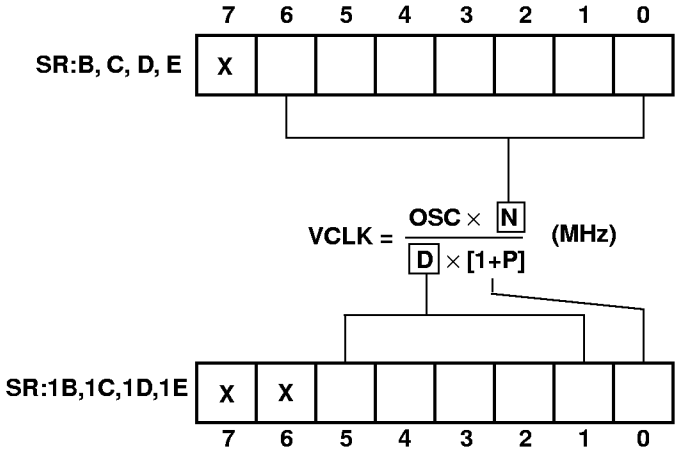


Figure G-2. Programmable Video Clock

Typically, there are a large number of combined numerator/denominator values that can program a common frequency. The choice among these combinations is made empirically. Better results can be obtained if the post-scalar is programmed to '1'.

G.4 Using MCLK as VCLK

When MCLK and VCLK are programmed to frequencies within ≈1% of each other (or to frequencies that are nearly multiples of each other), they can interfere with each other. This interference can show up as 'jitter' on the screen. The solution is to shut down the VCLK oscillator and use MCLK (or MCLK/2) as VCLK. Table G-4 shows examples of frequencies for which this solution must be used.

Table G-4. Memory Clock Used as Video Clock

MCLK	Graphics Display Mode	VCLK		Selection Criteria		
		Frequency	Source	SR1F[5:0]	SR1F[6]	SR1E[0]
50.1	64h at 60 Hz	25 MHz	MCLK/2	1Ch	1	1
50.1	66h at 60 Hz	25 MHz	MCLK/2	1Ch	1	1
50.1	58h at 72 Hz	50 MHz	MCLK	1Ch	1	0
50.1	5Ch at 72 Hz	50 MHz	MCLK	1Ch	1	0

Appendix H

Power Management

H.1 Introduction

The CL-GD7548 has two LCD power-management modes, Standby and Suspend. The CL-GD7548 also manages CRT power consumption through DPMS (display power management signaling) support.

H.2 Power Management

The CL-GD7548 provides several intelligent power-management features to enable the power-saving modes. For power-management BIOS calls discussed in this section, refer to the Cirrus Logic "CL-GD754X VGA BIOS External Function Specification" in the *CL-GD754X Application Book*. Table H-1 lists dedicated CL-GD7548 pins that facilitate power management.

Table H-1. Dedicated Pins for Power Management

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
ACTI / FCEVIDEO# / SBYI	86		Functions include: Activity sense Feature-Connector enable video# Standby mode input control	This pin may be used for one of three functions, ACTI, FCEVIDEO#, or SBYI. The function that the pin is used for depends on the configuration of Extension registers SR23[6] and SR24[7]. Two of the functions are related to power management:
(ACTI)		I	(1) Activity sense function. When this pin is configured for the activity sense function and the ACTI input pin is connected to another input pin, this pin can be used to sense various types of activity in order to initiate an action. A keyboard interrupt, for example, can be used to reset whatever internal timers have been set.	To use the ACTI function, set Extension register bits SR24[7] = '1' and SR23[6] = '1'. Then, to use any low-to-high activity on the ACTI pin: (1) To reset the internal Standby mode timer, set Extension register bits SR23[6] to '1' and CR2D[6] to '1'. (2) To reset the backlight control for the LCD, set Extension register bits SR23[6] to '1' and CR2D[3] to '1'.
(FCEVIDEO#)		I	(2) FCEVIDEO# function. When this pin is configured for the FCEVIDEO# function, this pin is not utilized for power management. In this case, the Standby mode must be initiated by software methods.	To use the FCEVIDEO# function, set Extension register SR24[7] = '0'.
(SBYI)		I	(3) Standby mode function. To configure this pin to initiate the Standby mode function, set Extension register bits SR24[7] = '1' and SR23[6] = '0'. (There are also two software-based methods of entering the Standby timer mode. For details, refer to Chapter 3.)	To use this pin to enter Standby mode, set Extension register SR23[6] to '0'. If this pin is not used, connect it to ground. When the LCD is on and this input is asserted high, the power-down sequence starts for the Standby mode. Standby mode terminates when this pin goes low (as long as Extension register CR20[4] = '0') and the Standby timer has been reset.

Table H-1. Dedicated Pins for Power Management *(cont.)*

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
BLI / SUSPI	87		Functions include: Backlight input control Suspend mode input control	This pin may be used for one of two functions, BLI or SUSPI. The function that the pin is used for depends on the pin connections and the configuration of Extension register SR23[5] and other registers. The functions are related to power management.
(BLI)		I	(1) LCD backlight input control function. When this pin is configured for the LCD backlight input control function, it turns off the LCD backlight. This function would be used for conditions under which the LCD is off, but CPU accesses are allowed and CRT outputs remain active.	To use the pin to turn off the LCD backlight: (1) Connect the pin to an external source. (2) Set Extension register SR23[5] to '1', in which case a high on this input turns the LCD backlight off.
(SUSPI)		I	(2) Suspend mode input control function. This mode is the most efficient power-saving mode. When this pin in configured to initiate the hardware-controlled Suspend mode, the CL-GD7548 bus is disabled. Consequently, attempts by the CPU to access the CL-GD7548 are ignored. In local bus applications, the bus controller must intercept CPU access attempts when the CL-GD7548 is in hardware-controlled Suspended mode, or else the local bus hangs. The Suspend mode can also be initiated with software commands. For details, refer to Chapter 3.	To use the pin for hardware-controlled Suspend: (1) Connect the pin to an external source. (2) Set Extension register SR23[5] = '0' to define this pin to function as the hardware-controlled Suspend mode input. (3) Disable software-controlled Suspend mode by setting Extension register CR20[3] to '0'. (4) Set the resolution of the debounce timer: CR20[7] = '1' sets a resolution of 1 sec. CR20[7] = '0' sets a resolution of 32 msec. (5) Initialize the debounce timer by setting Extension register CR23[7:4] to any non-zero value. (6) A stable high signal on this input initiates the hardware-controlled Suspend sequence.
CLK32K	7	I	32-KHz clock input function. This pin is used to provide memory refresh during Suspend mode. **NOTE:** This clock must be present and stable before the CL-GD7548 is placed into Suspend mode.	When Extension register CR2D[4] = '0' and the CL-GD7548 is in Suspend mode: (1) The OSC input pin is disabled. (2) A 32-kHz clock must be connected to the CLK32K pin. (The 32-kHz clock source for memory refresh in Suspend mode is derived from the CLK32K pin.) (3) To select an external 32-kHz clock for the pin, set Extension register CR29[6] to '1'.

Table H-1. Dedicated Pins for Power Management *(cont.)*

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
FPBL	105	O	Flat panel backlight power function. This pin can function in three ways:	
			(1) Normal flat panel power sequence functions, including Standby and Suspend modes.	(1) This pin is sequenced high or low automatically by the CL-GD7548 in three ways: (a) As part of normal power-up/down sequence (b) When switching between a CRT and LCD (c) Entering Suspend/Resume or Standby modes
			(2) For internal backlight timer functions.	(2) To use this pin with an internal backlight timer: (a) To configure the pin for internal backlight functions, connect the FPBL pin to the input of the LCD backlight control circuit. (b) To use the backlight timer, program Extension register CR21[7:4] for a time-out delay. (c) To reset the backlight timer, use one or more of the following methods: [1] To use any low-to-high activity on the ACTI timer pin to reset the backlight timer, set Extension register CR2D[3] to '1'. [2] To use keyboard activity to reset the backlight timer, set Extension register SR25[0] to '1'. [3] To use any VGA access (memory or I/O) to reset the backlight timer, set Extension register CR2D[2] to '1'.
			(3) With a software override bit for various control functions.	(3) To override power-up/down sequencing and other control functions, set Extension register CR23[3] to '1' and toggle CR23[2] to turn the LCD backlight output on and off. CAUTION: This action is not recommended, as flat panel damage may result.

Table H-1. Dedicated Pins for Power Management *(cont.)*

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
FPVCC	106	O	Flat panel VCC. This pin is part of the flat panel power sequencing, which includes Standby and Suspend modes. This pin can be controlled with a software override bit.	(1) Connect the pin to the flat panel VCC control circuit. (2) This pin is sequenced high or low automatically by the CL-GD7548 in three ways: (a) As part of normal power-up/down sequence (b) When switching between a CRT and LCD (c) Entering Suspend/Resume or Standby modes (3) To override all controls, set Extension register CR23[1] to '1', and toggle CR23[0] to turn FPVCC on or off. **CAUTION:** **This action is *not* recommended, as flat panel damage may result.**
FPVEE	102	O	Flat panel VEE. This pin is part of the flat panel power sequencing, which includes Standby and Suspend modes.	(1) Connect the pin to the flat panel VEE (contrast) control circuitry. (2) This pin is sequenced high or low automatically by the CL-GD7548 in three ways: (a) As part of normal power-up/down sequence (b) When switching between a CRT and LCD (c) Entering Suspend/Resume or Standby modes
PROG	148	O	Programmable output function. If a system uses a programmable VDD circuit, this pin must be used by the video BIOS and the circuit to select 3.3-V or 5.0-V core VDD operation. **NOTE:** The programmable VDD circuit is described in the Cirrus Logic application note, "Programmable Core Voltage", in the *CL-GD754X Application Book.*	If Extension register CR30[7]: (1) Is '1', PROG is set high, and the programmable VDD circuit switches the core VDD to 5.0 V. (2) Is '0', PROG is set low, and the programmable VDD circuit switches the core VDD to 3.3 V.

Table H-1. Dedicated Pins for Power Management *(cont.)*

Pin Name (Pin Function)	Pin No.	Pin Type	Pin Function Description	Pin Use
SBYST#	123	O	Standby mode status function. This pin can be configured to perform one of three possible functions: (1) For a power-management function, this pin can be used to indicate the status of Standby mode. (2) For a Feature Connector data function, this pin can be used for pixel data output. (3) For a 24-TFT LCD function, this pin can be used for the 24-bit TFT Green bit [0] LCD data output (that is, FP8).	 (1) If Extension register CR29[4] = '1', then SBYST# remains low, indicating that the CL-GD7548 is in Standby mode. (2) If pin 157 (MD [25] / FCPU) is configured for the Feature Connector function and Extension register SR24[7] = '1', this pin functions as FC pixel data output and is not used for power management. (3) If a 24-bit TFT LCD is connected, this pin is used for LCD data output, and the Standby Status function is not available.
SUSPST#	125	O	Suspend mode status. This pin can be configured to perform one of three possible functions. (1) For a power management function, this pin can be used to indicate the status of Suspend mode. (2) For a Feature Connector data function, this pin can be used for pixel data output (FCP1). (3) For a 24-TFT LCD function, this pin can be used for the 24-bit TFT Green bit [1] LCD data output (that is, FP9).	 (1) If Extension register CR29[7:6] = '1', then SUSPST# remains low, indicating that the CL-GD7548 is in Suspend mode. (2) If pin 157 (MD [25] / FCPU) is configured for the Feature Connector function and Extension register SR24[7] = '1', this pin functions as FC pixel data output and is not used for power management. (3) If a 24-bit TFT LCD is connected, this pin is used for LCD data output, and the Suspend Status function is not available.

H.2.1 Normal Power Mode

In normal power mode, either the LCD system, the CRT monitor, or both are being used. During normal power mode, the following occurs:

- The active display(s) receive power.
- Full-screen refresh is in effect.
- The CPU has access to the following:
  - — Video memory
  - — RAMDAC
  - — I/O registers
- Refresh is provided to video memory.

H.2.2 Standby Mode

When the system is not being actively used, the CL-GD7548 can be set up to automatically enter Standby mode. During Standby mode, the screen goes blank, but application programs the user may have launched continue to run normally. The device can be set up so the user can terminate Standby mode (by pressing a key, for example) and restore the screen.

When the system enters Standby mode, the LCD is turned off using the power-down sequence. As a result, since there is no screen refresh, normal clock rates may be replaced by slower clock rates, further reducing power consumption. When the system is in Standby mode, the following occur:

- The LCD power-down sequence occurs automatically when Standby mode is entered, and the LCD power-up sequence occurs automatically when Standby mode is exited.
- The VCLK oscillator is stopped.
- No clock is provided to the CRT controller.
- The RAMDAC is in the low power mode.
- Video display memory refresh occurs (at a slower refresh rate).
- The CPU accesses and modifies the video display memory and palette DAC.

H.2.2.1 Standby Mode: Initiating and Entering

The CL-GD7548 provides three methods for entering Standby mode. The transition can be initiated in software by using a hardware timer, or by using the Standby input pin (SBYI).

All methods for entering the Standby mode offer the features itemized above. One or more methods can be used simultaneously to start and/or maintain Standby mode. Standby mode is entered as follows:

1. To use software to start the Standby mode power-down sequence, set Extension register CR20[4] to '1'.
2. To use a hardware and software combination to start the Standby mode, use either of the following methods:
   - Program the hardware timer in Extension register CR21[3:0] in increments of one minute, up to 15 minutes. If the hardware timer is allowed to count down to zero, the Standby mode power-down sequence is started.
   - Program Extension register SR24[7] to '0' so that the Standby mode can be entered through hardware control. To select the Standby input function, connect the SBYI pin to an external source and set SR23[6] to '0'. When the SBYI pin is driven high, the Standby mode power-down sequence is started.

The above conditions must be removed to terminate Standby mode and start the power-up sequence.

H.2.2.2 Standby Mode: Status

The status of Standby mode can be obtained by checking the state of the SBYST# pin. If the CL-GD7548 is in Standby mode, Standby mode status (CR29[4]) is set high from the time the clocks are stopped until 32 µsec after the clocks are restarted. SBYST# output is low during this time.

Pin 123 is a multi-function pin that cannot be used as SBYST# if the following conditions exist:

- An external pull-up resistor is connected to pin 157, which configures the chip for Feature Connector functionality. (Pin 123 is then used for pixel data output.)
- A 24-bit TFT LCD is connected. (Pin 123 is then used for TFT green data output.)

H.2.2.3 Standby Mode: Terminating and Exiting

The LCD power-up sequence occurs automatically when Standby mode is terminated, that is, when any of the conditions for initiating Standby mode are removed as described below.

1. Reset the Standby-mode timer in one of the following ways:
   - To use activity on the ACTI input to reset the timer, set CR2D[6] to '1'. Since the ACTI pin is multifunctional, enable the ACTI input function by setting SR23[6] to '1'. (SR24[7] must be reset to '0' to enable ACTI.)
   - To use any VGA access (memory or I/O) to reset the timer, set CR2D[5] to '1'.
   - To use any keyboard access to reset the timer, set SR25[1] to '1'.
2. Terminate the Standby mode.
   - Terminate software-controlled Standby mode by setting CR20[4] to '0'.
   - Terminate hardware-controlled Standby mode by asserting the SBYI pin low.

If a power-up or power-down sequence is in progress when there is a request to terminate or initiate Standby mode, the power-up/down sequence is allowed to complete before the new request is initiated.

H.2.3 Suspend Mode

The CL-GD7548 Suspend mode is used to save power when the system is not being actively used for a long period of time. When the system enters Suspend mode, the following occur:

- The screens turn off.
- Application programs suspend operation.
- The CPU is prohibited from accessing video memory, I/O registers, or the palette DAC, in the case of hardware-controlled Suspend. In hardware-controlled Suspend mode, even though application programs cease to run in either foreground or background, all register states are preserved, and so the environment is maintained when Suspend mode terminates.

H.2.3.1 Suspend Mode: Hardware-Controlled

Hardware-controlled Suspend mode, which provides the most efficient means of power saving, is initiated by using the SUSPI pin. SR23[5] must be set to '0' to enable hardware-controlled Suspend mode. This pin uses a debounce timer to minimize accidental attempts to initiate Suspend mode.

In this mode, the input pads are shut off and the bus interface does not receive power. All I/O pins, except the dedicated Suspend mode input are de-activated, further reducing power consumption. Additional power is saved because CPU host access to video memory is denied. Also, if selected, a slower 32-kHz clock refreshes the video memory by performing CAS#-before-RAS# refresh. This slow clock input, which is recommended for maximum power savings, comes from one of two sources:

- By setting CR2D[4] to '1', a 32-kHz clock output results from dividing the 14.318-MHz clock by 432.
- By setting CR2D[4] to '0', an external 32-kHz clock input can be provided through the 32-kHz input. The 14.318-MHz input can then be removed to save power.

When the system is in hardware-controlled Suspend mode, the following occur:

- The LCD power-down sequence occurs automatically when Suspend mode is entered, and the LCD power-up sequence occurs automatically when Suspend mode is exited.
- The VCLK and MCLK oscillators automatically shut off when the Suspend sequence occurs.
- No CPU access is allowed to the following:
  - — Video memory
  - — RAMDAC
  - — I/O registers
- Although video display memory cannot by accessed by the CPU during Suspend mode, the contents are preserved. (This action is useful when a system remains inactive for a relatively long time.)
- Register data contents are retained.
- Unless DRAMs are self-refresh, the CL-GD7548 internal refresh clock for video memory is set to 32 kHz.

When using self-refresh DRAMs, Refresh Select (CR20[2:1]) must both be set to '1' so that static delays within the chip generate the necessary timings to initiate self-refresh.

H.2.3.2 Suspend Mode: Software-Controlled

Software-controlled Suspend mode is initiated by setting CR20[3] (Activate Suspend mode) to '1'. In contrast to the hardware-controlled Suspend mode, software-controlled Suspend mode allows the CPU to access all the internal registers, which requires an active clock and I/O capability, and therefore more power.

H.2.3.3 Suspend Mode: Initiating and Entering

Hardware-controlled Suspend mode is recommended, in order to minimize power consumption. Hardware-controlled Suspend mode is entered by connecting the SUSPI pin to an external source. When input to SUSPI is high, the Suspend mode is initiated. An internal debounce timer (Extension register CR23[7:4]) selects the time period that an input must remain high and stable before the Suspend mode is activated. Debounce Timer Resolution (in Extension register CR20[7]) determines the resolution of the timer (between 32 µsec and 1 sec).

NOTE: SUSPI / BLI Select (SR23[5]), and Activate Suspend Mode (CR20[3]) must be set to '0' to define the BLI / SUSPI pin function as hardware-controlled Suspend mode.

Software-controlled Suspend mode is entered by setting CR20[3] to '1'. In this mode, CPU access is still active, and the SUSPI pin is disabled.

NOTE: This mode is not recommended, as it requires more power than the hardware-controlled Suspend mode.

H.2.3.4 Suspend Mode: Sequence

The typical Suspend mode sequence is as follows:

1. The system receives a request to suspend.
2. The system interrupts the application. The interrupt routine calls the video BIOS Suspend routine. The video BIOS Suspend routine waits until all CPU cycles already in the CPU write buffer are executed.

   A CPU read verifies that the CPU write buffer is empty. When the CPU read is done, the CPU write buffer is empty. If a BitBLT operation is in progress, it suspends automatically at the first memory refresh cycle. After resuming, the BitBLT operation continues from the point of operation that it was suspended.

   The Suspend mode can be initiated while the CPU write FIFO contains CPU write cycles waiting to be executed. However, the Suspend mode must not be initiated while the RDY# signal is high and waiting for the completion of a cycle. To prohibit this action from occurring, the Suspend routine executes and then waits for the completion of a CPU read, but only if there are no BitBLT operations in progress. If a BitBLT operation is in progress, the Suspend routine skips to the next step in the Suspend sequence without waiting for the RDY# pin to tristate.

   Prior to proceeding with the Suspend mode sequence, the BIOS can execute several I/O reads and writes. If the core VDD (CVDD) was at 5.0 V, CVDD must be switched to 3.3 V as the last I/O executed before proceeding to the next step.
3. Set the SUSPI pin high. Using OEMSI (the OEM BIOS customizing utility provided by Cirrus Logic in the BIOS Development kit), the video BIOS must be customized for the I/O location of the SUSPI pin control. [Note that the SUSPI pin is to be controlled by a spare I/O port (a 1-bit output port) on the motherboard.]
4. SUSPST# output is set low.
5. At the end of the first memory refresh cycles (1, 3, or 5 CAS#-before-RAS# refreshes):
   a. The display memory control is switched to 32-kHz refresh cycles. No other memory cycle types can execute.
   b. Pad control is forced to Suspend mode and CPU inputs are disabled.
6. The CL-GD7548 executes LCD power-off sequencing. The sequence starts 60 µsec after the SUSPI pin is set high and requires approximately 150 msec to complete.
7. The CL-GD7548 stops VCLK and MCLK.
8. The 32-kHz clock can now be stopped and the system can be powered down.

H.2.3.5 Suspend Mode: Status

Suspend mode status can be obtained by checking SUSPST#. If the CL-GD7548 is in Suspend mode, Suspend Mode Status (CR29[7:6]) is set high from the time the clocks are stopped until 32 µsec after the clocks are restarted. SUSPST# output is low during this time.

SUSPST#, a multifunction pin, cannot be used for SUSPST# if any of the following conditions exist:

- An external pull-up resistor is connected to pin 157, which enables FC functionality. (Pin 125 is then used for Feature Connector pixel data output).
- FC Video Port Enable (SR24[7]) is set high, which enables FC functionality. (Pin 125 is then used for pixel data output.)
- A 24-bit TFT LCD is connected. (Pin 125 is then used for TFT LCD data G[1].)

H.2.3.6 Suspend Mode: Terminating and Exiting

The Suspend mode must be terminated/exited in the same manner that it was entered.

- When SUSPI is driven low, Suspend mode is terminated.
- In software, Suspend mode is terminated by setting CR20[3] to '0'.

When Suspend mode is terminated, the system returns to the same operational state it was in before Suspend mode was entered. The typical Resume sequence is as follows:

1. The system starts the 32-kHz clock.
2. The Resume Video BIOS call is executed, which sets SUSPI low. SUSPST# remains low.
3. The clock synthesizers start after 60 µsec. To ensure a stable signal before the next step in the sequence is executed, allow 64 msec to elapse.
4. The CPU pins are returned to their operational state after the last slow-refresh cycle is done or after the self-refresh end sequence is completed. Memory control is then passed onto the memory clock. Using the memory clock is the standard method for driving the display memory.
5. After 64 msec, the LCD VDD is on and all I/O registers are restored.
6. The LCD pads are enabled after another 32 msec.
7. After another 32 msec, the LCD backlight and bias are enabled and the system is fully resumed.

H.2.4 CRT-Only Power Mode

During the CRT-only operation, LCD drive signals are all inactive, and the LCD power-off sequence occurs automatically.

H.2.5 Backlight Input Control

The LCD backlight can be turned off through input from an external source. BLI input can be used in situations where reduction of LCD power consumption is necessary, but CPU access is still allowed and CRT outputs remain active. A specific example of this situation is a closed-cover condition where the backlight is not necessary, but CPU access is desired to complete an application task or active CRT outputs are desired to allow an external CRT to run.

To enable the BLI function on pin 87, set Extension register SR23[5] to '1'. When this input goes high, the LCD backlight is turned off.

H.2.6 Backlight Timer Power Mode

An additional internal timer allows the CL-GD7548 to control the backlight without having to enter a power-down mode. The Backlight timer, CR21[7:4], can be programmed in increments of one minute, up to 15 minutes. If the timer is allowed to count down to zero, the FPBL output goes low to disable the LCD backlight. Programming this register to '0' disables the Backlight timer. This timer can be programmed to be reset by activity on the ACTI input pin, by keyboard input, or by a VGA access.

H.2.7 ACTI Function

If the ACTI input is enabled, a low-to-high transition on this pin can be used to reset the internal timers for Standby mode, the backlight, or both. If Extension register SR23[6] is set to '1', it enables the ACTI function on pin 86 and Extension register CR2D[6,3] to control which timers are reset by activity on this pin. For example, this pin can be connected to the keyboard interrupt from the system logic to periodically reset the timer(s).

H.3 Techniques for Reducing Power Consumption

H.3.1 Power Reduction in Suspend Mode

In a CMOS device such as the CL-GD7548, power is consumed whenever inputs cross CMOS thresholds. Since the CPU address/data buses are inputs to the CL-GD7548, the following alternatives are available to reduce power when the system is in Suspend mode.

- When using the hardware-controlled Suspend mode, set registers SR23[5] = '0' and CR20[3] = '0' to isolate the CL-GD7548 from the CPU address/data buses. In this case, the SUSPI pin disables CPU access to the CL-GD7548.
- Hold the buses quiescent (program them either a '0' or '1') so that inputs do not cross CMOS thresholds and power is not consumed.
- If the CPU processor allows, shut down the CPU I/O ports and stop the CPU clock connected to the LCLK pin of the CL-GD7548.
- A 32-kHz oscillator input must be used and the 14.318-MHz clock must be turned off.

To reduce the power used by the memory interface, use low-power CMOS DRAM(s). When not being accessed, CMOS DRAMs do not draw significant current and are effectively powered-down. Self-refresh DRAMs may be used to further reduce power consumption.

H.3.2 Mode-Dependent Voltage Switching

To minimize operating power consumption but still allow use of specific modes (such as 24-bit color mode) that require 5.0-V operation from the VGA core, the CL-GD7548 can utilize an external circuit to allow core voltage switching driven by the graphics desired. Active power consumption is minimized because the graphic subsystem can be set to operate at 3.3 V. A 5.0-V operation would occur only in specific modes. Also, even though the core may be switched to 5.0 V, the DRAM, the CPU host bus interface, and LCD VDD can still be set for 3.3-V operation to further minimize active power.

The video BIOS supports INT 10h and 15h function calls that define the minimum voltage requirements for modes to operate, allowing the system to determine if the set mode must be completed. If the CL-GD7548 is running at 3.3 V and requests a mode that requires 5.0 V, an INT 15h function call notifies the system BIOS of the voltage requirement.

If the voltage switching circuit is present, the system allows the set mode to proceed by returning an INT 10h call to the video BIOS. The video BIOS sets CR30[7] to '1'. This action sets the PROG pin output high, signaling the external circuit to supply 5.0 V to the core VDD and allowing the set mode call to complete.

When the CL-GD7548 is switched back to a mode that requires only 3.3-V Core operation, a similar set of INT 15h and INT 10h calls allow CR30[7] to be reset to '0'. This action sets PROG low and signals the circuit to supply 3.3 V to the core VDD.

The external circuit and the BIOS function calls supporting this capability are described in more detail in the Cirrus Logic application notes, "A Programmable Core-Voltage Solution", and "CL-GD754X VGA BIOS External Function Specification", in the *CL-GD754X Application Book*.

H.3.3 Complete Power-Down of the Graphics Controller

The CL-GD7548 can support system implementations where the VGA subsystem is powered off, providing maximum power savings. The critical task for the CL-GD7548 is to properly execute LCD power-down sequencing before shutting off power. Software tasks are the most critical because the VGA controller register states and the contents of video memory must be saved to a system-specified location and then properly restored upon power-up to the graphics subsystem.

The CL-GD7548 BIOS has Save/Restore functions for the VGA and Extension register contents. Cirrus Logic also has sample code available of programs that save the contents of video memory. Both are necessary to support this function. Cirrus Logic can provide source code demonstrating Save/Restore functionality for both display memory and registers, allowing the system designer to ensure proper operation of this implementation.

H.4 Green Computing

The CL-GD7548 features comprehensive PC power-management functions that support compliance with the United States Environmental Protection Agency's Energy Star Computer Program.

H.4.1 Display Power Management Signaling (DPMS)

The method by which the greatest power savings can be obtained by putting the monitor into a low-power mode that require the monitor respond to DPMS (display power management signaling).

The VESA (Video Electronics Standards Association) DPMS Proposal defines four levels of display power. Through register control, the CL-GD7548 can support each of these four levels. The DPMS modes in the CL-GD7548 can operate independently of the power modes that the CL-GD7548 supports. The only time the CL-GD7548 power management mode is directly tied to the DPMS register setting is in timer-initiated Standby because this mode is a hardware timer-driven mode and there is no opportunity for the BIOS to program any of the CL-GD7548 registers. Under this condition, the CRT is internally forced by the controller into the DPMS Standby state (VSYNC is automatically provided with a 32-kHz clock) and it disregards any value in GRE[2:1].

Table H-2 shows DPMS register values (GRE[2:1]) in the CL-GD7548, the resultant DPMS states, and the DPMS mode relationship to the power management modes.

Table H-2. CL-GD7548 DPMS Register Programming

GRE [2:1] Setting	DPMS State	DPMS Compliance	Conditions				CL-GD7548 Power Modes
			VSYNC	HSYNC	DAC Power	CRT Recovery	
00	ON = Full operation	Mandatory	Active	Active	On	N/A	Active
01	STANDBY= Operating state of minimal power reduction	Optional	Active	Inactive	Off	Short	Active, Standby, or Suspend
10	SUSPEND= Significant reduction of power consumption	Mandatory	Inactive	Active	Off	Long	Active, Standby, or Suspend
11	OFF= Lowest level of power consumption	Mandatory	Inactive	Inactive	Off	System-dependent	Active, Standby, or Suspend

H.4.2 Static HSYNC and VSYNC

HSYNC is static if GRE[1] is programmed to a '1', and the sense is as programmed into MISC[6]. VSYNC is static if GRE[2] is programmed to a '1', and the sense is as programmed into MISC[7].

If either GRE[1] or GRE[2] is programmed to a '1', the DAC is powered down. This action satisfies the requirement in the VESA proposal which states, "...host system sets the video image information to the blank level prior to the host transmitting the Stand-by/Suspend/Off signal to the display". This action significantly reduces the power in the CL-GD7548.

H.4.3 Optimizing Use of DPMS and Controller Power Management Modes

When the CL-GD7548 is in CRT-only mode and the CRT is in DPMS Standby or Suspend mode, power consumption can be minimized by having the BIOS reduce the video clock and the memory clock frequencies. Similarly, to ensure there is no power to the CRT, the BIOS must set DPMS to 'Off' when the CL-GD7548 is in LCD-only mode.

Prior to initiating the CL-GD7548 Suspend mode, the BIOS can program GRE[2:1] to any of the DPMS power save states (Standby, Suspend, or Off). The 32-kHz input that the CL-GD7548 uses for display memory refresh while in the Suspend mode can also be used as the synchronization pulse required if DPMS Standby or Suspend mode is requested. This action allows a system designer the flexibility to select the CRT recovery time desired when resuming from the CL-GD7548 Suspend state. Even in the case of hardware-initiated Suspend mode, it is assumed that some time period is allocated for system housekeeping before Suspend mode is actually initiated, which allows DPMS programming to occur.

H.5 VESA® VBE/PM BIOS Functions

The CL-GD7548 is fully compliant with the VESA display power management BIOS extensions, VBE/PM Version 1.0. The following sections describe these calls.

H.5.1 Report VBE/PM Capabilities

Input:	AH = 4fh		VESA Extension
	AL = 10h		VBE/PM Services
	BL = 00h		Report VBE/PM Capabilities
	ES:DI		Null pointer, must be 0000:0000h
			Reserved for future use
Output:	AX =		Status
	BH =		Power-saving state signals supported by the controller (Note 1)
			1 = supported, '0' = not supported
		00h	On
		01h	Standby
		02h	Suspend
		04h	Off
		08h	Reduced on (intended for LCD displays)

NOTES:

1) The attached display may not support all power states that can be signaled by the controller. It is the responsibility of the power-management program to determine the power-saving states that are offered by the controller. If the controller has a means of determining which power-saving state is implemented in the attached display device, this function reports the power saving states that are supported by both the controller and the display.

2) \REDUCED ON is not defined in VBE/PM Version 1.0 and is not implemented.

H.5.2 Set Display Power State

Input:	AH = 4Fh		VESA Extension
	AL = 10h		VBE/PM Services
	BL = 01h		Set Display Power State
	BH =		Requested Power state
		00h	On
		01h	Standby
		02h	Suspend
		04h	Off
		08h	Reduced on (intended for LCDs)
Output:	AX =		Status: If the requested state is not available, this function returns AX = 014Fh, indicating that the function is supported, but that the call failed. In this case, the BH register and Display Power State are left unchanged.
	BH =		Unchanged

H.5.3 Get Display Power State

Input: AH = 4Fh VESA Extension
AL = 10h VBE/PM Services
BL = 02h Get Display Power State

Output: AX = Status: If this function is not supported by the controller hardware, AX = 014Fh must be returned in the status.
BH = Power state currently requested by the controller
00h On
01h Standby
02h Suspend
04h Off
08h Reduced on (intended for LCDs)

Appendix I

Signature Generator

I.1 Introduction

To automatically test the CL-GD7548 video-output logic at full speed, the CL-GD7548 has SG (signature generator) logic. With the addition of this feature, it is possible to capture a unique 16-bit signature for any given setup of graphics mode and display memory data. An error in the display memory interface, control logic, or pixel-data manipulation produces a different signature that can be compared to a known good signature value obtained from the same image. This comparison allows a test technician to quickly and accurately test a video screen without having to visually inspect the screen for errors. This method is used extensively in the Manufacturing Test.

I.2 Signature Generator Test

To run the SG, bits must be written in Extension register SR18 (the Signature Generator Control register) to initialize and arm the SG. A status bit reflects that the SG is running. When the Status bit changes state to 'not running', the signature may be read from Extension registers SR19 and SR1A.

NOTE: The signature is a function of the displayed pixels, not the display data. If the display screen includes blinking attributes or a blinking cursor, then the signature is different for those frames in which the pixel is blinked off, compared to frames in which the pixel is blinked on.

I.3 Signature Generator Control Register Definition

The Signature Generator Control register definitions are as follows:

Table i-1. SR18 Signature Generator Control Register Definitions

SR18 Bit	SR18 Bit Function
SR18[7]	LCD Signature Generator Enable / Status 0 = LCD Signature Generator has finished running and signature data is ready (read) 1 = Enable LCD Signature Generator
SR18[6:5]	Reserved
SR18[4:2]	Pixel Data Select. These bits select one of the 8 Pixel Data bits to use as SG input: '111' = Pixel Data Bit 7 '110' = Pixel Data Bit 6 '101' = Pixel Data Bit 5 '100' = Pixel Data Bit 4 '011' = Pixel Data Bit 3 '010' = Pixel Data Bit 2 '001' = Pixel Data Bit 1 '000' = Pixel Data Bit 0
SR18[1]	Reset Signature Generator 0 = Reset the Signature Generator 1 = Allow the Signature Generator to operate under the control of SR18[0]
SR18[0]	Signature Generator Enable / Status 0 = Signature Generator has finished running and signature data is ready (read) 1 = Start generating signature on next VSYNC (write) **NOTE:** SR18[0] must be a 1 to start the SG. SR18[0] is cleared when the SG is done.

The SG low- and high-byte results are read from Extension registers SR19 and SR1A, respectively.

- SR19[7:0]: These bits are the low byte of the 16-bit SG result from one video frame of signature data.
- SR1A[7:0]: These bits are the high byte of the 16-bit SG result from one video frame of signature data.

I.4 Signature Generator Sample Code

The following 'C' code example describes how a programmer captures eight signatures for any given display screen. It is assumed that the display screen is already being displayed and no blinking attributes (in text modes) are being displayed.

```
signature_capture ()          /* Capture eight signatures for any given mode */
   {
   unsigned int result,i,SR19,SR1A;
   int SIG [8];
   union REGS in;

   in.x.ax = 0x0100;          /* Shut off the cursor, if in text mode */
   in.x.cx = 0x2000;
   int86x (0x10,&in,&out,&seg);
   outp (0x3c4,6);            /* Unlock Extension registers */
   for (i = 0;i <= 7; i++) { /* Cycle through all pixel data bits */
      outp (0x3c4,0x18);              /* Arm SG and set for pixel data bit */
      outp (0x3c5, (2 | (i<<2)));     /* Reset */
      outp (0x3c5, (i << 2));         /* Select the data bit */
      outp (0x3c4,0x18);
      outp (0x3c5, (1 | (i << 2)));   /* and start the SG */
      result = inp (0x3c5);           /* Pre-read SG status */
      while ((result & 0x01) != 0) {  /* Wait until signature is done */
         outp (0x3c4,0x18);
         result = inp (0x3c5);        /* Read the status */
     }
      outp (0x3c4,0x19);              /* Get low signature byte */
      SR19 = inp (0x3c5);
      outp (0x3c4,0x1A);              /* Get high signature byte */
      SR1A = inp (0x3c5);
      SIG [i] = (SR1A << 8) + SR19;
  }                                   /* End of for */
  }
```

Appendix J

Pin-Scan Testing

J.1 Introduction

Pin-scan testing automatically verifies if CL-GD7548 pins have been properly soldered to a circuit board. This test detects pins that are either not connected to the board or shorted to a neighboring pin or trace. A circuit board tester is required when using the CL-GD7548 Pin-Scan Test mode. The frequency of the tester must be lower than 100 kHz.

Advantages of Pin-Scan Testing

The advantages of pin-scan testing are:

- Simple test patterns can verify full-board connectivity.
- During the test, the pins are automatically connected sequentially in a single chain around the CL-GD7548 so that the value on each output pin depends only on the values applied to all other pins, rather than on the internal state of the VGA processor.
- The pin-scan logic is strictly combinatorial so that no clock pulses are required.

J.2 Pin-Scan Test Performance

The pin-scan test is performed as follows:

1. To enter the Pin-Scan Test mode, as shown in Figure J-1, drive RESET# low at least 20 ns while TWR# is low and MD25 is high. Then, drive RESET# high to keep Extension register bit SR24[7] equal to '1'.
2. Drive all the input pins to '0'.
3. Verify that the values on the output pins match the predicted values, which are shown in the third column from the right of Table J-1.
4. On subsequent test cycles, individually drive each input pin to a '1', and verify that all the affected output pins change to the predicted values as shown in the second column from the right of Table J-1. In the table, pin numbers are listed according to the pin-scan order: RDYRTN# is the first input, and INTR is the last output.

   NOTE: Pin names in Table J-1 are for '486 or VESA® VL-Bus™ implementations. When configuring the CL-GD7548 for PCI Bus, a few pins either change pin names or are not connected.

5. To exit the Pin-Scan Test mode, drive the RESET# from low to high while TWR# is high, as shown in Figure J-1

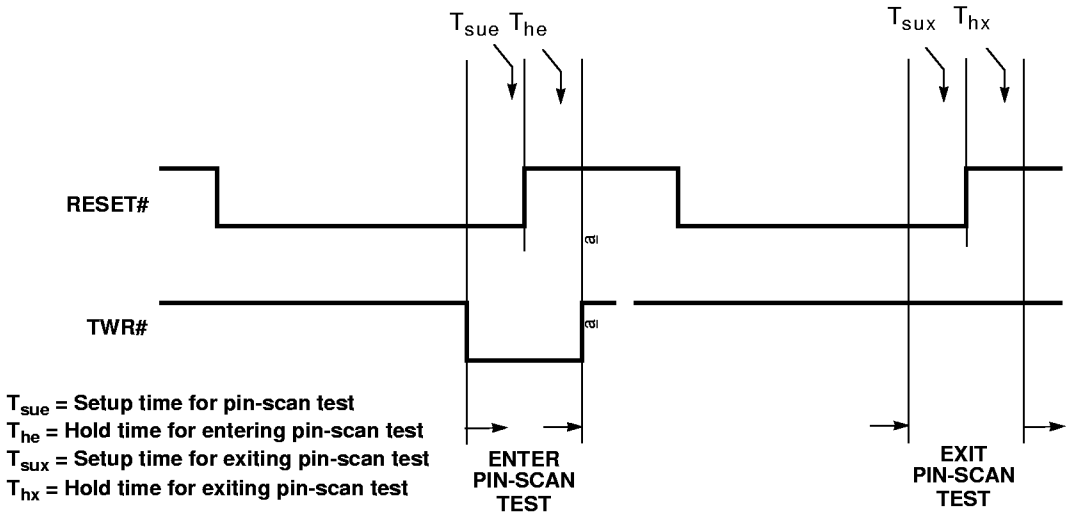


Figure J-1. Entering and Exiting the Pin-Scan Test Mode

Pins Not Tested

In the pin-scan test, the following pins are not tested:

- RESET# (pin 12) and TWR# (pin 100)
- All the power/ground pins and clock filter pins (MFILTER and VFILTER)
- RED, GREEN, and BLUE
- A7, A8, LDEV#, RDY#, and LCLK

J.3 Pin-Scan Test Results

During the test, if the value applied to an input pin is changed but none of the affected output pins change to the correct logic level in response, then that input pin is either shorted or not soldered correctly.

If the value applied to an input pin is changed, but *one (or some)* of the affected output pins do not change to the correct logic level in response, then that output pin is either shorted or not soldered correctly.

Table J-1. Pin-Scan Order

Pin No.	CL-GD7548 Pin Names for '486 Bus or VESA VL-Bus Interfaces	In/ Out	If all inputs = '0', predicted value of this pin is:	If all inputs except TWR# = '1', predicted value of this pin is:	CL-GD7548 Pin Names for PCI Bus Interfaces
8	RDYRTN#	In	0	1	IRDY#
9	ADS#	In	0	1	FRAME#
10	W/R#	In	0	1	IDSEL
11	M / IO#	In	0	1	No connection
13	BE3#	In	0	1	C / BE3#
14	BE2#	In	0	1	C / BE2#
15	BE1#	In	0	1	C / BE1#
16	BE0#	In	0	1	C / BE0#
17	A2	In	0	1	No connection
18	A3 / ZVP0	In	0	1	No connection
19	A4 / ZVP1	In	0	1	No connection
20	A5 / ZVP2	In	0	1	No connection
21	A6 / ZVP3	In	0	1	No connection
24	A9 / ZVP4	In	0	1	No connection
25	A10 / ZVP5	In	0	1	No connection
26	A11 / ZVP6	In	0	1	No connection
27	A12	In	0	1	No connection
28	A13	In	0	1	No connection
29	A14	In	0	1	No connection
30	A15	In	0	1	No connection
31	A16	In	0	1	No connection
32	A17	In	0	1	No connection
33	A18	In	0	1	No connection
34	A19	In	0	1	No connection
35	A20	In	0	1	No connection
37	A21	In	0	1	No connection
38	A22	In	0	1	No connection
39	A23	In	0	1	No connection
40	A24 / HIMEM0	In	0	1	No connection
41	A25 / HIMEM1	In	0	1	No connection

Table J-1. Pin-Scan Order *(cont.)*

Pin No.	CL-GD7548 Pin Names for '486 Bus or VESA VL-Bus Interfaces	In/ Out	If all inputs = '0', predicted value of this pin is:	If all inputs except TWR# = '1', predicted value of this pin is:	CL-GD7548 Pin Names for PCI Bus Interfaces
43	D31	In	0	1	AD31
44	D30	In	0	1	AD30
45	D29	In	0	1	AD29
46	D28	In	0	1	AD28
48	D27	In	0	1	AD27
49	D26	In	0	1	AD26
50	D25	In	0	1	AD25
51	D24	In	0	1	AD24
53	D23	In	0	1	AD23
54	D22	In	0	1	AD22
55	D21	In	0	1	AD21
56	D20	In	0	1	AD20
57	D19	In	0	1	AD19
58	D18	In	0	1	AD18
59	D17	In	0	1	AD17
60	D16	In	0	1	AD16
61	D15	In	0	1	AD15
63	D14	In	0	1	AD14
64	D13	In	0	1	AD13
65	D12	In	0	1	AD12
66	D11	In	0	1	AD11
68	D10	In	0	1	AD10
69	D9	In	0	1	AD9
70	D8	In	0	1	AD8
71	D7	In	0	1	AD7
72	D6	In	0	1	AD6
74	D5	In	0	1	AD5
75	D4	In	0	1	AD4
76	D3	In	0	1	AD3
77	D2	In	0	1	AD2

Table J-1. Pin-Scan Order *(cont.)*

Pin No.	CL-GD7548 Pin Names for '486 Bus or VESA VL-Bus Interfaces	In/ Out	If all inputs = '0', predicted value of this pin is:	If all inputs except TWR# = '1', predicted value of this pin is:	CL-GD7548 Pin Names for PCI Bus Interfaces
78	D1	In	0	1	AD1
79	D0	In	0	1	AD0
81	SLEEP# / ZVPCTL	In	0	1	SLEEP#
85	OSC / XVCLK	In	0	1	OSC / XVCLK
86	ACTI / DDCD / FCEVIDEO# / SBYI	In	0	1	ACTI / DDCD / FCEVIDEO# / SBYI
87	BLI / SUSPI	In	0	1	BLI / SUSPI
89	CLK32K	In	0	1	CLK32K
91	HSYNC	Out	1	0	HSYNC
93	VSYNC	Out	0	1	VSYNC
94	NTSC / PAL	Out	1	0	NTSC / PAL
95	CSYNC	Out	0	1	CSYNC
101	FCBLANK# / HREFI	In	0	1	FCBLANK# / HREFI
102	FPVEE<BIAS>	Out	1	1	FPVEE<BIAS>
103	DDCC / FCDCLK / VCLK	In	0	1	DDCC / FCDCLK / VCLK
105	FPBL	Out	0	1	FPBL
106	FPVCC	Out	1	0	FPVCC
108	FPDE / XCLKU	Out	0	1	FPDE / XCLKU
110	LFS	Out	1	0	LFS
112	LLCLK	Out	0	1	LLCLK
113	FPVDCLK	Out	1	0	FPVDCLK
114	FP0 / FCVCLK / ZVPCLKI	In	0	1	FP0 / FCVCLK / ZVPCLKI
115	FP1 / OVRW# / VACTI	In	0	1	FP1 / OVRW# / VACTI
116	FP2	Out	0	1	FP2
117	FP3 / MOD	Out	1	0	FP3 / MOD
118	FP4	Out	0	1	FP4
119	FP5	Out	1	0	FP5
120	FP6	Out	0	1	FP6
122	FP7	Out	1	0	FP7
123	FP8 / SBYST# / FCP0	In	0	1	FP8 / SBYST# / FCP0
125	FP9 / SUSPST# / FCP1	In	0	1	FP9 / SUSPST# / FCP1

Table J-1. Pin-Scan Order *(cont.)*

Pin No.	CL-GD7548 Pin Names for '486 Bus or VESA VL-Bus Interfaces	In/ Out	If all inputs = '0', predicted value of this pin is:	If all inputs except TWR# = '1', predicted value of this pin is:	CL-GD7548 Pin Names for PCI Bus Interfaces
126	FP10	Out	0	1	FP10
127	FP11	Out	1	0	FP11
128	FP12	Out	0	1	FP12
129	FP13	Out	1	0	FP13
130	FP14	Out	0	1	FP14
131	FP15	Out	1	0	FP15
133	FP16 / FCP2	In	0	1	FP16 / FCP2
134	FP17 / FCP3	In	0	1	FP17 / FCP3
135	FP18	Out	0	1	FP18
136	FP19	Out	1	0	FP19
137	FP20	Out	0	1	FP20
138	FP21	Out	1	0	FP21
139	FP22	Out	0	1	FP22
140	FP23	Out	1	0	FP23
141	FCP4	In	0	1	FCP4
142	FCP5	In	0	1	FCP5
143	FCP6	In	0	1	FCP6
144	FCP7	In	0	1	FCP7
146	TVON / XRDACCS	Out	0	1	TVON / XRDACCS
147	FCESYNC# / VSI	In	0	1	FCESYNC# / VSI
148	PROG	Out	1	1	PROG
149	SW1	In	0	1	SW1
150	SW2	In	0	1	SW2
151	MD31	In	0	1	MD31
152	MD30	In	0	1	MD30
153	MD29	In	0	1	MD29
154	MD28	In	0	1	MD28
155	MD27	In	0	1	MD27
156	MD26	In	0	1	MD26
157	MD25 / FCPU	In	0	1	MD25 / FCPU

Table J-1. Pin-Scan Order *(cont.)*

Pin No.	CL-GD7548 Pin Names for '486 Bus or VESA VL-Bus Interfaces	In/ Out	If all inputs = '0', predicted value of this pin is:	If all inputs except TWR# = '1', predicted value of this pin is:	CL-GD7548 Pin Names for PCI Bus Interfaces
158	MD24	In	0	1	MD24
159	MD23	In	0	1	MD23
160	MD22	In	0	1	MD22
161	MD21 / S46PU	In	0	1	MD21 / S46PU
163	MD20 / SLEEPPU	In	0	1	MD20 / SLEEPPU
164	MD19 / XCLKPU	In	0	1	MD19 / XCLKPU
165	MD18	In	0	1	MD18
166	MD17	In	0	1	MD17
167	MD16 / PCIPU	In	0	1	MD16 / PCIPU
169	CAS3# / WE3#	In	0	1	CAS3# / WE3#
170	CAS2# / WE2#	In	0	1	CAS2# / WE2#
171	MA9	Out	0	0	MA9
172	MA8	Out	1	1	MA8
173	MA7	Out	0	0	MA7
174	MA6	Out	1	1	MA6
175	MA5	Out	0	0	MA5
176	MA4	Out	1	1	MA4
177	MA3	Out	0	0	MA3
178	MA2	Out	1	1	MA2
179	MA1	Out	0	0	MA1
180	MA0	Out	1	1	MA0
181	CAS# / WE#	In	0	1	CAS# / WE#
182	OE#	Out	0	1	OE#
183	RAS0	Out	1	0	RAS
184	RAS1	Out	0	1	RAS1
186	MD15	In	0	1	MD15
187	MD14	In	0	1	MD14
188	MD13	In	0	1	MD13
189	MD12	In	0	1	MD12
190	MD11	In	0	1	MD11

Table J-1. Pin-Scan Order *(cont.)*

Pin No.	CL-GD7548 Pin Names for '486 Bus or VESA VL-Bus Interfaces	In/ Out	If all inputs = '0', predicted value of this pin is:	If all inputs except TWR# = '1', predicted value of this pin is:	CL-GD7548 Pin Names for PCI Bus Interfaces
191	MD10	In	0	1	MD10
193	MD9	In	0	1	MD9
194	CAS0# / WE0#	In	0	1	CAS0# / WE0#
195	CAS1# / WE1#	In	0	1	CAS1 / WE1#
196	MD8	In	0	1	MD8
197	SW0 / MCLK / XMCLK	In	0	1	SW0 / MCLK / XMCLK
202	MD7	In	0	1	MD7
203	MD6	In	0	1	MD6
204	MD5	In	0	1	MD5
206	MD4	In	0	1	MD4
207	MD3	In	0	1	MD3
208	MD2	In	0	1	MD2
1	MD1	In	0	1	MD1
2	MD0	In	0	1	MD0
5	INTR	Out	1	1	INTR#

Appendix K

Programming for Extended Display Memory Modes

K.1 Introduction

The CL-GD7548 is capable of supporting a wide range of Extended VGA and Super VGA high-resolution display modes on both LCDs and CRT monitors, including the following:

- 1280 × 1024 CRT monitors: up to 16 colors (interlaced)
- 1024 × 768 CRT monitors: up to 256 colors
- 800 × 600 LCDs and CRT monitors: up to 64K colors
- 640 × 480 LCDs and CRT monitors: up to 16M colors

In this appendix, the Extended VGA display modes are described in terms of:

- Display memory organizations:
  - — Planar mode: 16-color [Section K.2.1]
  - — Packed-pixel modes:
    - — 256-color [Section K.2.2]
    - — Direct-color (32K and 64K colors) [Section K.2.3]
    - — Mix (either 32K-color or 256-color) [Section K.2.4]
    - — True-color 24-bit (16M colors) [Section K.2.5]
- Extended display memory addressing and mapping techniques [Section K.3]
- Programming examples demonstrating how to implement some of these features [Section K.4]

For information on all the extended display modes supported by the CL-GD7548, refer to Chapter 4.

K.2 Comparison of Planar and Packed-Pixel Display Memory Modes

Table K-1 compares the display memory organization of the planar and packed-pixel memory modes.

Table K-1. Comparison of Planar Mode and Packed-Pixel Display Memory Modes

Item of Comparison	Planar Display Memory Mode	Packed-Pixel Display Memory Mode
The setting for CL-GD7548 Extension register SR7[0]	Extension register SR7[0] = 0	Extension register SR7[0] = 1
Number of colors displayed	Only up to 16 colors can be displayed at one time.	256, 32K, 64K, and 16M[a] colors can be displayed at one time
Bits per pixel	4 bits	1, 4, 8, 15, 16, or 24 bits[a]
Placement of pixel data in display memory	Four display memory planes are used. Each pixel is dispersed across the four display memory bit planes.	Only one display memory plane is used. All pixel data are in this same display memory plane.
Address generation	Address bits are read across the four display memory bit planes.	CL-GD7548 memory controller handles all address generation. To the CPU, the display memory appears as follows: • In segmented mode, display memory appears as if it were sequential, with 64 Kbytes of linearly addressable display memory in segmented mode. • In linear addressing mode, display memory appears as 1 or 2 Mbytes of linearly addressable memory.
Page address mapping	Only display mode resolutions above 1024 × 768 require page address mapping.	All display mode resolutions require page address mapping.

[a] When Extension register SR7[0] = 1, the default display mode is the 256-color packed-pixel mode, with 8 bits per pixel.

K.2.1 Planar Mode: 16-Color

The CL-GD7548 16-color planar display mode is enabled when Sequencer register bit SR4[2] is set to '1' and bit SR4[3] is set to '0'. This standard IBM VGA display mode requires 4 bits per pixel. This VGA mode represents a pixel by dispersing bits of information across 4 display memory planes, with 1 bit per plane. The display memory is organized as bytes, with 8 pixels per byte.

The memory planes are overlaid in the CPU memory address space so that each plane occupies the same CPU address. For read/write operations, the CPU can access any of these planes independently by programming the Sequencer register SR2. Figure K-1 shows the display memory organized in four planes for the 16-color planar mode. The color information for each pixel is stored in corresponding bits across four planes. The figure also depicts how bank 0 and bank 1, which are used in paging, are aligned across each plane.

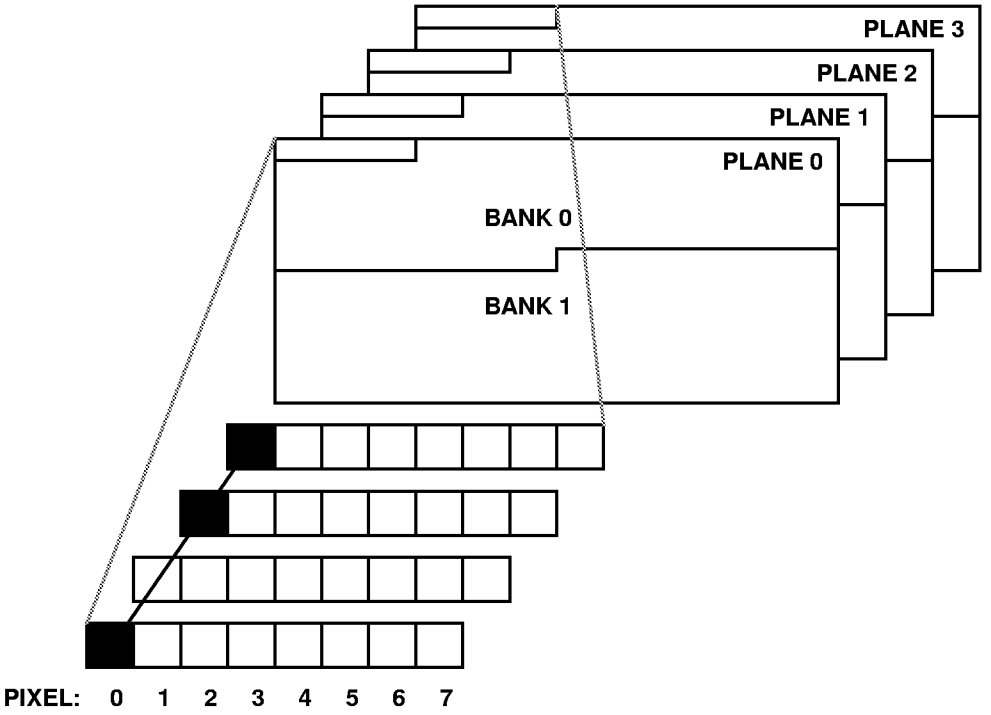


Figure K-1. 16-Color Planar Modes

The standard IBM VGA supports 256 Kbytes of display memory. In 16-color planar mode, the display memory is divided into four planes with 64 Kbytes per plane. Normally, the 64-Kbyte segment of each plane is mapped in A0000h to AFFFFh, and the CPU can easily address each of the display memory planes.

However, a problem arises for those display modes that require more than 64 Kbytes of addressable video memory per plane. For example, the 1024×768, 16-color planar mode requires 98,304 bytes, or an additional 32,768 bytes more addressable display memory per plane. The problem of having more than 64 Kbytes of addressable display memory is solved by using the extended display memory addressing techniques discussed in Section K.3.

K.2.2 Packed-Pixel Mode: 256-Color Display Mode

By setting Extension register bit SR7[0] to '1', the 256-color packed-pixel mode is enabled. When Sequencer register bit SR4[3] is set to '1', this mode becomes Chain-4 mode.

The following figure shows how 8-bit-per-pixel (packed-pixel mode) bytes are stored in terms of the physical plane organization.

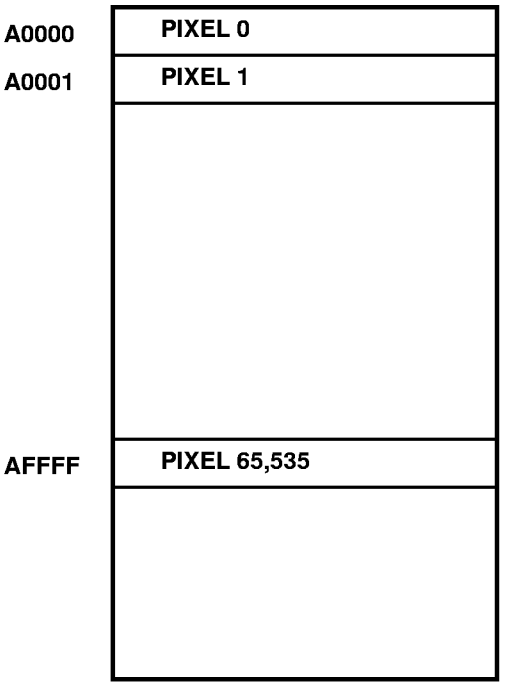


Figure K-2. 256-Color Packed-Pixel Mode

The CL-GD7548 on-chip memory controller makes this organization completely transparent. Hence, to the CPU, addressing is sequential. For example, at segment A0000h, pixel 0 resides at offset 0, pixel 1 resides at offset 1, and pixel 65,535 resides at offset 65,535.

To address display memory that is beyond the 64-Kbyte segment boundary, the CL-GD7548 supports a display memory paging technique that allows up to 2 Mbytes of display memory to be paged into the CPU address range.

In Linear Memory Addressing mode, display memory paging is not required.

K.2.3 Packed-Pixel Mode: Direct-Color (32K and 64K Colors) Display Mode

The CL-GD7548 supports direct-color packed-pixel modes that are capable of displaying up to either 32,768 (32K) colors or 65,536 (64K) colors simultaneously, at screen resolutions of up to 800 × 600. Color information used to display these colors simultaneously is:

- 15 bits per pixel for 32K colors
- 16 bits per pixel for 64K colors

To enable direct-color display modes, Extension register bit SR7[0] is set to 1, and then the CL-GD7548 internal palette DAC is set to direct-color modes by programming Extension register HDR (the Hidden DAC register).

Figure K-3 shows how 15-bit pixel data (for 32K colors) is stored relative to the physical plane organization. The RGB color information is stored in RGB 5-5-5 format (5 bits each for red, green, and blue). Two bytes per pixel are used for storing the color information. The most-significant bit (bit 15) is ignored.

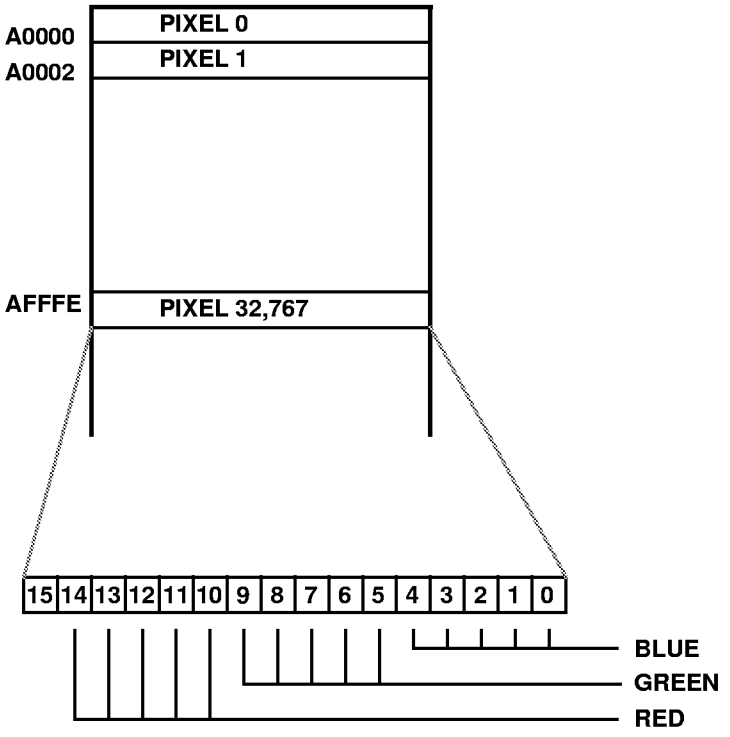


Figure K-3. 32,768 Color (15-Bit) Packed-Pixel Mode

Figure K-4 shows how 16-bit pixel data (for 64K colors) is stored in terms of the physical plane organization. The RGB color information is stored in RGB 5-6-5 format (5 bits of red, 6 bits of green, and 5 bits of blue). Two bytes per pixel are used for storing the color information.

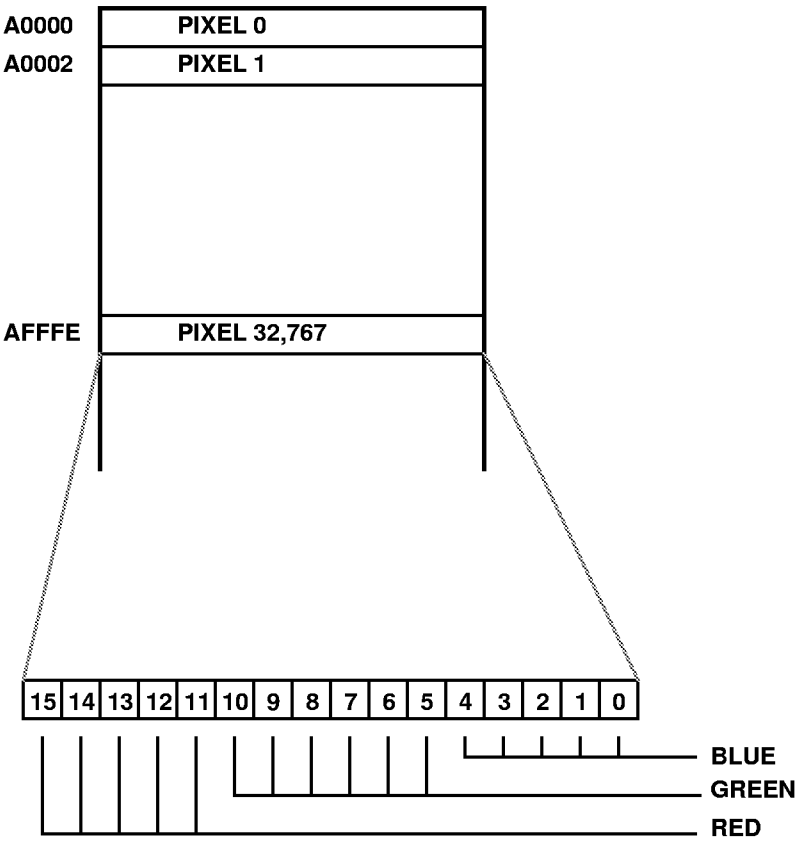


Figure K-4. 65,536 Color (16-Bit) Packed-Pixel Mode

As in the 256-Color Packed-Pixel Display mode (refer to Section K.2.2), the CL-GD7548 on-chip memory controller makes this organization completely transparent, and so to the CPU, addressing is sequential. For example, at segment A0000h, pixel 0 resides at offset 0 and offset 1; pixel 1 resides at offset 2 and offset 3; and pixel 32,767 resides at offset 65,534 and offset 65,535.

To address display memory that is beyond the 64-Kbyte segment boundary, the CL-GD7548 supports a display memory paging technique that allows up to 2 Mbytes of display memory to be paged into the CPU address range.

K.2.4 Packed-Pixel Mode: Mixed (Either 32K-Color or 256-Color) Display Mode

The CL-GD7548 supports a Mixed-Color mode that is capable of combining RGB 5-5-5 format (32K-color packed-pixel mode) and 8-bit-per-pixel format (256-color packed-pixel mode).

To enable the Mixed-Color mode, Extension register SR7[0] is set to '1', and then the CL-GD7548 internal palette DAC is set to a mixed-mode format by programming Extension register HDR (the Hidden DAC register).

In the mixed-mode operation, pixel data bit [15] is used to choose between the 32K-color and the 256-color modes as follows:

- If bit[15], the most-significant bit of the 16-bit pixel data, is '0', then bits [14:0] are treated as RGB 5-5-5 data.
- If the most-significant bit is set to '1', then bits [7:0] choose a palette entry in the palette DAC LUT (lookup table) to display 256 colors simultaneously, and bits [14:8] are ignored.

Figure K-5 shows how the mixed-color packed-pixel data is stored in terms of the physical plane organization.

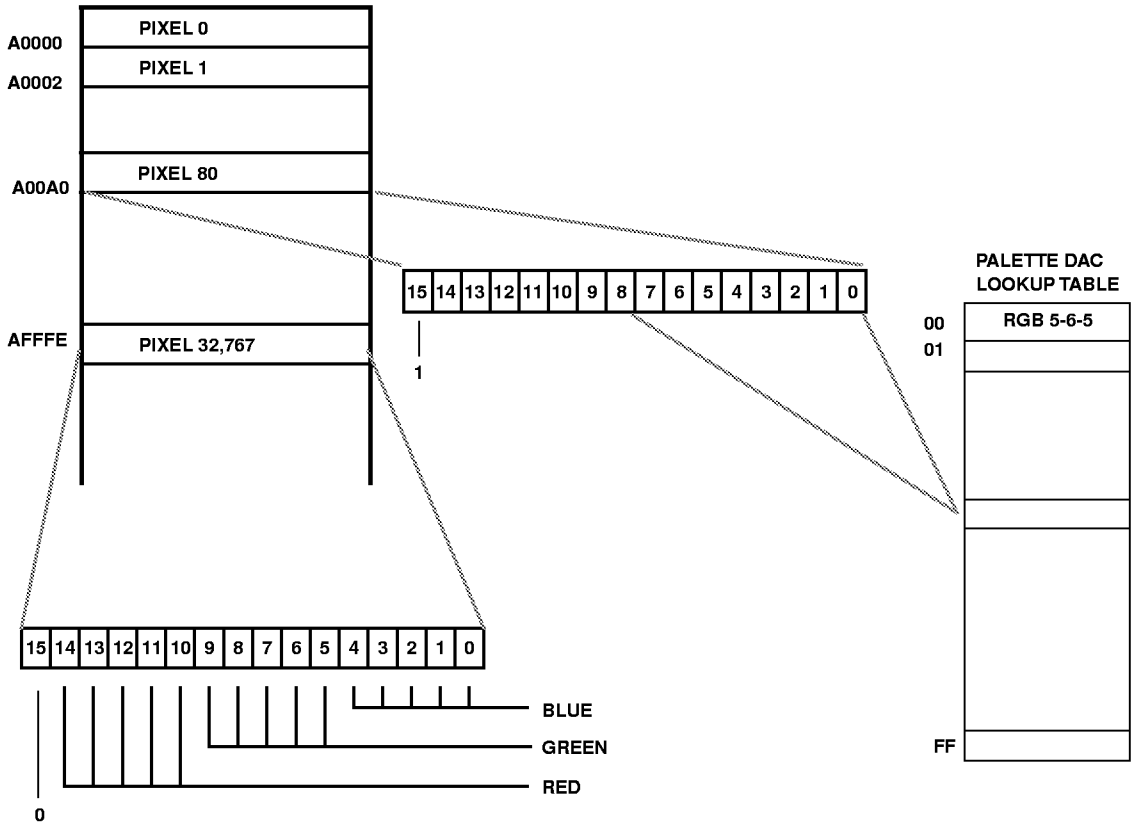


Figure K-5. Mixed-32,768-Color (15-Bit) Packed-Pixel Data Format

The CL-GD7548 on-chip memory controller makes this organization completely transparent, and so to the CPU, addressing is sequential. For example, at segment A0000h, pixel 0 resides at offset 0 and offset 1; pixel 1 resides at offset 2 and offset 3; and pixel 32,767 resides at offsets 65,534 and 65,535.

To address display memory that is beyond the 64-Kbyte segment boundary, the CL-GD7548 supports a display memory paging technique that allows up to 2 Mbytes of display memory to be paged into the CPU address range.

K.2.5 Packed Pixel Mode: True Color, 24-Bit (16.8 Million Colors)

The CL-GD7548 supports a True-Color mode capable of displaying 16.8 million colors simultaneously at screen resolutions of up to 640 × 480. To display 16.8 million colors in TARGA™-compatible mode, 24 bits per pixel of RGB color information (8 bits each for red, green, and blue) are used.

To enable the Mixed-Color mode, Extension register SR7[0] is set to '1', and the CL-GD7548 internal palette DAC is set to a True-Color-mode format by programming the Hidden DAC register (HDR).

Figure K-6 shows how 24-bit pixel data is stored in terms of the physical plane organization. Three bytes per pixel are used for storing the color information.

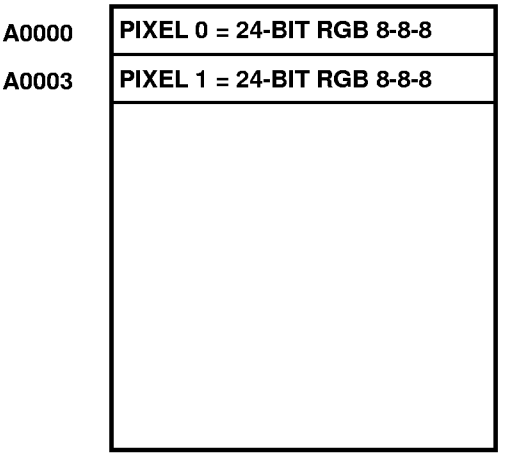


Figure K-6. 24-Bit True Color Packed-Pixel Mode

The CL-GD7548 on-chip memory controller makes this organization of the physical plane completely transparent. Hence, to the CPU, the byte addressing is sequential. For example, at segment A0000h, pixel 0 resides at offset 0 to offset 2 as follows:

- Blue color information at offset 0
- Green color information at offset 1
- Red color information at offset 2

Similarly, pixel 1 resides at offset 3 to offset 5; pixel 21,845 resides at offset 65,533 to offset 65,535.

To address display memory beyond the 64-Kbyte-segment boundary, the CL-GD7548 supports a display memory paging scheme that allows up to 2 Mbytes of display memory to be paged into the CPU address range.

K.3 Extended Display Memory Addressing Techniques

The CL-GD7548 addresses up to 2 Mbytes of display memory. However, in the DOS environment, at A0000h–BFFFFh, only 128 Kbytes of address space are reserved for video display memory. As a result, if the CL-GD7548 has to share this memory space with MDA, Hercules®, or CGA controllers, it is left with only a single 64-Kbyte segment from A0000h to AFFFFh.

To extend the address space for the display memory, the CL-GD7548 supports the techniques shown in Table K-2 for display memory address mapping.

Table K-2. Display Memory Address Mapping Techniques

Mapping Technique	Reference	Description of Mapping Technique
Linear	Section K.3.1	Allows display memory to be mapped to a continuous 2-Mbyte region above the standard 1-Mbyte DOS address space.
Single-Page	Section K.3.2	Allows one 64-Kbyte segment of display memory to be mapped into CPU address space.
Dual-Page	Section K.3.3	Allows two 32-Kbyte segments of display memory to be mapped into CPU address space.

K.3.1 Linear Address Mapping

Linear address mapping allows display memory to be mapped to a continuous 2-Mbyte region above the standard 1-Mbyte DOS address space. This action allows application programs to access the display memory as a linearly addressed string of up to 2 Mbytes, instead of being constrained to a 64-Kbyte window.

To use the CL-GD7548 linear-addressing feature:

- The drivers that are used must be written so as to ensure compatibility with the operating system.
- Extension register GRB[0] must be set to '0'.

K.3.2 Single-Page Address Mapping

Single-page address mapping extends the address space for video display memory. As shown in Figure K-7 below, and as described in this section, single-page address mapping allows the following actions:

- Any 64-Kbyte segment (or 'page') of display memory can be mapped into address range A0000h–AFFFFh of the CPU host address.
- The Start Page Address can begin:
  - — At any 4-Kbyte boundary of 1-Mbyte display memory
  - — At any 16-Kbyte boundary of 2-Mbyte display memory

After the 64-Kbyte segment of display memory is mapped into the host CPU address range, it can be accessed by the CPU for read and write operations.

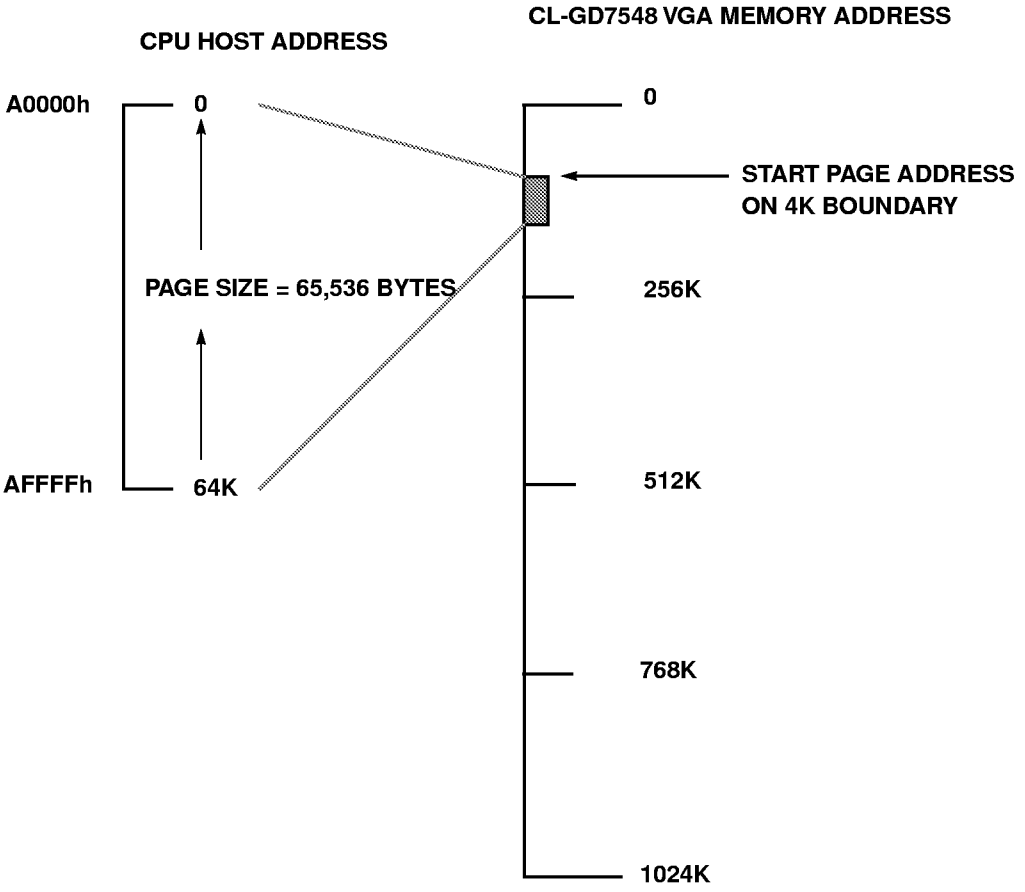


Figure K-7. Single-Page Address Mapping Technique

To select a 64-Kbyte segment of display memory and map it into the host CPU address range, take the following actions:

- To always select only a 64-Kbyte segment of display memory (and never two 32-Kbyte segments), select Offset Register 0 by setting the Extension register bit GRB[0] to '0'.
- To select the desired address, program Extension register GR9 (Offset register 0). The value that is programmed into these register bits is then added to CPU address bits to provide the address for mapping the display memory.

Figure K-8 and Figure K-9 show how Offset register 0 and the CPU Address bits are added to generate the display memory address.

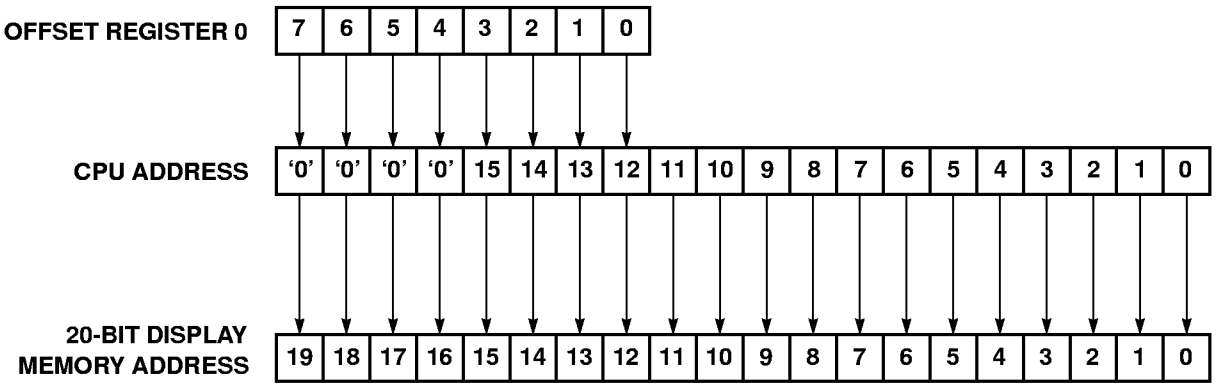


Figure K-8. 64K Page-Mode Remapping Adder Alignment for 1-Mbyte Memory

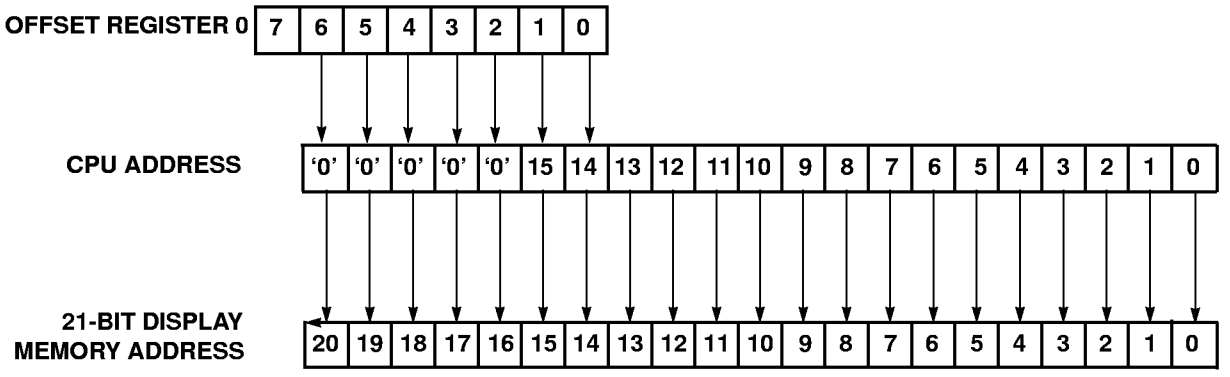


Figure K-9. 64K Page-Mode Remapping Adder Alignment for 2-Mbytes Memory

K.3.3 Dual-Page Address Mapping

Dual-page address mapping is used for read-modify-write operations on large blocks of data. As shown in Figure K-10, and as described in this section, dual-page address mapping allows the following:

- Two 32-Kbyte segments (or 'pages') of display memory can be mapped into address ranges A0000h–A7FFFh and A8000h–AFFFFh of the host CPU address.
- The 32-Kbyte segments may be either separate or overlapping.
- The Start Page Address can begin at any 4-Kbyte boundary of display memory.

After the two 32-Kbyte segments of display memory are mapped into the CPU host address range, they can be accessed by the CPU for read and write operations. This action allows for block transfers of data bits, by using repeated 'move string' DMA instructions.

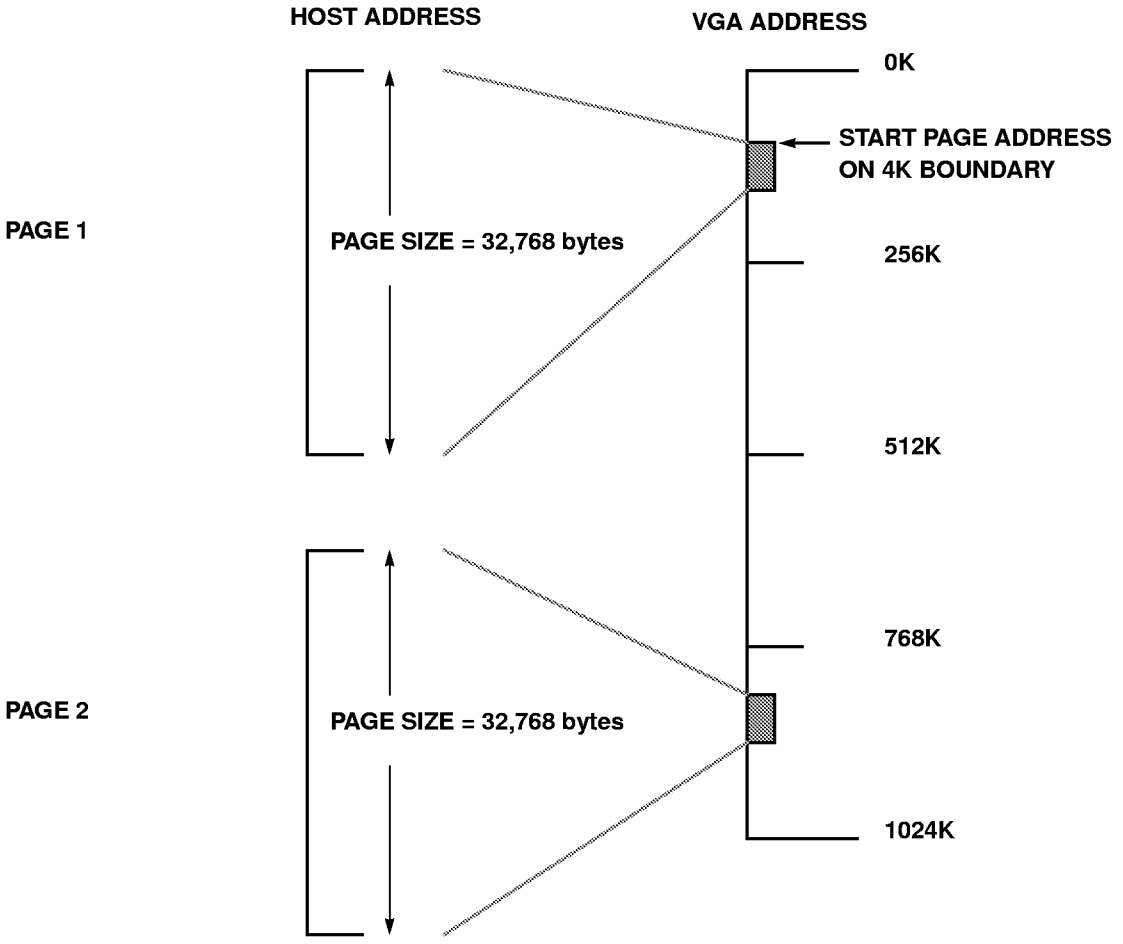


Figure K-10. Dual-Page Address Mapping Scheme

To select any two separate or overlapping 32-Kbyte segments of display memory and then map them into the CPU host address range, perform the following actions:

- Select which one of the two CL-GD7548 Offset registers is used to calculate the resulting value of the display memory address as follows:
  - — To select Offset register 0, set Extension register GRB[0] to '1'.
  - — To select Offset register 1, clear Extension register GRB[0] to '0'.
- Program the start page addresses as follows:
  - — To determine the start address of page 1, program Offset register 0 in Extension register GR9[7:0].
  - — To determine the start address of page 2, program Offset register 1 in Extension register GRA[7:0].
- The start page address can begin
  - — At any 4-Kbyte boundary of 1-Mbyte display memory
  - — At any 16-Kbyte boundary of 2-Mbyte display memory

For a page size of 32 Kbytes, Figure K-11 shows how an Offset register (either 0 or 1) and CPU address bits are added to find the resulting display memory address of 1-Mbyte display memory. Note that in the figure, bit 15 of the CPU address selects whether Offset register 0 or Offset register 1 is used for the display memory addressing.

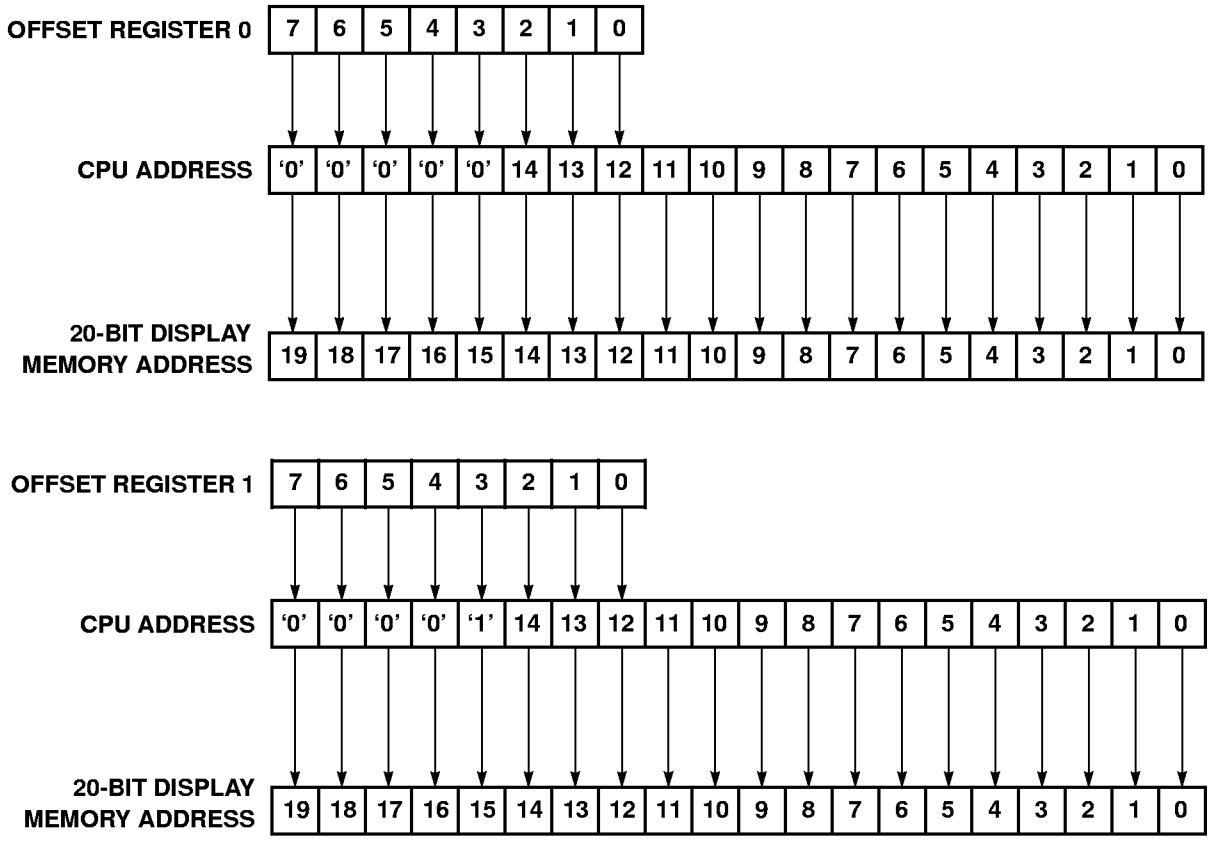


Figure K-11. 32K Page-Mode Remapping Adder Alignment for 1-Mbyte Display Memory

The following table lists the CL-GD7548 Extension registers that control the CPU base address and display memory mapping functions:

Table K-3. CL-GD7548 Extension Registers

Function	Name of Extension Register	Port	Index	Bit	Value
Single-page	GRB: Graphics Controller Mode Extensions	3CF	0B	GRB[0]	0
Dual-page	GRB: Graphics Controller Mode Extensions	3CF	0B	GRB[0]	1
Offset register granularity: 4 Kbyte	GRB: Graphics Controller Mode Extensions	3CF	0B	GRB[5]	0
Offset register granularity:16 Kbyte	GRB: Graphics Controller Mode Extensions	3CF	0B	GRB[5]	1
Linear addressing	SR7: Graphics Controller Mode Extensions	3C4	07	SR7[7:4]	15...0
Offset register 0	GR9: Offset register 0	3CF	09	GR9[7:0]	255...0
Offset register 1	GRA: Offset register 1	3CF	0A	GRA[7:0]	255...0

K.4 VGA Programming Examples

This section provides the CL-GD7548 software programming examples.

K.4.1 Unlocking the CL-GD7548 Extension Registers

To identify a CL-GD754X VGA as the VGA controller that is being used, call the extended VGA BIOS inquiry function by using INT 10h. However, if an extended VGA BIOS is not available, then identify a controller by:

- Programming the Unlock All Extension register (Extension register SR6) to enable the CL-GD7548 extension registers.
- Reading the Chip ID register (Extension register CR27).

The following code show the steps to enable/disable CL-GD7548 extended register access:

```
Enable Extension Register Macro:
;    Function:
;    Enabling Extensions
;     Calling Protocol:
;    enable_extensions

     enable_extensions macro
     mov   dx,03c4h             ; Select Extended register SR6 i/o port
     mov   al,06h               ; Unlock All Extension register index
     mov   ah,12h               ; Load with xxx1x010 to enable extension
     out   dx,ax                ; Write index and data
     endm


Disable Extension Register Macro:

     ; Function:
     ;     Disabling Extensions

     ; Calling Protocol:
     ;     disable_extensions

     disable_extensions macro
     mov   dx,03c4h             ; Select Extended register SR6 I/O port
     mov   al,06h               ; Unlock All Extension register index
     mov   ah,00h               ; Load with 00 to disable extension
     out   dx,ax                ; Write index and data
     endm
```

K.4.2 Identifying a CL-GD7548 VGA Controller

Extension register CR27 (Chip ID register) is used to identify a CL-GD754X VGA controller. The following sample code shows how to program the extension registers to read the chip ID for a CL-GD7548 and how to determine the chip type.

```
;Function: Identify Cirrus Logic CL-GD7548 Super VGA LCD Controller
;Input Parameters:;none
;Output Parameters:
;      AL =00    ID FAILED
;      AL =0B    CL-GD7548
; Calling Protocol:
; VGAchip = Id_CL-GD7548()*/

_Id_CL-GD7548 proc far
      mov      dx,03c4h    ; Load Unlock All Extensions I/O port
      mov      al,06       ; Load SR6 register index
      out      dx,al       ; Write index and data register
      inc      dx          ;
      in       al,dx       ; Read data register
      mov      ah,00h      ;
      cmp      al,12h      ; Check SR6 read back value
      jne      chk29       ; See if this is a CL-GD7548 (no SR6)
exit: mov      al,ah       ; Return in AL the chip ID value
      xor      ah,ah       ; zero AH
      ret
chk29:mov      dx,03d4h    ; Load chip ID CR27 I/O port return
      mov      al,27h      ; Select CR27 index
      out      dx,al       ;
      inc      dl          ;
      in       al,dx       ; Read chip ID
      and      al,fch      ; Clear bits 0 and 1
      cmp      al,2ch      ; Check for CL-GD7548 ID
      mov      al,0bh      ;
      je       exit        ; Yes it was
      xor      al,al       ; No it wasn't
      jmp      exit
_Id_CL-GD7548 endp
```

K.4.3 Initializing the CL-GD7548 Extended Display Mode By Using an INT 10h Call

The following listing is used to initialize the desired extended display mode by calling the Cirrus Logic VGA BIOS set mode function. (This example is for the CL-GD7548.)

```
; Set display mode
; Set up Extended display mode supported by CL-GD7548 VGA BIOS
;
; Calling Protocol
; al = desired CL-GD7548 display mode number
; Return
; al = current display mode
;
Set_Video_Mode proc near
      mov ah,0    ; VGA BIOS setmode function 0
      int 10H     ; Call VGA BIOS interrupt 10 Hex, al = mode number
      mov ah,0Fh  ; VGA BIOS get current display mode number
      int 10h     ;
      ret         ; Return current display mode number in al
Set_Video_Mode endp
```

K.4.4 Programming Mapping Registers

K.4.4.1 Setting Up Single-Page Mapping

The following code listing shows how to program Extension register GRB to set up single-page mapping.

```
; Single Page Mapping
; Set up Single-Page Mapping

; Calling Protocol
;     Set_Single_Page

Set_Single_Page proc near
;Set up CPU Base Address Control register for single-page, 64K page size
      mov      dx,03ceh    ; Select Extension register I/O port GRB
      mov      al,0bh      ; Select GRB register index
      out      dx,al       ; Write index register
      inc      dx          ; Increment dx to read data port
      in       al,dx       ; Read data
      and      al,feh      ; Apply mask to set GRB[0] = 0
      out      dx,al       ; Write I/O port with new data
      ret
Set_Single_Page   endp
```

K.4.4.2 Programming for Single-Page Address Mapping with a 64-Kbyte Segment

The following code listing shows how to program Offset Register 0 (GR9) to map a desired page (64 Kbytes) of display memory into the CPU address.

```
; Function:
; Load the Single-Page Offset Register 0 with the new start address
; of a 64-Kbyte segment
; Input:
; bl = 0..255
; Page number for start address of desired 64-Kbyte segment
;
; Calling Protocol:
; Select_Single_Page

Select_Single_Page macro
      mov      dx,3CEh     ; Load Extension register GR9 I/O port
      mov      al,09h      ; Load Offset Register 0 index
      mov      ah,bl       ; Get page number
      out      dx,ax       ; Program selected page
Select_Single_Page endm
```

K.4.4.3 Setting Up Dual-Page Address Mapping

The following code listing shows how to program Extension register GRB to set up dual-page mapping.

```
; Dual-Page Mapping
;      Set up Dual-Page Mapping
;
; Calling Protocol
;      Set_Dual_Page

Set_Dual_Page proc far

; Set up Extension register GRB for dual-page size
      mov      dx,03ceh    ; Select Extension register I/O port
      mov      al,0bh      ; Select CPU Base Address register index
      out      dx,al       ; Write Index register
      inc      dx          ; Increment dx to read data port
      in       al,dx       ; Read data
      or       al,01h      ; Data = enable 32K page size, dual page
      out      dx,al       ; Write I/O port with new data
      ret
Set_Dual_Page  endp
```

K.4.4.4 Programming for Dual-Page Address Mapping with a 32-Kbyte Segment

The following code listing shows how to program Extension registers GR9 and GRA to set up dual-page remapping with a 32-Kbyte segment.

```
; Function:
; Load the Dual-Page Remapping registers with the new star address
; at 32-Kbyte segments

; Input:
; bl = 0..255  page number for segment mapped to A0000h-AFFFFh
; bh = 0..255  page number for segment mapped to A8000h-AFFFFh

; Calling Protocol:
;      Select_Dual_Pages

Select_Dual_Pages macro
      mov      dx,3CEh     ; Load extension register I/O port
      mov      al,09h      ; Load CPU Base Addr. Mapping Register A index
      mov      ah,bl       ; Get page number for A0000h-A7FFFh mapping
      out      dx,ax       ; Program selected page
      mov      al,0ah      ; Load CPU Base Addr. Mapping Register A index
      mov      ah,bh       ; Get page number for A8000h-AFFFFh mapping
      out      dx,ax       ; Program selected page
Select_Dual_Pages endm
```

Appendix L

Hardware Configuration Notes

L.1 Introduction

The CL-GD7548 memory data pins MD[25:16] are used to program the CL-GD7548 for operation. The resistance that appears on the memory data pins is read during the low-to-high transition of the system reset pulse, and the resulting status of the inputs is stored in Extension registers SR22 and SR24. If an external pull-up resistor:

- Is not present on a memory data pin, the pin is read as low because of the CL-GD7548 internal pull-down resistor.
- Is present on a memory data pin, the pin is read as high.

The hardware configuration data can be latched into Extension registers SR22 and SR24 by programming software for the high-to-low transition of Extension register bit SR24[3]. This action can be used if the system reset is not long enough to read the hardware configuration data.

NOTE: Some of the software-programmable register bits that are used to select the desired function of some multi-function pins are covered in the Cirrus Logic 'motherboard' application notes in the *CL-GD754X Application Book*.

L.2 Configuration Summary

Each of the CL-GD7548 memory data pins MD[25:16] has an internal pull-down resistor. If no pull-up resistor is attached, the default is a '0'. If a 1 is to be loaded into the latch associated with a given MD line, an external pull-up resistor (typically 10 kΩ or less) must be added. The following table provides an overview of the configuration bits. The last column describes the CL-GD7548 pin functions when a pull-up resistor is installed on the CL-GD7548 MD line.

Table L-1. Configuration Bits

CL-GD7548 Pin (Memory Data Bit)	Extension Register	Extension Register Setting	Function of CL-GD7548 Pin When Pull-up Resistor Is Installed on the Memory Data Pin
157 (MD25)	SR24[7]	0	Normal operation – No Feature Connector
		1	Feature Connector enabled
158 (MD24)	–	0	Don't care
		NA	Not supported. Pull-up resistor must not be used.
159 (MD23)	–	0	Don't care
		NA	Not supported. Pull-up resistor must not be used.
160 (MD22)	–	0	Normal I/O
		NA	Not supported. Pull-up resistor must not be used.
161 (MD21)	SR22[5]	0	Select Sleep Address 3C3h (for VL-Bus mode only)
		1	Select Sleep Address 46E8h (for VL-Bus mode only)
163 (MD20)	SR22[4]	0	Normal operation – No Hardware Sleep capability
		1	Hardware Sleep capability
164 (MD19)	SR22[3]	0	Select internal memory clock (MCLK) and video clock (VCLK)
		1	Select external memory clock and video clock (for test purposes only)
165 (MD18)	–	0	Don't care
		NA	Not supported. Pull-up resistor must not be used.
166 (MD17)	–	0	Don't care
		NA	Not supported. Pull-up resistor must not be used.
167 (MD16)	SR22[0]	0	Select VESA VL-Bus
		1	Select 32-bit PCI bus

L.3 Configuration Details

L.3.1 PCI Bus Configurations

To configure the CL-GD7548 for the 32-bit PCI bus, an external pull-up is placed on the MD16 / PCIPU pin. When a pull-up is placed on:

- The MD16 / PCIPU pin, a 1 is read into Extension register SR22[0]. This configuration sets the PCI bus burst cycle to a minimum of 8 host CPU clock cycles.

L.3.2 VESA® VL-Bus™ Configurations

The VESA VL-Bus is the default CPU bus configuration for the CL-GD7548. No external pull-up is placed on the MD16 / PCIPU pin, which reads back a 0 into Extension register SR22[0].

L.3.3 External Clock Configuration

To configure the CL-GD7548 for external XMCLK and XVCLK inputs, an external pull-up is placed on the MD19 / XCLKPU pin. As a result, a 1 is read back into Extension register SR22[3], which powers-down the internal clock synthesizers for MCLK and VCLK and enables the external XMCLK and XVCLK inputs.

L.3.4 Sleep Address Configuration

To configure the CL-GD7548 for a sleep address, an external pull-up is placed on the MD20 / SLEEPPU pin, which reads back a 1 into Extension register SR22[4]. To select a sleep address of:

- 46E8h, an external pull-up is also placed on the MD21 / S46PU pin, which reads back a 1 in Extension register SR22[5].
- 3C3h (the default sleep address), no pull-up is placed on the MD21 / S46PU pin, which reads back a 0 in Extension register SR22[5].

L.3.5 Feature Connector Configuration

To configure the CL-GD7548 for the Feature Connector Port, an external pull-up is placed on the MD25 / FCPU pin. As a result, a 1 is read back into Extension register SR24[7] on the low-to-high transition of the system reset pulse and all appropriate CL-GD7548 pins and registers are configured for the Feature Connector video port.

NOTE: The options for fast VESA VL-bus (>33 MHz) on MD16/SR22[2] and the expanded PCI burst cycle (16 host CPU clock cycles) on MD23/SR22[7] are no longer supported on the CL-GD7548.

Appendix M

Memory-Mapped I/O

M.1 Introduction

The CL-GD7548 allows memory-mapped I/O accesses to occur to the BitBLT-control registers discussed in Appendix A. (That is, application programs can access the BitBLT-control registers as memory locations.) When multiple registers must be changed at once, the memory-mapped I/O method of accessing the BitBLT-control registers can occur up to four times faster than using register I/O.

During a memory-mapped I/O access, the register address is implied in the address rather than being transferred as part of the data (that is, in the index field). As a result, the data transfer rate is doubled. Furthermore, because double-word transfers are allowed, the data transfer rate is doubled again.

NOTE: Memory-mapped I/O can only be used in conjunction with linear addressing.

M.2 Memory-Mapped I/O Method of Accessing BitBLT-Control Registers

For memory-mapped I/O, the sequence is the following:

1. Memory-mapped I/O is enabled by programming Extension register bit SR17[2] to 1.
2. While Extension register bit SR17[2] is a 1, for memory-mapped I/O to occur, Graphics Controller register bits GR6[3:2] must be programmed to '01'.
3. At this time, if the CL-GD7548 is not programmed for linear addressing, the window into display memory is 64 Kbytes (A000:0h to AFFF:Fh).

   Beginning at B800:0h, a block of 256 bytes of memory address space is reserved. (Address bits A14:A8 are a 'don't care', and so the block is actually aliased at every 256-byte boundary). This block can be accessed using byte, word, or double-word cycles.

   1) Linear addressing requires programming Extension register bits SR7[7:4], SR2D[7:6], and GRB[0]. For more information on linear addressing, refer to Section 3.5.1.
   2) For more information on the window into display memory, refer to Section K.3.2.

With memory-mapped I/O, all registers are write-only (except Extension register GR31, which is read/write). In local bus configurations, if write-only memory-mapped registers are read, the data are indeterminate, and the CL-GD7548 returns RDY#.

For memory-mapped I/O, if the linear addressing mode:

- *Is enabled* (using Extension register bits SR4[7:4], SR2D[7:6], and GRB[0]), then Extension register bit SR17[6] must be programmed to 1. In this case, for memory-mapped I/O, the memory address space can be located only at the highest 256 bytes of the linear address space.
- *Is not enabled*, Extension register bit SR17[6] is a 'don't care'.

Table M-1 indicates the registers that are accessible using memory-mapped I/O.

Table M-1. Registers Accessed Using Memory-Mapped I/O

Offset (hex)	Graphics Controller Register	Extension Register	Register Description
00	GR0		Background Color Byte 0
01		GR10	Background Color Byte 1
02		–	Reserved
03		–	Reserved
04	GR1		Foreground Color Byte 0
05		GR11	Foreground Color Byte 1
06		–	Reserved
07		–	Reserved
08		GR20	BitBLT Width Byte 0
09		GR21	BitBLT Width Byte 1
0A		GR22	BitBLT Height Byte 0
0B		GR23	BitBLT Height Byte 1
0C		GR24	BitBLT Destination Pitch Byte 0
0D		GR25	BitBLT Destination Pitch Byte 1
0E		GR26	BitBLT Source Pitch Byte 0
0F		GR27	BitBLT Source Pitch Byte 1
10		GR28	BitBLT Destination Start Address Byte 0
11		GR29	BitBLT Destination Start Address Byte 1
12		GR2A	BitBLT Destination Start Address Byte 2
13		–	Reserved
14		GR2C	BitBLT Source Start Address Byte 0
15		GR2D	BitBLT Source Start Address Byte 1
16		GR2E	BitBLT Source Start Address Byte 2
17		–	Reserved
18		GR30	BitBLT Mode
19		–	Reserved
1A		GR32	BitBLT Raster Operation (ROP)
1B		–	Reserved
1C		GR34	BitBLT Transparent Color Select Low

Table M-1. Registers Accessed Using Memory-Mapped I/O *(cont.)*

Offset (hex)	Graphics Controller Register	Extension Register	Register Description
1D		GR35	BitBLT Transparent Color Select High
1E–1F		–	Reserved
20		GR38	BitBLT Transparent Color Mask Low
21		GR39	BitBLT Transparent Color Mask High
22-3F		–	Reserved
40		GR31	BitBLT Start/Status (Read/Write)
41-FF		–	Reserved

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