4.5V~100V, 1.5A, Synchronous, DC-DC Step-Down Converter

CJ92920 DC-DC

1 Introduction

The CJ92920 is a 100V/1.5A, synchronous step-down converter with built-in high-side and low-side power MOSFETs. Utilizing the advanced COT control method reduces the size of the total solution and achieves excellent load-transient performance. The integrated BST charge circuit minimizes both cost and solution size. High duty Ton extension feature makes it ideal for applications that require low drop-out voltage. 240μA quiescent current saves power, and low off-current makes it suitable for battery powered applications.

The CJ92920 also has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, output over voltage protection, FB open protection and thermal shutdown in case of excessive power dissipation.

The CJ92920 is available in a space-saving ESOP8 package.

2 Available Packages

PART NUMBER	PACKAGE
CJ92920	ESOP8

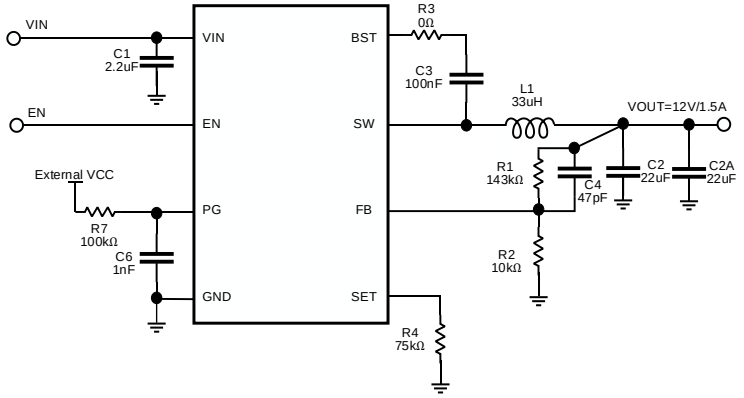
3 Features

- 4.5V to 100V Wide Input Range
- 1.5A Output Current Capability
- Integrated 400mΩ/120mΩ Low On-Resistance Power MOS.
- Constant-On-Time Control with Constant Switching Frequency.
- 240μA Low Quiescent Current
- 4μA Low Input Current at Off-state
- Programmable Switching Frequency from 300kHz to 800kHz
- Selectable FPWM/PFM mode
- Built-in Pull-up Current at EN Pin
- Internal 2ms Soft Start
- Integrated BST Charge Circuit
- Low Drop Out Mode Support 97% Duty Cycle
- Pre-bias Start-up
- Available in ESOP8 package

4 Applications

- Battery powered tools
- E-bike powers, E-motors
- Industry applications

Typical Application



5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJ92920-PBN	ESOP8	-40 ~ 125°C	RoHS & Green	Level 3 168HR	Tape and Reel 4000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by JSCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products.

Customized: Products manufactured to meet the specific needs of customers.

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available.

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers.

Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

ESOP8

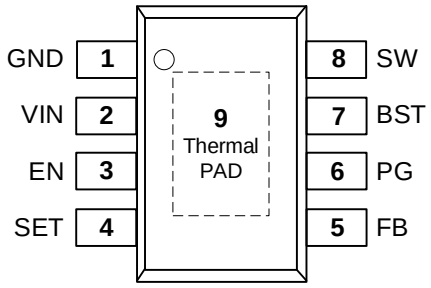


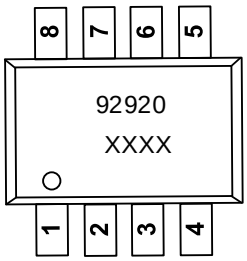
Figure 6-1 Pin Configuration

6.2 Pin Function

PIN		I / O(1)	DESCRIPTION
No.	NAME		
1	GND	G	Ground pin of IC. Connect to the ground of the system.
2	VIN	P	Supply input terminal to internal bias LDO and high-side FET. Connect to input supply and input bypass capacitors CIN. Input bypass capacitors must be directly connected to this pin and GND.
3	EN	I	Enable of the part. Pull down this pin to shut down the part. Internally pulled up by current source.
4	SET	I	Frequency and Mode selection.
5	FB	I	Feedback. Connect a resistor divider to set the output voltage.
6	PG	O	Power Good Indicator. Open drain structure. Need connect to an external Voltage source through a pull-up resistor (e.g.100kΩ). Floating it if not used.
7	BST	P	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
8	SW	P	Switching node of power stage. Connect to power inductor.
9	EP	-	Exposed Pad. Connect exposed pad to the PCB GND plane to achieve good thermal performance.

(1) I-INPUT, O-Output, P-Power, G-Ground

6.3 Marking Information



"92920": Device code.
"XXXX": Date Code.

7 Specifications

7.1 Absolute Maximum Ratings

(TA = 25°C, unless otherwise specified) (1)

SYMBOL	CHARACTERISTIC	VALUE	UNIT
V_{IN}	VIN to GND	-0.3 ~ 105	V
V_{SW}	SW to GND	-0.3 ~ 105	V
V_{BST} - V_{SW}	BST to SW	6	V
I_{EN}	Max Input current to EN pin	100	uA
All other pins		-0.3 ~ 6	V
TJ	Junction temperature	-40 ~ 150	°C
Tstg	Storage temperature	-65 ~ 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

SYMBOL	PARAMETER	MIN.	NOM.	MAX.	UNIT
V_{IN}	VIN to GND	4.5		100	V
V_{OUT}	VOUT to GND	0.8		28	V
I_{OUT}	Continuous Output Current	0		1.5	A
TJ	Junction temperature	-40		125	°C

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge	Human body model (HBM) (1)	±2000	V
$V_{ESD-CDM}$		Charged-device model (CDM) (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

SYMBOL	THERMAL METRIC	ESOP8	UNIT
$R_{\Theta JA}$ (1)	Junction-to-ambient thermal resistance	41.1	℃/W
$R_{\Theta JC(top)}$ (1)	Junction to case (top) thermal resistance	53.1	℃/W
$R_{\Theta JB}$ (1)	Junction-to-board thermal resistance	23.1	℃/W

(1) The value given in this table is only valid in comparison with other packages and cannot be used for design purposes. These values were measured on JESD 51-7, 4-layer JEDEC PCB board.

7.5 Electrical Characteristics

V_{IN}=60V and T_A=25°C, unless otherwise specified.

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VIN_{UV_R}	VIN UVLO rising voltage			4.3		V
VIN_{UV_F}	VIN UVLO falling voltage			4		V
VIN_{UV_HYS}	Hysteresis voltage of VIN UVLO			0.3		V
I_S	Shut down current from VIN	V_{EN}=0V		4		μA
I_Q	No switch Quiescent current from VIN	V_{FB}=0.82V		240		μA
EN						
V_{EN_R}	Enable rising voltage			1.2		V
V_{EN_F}	Enable falling voltage			1		V
$I_{EN\_PULL\_UP}$	Enable pull-up current	V_{EN}=Low		1		μA
		V_{EN}=High		4.5		μA
$V_{ENCLAMP}$	EN clamp voltage	V_{EN} voltage at 100μA current		6		V
FEEDBACK						
V_{FB}	Feedback voltage		0.768	0.78	0.792	V
V_{FB_UV}	Feedback voltage under voltage threshold			90		mV
POWERSTAGE						
R_{HS_ON}	High Side MOS ON resistance	V_{BST}-V_{SW}=5V		400		mΩ
R_{LS_ON}	Low Side MOS ON resistance			120		mΩ
I_{LKG_HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V			1	uA
CURRENT LIMIT						
I_{LIMIT_HS}	High side current limit threshold			3		A
SOFT START						
T_{SS}	Soft-start time	V_{FB} from 10% to 90%		2		ms
FREQUENCY						
F_{SW}	FPWM Mode Switching frequency	SET Pin short to GND		300		kHz
		R_{SET} = 18.7K		500		
		R_{SET} = 37.4K		800		
	PWM Mode Switching frequency	R_{SET} = 75K		300		
		R_{SET} = 150K		500		
		SET Pin Float		800		
T_{ON_MIN} (1)	Min on time			120		ns
T_{ON_MAX}	Max on time			10		μs

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{OFF_MIN} (1)	Min off time			350		ns
POWER GOOD						
V_{PG_UV}	FB falling			87		%
	FB rising			93		%
V_{PG_OV}	FB falling			106		%
	FB rising			112		%
R_{PG_ON}		Sink 3mA		55		Ω
T_{PG_DELAY} (1)	PG falling delay time			12		us
OVER TEMP						
T_{OTP_R} (1)	Thermal shutdown entry threshold			140		°C
T_{OTP_F} (1)	Thermal shutdown recovery threshold			130		°C

(1) Guaranteed by design and engineering sample characterization

8 Detailed Description

8.1 Overview

The CJ92920 is a 100V/1.5A, synchronous step-down converter with built-in high-side and low-side power MOSFETs. Utilizing the advanced COT control method reduces the size of the total solution and achieves excellent load-transient performance. The integrated BST charge circuit minimizes both cost and solution size. High duty Ton extension feature makes it ideal for applications that require low drop-out voltage. 240μA quiescent current saves power, and low off-current makes it suitable for battery powered applications.

The CJ92920 also has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, output over voltage protection, FB open protection and thermal shutdown in case of excessive power dissipation.

8.2 Functional Block Diagram

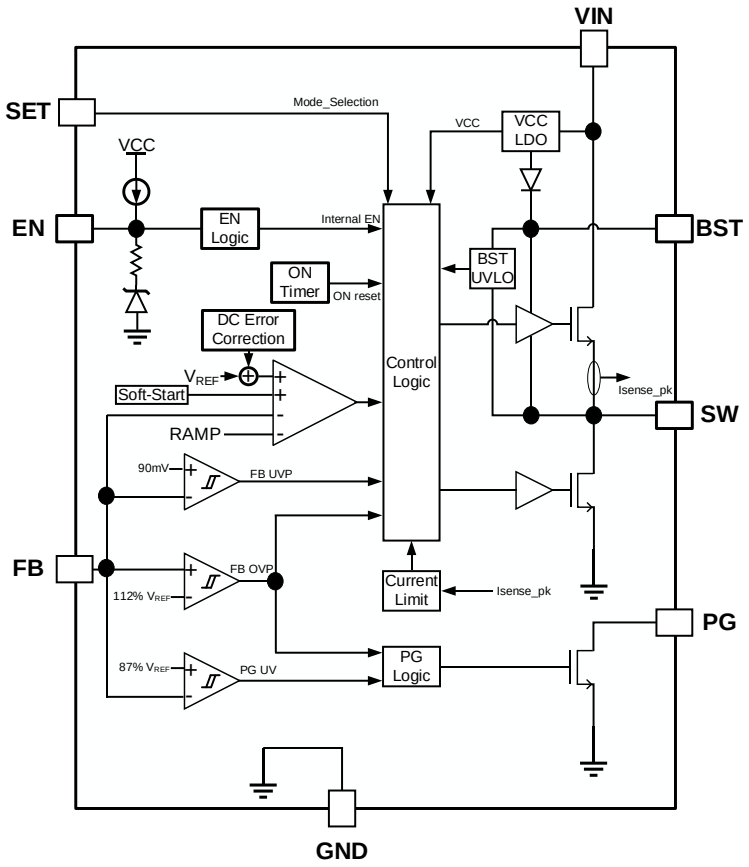


Figure 8-1 Block diagram-

8.3 Feature Description

8.3.1 COT Control Loop Operation

The CJ92920 is a fully integrated, synchronous, step-down switch-mode converter. It employs Constant-on-time (COT) control to provide fast transient response and simplify loop stabilization. The high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on-time is determined by both the output and input voltage, keeping the switching frequency relatively constant across the input voltage range. After the on-time elapses, the HS-FET is turned off and will turn on again when V_{FB} drops below V_{REF}. This repeated operation regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is off to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To prevent shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET

off and HS-FET on period.

During the LS-FET period, if LS-FET remains on until next HS-FET on pulse is coming, this is called FPWM(Forced Pulse Width Modulation) mode. If the LS-FET shuts down when inductor current falls to zero amps, and the SW enters Hi-Z state until next HS-FET on pulse, this is called PFM (Pulse Frequency Modulation) mode, see below for detailed instructions.

8.3.2 Light-Load Operation

The CJ92920 can be configured to operate in either FPWM mode or PFM mode, as is shown in Figure 8 and Figure 8.

In FPWM mode, the IC's switching frequency remains relatively consistent despite changes in load current, this helps to minimize light load V_{OUT} ripple, meantime simplifies the design of second stage filter used to damp the power stage noise. However, due to more frequent switching of the internal power MOS, light load efficiency is lower compared to PFM mode.

In PFM mode under light load condition, V_{FB} cannot reach V_{REF} after the inductor current approaches zero, a current modulator then takes control of the LS-FET and limits the inductor current around zero, and the LS-FET driver enters Hi-Z state. This results in slow output voltage drop, and the CJ92920 reduces the switching frequency naturally to achieve high efficiency. As a trade-off, PFM mode experiences larger VOUT ripple. See the Operation Mode and Frequency Selection for detail setting methods of work mode and switching frequency.

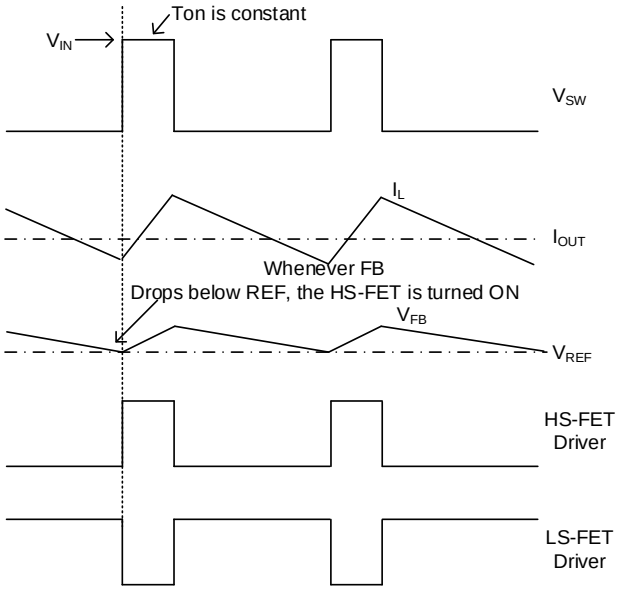


Figure 8-2 FPWM Operation

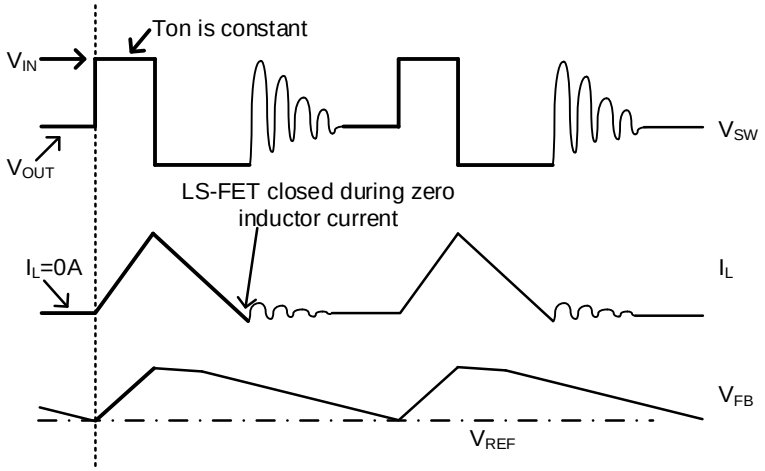


Figure 8-3 PFM Operation

8.3.3 Heavy-Load Operation

For FPWM mode, the operating mechanism remains the same as in light load condition

For PFM mode, as the load current increases, the current modulator's regulation time shorten. The HS-FET is turned on more frequently, causing the switching frequency to increase accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined using Equation (1).

$$\mathbf{I}_{OUT\_Critical} = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{2\times L\times f_{SW}\times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Subsequently, the switching frequency remains relatively constant across the output current range.

8.3.4 Enable (EN) Control

The CJ92920 has a dedicated enable control pin with positive logic. To turn on the regulator, drive the EN pin voltage higher than 1.2V(typical). To turn it off, drive the EN pin voltage lower than 1V (typical).

The EN pin includes an internal pull-up current source, allowing the CJ92920 to automatically startup when the EN pin is floating. More than 4.5μA pulldown current is required to shut down the regulator via EN pin. Once the EN pin is pulled low, its internal pull-up current will decrease to 1μA to reduce the shutdown current.

By using the two external resistor dividers, it is easy to optimize the system's start and stop voltage via EN pin:

Start voltage setting:

$$V_{START} = 1.2 \times \frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} - 1uA \times R_{ENUP} \quad (2)$$

Stop voltage setting:

$$V_{STOP} = 1 \times \frac{R_{ENUP}+R_{ENDN}}{R_{ENDN}} - 4.5uA \times R_{ENUP} \quad (3)$$

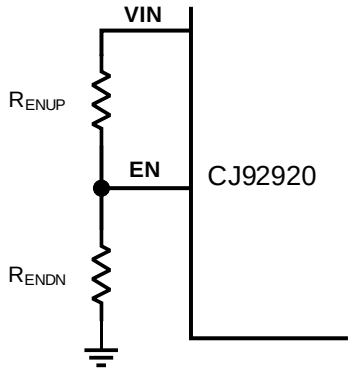


Figure 8-1 EN network

8.3.5 Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltage. The CJ92920s' UVLO comparator monitors the input voltage. With a rising threshold of 4.3V and a falling threshold of 4V.

8.3.6 Internal Soft Start (SS)

Soft start (SS) prevents the output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1V. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF},

the error amplifier uses V_{SS} as the reference. Once V_{SS} exceeds V_{REF}, the error amplifier switches to using V_{REF} as the reference. The SS time is set to 2ms internally.

8.3.7 Operation Mode and Frequency Selection

The CJ92920 provides both FPWM and PFM mode under light-load condition. It offers four options for switching frequency and operation mode selection via choosing different resistor values between SET and GND. Refer to the details below.

Table 1 Switching frequency set resistor selection

SET	Operation Mode	Switching Frequency
SET Pin short to GND	FPWM	300kHz
R_{SET} = 18.7kΩ	FPWM	500kHz
R_{SET} = 37.4kΩ	FPWM	800kHz
R_{SET} = 75kΩ	PFM	300kHz
R_{SET} = 150kΩ	PFM	500kHz
SET Pin Float	PFM	800kHz

8.3.8 Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The CJ92920 features both valley current limit and peak current limit control. When the LS-FET is on and the inductor current reaches the valley current limit, the LS-FET limit comparator is enabled. The device then enters overcurrent protection (OCP) mode, and the HS-FET waits until the valley current limit is no longer present before turning on again. During the HS-FET period, the inductor current is compared with the peak current limit. If the current peak limit is triggered, the HS-FET on pulse will be terminated immediately. The output voltage drops until VFB falls below UVP threshold. Once FB UVP is triggered, the CJ92920 enters hiccup mode to periodically restart the part.

During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition persists after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output returns to regulation level. OCP is a non-latch protection.

8.3.9 Power Good Indication

The CJ92920 uses a power-good (PG) output to indicate whether the output voltage of the buck regulator ready or not. The PG pin is an open drain output. Once the FB pin is between 87% and 112% of the internal voltage reference the PG pin is de-asserted and the pin floats. A pull-up resistor of 10 kΩ to 100kΩ to a voltage source that is 5.5 V or less is recommended. A higher pull-up resistance reduces the amount of current drawn from the pull-up voltage source when the PG pin is asserted low. A lower pull-up resistance reduces the switching noise seen on the PG signal. The PG is in a defined state once the input voltage is greater than 2 V but with reduced current sinking capability. The PG will achieve full current sinking capability as input voltage approaches 3 V. The PG pin is pulled low when the FB is lower than 87% or greater than 112% of the nominal internal reference voltage. Also, PG is pulled low, if UVLO or thermal shutdown are asserted or the EN pin pulled low.

8.3.10 Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 140°C (typical), the entire chip shuts down. Once the temperature falls below the lower threshold (typically 120°C), the chip is re-enabled, and a soft start is initiated.

9 Application and Implementation

9.1 Typical Application Circuit

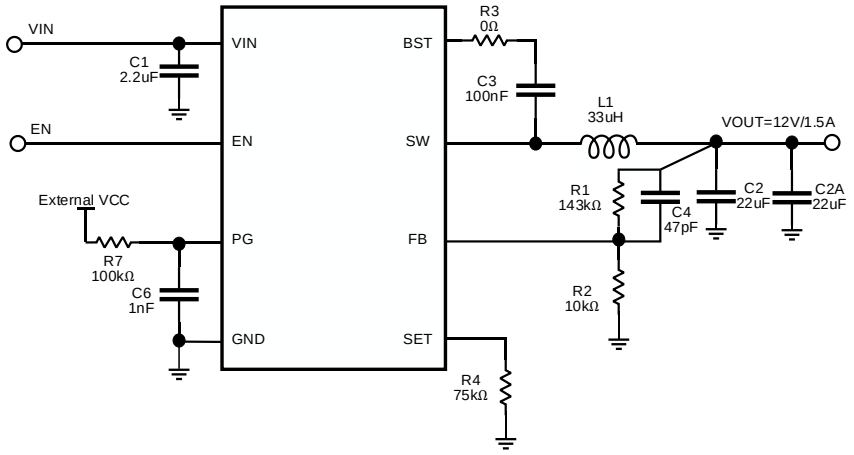


Figure 9-1 V_{IN}=48V, V_{OUT}=12V, I_{OUT}=1.5A, F_{SW}=300KHz, PFM MODE

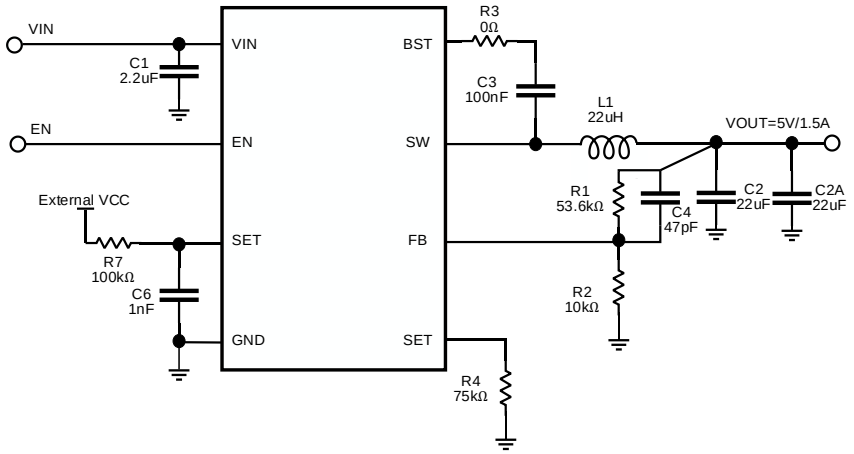


Figure 9-2 V_{IN}=48V, V_{OUT}=5V, I_{OUT}=1.5A, F_{SW}=300KHz, PFM MODE

9.2 Component Selection

9.2.1 Setting the Output Voltage

The output voltage of the CJ92920 can be adjusted using external resistor dividers. The reference voltage is fixed at 0.78V. The feedback network is in Figure 9-3.

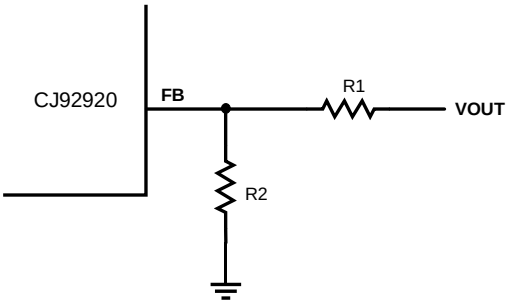


Figure 9-3 Feedback Network

Choose R1 and R2 using Equation:

$$V_{OUT} = V_{FB} \times \frac{(R1+R2)}{R2} \quad (4)$$

9.2.2 Selecting the Inductor

An inductor is necessary for providing a constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but it also has a larger physical footprint, higher series resistance, and lower saturation current.

For most designs, the inductance value can be derived from the following Equation:

$$L = \frac{(V_{IN}-V_{OUT})\times V_{OUT}}{\Delta I_L \times f_{SW} \times V_{IN}} \quad (5)$$

Where ΔIL is the inductor ripple current.

Select the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated using the following Equation:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (6)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages (1)

VOUT (V)	R1 (kΩ)	R2 (kΩ)	Cff(pF)	L (μH)	COUT(μF)
12	143	10	47	33	2 x 22
5	53.6	10	47	22	2 x 22

(1) For a detailed design circuit, please refer to the Typical Application Circuit

9.2.3 Selecting the Output Capacitor

The output capacitor maintains the DC output voltage ripple. Ceramic, tantalum, or low-ESR electrolytic capacitors can be used. For best results, use low ESR capacitors to minimize the output voltage ripple. The output voltage ripple can be estimated with Equation:

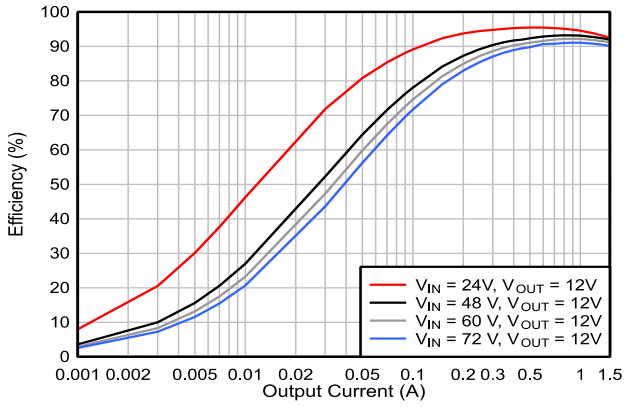
$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW}\times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8\times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

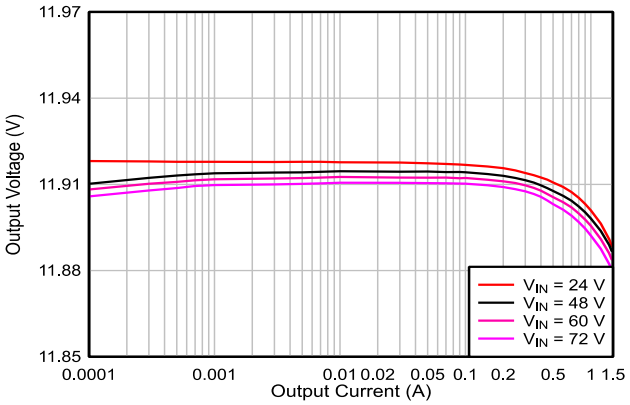
The characteristics of the output capacitor also affect the stability of the regulation system. The CJ92920 can be optimized for a wide range of capacitance and ESR values.

9.3 Application Curve

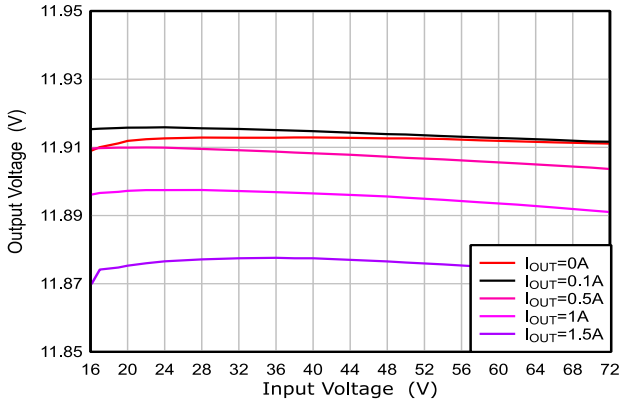
V_{IN}= 48V, V_{OUT}= 12V, C_{IN}= 2.2μF, C_{OUT} =2 x 22μ, L1= 33μF, F_{SW}= 300kHz, and T_A = +25°C, unless otherwise noted.



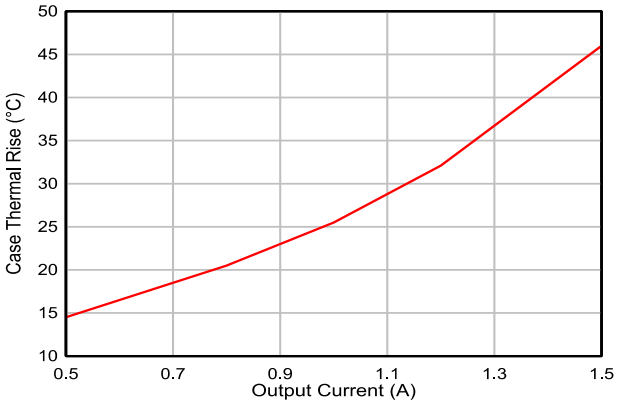
Efficiency vs. Load Current
(PFM MODE, DCR=65mΩ)



Load Regulation
(PFM MODE, DCR=65mΩ)

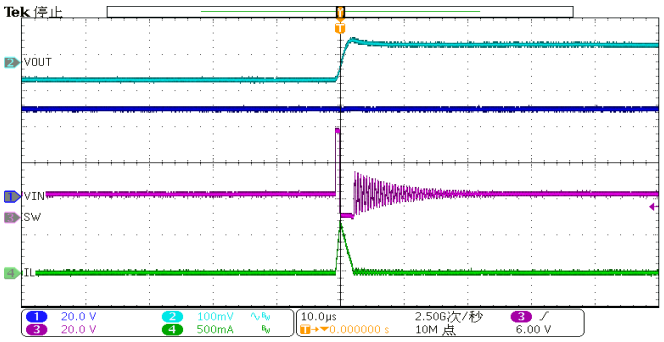


Line Regulation
(PFM MODE, DCR=65mΩ)

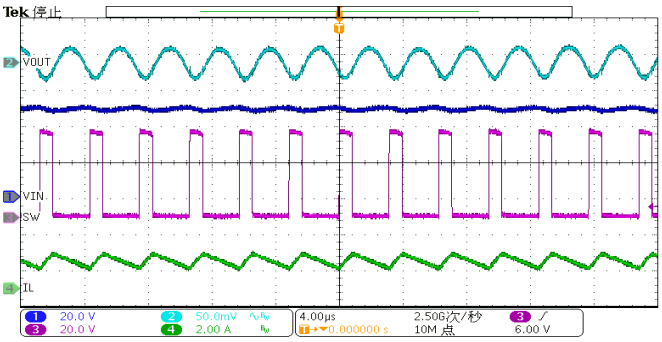


Thermal Rise
(PFM MODE, no air flow)

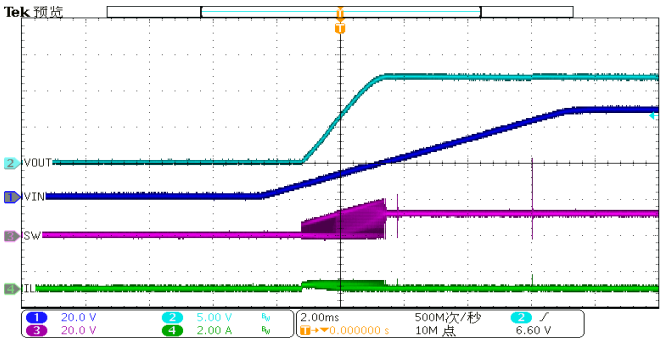
V_{IN}= 48V, V_{OUT}= 12V, C_{IN}= 2.2μF, C_{OUT} =2 x 22μ, L1= 33μF, F_{SW}= 300kHz, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



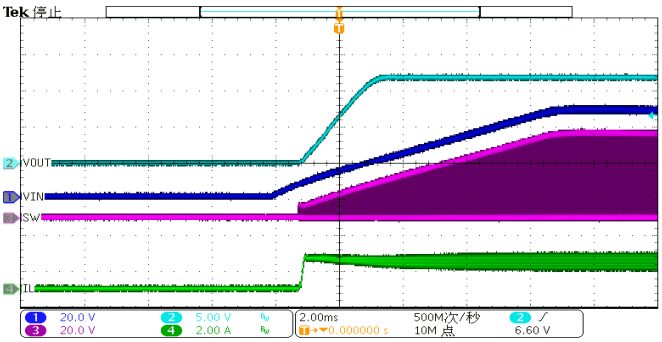
Output Voltage Ripple
(I_{OUT} =0A, PFM MODE)



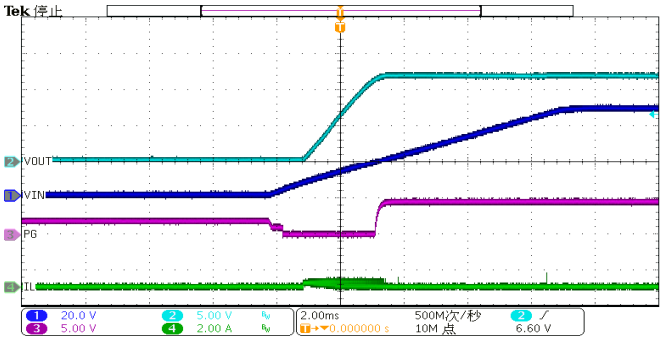
Output Voltage Ripple
(I_{OUT} =1.5A)



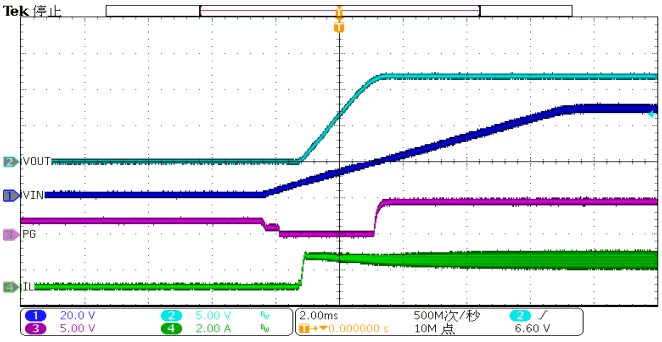
Start-Up through V_{IN}
(I_{OUT} =0A, PFM MODE)



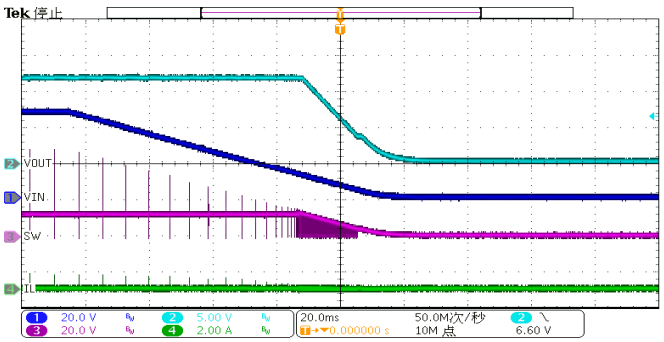
Start-Up through V_{IN}
(I_{OUT} =1.5A)



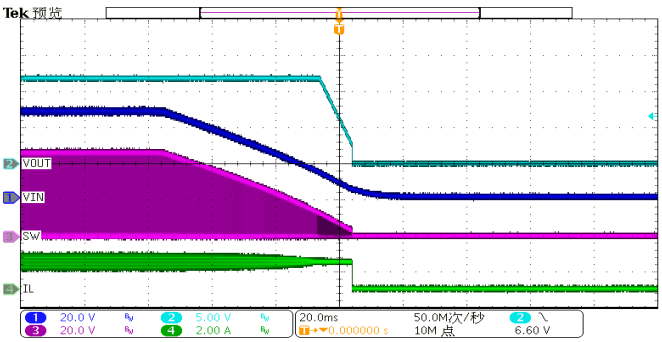
Start-Up through V_{IN}
(I_{OUT} =0A, PFM MODE with PG)



Start-Up through V_{IN}
(I_{OUT} =1.5A with PG)

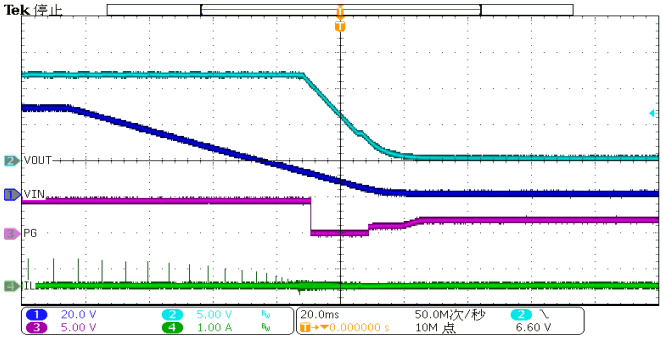


Shut Down through V_{IN}
(I_{OUT} =0A, PFM MODE)

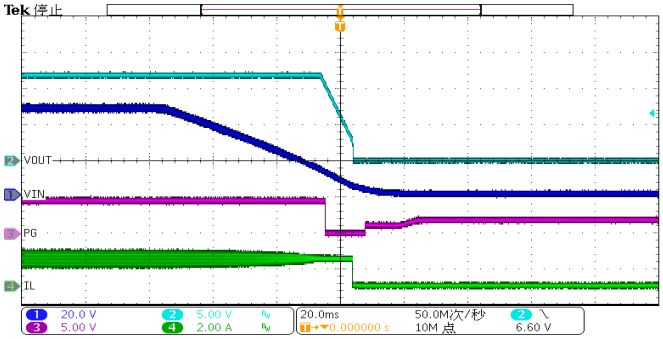


Shut Down through V_{IN}
(I_{OUT} =1.5A)

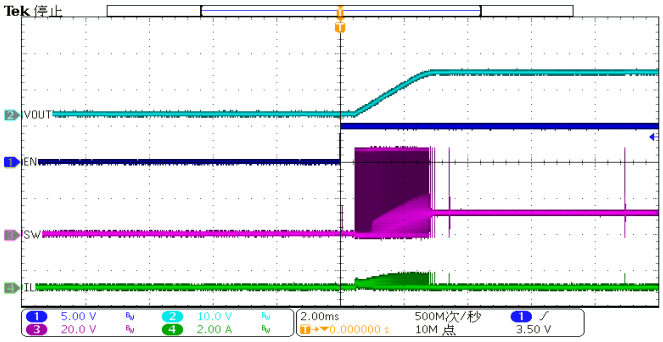
V_{IN}= 48V, V_{OUT}= 12V, C_{IN}= 2.2μF, C_{OUT} =2 x 22μ, L1= 33μF, F_{SW}= 300kHz, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



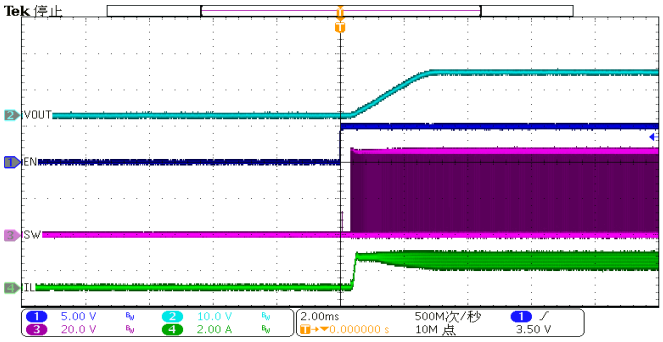
Shut Down through V_{IN}
(I_{OUT} =0A, PFM MODE with PG)



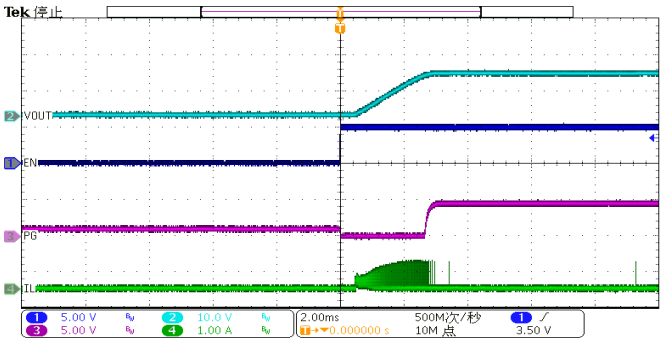
Shut Down through V_{IN}
(I_{OUT} =1.5A with PG)



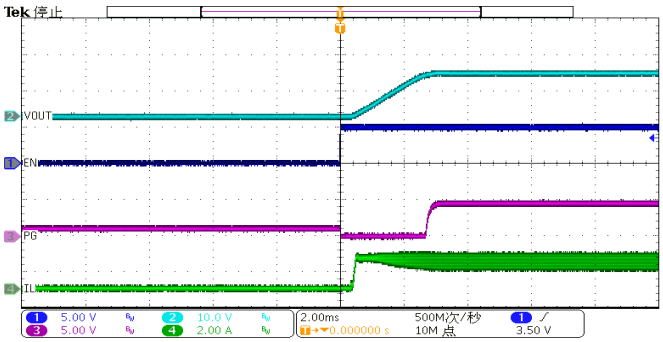
Start-Up through EN
(I_{OUT} =0A, PFM MODE)



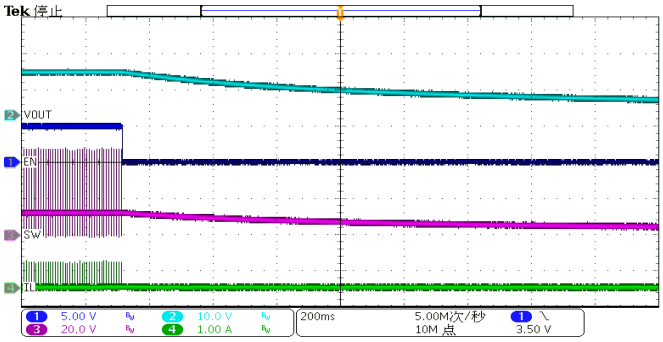
Start-Up through EN
(I_{OUT} =1.5A)



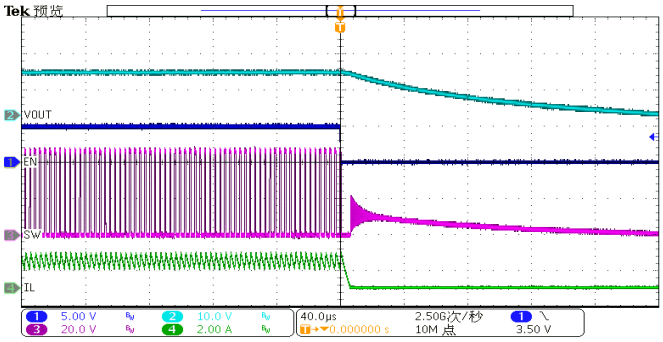
Start-Up through EN
(I_{OUT} =0A, PFM MODE with PG)



Start-Up through EN
(I_{OUT} =1.5A with PG)

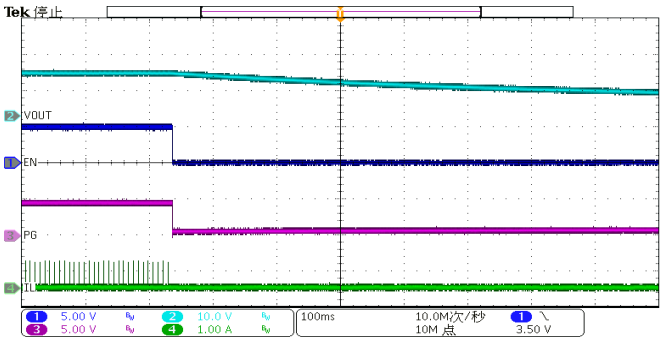


Shut Down through EN
(I_{OUT} =0A, PFM MODE)

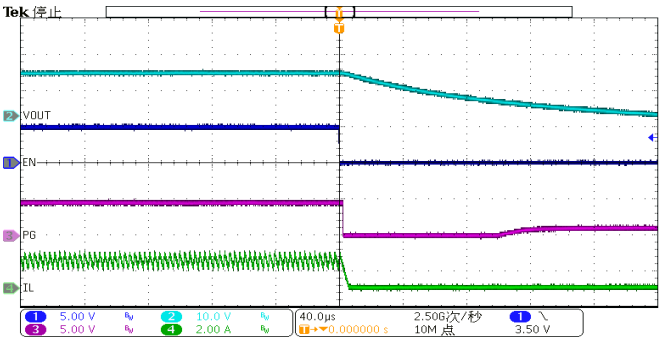


Shut Down through EN
(I_{OUT} =1.5A)

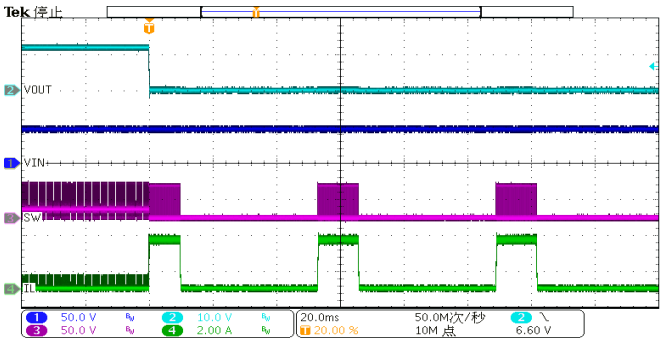
V_{IN}= 48V, V_{OUT}= 12V, C_{IN}= 2.2μF, C_{OUT} =2 x 22μ, L1= 33μF, F_{SW}= 300kHz, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



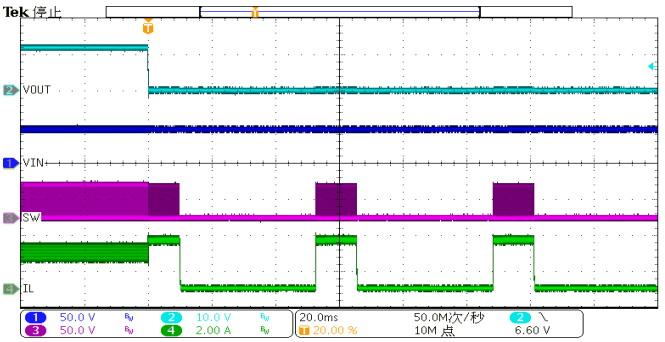
Shut Down through EN
(I_{OUT} =0A, PFM MODE with PG)



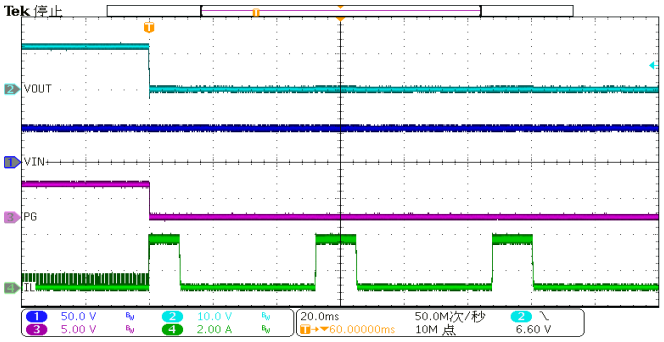
Shut Down through EN
(I_{OUT} =1.5A with PG)



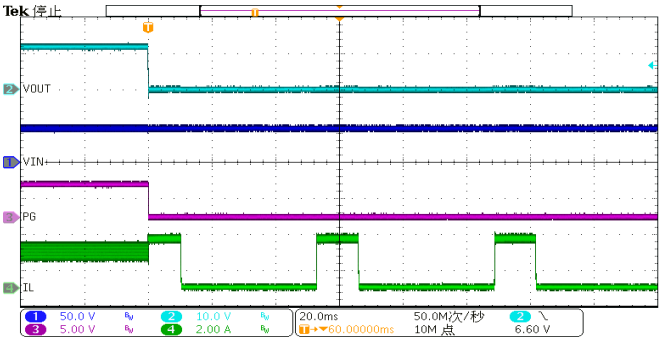
Short-Circuit Entry
(I_{OUT} =0A, PFM MODE)



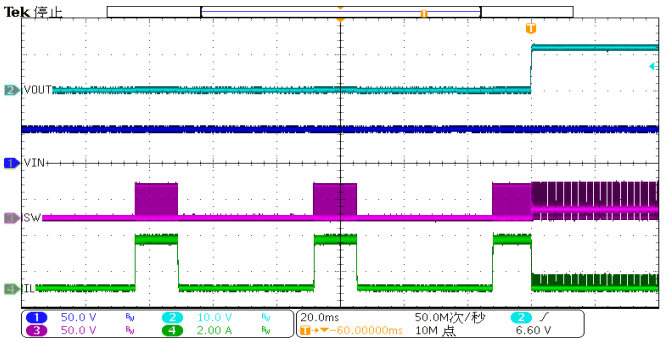
Short-Circuit Entry
(I_{OUT} =1.5A)



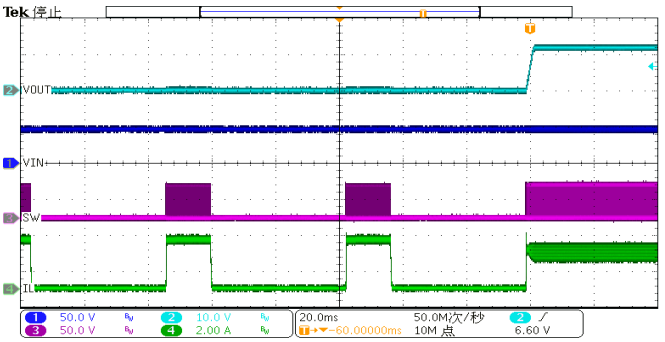
Short-Circuit Entry
(I_{OUT} =0A, PFM MODE with PG)



Short-Circuit Entry
(I_{OUT} =1.5A with PG)

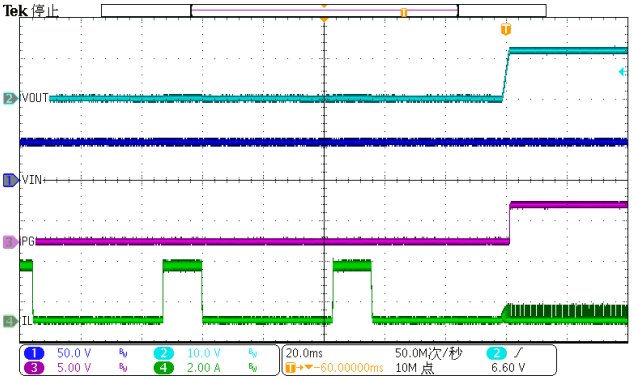


Short-Circuit Recovery
(I_{OUT} =0A, PFM MODE)

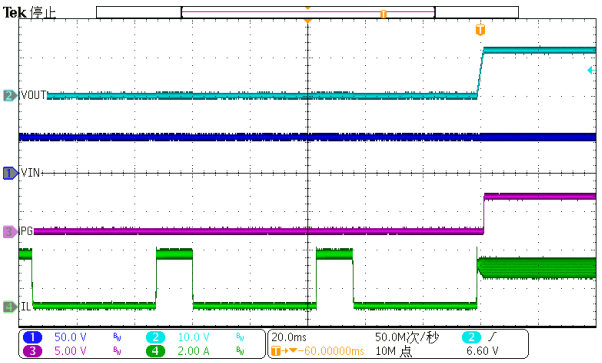


Short-Circuit Recovery
(I_{OUT} =1.5A)

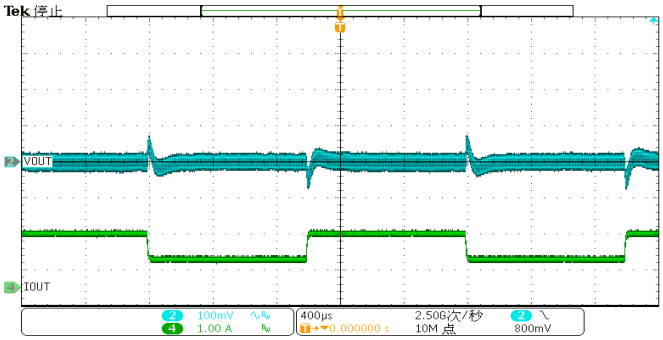
V_{IN}= 48V, V_{OUT}= 12V, C_{IN}= 2.2μF, C_{OUT} =2 x 22μ, L1= 33μF, F_{SW}= 300kHz, PG external pulled up to 5V, and T_A = +25°C, unless otherwise noted.



Short-Circuit Recovery
(I_{OUT} =0A, PFM MODE with PG)



Short-Circuit Recovery
(I_{OUT} =1.5A with PG)



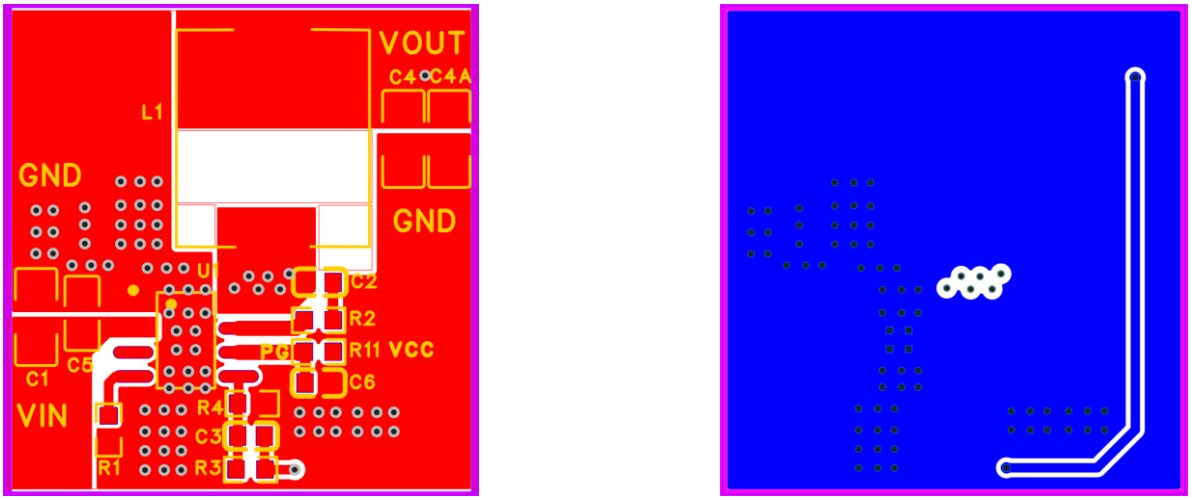
Load Transient
(I_{OUT}= 0.75A to 1.5A, slew rate=2.5A/ μs)

10 Layout

10.1 Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to the figure below and follow the guidelines below.

- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors as close to FB as possible.
- Keep the switching node (such as SW, BST) far away from the feedback network.
- Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.



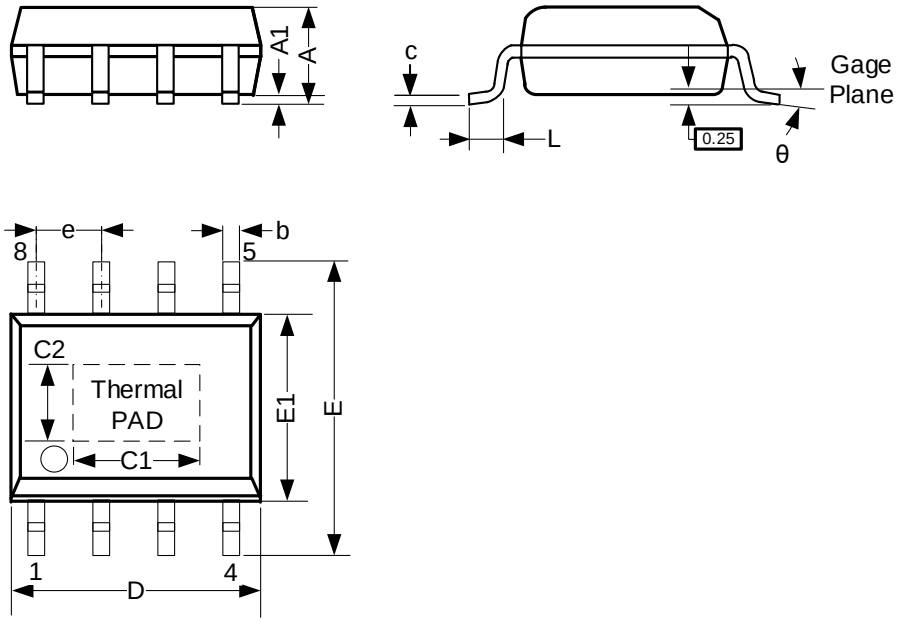
Top Layer Bottom Layer

Figure 10-1 Recommend PCB Layout

11 Mechanical Information

11.1 ESOP8 Mechanical Information

ESOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.30	–	1.70
A1	0.00	–	0.15
b	0.33	–	0.51
c	0.19	–	0.25
C1	2.16	–	2.46
C2	2.26	–	2.56
D	4.80	–	5.00
E	5.80	–	6.20
E1	3.80	–	4.00
e	1.27 BSC		
L	0.41	–	1.27
θ	0°	–	8°

12 Notes and Revision History

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of JSCJ -- ***https:www.jscj-elec.com*** for more details.

12.2 Notes

Electrostatic Discharge Caution

This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. JSCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses JSCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. JSCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

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