United Monolithic Semiconductors

CHZ050A-SEA

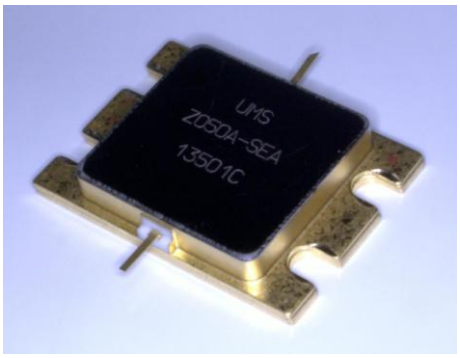
50W C Band HPA

GaN HEMT on SiC

Description

The CHZ050A-SEA is an input and output internally-matched packaged Gallium Nitride High Electron Mobility Transistor. It allows broadband solutions for a variety of RF power applications in C-band. It is proposed in a low parasitic, low thermal resistance package, and doesn't require any external matching circuitry.

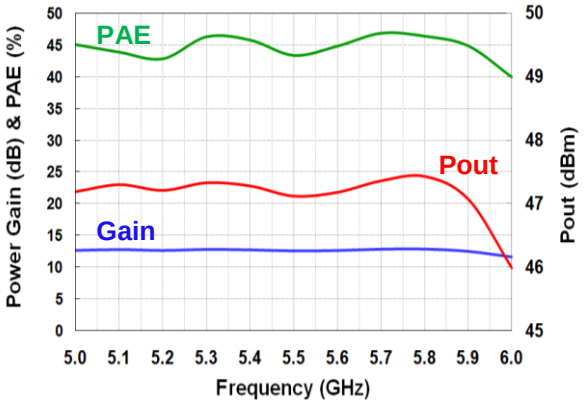
The CHZ050A-SEA is well suited for pulsed radar and satcom applications. It is developed on a 0.5µm gate length GaN HEMT process, and is available as a hermetic flange ceramic metal power package



Main Features

- Bandwidth : 5.2-5.8 GHz
- Pulsed operating mode
- High power: > 50W
- High Efficiency: up to 45%
- DC bias: V_{DS} =50V @ I_{D_Q} =400mA
- MTTF > 10^6 hours @ Tj=200°C
- 50Ω input and output matched
- External input/output bias tees required
- RoHS Flange Ceramic package

V_{DS} = 50V, I_{D_Q} = 400mA
Pulse mode (25µs-10%) Pin = 35dBm



Intrinsic performances of the packaged device

Main Electrical Characteristics

Tcase= +25°C, Pulsed mode, F = 5.2-5.8 GHz, V_{DS}=50V, I_{D_Q}=400mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	13	15		dB
P_{SAT}	Saturated Output Power	50	60		W
PAE	Max Power Added Efficiency	40	45		%
G_{PAE_MAX}	Associated Gain at Max PAE		12		dB

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Recommended Operating Ratings

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage	20		50	V	
V_{GS_Q}	Gate to Source Voltage		-1.9		V	V_D=50V, I_{D_Q}=400mA
I_{D_Q}	Quiescent Drain Current		0.4	1.3	A	V_D=50V
I_{D_MAX}	Drain Current		3	(1)	A	V_D=50V, Compressed mode
I_{G_MAX}	Gate Current (forward mode)		0	32	mA	Compressed mode
T_{j_MAX}	Junction temperature			200	°C	
Pw	Maximum pulse width			0.5	ms	
DC	Maximum duty cycle			10	%	MTTF=10e6

(1) Limited by dissipated power

DC Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-3	-2	-1	V	V_D=50V, I_D= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		10 (1)		A	V_D=7V, V_G=2V
I_{G_leak}	Gate Leakage Current (reverse mode)	-4			mA	V_D=50V, V_G=-7V
V_{BDS}	Drain-Source Break-down Voltage		200		V	V_G=-7V, I_D=20mA
RTH	Thermal Resistance		2.5		°C/W	CW
$RTH_{0.5ms}$	Thermal Resistance		1.45		°C/W	Duty cycle = 10% Pulse width =0,5ms

(1) For information, limited by I_{D_MAX} , see on Absolute Maximum Ratings

RF Characteristics (Pulsed)

Tcase= +25°C, Pulse mode (1), F = 5.5GHz, V_{DS}=50V, I_{D_Q}=200mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	13	15		dB
P_{SAT}	Saturated Output Power	50	60		W
PAE	Max Power Added Efficiency	40	45		%
G_{PAE_MAX}	Associated Gain at Max PAE		12		dB
S11	Input matching		-10		dB

(1) Input RF and gate voltage are pulsed. Conditions are 25µs width, 10% duty cycle and 1µs offset between RF and DC pulse.

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plans defined by the leads of the package, at the connection interface with the PCB.

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Absolute Maximum Ratings

Tcase= +25°C[(1), (2), (3)]

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Voltage	60	V	
V_{GS_Q}	Gate-Source Voltage	-10, +2	V	(6)
I_{G_MAX}	Maximum Gate Current in forward mode	96	mA	
I_{G_MIN}	Maximum Gate Current in reverse mode	-16	mA	
I_{D_MAX}	Maximum Drain Current	5	A	(4)
P_{IN}	Maximum Input Power (typical)	41	dBm	(5)
$Pw_{\_MAX}$	Maximum pulse width	5	ms	
$DC_{\_MAX}$	Maximum duty cycle	50	%	
T_j	Junction Temperature	220	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{Case}	Case Operating Temperature	See note	°C	(4)

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.
(3) The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.
(4) Max junction temperature must be considered
(5) Within 5.2-5.8GHz - Linked to and limited by I_{G_MAX} & I_{G_MIN} values
(6) V_{GS_Q} max limited by I_{D_MAX} and I_{G_MAX} values

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Typical S-parameters (simulation)

Tcase= +25°C, CW mode, VD=50V, ID_Q=400mA.

Freq (GHz)	Mag S(1,1)	PhS11 (°)	Mag S(2,1)	PhS21 (°)	Mag S(1,2)	PhS12 (°)	Mag S(2,2)	PhS22 (°)
0.25	0.830	-173.0	11.800	35.4	0.005	-52.8	0.701	-160.0
0.50	0.899	162.0	3.890	-7.3	0.003	-95.2	0.861	172.0
0.75	0.927	142.0	1.940	-35.8	0.002	-128.0	0.912	150.0
1.00	0.939	123.0	1.230	-59.2	0.001	-158.0	0.930	129.0
1.25	0.944	105.0	0.916	-81.1	0.001	173.0	0.936	109.0
1.50	0.946	86.9	0.774	-103.0	0.001	150.0	0.935	87.4
1.75	0.946	68.8	0.722	-126.0	0.001	131.0	0.928	63.6
2.00	0.946	50.4	0.733	-151.0	0.001	110.0	0.917	36.2
2.25	0.944	31.6	0.794	-179.0	0.002	87.3	0.899	3.2
2.50	0.942	12.2	0.894	150.0	0.002	61.0	0.877	-37.0
2.75	0.938	-7.8	1.010	114.0	0.003	30.8	0.856	-84.3
3.00	0.932	-28.7	1.100	77.1	0.003	-0.8	0.847	-134.0
3.25	0.923	-50.7	1.180	40.3	0.004	-32.2	0.850	179.0
3.50	0.908	-74.2	1.300	4.8	0.005	-63.3	0.854	138.0
3.75	0.882	-99.8	1.500	-30.5	0.006	-95.6	0.850	102.0
4.00	0.838	-129.0	1.870	-67.5	0.008	-130.0	0.832	67.7
4.25	0.760	-162.0	2.500	-109.0	0.011	-169.0	0.788	32.1
4.50	0.619	156.0	3.470	-158.0	0.015	145.0	0.694	-8.9
4.75	0.407	102.0	4.590	143.0	0.019	90.8	0.530	-60.2
5.00	0.221	21.7	5.230	78.3	0.020	32.3	0.351	-127.0
5.25	0.214	-71.2	5.210	15.1	0.017	-23.5	0.287	155.0
5.50	0.251	-132.0	5.000	-45.1	0.014	-75.4	0.289	93.6
5.75	0.211	179.0	4.950	-106.0	0.012	-129.0	0.224	50.1
6.00	0.051	113.0	4.870	-175.0	0.011	169.0	0.077	86.5
6.25	0.237	-91.9	3.950	107.0	0.010	97.7	0.408	100.0
6.50	0.500	-146.0	2.340	32.4	0.007	32.1	0.708	57.1
6.75	0.657	167.0	1.210	-28.2	0.005	-15.9	0.848	20.7
7.00	0.735	124.0	0.632	-78.0	0.003	-49.6	0.905	-9.4
7.25	0.771	81.0	0.350	-122.0	0.002	-75.3	0.931	-35.9
7.50	0.790	36.1	0.203	-162.0	0.001	-94.0	0.943	-60.4
7.75	0.809	-9.7	0.121	158.0	0.001	-93.4	0.949	-83.7
8.00	0.834	-53.6	0.072	121.0	0.001	-7.8	0.951	-106.0
8.25	0.860	-92.6	0.043	84.9	0.002	-13.5	0.951	-128.0
8.50	0.884	-126.0	0.027	51.0	0.003	-33.2	0.949	-150.0
8.75	0.902	-153.0	0.018	17.9	0.004	-54.4	0.948	-171.0
9.00	0.915	-177.0	0.013	-14.8	0.004	-75.8	0.946	169.0
9.25	0.925	163.0	0.011	-46.6	0.005	-97.1	0.943	149.0
9.50	0.933	146.0	0.009	-76.7	0.006	-119.0	0.938	128.0
9.75	0.938	130.0	0.009	-105.0	0.006	-142.0	0.929	107.0
10.00	0.943	116.0	0.009	-134.0	0.007	-168.0	0.910	83.7

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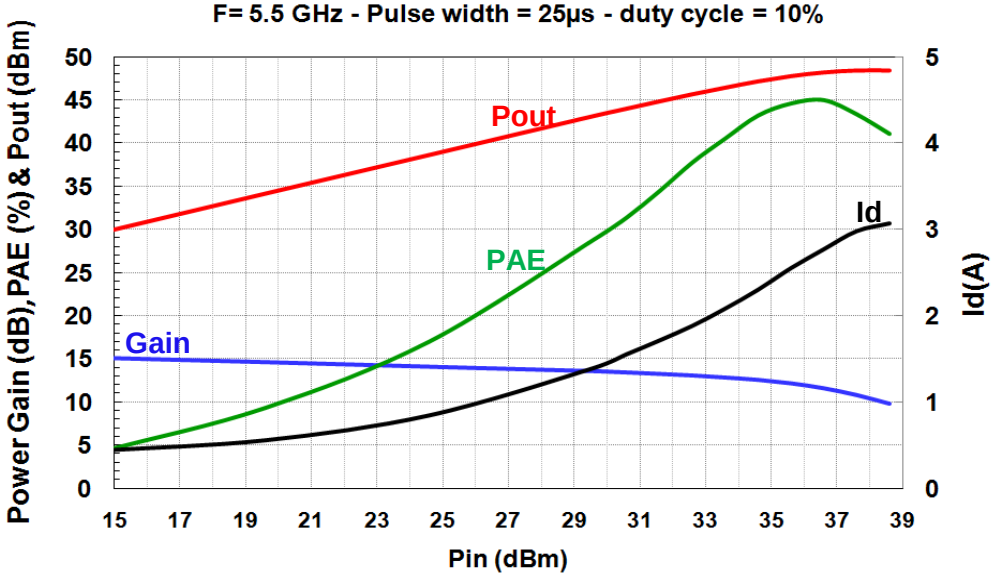
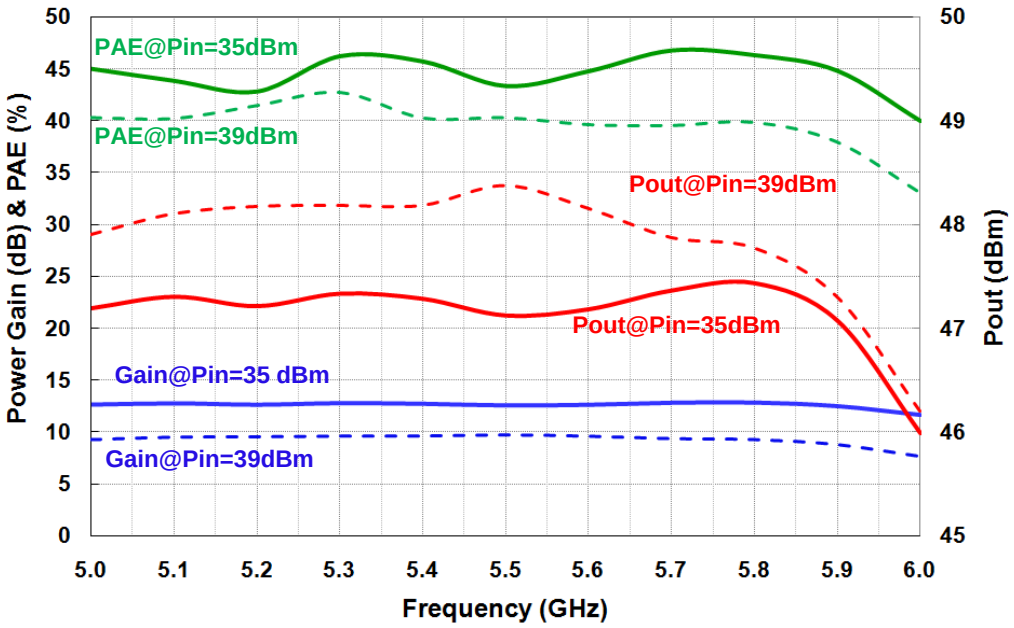
Typical Performance on Demonstration Board (Ref. 61499536B)

Measured on evaluation board 61499536B.
Losses of 0.4 dB at input and output are de-embedded.
Tcase = +25°C, RF Pulsed mode , Gate biasing not pulsed

Measured Pout, Gain, PAE & Id
RF pulsed , Biasing not pulsed
V_{DS} = 50V, I_{DQ} = 400mA DC
F= 5.5 GHz - Pulse width = 25µs - duty cycle = 10%



Measured Pout , PAE & Gain
RF pulsed , Biasing not pulsed
V_{DS} = 50V, I_{DQ} = 400mA DC
Pulse width = 25µs - duty cycle = 10%



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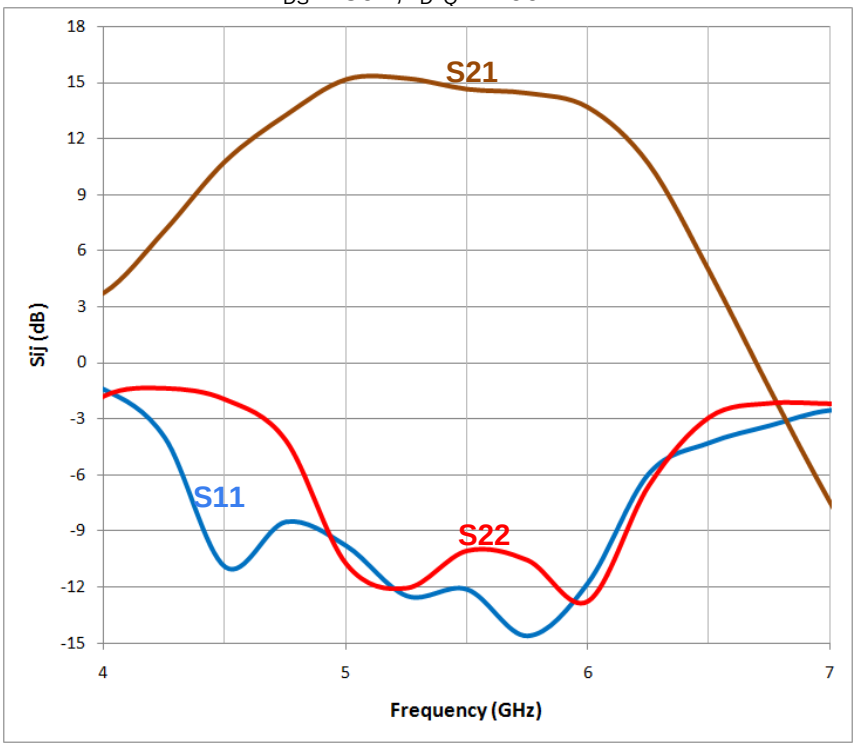
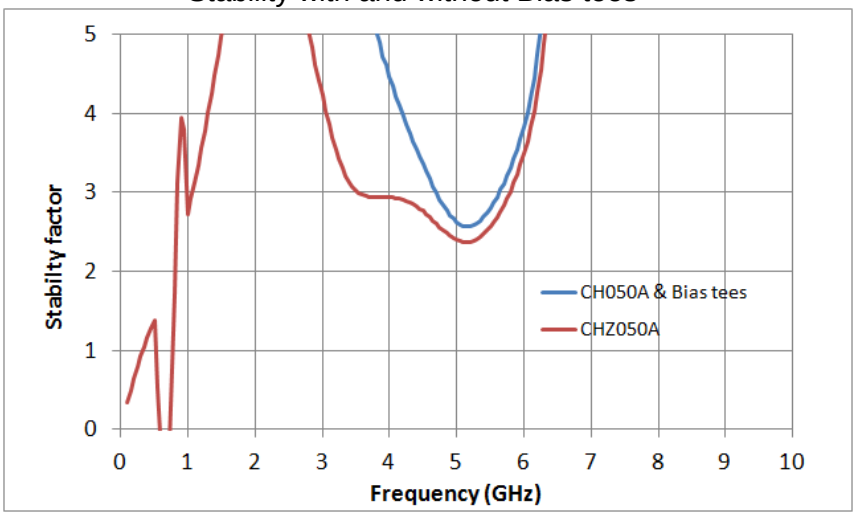
Typical Performance on Demonstration Board (Ref. 61499536B)

Calibration and measurements are done on the connector reference accesses of the demonstration boards
Tcase = +25°C, CW mode

Measured S parameters
V_{DS} = 50V, $I_{D\ Q}$ = 400mA



Stability with and without Bias tees (1)



(1) Proper serial resistor in DC path of input bias tee losses at low frequencies provides stability. (See resistor R1 on 61499536B demonstration board)

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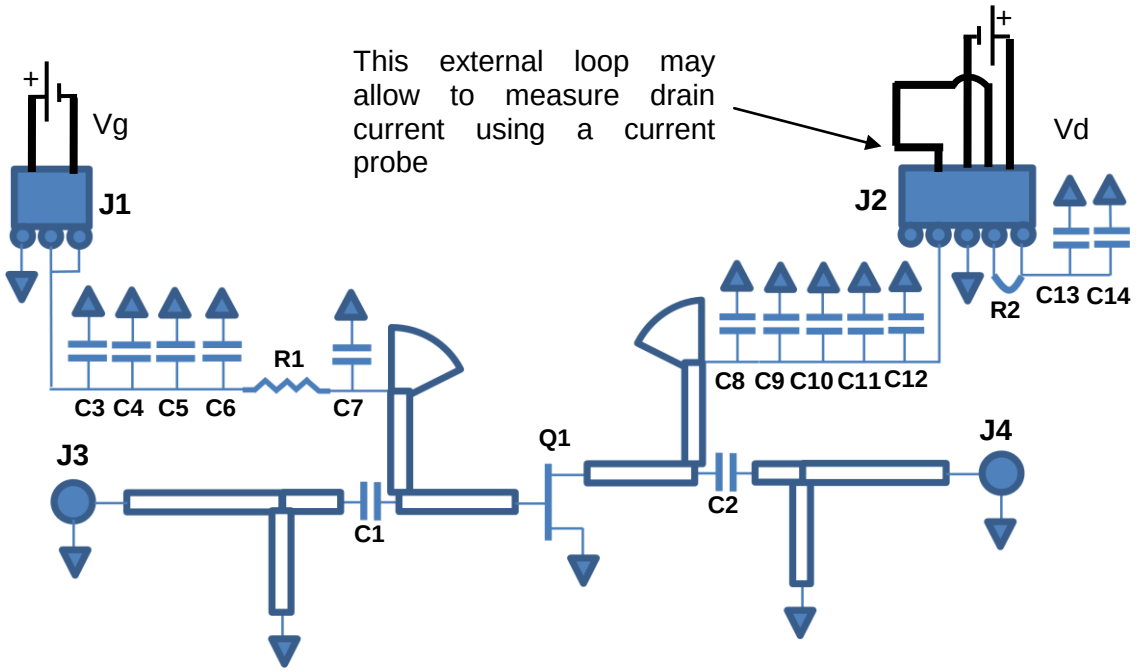
Demonstration Amplifier Low Frequency Equivalent Schematic

(Ref. 61499536B)



Demonstration Amplifier (Ref. 61499536B) / Bill of Materials

Designator	Type	Value - Description	Qty
C1, C2	Capacitor	4.7pF, +/- 0.05pF, 0603	2
C3, C12	Capacitor	240pF, +/- 5%, 0805	2
C4, C11	Capacitor	150pF, +/- 0.25%, 0803	2
C5, C10	Capacitor	82pF, +/- 5%, 0603	2
C6, C9	Capacitor	22pF, +/- 5%, 0603	2
C7,C8	Capacitor	8.2pF, +/- 0.25pF, 0603	2
C13	Capacitor	1µF, +/- 10%, 1204	1
C14	Capacitor	68µF, +/- 10%, 1204	1
R1	Resistor	22Ω, +/- 1%, 0603	1
R2	Resistor	Jumper 0Ω +/- 1%, 0805	1
J1	Connector	SMD 3 contacts	1
J2	Connector	SMD 5 contacts	1
J3,J4	Connector	SMA	2
Q1	Transistor	CHZ050A-SEA	1
	PCB	RO4003 – thickness 0.508 mm – Er=3.5	1

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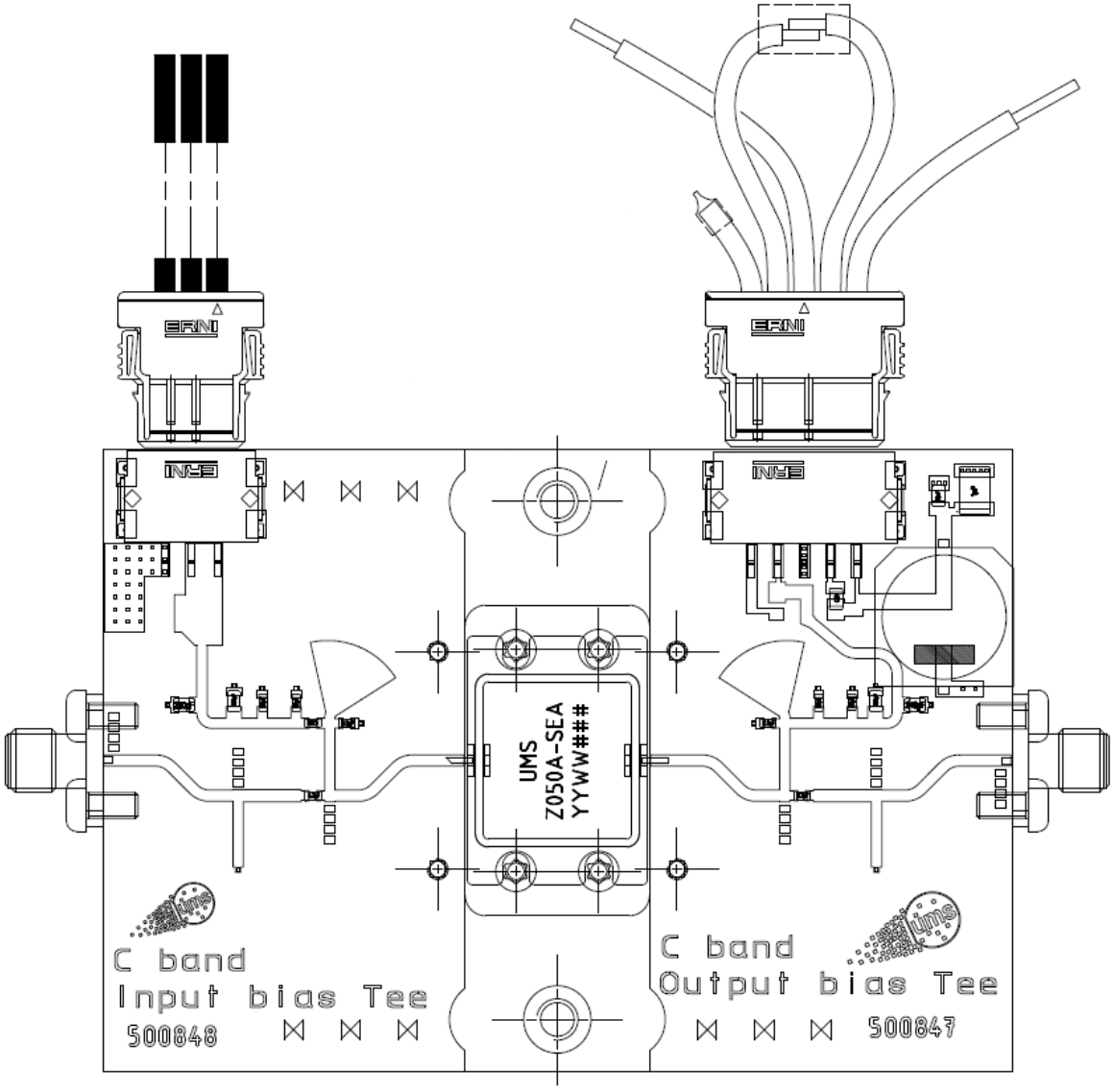
Demonstration Amplifier Circuit (Ref. 61499536B)



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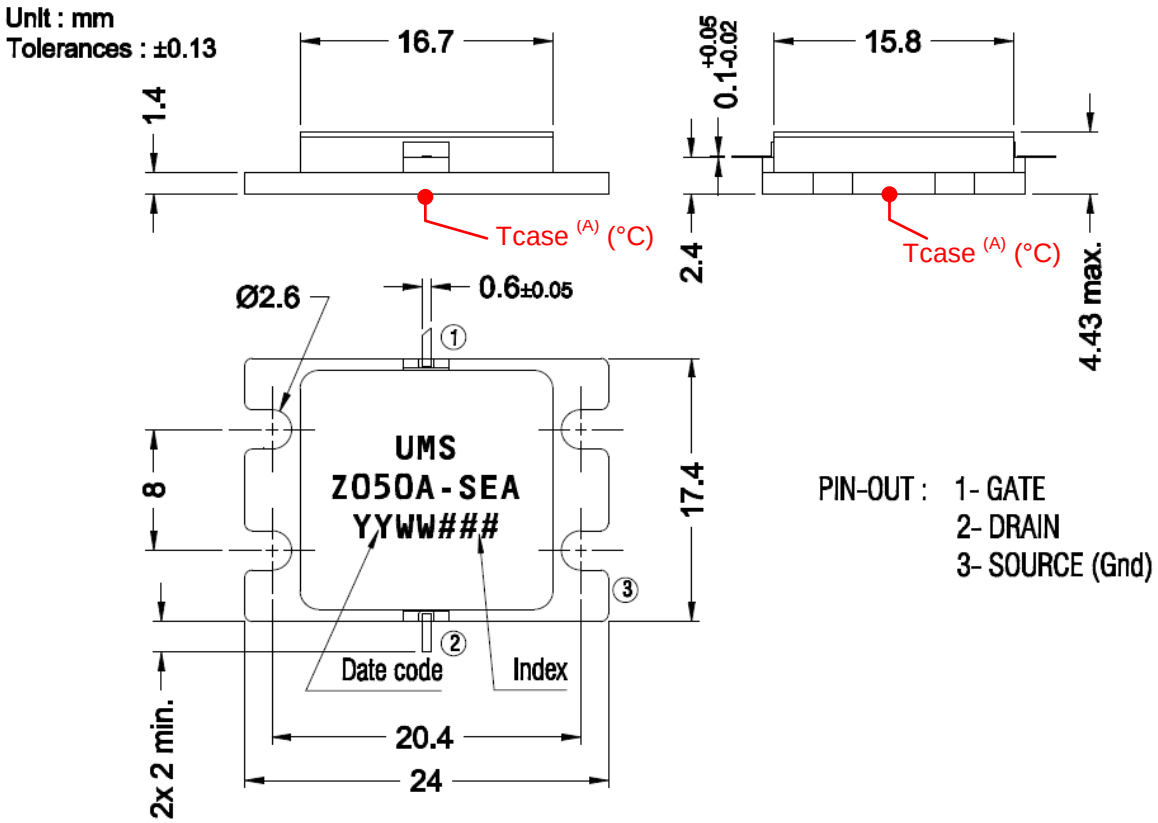
Package outline



(A) Tcase locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design.
Chamfered lead indicates the gate access of the packaged transistor.

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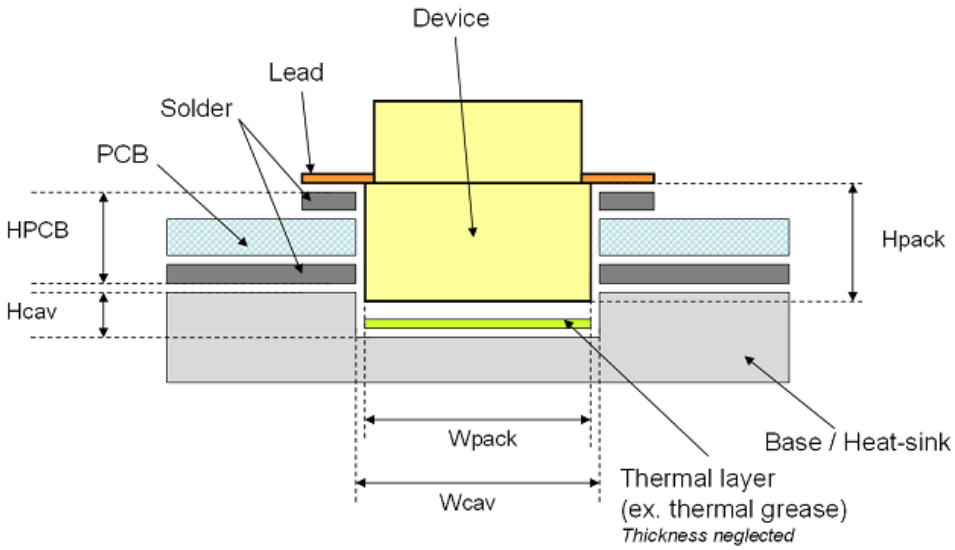
Recommended Assembly Procedure

CHZ050A-SEA is available as a flange package to be bolted down onto a thermal heat sink also used as main electrical ground. Use preferably screw M2 and flat washers.
Thermal and electrical resistance at the package to heat sink interface has to be as low as possible. Thermal electrically conductive grease or conductive thin layer like indium sheets are recommended between the package and the heat sink.
In case a thermal grease is selected, we recommend to use material offering thermal conductivity >5W/m.K and electrical resistivity <0.01 ohm.cm. The grease layer thickness should be about 25µm (1 mil).
Contact interface quality can be improved by cleaning process prior device mounting on the heat-sink. Such operation will enhance the thermal and electrical contact by oxides removal at each interface.
Package leads can be soldered on printed circuit board traces by using RoHS solder past.
Cavity depth and width to be performed into the heat-sink where the device will be mounted are important to achieve the best performances. These dimensions have to be optimized in order to minimize the distance between device and signal traces made on the printed circuit board (PCB). But they also have to be calculated in order to accommodate device variations in height. The following drawing gives the relationship between device dimensions (Hpack & Wpack) and optimal cavity depth (Hcav) and width (Wcav) depending on the printed circuit-board configuration (HPCB)



$Hcav = (Hpack_{min} - HPCB_{max})\ ^{+0}_{/-\ 0.05}$

$Wcav = (Wpack_{max} + 0.4)\ ^{+/-\ 0.05}$

dimensions are in mm

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Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Package:	CHZ050A-SEA/XY Tray: XY = 26

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