CHT-CG50 DATASHEET

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(Last modified date)

Versatile High-Temperature Clock Generator

General Description

The CHT-CG50 is a versatile High-Temperature crystal clock generator with extended functional capabilities. The chip features a programmable crystal oscillator driver with an enable/disable control signal, an external clock input, a programmable divider chain and a programmable strength three-state output buffer. Using an external crystal, it is intended to provide reliable precision performance throughout the -55 to +225°C temperature range for supply voltages between 3.3V and 5V.

The CHT-CG50 can operate with crystals from 1MHz to 50MHz. The output frequency can be selected by means of a programmable divider, providing division factors of one, two, four and eight. The programmability of the crystal driver allows working with a wide range of crystals. A crystal driver enable pin (**/XtalEn**) is included for extremely low power applications, as well as an output enable pin (**/OE**). In applications requiring only a precision divider chain, where an external clock source is already present, the crystal driver may be bypassed by means of inputs **ExtClkIn** and **ExtClkEn**.

Features

- Power supply:
  - 5V +/-10% (1MHZ – 50MHz)
  - 3.3V +/-5% (1MHZ – 30MHz)
- Qualified from -55 to +225°C (Tj)
- Two input sources: crystal (1 to 50 MHz), external clock (DC to 50MHz)
- Operation from 32.768kHz crystals
- Programmable frequency divider: fin, fin/2, fin/4 and fin/8
- Programmable crystal driver and output driver strength
- Available in CDIL24 ceramic package.
- Validated at 225°C for 43800 hours (and still on-going)
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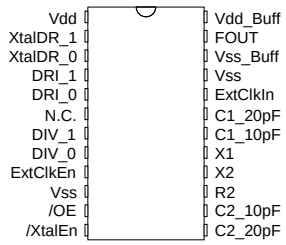
Applications

- Well logging, Automotive, Aeronautics & Aerospace
- Precision timing

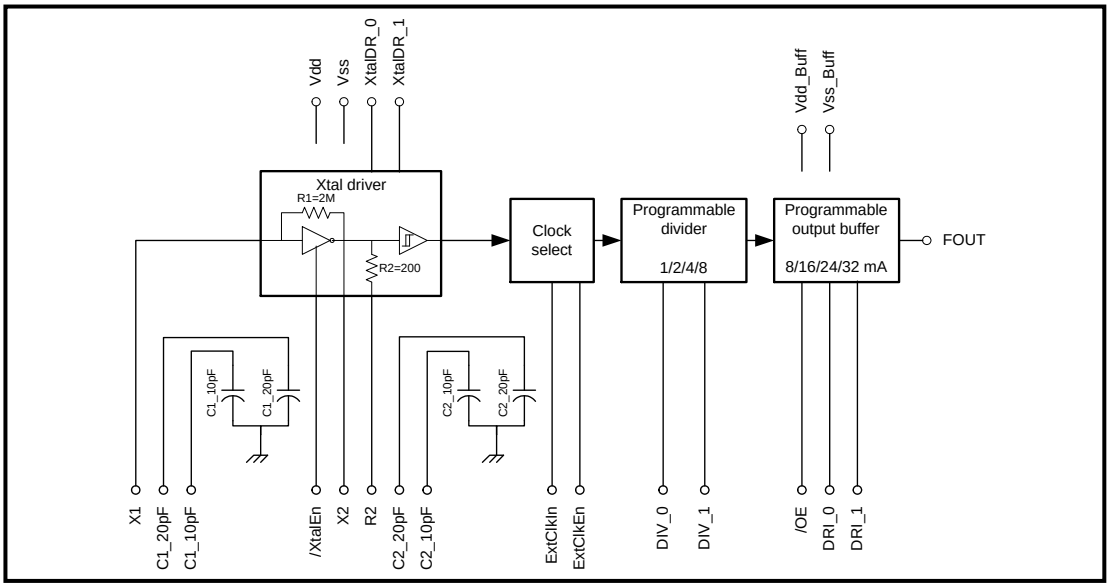
Package Configurations[1]

CG50
DIL24



[1] Other packages available upon request.

Functional Block Diagram



Pin Description (DIL24)

1 Vdd Circuit core power supply terminal.

2 XtalDR_1
3 XtalDR_0 Inputs to set the crystal drive strength.

TRUTH TABLE

XtalDR_1	XtalDR_0	Strength
0	0	Lowest
0	1	Low
1	0	High
1	1	Highest

4 DRI_1
5 DRI_0 Inputs to set the output buffer strength.

TRUTH TABLE

DRI_1	DRI_0	Strength
0	0	8mA
0	1	16mA
1	0	24mA
1	1	32mA

7 DIV_1
8 DIV_0 Inputs to set the division factor.

TRUTH TABLE

DIV_1	DIV_0	Factor
0	0	1
0	1	2
1	0	4
1	1	8

9 ExtClkEn When driven HIGH, operation from the external clock source is selected.

10 Vss Circuit core ground terminal.

11 /OE When driven LOW, output is enabled, When driven HIGH, output is at high impedance.

12 /XtalEn When driven LOW, the crystal oscillator is enabled. When driven HIGH, the crystal oscillator is stopped.

13 C2_20pF
14 C2_10pF Built-in capacitors with a common terminal connected to Vss.

15 R2 Terminal of a 200Ω resistor. The other terminal of this resistor is connected to X2.

16 X2 Output of crystal driver

17 X1 Input of crystal driver

18 C1_10pF
19 C1_20pF Built-in capacitors with a common terminal connected to Vss.

20 ExtClkIn Input for an external clock source.

21 Vss Circuit core ground terminal.

22 Vss_Buff Output buffer ground terminal.

23 FOUT Output signal.

24 Vdd_Buff Output buffer power supply terminal.

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND	-0.5 to 6.0V
Voltage on any Pin to GND	-0.5 to V_{DD}+0.3V

ESD Rating

Human Body Model	Class0 (<250V)

Operating Conditions

Supply Voltage V_{DD} to GND	3.3V to 5V
Junction temperature	-55°C to +225°C

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.*

Electrical Characteristics

Unless otherwise stated: V_{DD}=5V, T_j=150°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage **V_{DD}**		3.13		5.5	V
Current consumption[1] **Idd**	V_{DD} = 3.3V, F_{IN} = 1MHz Output disabled (/OE: HIGH)		0.1	**0.16**	mA
	V_{DD} = 3.3V, F_{IN} = 1MHz Output enabled (/OE: LOW) C_L = 22pF		0.25	**0.32**	
	V_{DD} = 3.3V, F_{IN} = 27MHz Output disabled (/OE: HIGH)		0.64	**0.67**	
	V_{DD} = 3.3V, F_{IN} = 27MHz Output enabled (/OE: LOW) C_L = 22pF		4.73	**4.79**	
	V_{DD} = 5V, F_{IN} = 1MHz Output disabled (/OE: HIGH)		0.41	**0.69**	
	V_{DD} = 5V, F_{IN} = 1MHz Output enabled (/OE: LOW) C_L = 22pF		0.65	**0.94**	
	V_{DD} = 5V, F_{IN} = 27MHz Output disabled (/OE: HIGH)		1.33	**1.40**	
	V_{DD} = 5V, F_{IN} = 27MHz Output enabled (/OE: LOW) C_L = 22pF		7.91	**8.06**	
	V_{DD} = 5V, F_{IN} = 35MHz Output disabled (/OE: HIGH)		1.91	**1.96**	
	V_{DD} = 5V, F_{IN} = 35MHz Output enabled (/OE: LOW) C_L = 22pF		10.61	**10.74**	
	V_{DD} = 5V, F_{IN} = 50MHz Output disabled (/OE: HIGH)		2.15	**2.35**	
	V_{DD} = 5V, F_{IN} = 50MHz Output enabled (/OE: LOW) C_L = 22pF		14.26	**14.37**	
Minimum HIGH level output voltage **V_{OH}**	R_{LOAD} = 600Ω	**4.67**			V
Maximum LOW level output voltage **V_{OL}**	R_{LOAD} = 600Ω			**0.30**	V
Minimum HIGH level input voltage **V_{IH}**		**3.15**			V
Maximum LOW level input voltage **V_{IL}**				**1.35**	V
Internal capacitors					
Initial accuracy			17		%
Temperature drift	ΔT = 225°C - 25°C		0.6		%
TC1	$C(T) = C(T_0)$ [1+TC1.$(T-T_0)$+ TC2.$(T-T_0)^2$]		0.023		10^{-3}/K
TC2			0.013		$10^{-6}/K^2$

[1] The given value includes the consumption due to the load. Current consumption due to a capacitive load must be computed according to $I_{LOAD} = C_L.V_{DD}.f$.

AC Electrical Characteristics

Unless otherwise stated: V_{DD}=5V, T_j=150°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Frequency range **F_{IN}**		1		50	MHz
Duty cycle @ 50% V_{DD} **DC**[1] [2]	F_{IN}=1MHz, V_{DD} = 5V		52/48	**53/47**	%
	F_{IN}=27MHz, V_{DD} = 5V		45/55	**44/56**	
	F_{IN}=35MHz, V_{DD} = 5V		44/56	**44/56**	
	F_{IN}=50MHz, V_{DD} = 5V		42/58	**42/58**	
Output rise time[3] 10% to 90% V_{DD} **t_r**	Vdd = 5V, Z_{LOAD} = 1MΩ // 22pF		**3.0**		ns
	Vdd = 5V, Z_{LOAD} = 600Ω // 15pF		2.5		
Output fall time[4] 10% to 90% V_{DD} **t_f**	Vdd = 5V, Z_{LOAD} = 1MΩ // 22pF		**2.5**		ns
	Vdd = 5V, Z_{LOAD} = 600Ω // 15pF		2.1		
Oscillation established after Vdd goes high[4] **$t_{power-on}$**	V_{DD} from 0 to 5V		1.2 **3.2**		ms
Oscillation established after /XtalEn goes LOW[5] **$t_{start-up}$**	V_{DD} = 5V /XtalEn from LOW to HIGH		0.6 **1.4**		ms
Equivalent capacitance at driver input (X1) C_{X1}	Passive[5]. Freq= 1MHz	**0.89**		**0.93**	pF
	Active[6]. Freq= 1MHz	**1.56**		**2.81**	
Equivalent capacitance at driver output (X2) C_{X2}	Freq= 1MHz	**0.54**		**0.91**	pF
Equivalent capacitance at limiting resistor (R2) C_{R2}	Freq= 1MHz	**0.27**		**0.35**	pF

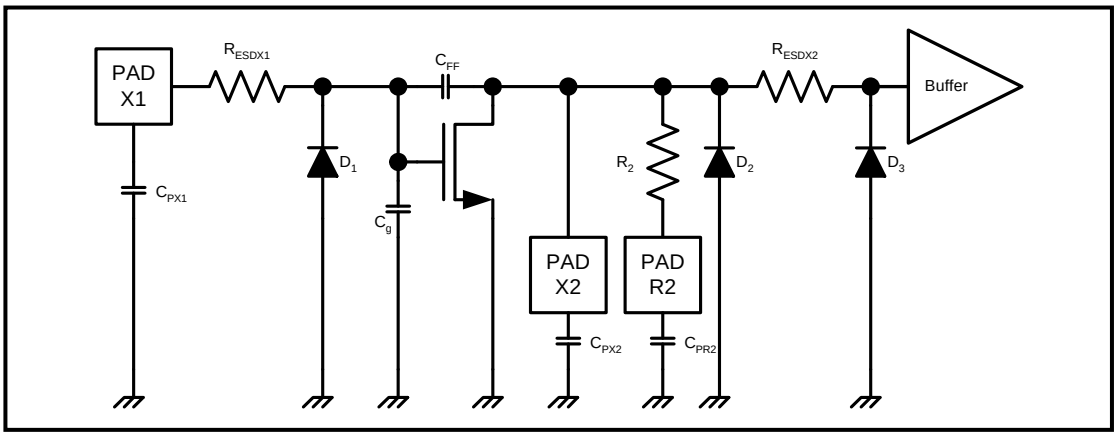
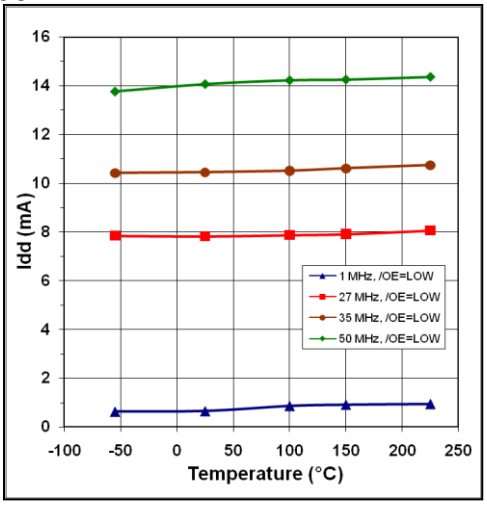


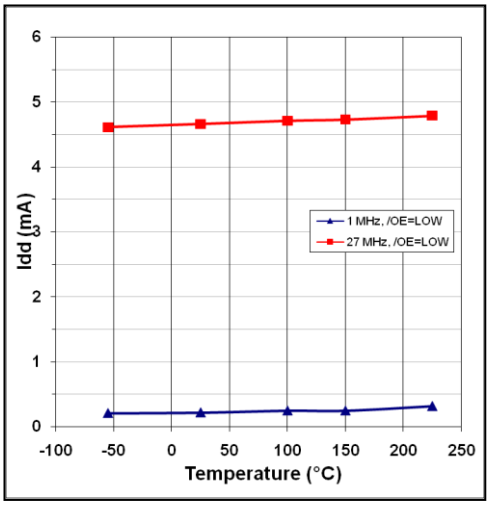
Figure 1. CHT-CG50: equivalent simplified diagram for the determination of capacitances at X1 and X2.

[1] Duty cycle is measured with a unitary division factor and Z_{LOAD} = 1050Ω // 22pF.
[2] Depends on used crystal and **R2** value.
[3] Depends on load conditions and **DRI_0**, **DRI_1** settings.
[4] Depends on used crystal and **XtalDR_0**, **XtalDR_1** settings.
[5] Considers all capacitances but without taking into account Miller effect on C_{FF} (see **Figure 1**).
[6] Considers all capacitances including Miller effect on C_{FF} (see **Figure 1**).

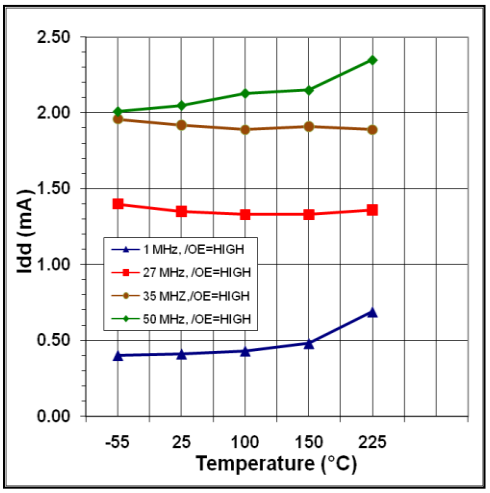
Typical Performance Characteristics



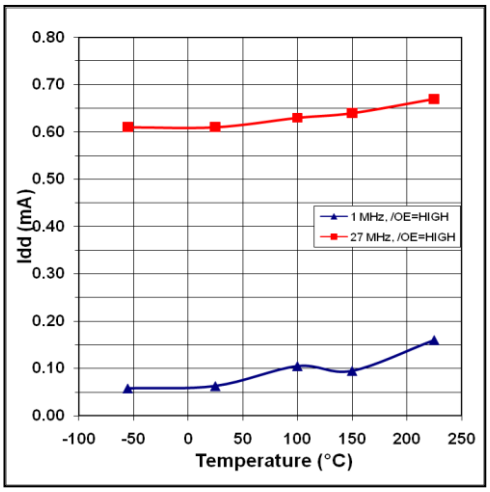
Current consumption, V_{DD} = 5V, /OE = LOW, C_L = 22pF



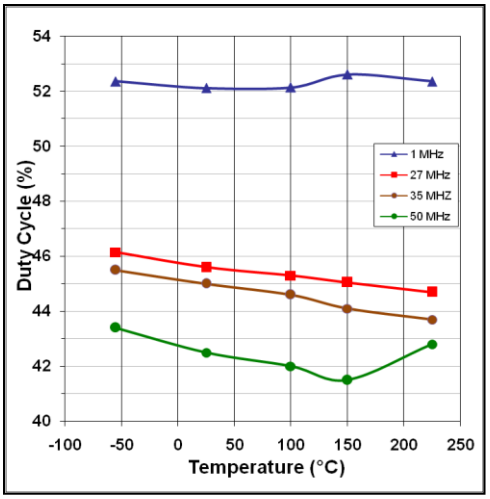
Current consumption, V_{DD} = 3.3V, /OE = LOW, C_L = 22pF



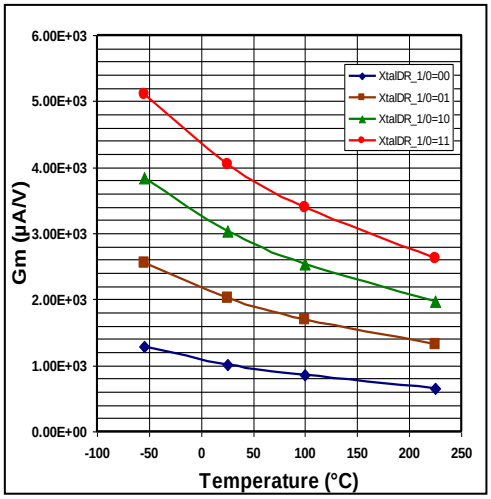
Current consumption, V_{DD} = 5V, /OE = HIGH



Current consumption, V_{DD} = 3.3V, /OE = HIGH



Duty cycle, V_{DD} = 5V



Transconductance of crystal driver, V_{DD} = 5V

Circuit Functionality

Operating conditions

The CHT-CG-050 is qualified for supply voltages ranging from 3.3V up to 5.5V.

The operating temperature range extends from -55°C to +225°C.

Crystal driver

XtalDR_0 and **XtalDR_1** allow the crystal driver to change its strength to be able to oscillate with a wide range of crystals, under any supply (3.3V to 5V) and temperature (up to 225°C) condition.
The presence of integrated passive components offers a great versatility to the final user. Highly temperature-stable capacitors allow for a nearly-constant crystal load along the whole temperature range. Internal passive components can be bypassed or tied to ground if needed.
/XtalEn enables or disables the crystal oscillator to operate, allowing the CHT-CG-050 to be embedded into power-optimized high-temperature applications.

Clock source selector

By means of **ExtClkEn** and **ExtClkIn**, the CHT-CG-050 is able to operate either from its internal crystal oscillator or from an external clock source.

Frequency divider

Four division factors (1, 2, 4 and 8) can be selected depending on the levels at the control lines **DIV_0** and **DIV_1**.

Output buffer

A programmable-strength output buffer, controlled by **DRI_0** and **DRI_1**, enables the CHT-CG-050 to drive a large range of output loads, improving the output signal integrity. The four possible output strengths are 8mA, 16mA, 24mA and 32mA.
The output buffer has supply terminals independent from the rest of the circuit, allowing the system designer to properly decouple them in noise-sensitive application.

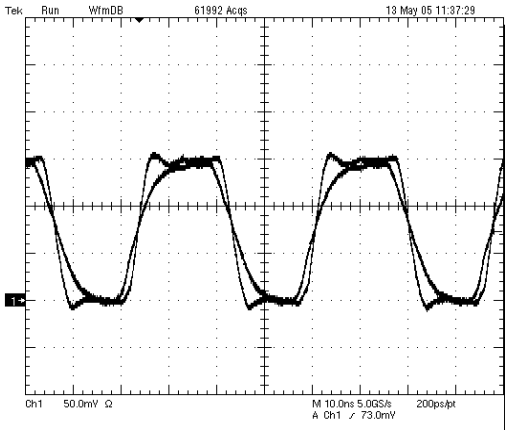


Figure 2. Effect of **DRI_0** and **DRI_1** on the output signal.

Figure 2 shows the superposition of the output signal when **DRI_0**, **DRI_1** = LOW and **DRI_1** is then set to HIGH, V_{DD}=3.3V, T=235°C, Freq = 27MHz. As a result, the signal integrity is improved.

Packaging options

As mentioned above, the layout of the CHT-CG-050 allows for a very high level of flexibility for the system designer. Several packaging configurations are possible, from 8-pin to 24-pin standard carriers.
At the packaging stage, many functional features can be enabled or safely disabled in order to optimize the form factor according to the final user needs.

Typical application

The CHT-CG-050 offers the final user several possible configurations depending upon the characteristics of the target application.

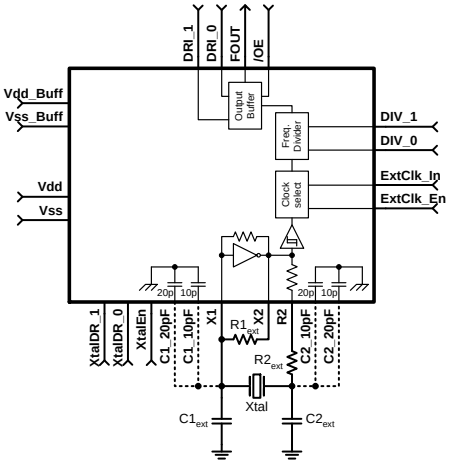


Figure 3. Full configuration.

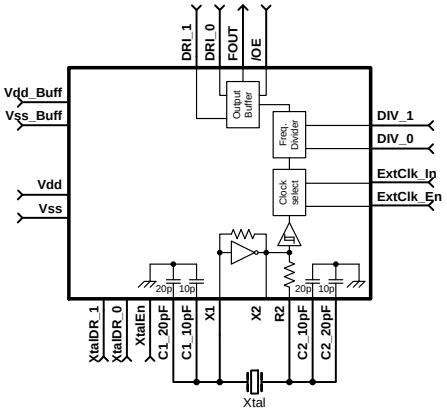


Figure 4. Minimal configuration.

Dashed lines in Figure 3 indicate optional connections. Figure 4 shows the minimal possible configuration with no external components. Any configuration in between those of Figure 3 and Figure 4 can be obtained by properly bypassing or tying to ground the corresponding internal component.

Any programmable feature can be changed on-the-fly, allowing the CHT-CG-050 to accommodate to new operating conditions in smart or adaptive applications.

Output impedance matching

The CHT-CG50 is able to provide an output signal with very short transition times (<10ns). During this transition periods, the output signal must be seen as a signal with a frequency above 100MHz. Under this assumption, PCB traces or cables connected to the output represent inductors or even transmission lines.

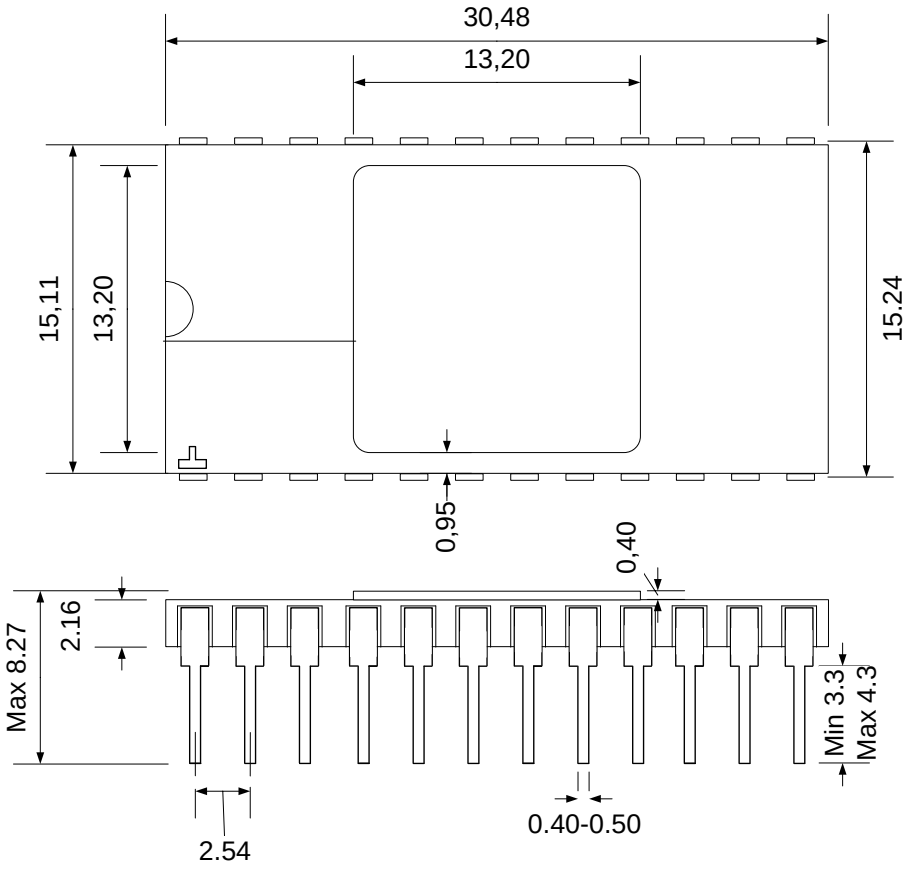
Signal integrity good practices must be considered when driving PCB traces or cables with the CHT-CG50 output. PCB traces or cables can induce ringing and even reflections back to the output buffer. Too much reflection onto the output buffer may cause overshoots and undershoots on the CHT-CG50 terminals exceeding the Absolute Maximum Ratings of the device leading to permanent damage.

To reduce or avoid ringing or signal reflection, impedance matching considerations must be taken into account. To do so, adapt the CHT-CG50 output drives strength (**DRI_0** and **DRI_1**) to the final application load conditions, place capacitive loads as close as possible of the CHT-CG50 output, keep traces and cables as short as possible and, when driving long traces or cables cannot be avoided, place a resistor in series with the output as close to it as possible in order to match the trace or cable impedance. This resistor, generally in the range from 10Ω to 100Ω must be experimentally determined given the final application load conditions.

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-CG50-DIL24-T	Ceramic DIL24	-55°C to +225°C	CHT-CG50

Package Dimensions



Drawing CDIL24 (mm +/-10%)

Contact & Ordering

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