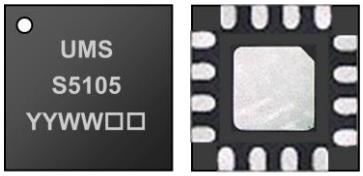
CHS5105-QAG

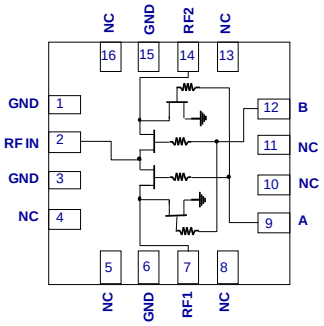
DC-4GHz Reflective SPDT

GaAs Monolithic Microwave IC in SMD leadless package

Description

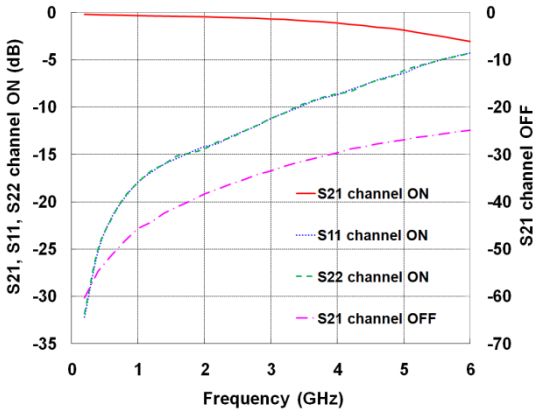
The CHS5105-QAG is a monolithic FET based reflective switch.
It is designed for a wide range of applications, from military to commercial systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.





Main Features

- Broadband performance: DC-4GHz
- Low insertion loss: 0.7dB
- Isolation: 40dB
- Return loss: 16dB
- Input P1dB: 30dBm
- QAG-QFN3x3
- MSL1



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	DC		4	GHz
IL	On state insertion loss		0.7		dB
ISOL	Off state isolation		40		dB
RL	On state return loss		16		dB
IP1dB	Input Power @1dB gain compression		30		dBm

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Electrical Characteristics (1)

Tamb.= +25°C, specifications are given for 50Ω source and load impedances.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Freq	Frequency range		DC		4	GHz
IL	On state insertion loss (2)	DC - 2GHz DC - 4GHz		0.3 0.7		dB
ISOL	Off state isolation	DC - 2GHz DC - 4GHz		45 35		dB
RL	On state input and output return losses	DC - 2GHz DC - 4GHz		16 12		dB
VH	Control voltage high level			0	0.5	
VL	Control voltage low level		-8	-5		V
IP1dB	Input Power @1dB gain compression.	DC - 1GHz VL=-5V/VH=0V VL=-8V/VH=0V 1GHz - 4GHz VL=-5V/VH=0V VL=-8V/VH=0V		 27 30 30 33		dBm
Ton / Toff	Switching time	50% control to 90% RF, and 50% control to 10% RF		10		ns
Ic	Current consumption on the control supply voltage	Freq. ≥0.5GHz Pin≤33dBm VH= 0V VL=-5V VL=-8V		 150 50 300		µA

(1) These values are representative of on-board measurements with correction of the board losses.

(2) Variation rate of insertion loss with temperature in the range -40°C to +85°C: 0.002dB/°C

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VH	High level control voltage	0.8	V
VL	Low level control voltage	-10	V
Pin	Maximum peak input power overdrive (2)	37	dBm
Tj	Junction temperature(3)	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s, Frequency >1GHz

(3) Thermal Resistance channel to ground paddle <33°C/W for Tamb. = +85°C.

SPDT truth table

PAD A	PAD B	Electrical path RFC to RF1	Electrical path RFC to RF2
VH	VL	ON	OFF
VL	VH	OFF	ON

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.

The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the PCB system must be designed to comply with this requirement.

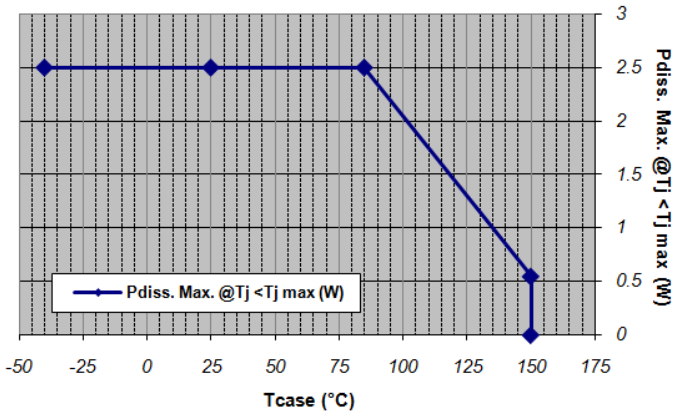
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

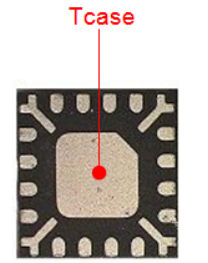
DEVICE THERMAL SPECIFICATION : CHS5104-QAG		
Recommended max. junction temperature (Tj max)	:	168 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power (Pdiss. Max.)	:	2.5 W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	30 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<33 °C/W
Minimum Tcase operating temperature(3)	:	-40 °C
Maximum Tcase operating temperature(3)	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

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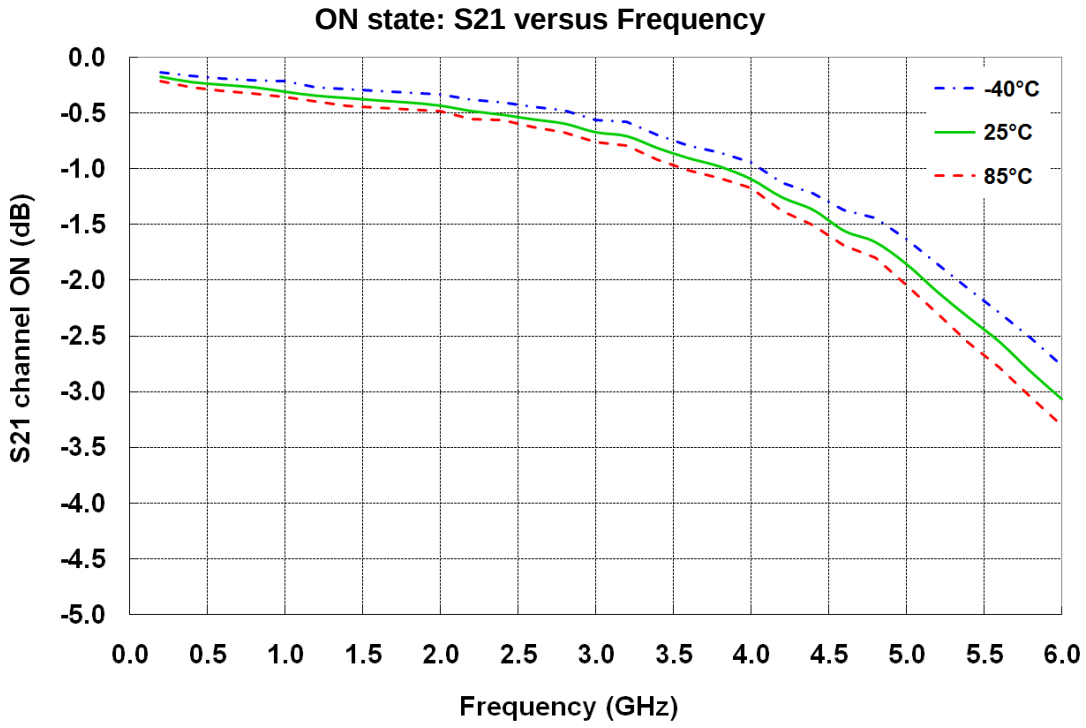
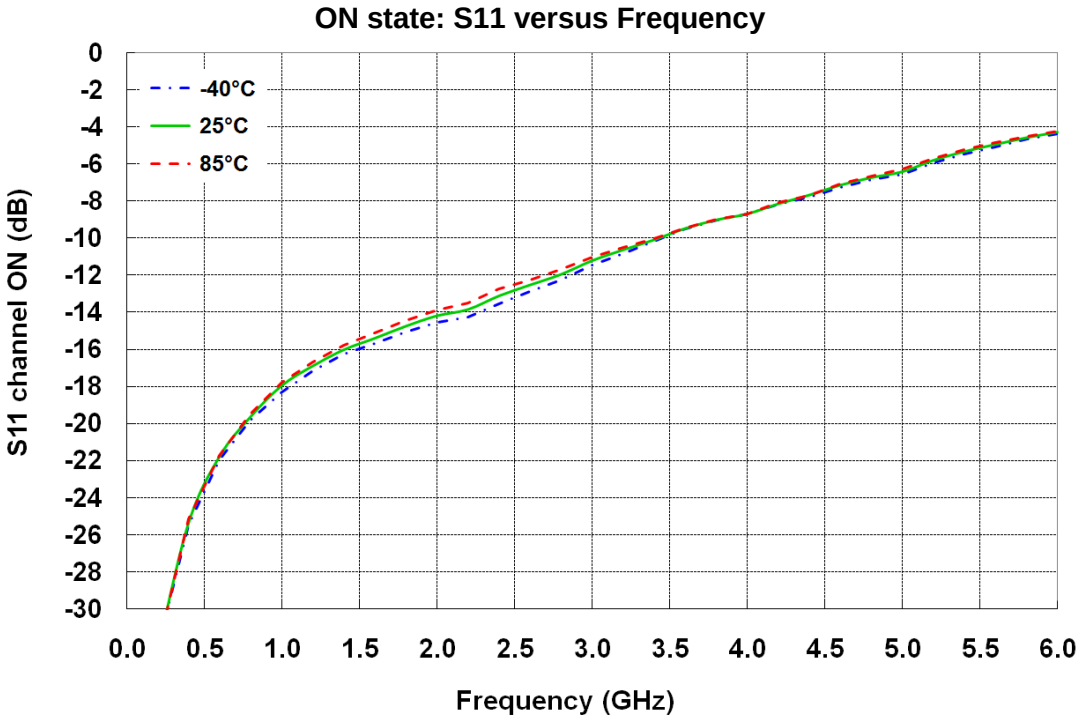
Typical Board Measurements

Tamb.= +25°C, VH=0V / VL=-5V
Note: board losses are corrected





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Typical Board Measurements

Tamb.= +25°C, VH=0V / VL=-5V
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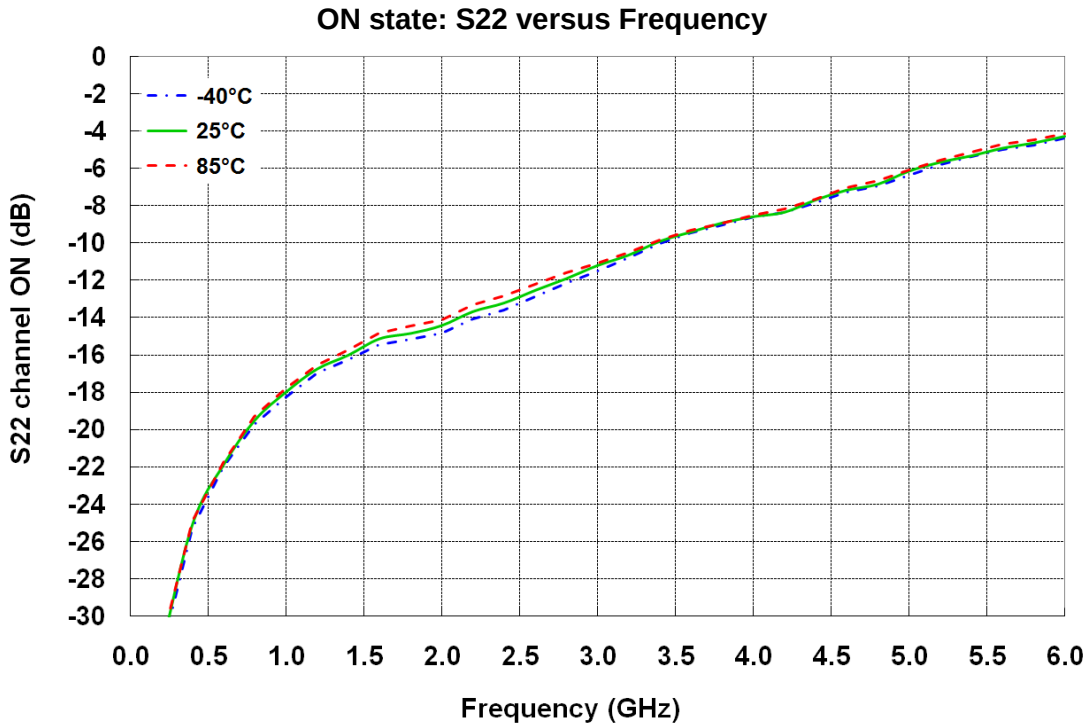

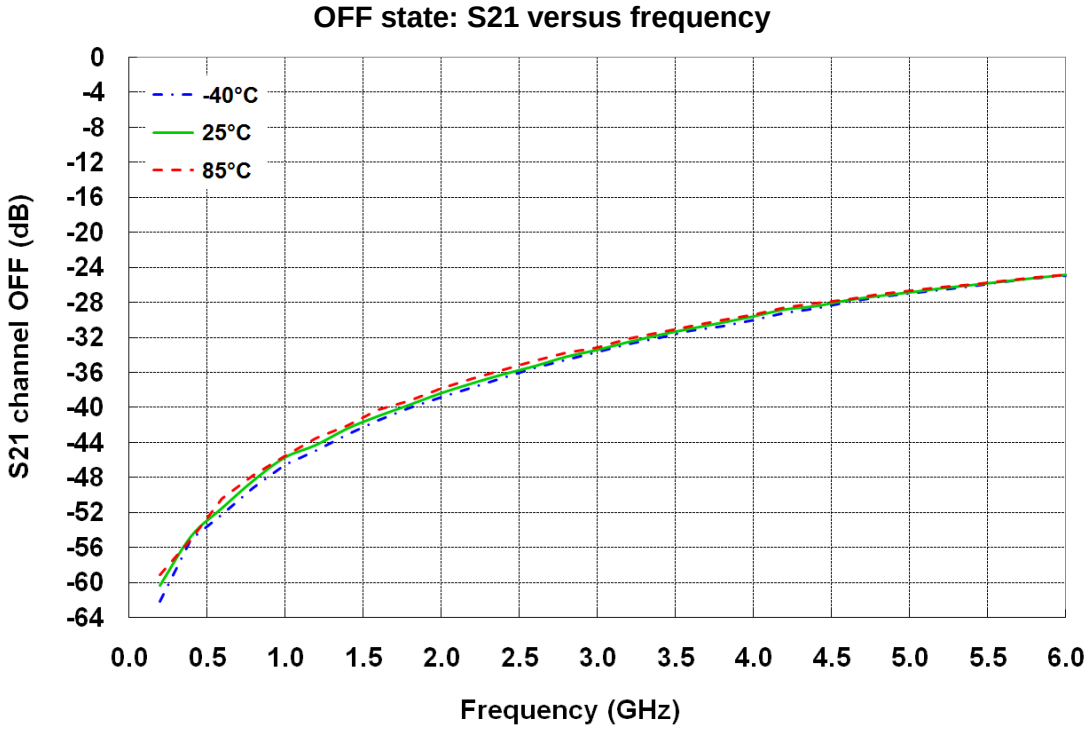

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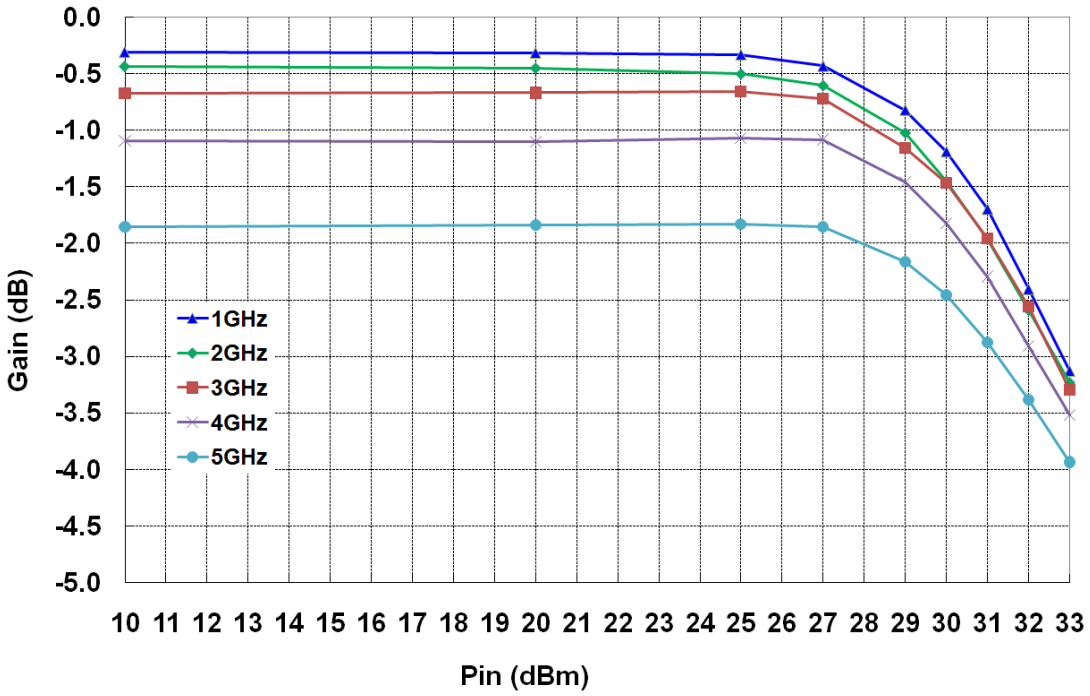
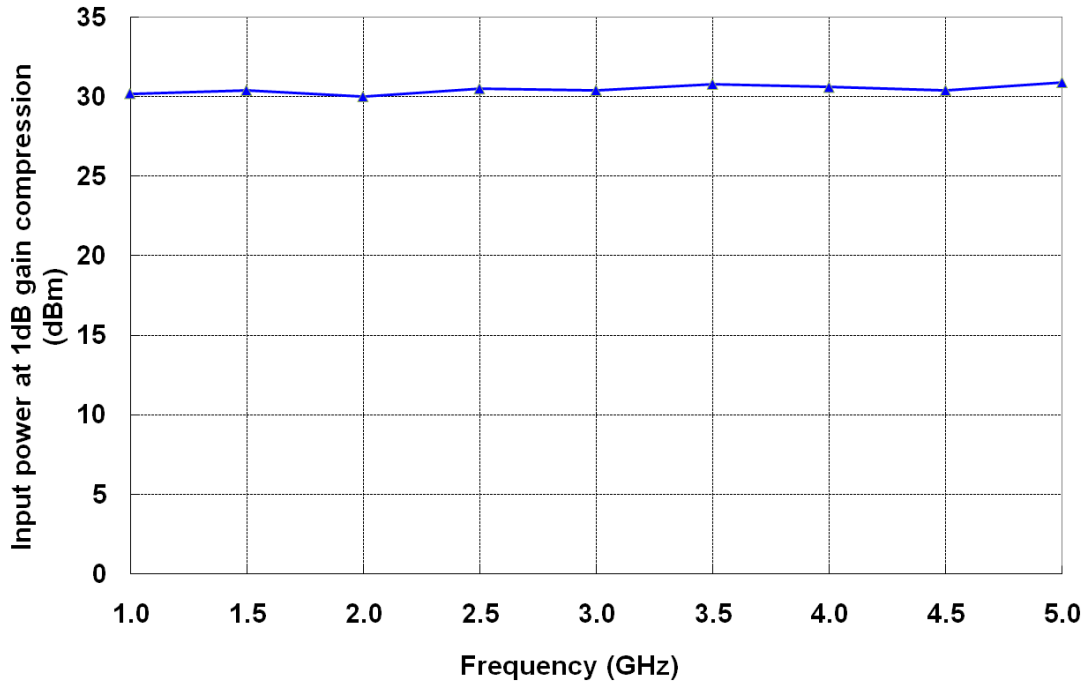
Typical Board Measurements

Tamb.= +25°C, VH=0V / VL=-5V
Note: board losses are corrected

Insertion Loss variation versus input power



Input power at 1dB gain compression versus frequency



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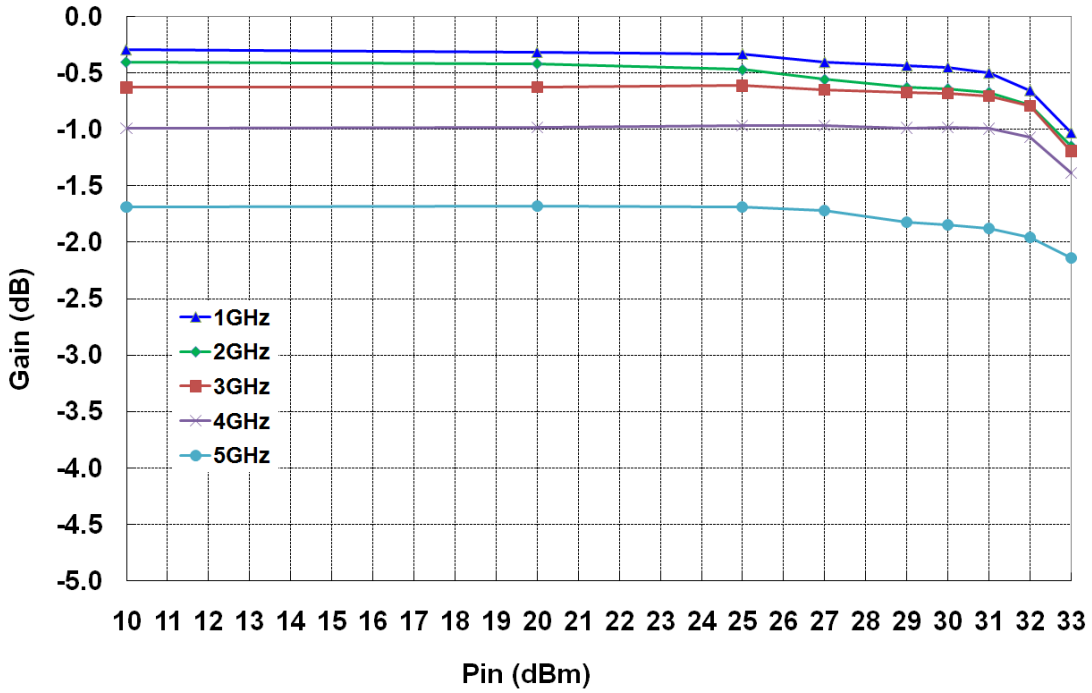
Typical Board Measurements

Tamb.= +25°C, VH=0V / VL=-8V
Note: board losses are corrected

Insertion Loss variation versus input power



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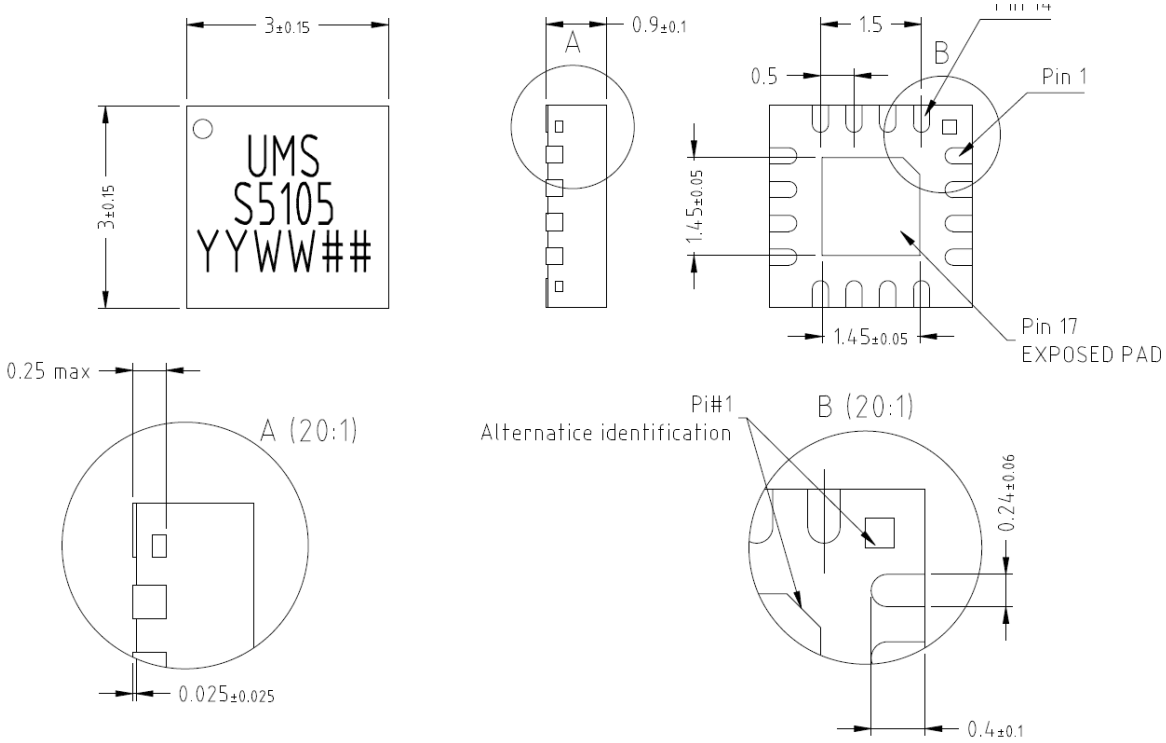
Package outline [1]



Matt tin, Lead Free	(Green)	1- Gnd[2]	9- A
Units :	mm	2- RFC	10- Nc
From the standard :	JEDEC MO-220	3- Gnd[2]	11- Nc
	(VGGD)	4- Nc	12- B
17-	GND	5- Nc	13- Nc
		6- Gnd[2]	14- RF2
		7- RF1	15- Gnd[2]
		8- Nc	16- Nc

[1] The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

[2] It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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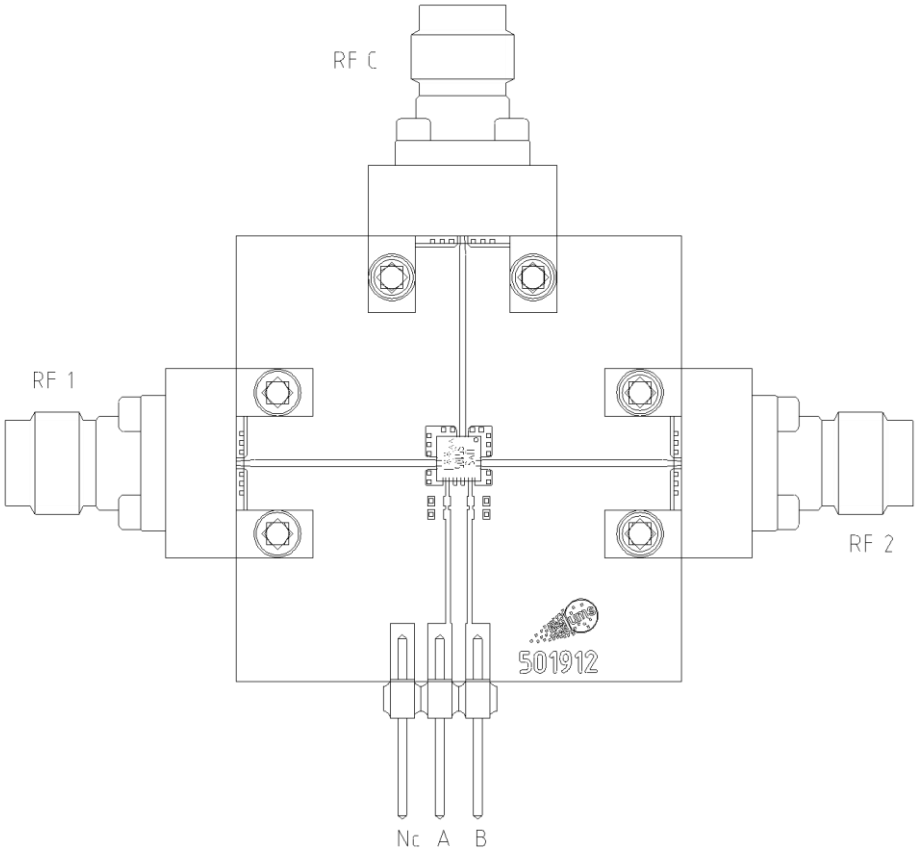
Evaluation mother board

- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for implementation of this product on a module board.
- See application note AN0017 for details.



Recommendation on decoupling

Label	Type	Decoupling	Comment
A, B	Control voltage	Not required	SPDT switch pad control
RFC, RF1, RF2	RF access	External DC block must be used to ensure DC decoupling	The MMIC is DC coupled

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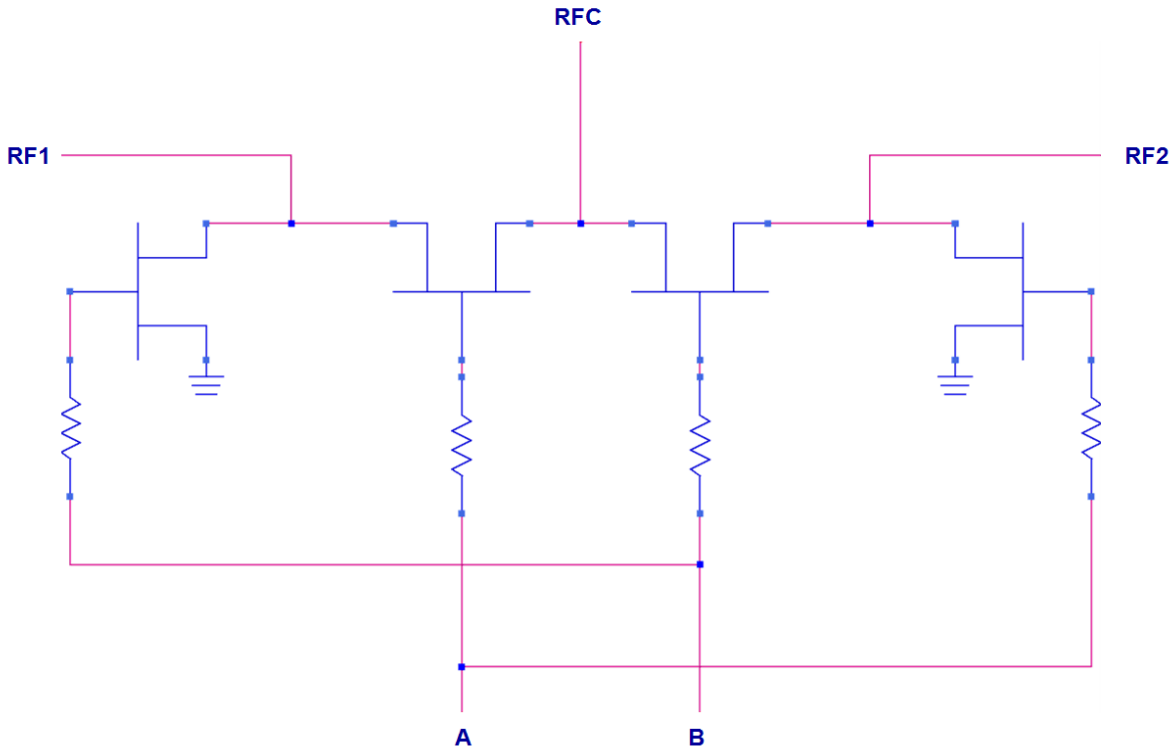
Notes

The DC connections do not include any decoupling capacitor in package; therefore it might be necessary to provide a good external DC decoupling on the PC board, as close as possible to the package.

DC Schematic



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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 3x3 package:	CHS5105-QAG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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