

36-43.5GHz Power Amplifier

GaAs Monolithic Microwave IC in bare die

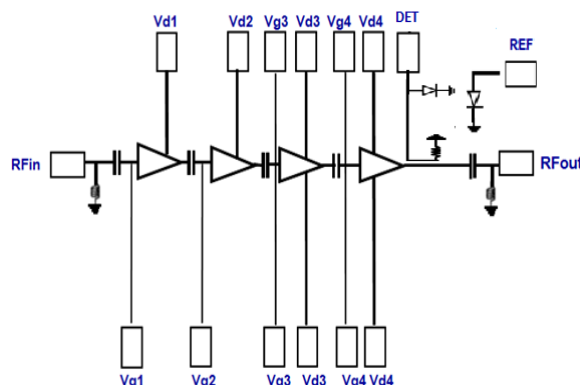
Description

The CHA5659-98F is a four stage monolithic GaAs High Power Amplifier producing 1.3 Watt output power. It is highly linear, with possible gain control and integrates a power detector. ESD protections are included.

It is designed for Point To Point Radio or K-band SatCom applications.

The CHA5659-98F is recommended with the CHA3398-98F as a driver.

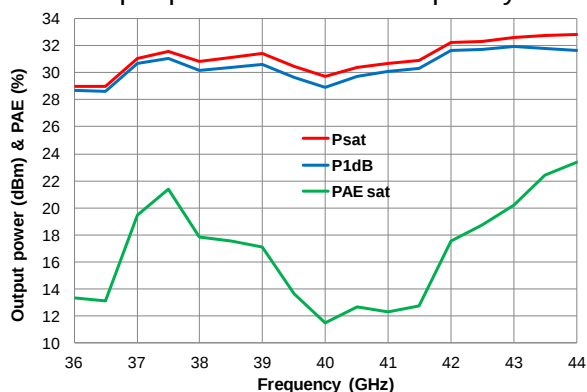
The circuit is manufactured with a pHEMT process, 0.15µm gate length.



Main Features

- Broadband performances: 36-43.5GHz
- 31dBm saturated power
- 38dBm OIP3
- 22dB gain
- Gain control up to 15dB
- DC bias: Vd = 6.0Volt @ Idq = 0.8A
- Chip size 3.60x3.00x0.07mm

Output power & PAE vs frequency



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	36.0		43.5	GHz
Gain	Linear Gain		22		dB
Psat	Saturated output power		31		dBm
OIP3	Output IP3		38		dBm

Specifications

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	36.0		43.5	GHz
Gain	Small Signal Gain		22		dB
ΔG	Gain variation in temperature		± 0.04		dB/°C
Psat	Saturated Output Power		31		dBm
OIP3	Output IP3		38		dBm
P1dB	Pout at 1dB of compression		30		dBm
PAE	PAE at saturation		15		%
CG	Gain control range		15		dB
Rlin	Input Return Loss		8		dB
Rlout	Output Return Loss		10		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF} - V_{DET} up to Psat		20 to 2000		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		0.8		A

These values are representative of on-board measurements.

Electrostatic discharge sensitive device observe handling precautions!

Absolute Maximum Ratings ^{1, 2}T_{amb}. = +25°C

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	8	V
I _d	Drain bias current	1900	mA
V _g	Gate bias voltage	-2 to 0	V
V _{dg}	External drain-gate excursion	12	V
P _{in}	Maximum Input Power	+15	dBm
T _j	Maximum Junction temperature	175	°C

¹ Operation of this device above anyone of these parameters may cause permanent damage.

² These are stress rating only, and functional operation of the devices at these conditions is not implies.

Recommended Operating Range ^{3, 4}

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	5 to 6	V
I _d	Drain bias current	640 to 800	mA
V _g	Gate bias voltage	-2 to 0	V
P _{in}	Maximum peak input power overdrive	15	dBm
T _a	Operating temperature range	-40 to 95	°C

³ Electrical performances are defined for specified test conditions

⁴ Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

T _a	Operating temperature range	-40 to +95	°C
T _{stg}	Storage temperature range	-55 to +150	°C

Typical Bias ConditionsT_{amb} = +25°C

Symbol	Parameter	Values	Unit
V _{d1}	DC Drain voltage 1 st stage	6V	V
V _{d2}	DC Drain voltage 2 nd stage	6V	V
V _{d3}	DC Drain voltage 3 rd stage	6V	V
V _{d4}	DC Drain voltage 4 th stage	6V	V
V _{g1}	DC Gate voltage 1 st stage	-0.65	V
V _{g2}	DC Gate voltage 2 nd stage	-0.65	V
V _{g3}	DC Gate voltage 3 rd stage	-0.65	V
V _{g4}	DC Gate voltage 4 th stage	-0.65	V

Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.

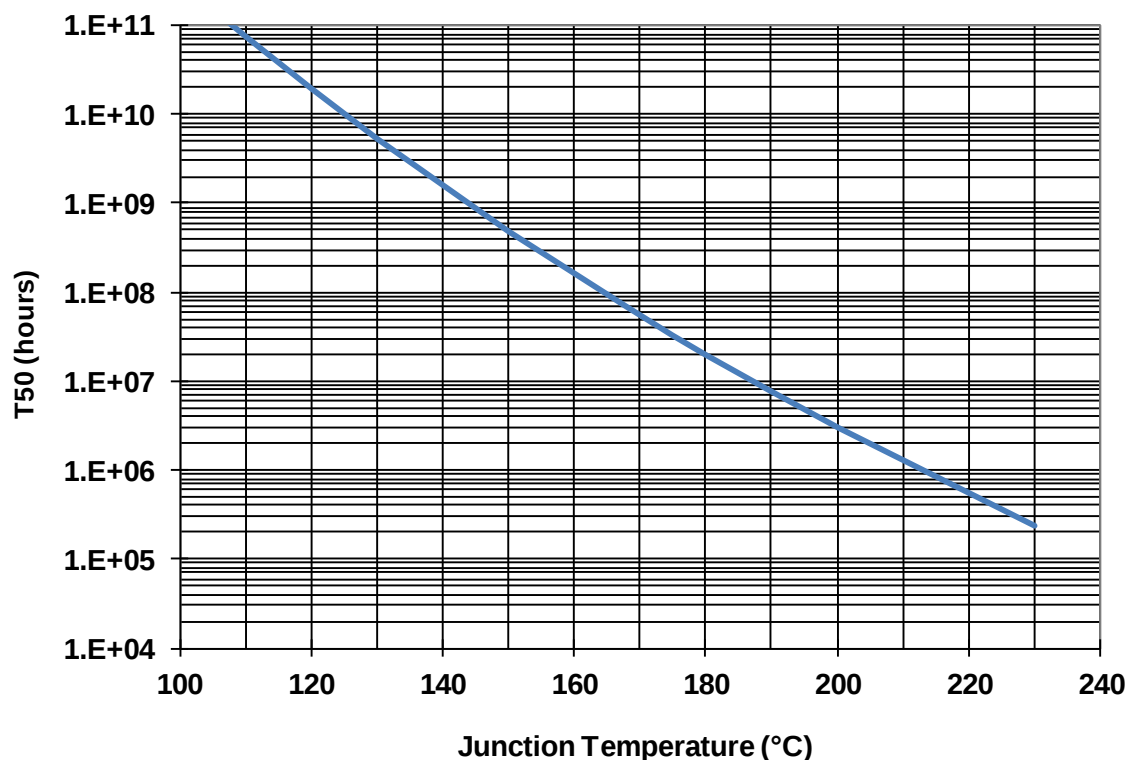
The temperature $T_{b\text{ chip}}$ is defined as the chip back side temperature.

The system maximum temperature must be adjusted in order to guarantee that T_{junction} remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the PCB system must be designed to comply with this requirement.

Parameter	Biasing conditions	T_{junction} (°C)	R_{TH} (°C/W)	T_{50} (hours)
$R_{\text{TH}}^{(1)}$ Thermal Resistance (Back of the chip)	$V_d = 6V$ $I_{dq} = 800mA$ $P_{diss} = 4.8W$	170	17.8	$5.3E+07$
$R_{\text{TH}}^{(1)}$ Thermal Resistance (Back of the chip)	$V_d = 5V$ $I_{dq} = 640mA$ $P_{diss} = 3.2W$	125	12.5	$9.0E+09$

⁽¹⁾ Assuming 85°C $T_{b\text{ chip}}$



Typical on-wafer Sij parameters (Pulsed mode)

Tamb.= +25°C, Vd = +6.0V, Id = 800mA, Pulse width = 25µs, Duty cycle = 10%

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
5	-0.6	138.1	-77.6	-84	-92.5	129.1	-0.2	164.4
6	-0.7	124.1	-80.1	99.6	-72.7	-61.7	-0.3	160.7
7	-1.1	103	-90.3	61.3	-59.4	-79.1	-0.3	156.6
8	-1.7	68.1	-80.7	-44	-45.7	-109.1	-0.4	151.8
9	-2.8	7.6	-87.2	-163.2	-34.5	-168.6	-0.6	145.5
10	-2.6	-67.9	-86.5	177.9	-25.6	129.5	-1	136.6
11	-1.9	-119.5	-73	-128.7	-17.3	62.6	-2	120.5
12	-1.6	-149.4	-65.2	-110.2	-9.1	-21.5	-7.7	76.4
13	-1.7	-167.8	-55.8	-160	-6.5	-134.5	-5.1	-137.1
14	-2	-179.7	-56.2	160.2	-9.8	143.6	-1.2	-176.8
15	-2.2	171.6	-56.4	110.6	-13.2	78.2	-0.6	167.3
16	-2.4	165.3	-57.7	92	-16.9	30.3	-0.5	157.7
17	-2.4	159.6	-56.6	49	-20.9	-5.6	-0.5	151
18	-2.3	153.7	-58.3	22.3	-23.5	-28.7	-0.4	145
19	-2.3	147.7	-62	-45.8	-24.7	-52.8	-0.5	139.4
20	-2.4	142	-67.5	166.1	-26.1	-72.9	-0.6	133.5
21	-2.4	135.7	-65.7	132.3	-27	-95.1	-0.6	127.5
22	-2.5	129	-58.7	83.6	-28.5	-104.7	-0.6	121.2
23	-2.7	122.9	-60.9	67.9	-27	-100.7	-0.7	114.7
24	-2.7	115.8	-60.6	34.6	-22.6	-109.5	-0.8	106.6
25	-2.7	108.4	-76.2	95.1	-18.1	-126.1	-0.9	97.7
26	-3	99.9	-58.4	19.3	-13.9	-154.3	-1	87.1
27	-3.2	90.6	-56.4	21.2	-9.9	-179	-1.3	73.6
28	-3.2	81	-57.1	-27.8	-4.4	152.8	-1.5	56.4
29	-3.4	69.6	-54.6	-28.9	1.1	116	-2.3	34.1
30	-3.6	57.2	-54.1	-29.3	7.2	73.3	-4	2.9
31	-3.8	43.5	-58.6	-47.7	13.2	21.4	-7	-42.1
32	-4.2	28.7	-52.4	-39.3	18.9	-43.1	-12	-108.4
33	-4.8	15.7	-51.4	-64	23	-114.3	-16.8	177.4
34	-5.3	4	-54.3	-93.7	25.4	169.1	-20.4	126.4
35	-5.3	-13.2	-51.2	-96.8	25.9	93.6	-21.4	135.1
36	-5.5	-28.1	-52	-118.8	25.9	29.1	-21.1	114.7
37	-6.4	-46.5	-59.7	178.5	26	-38.8	-20.5	120.2
38	-7.3	-57.2	-58.5	139.4	25.5	-97.5	-20.7	108.3
39	-8.4	-70	-71.3	-131.3	25.2	-157.6	-20.8	100.9
40	-9.9	-80.9	-57.4	9.4	25.4	141.4	-19.1	93.6
41	-11.7	-84.3	-61.6	130.4	25.3	78	-16.7	73.3
42	-14.5	-78.7	-58.6	-45.4	25.7	12.3	-13.4	48.5
43	-14.3	-62.6	-58.6	88.4	25.8	-61.7	-9.7	27.9
44	-14.3	-35.4	-56.5	73.4	25.8	-150.1	-5	-2.6
45	-6.5	-27.2	-60.1	-99.9	20.5	110.3	-3.5	-41.2

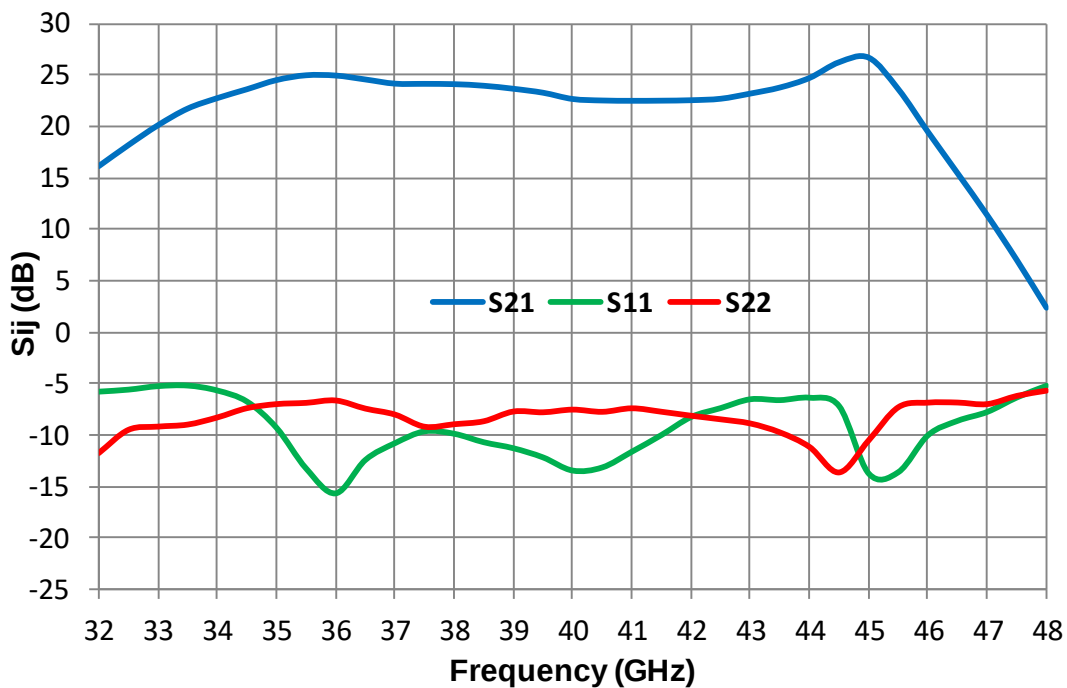
Typical Board Measurements (CW)

Tamb. = +25°C, Vd = +6V, Idq = 800mA & Vd = +5V, Idq = 640mA

Measurement performed in the access plans of the die.

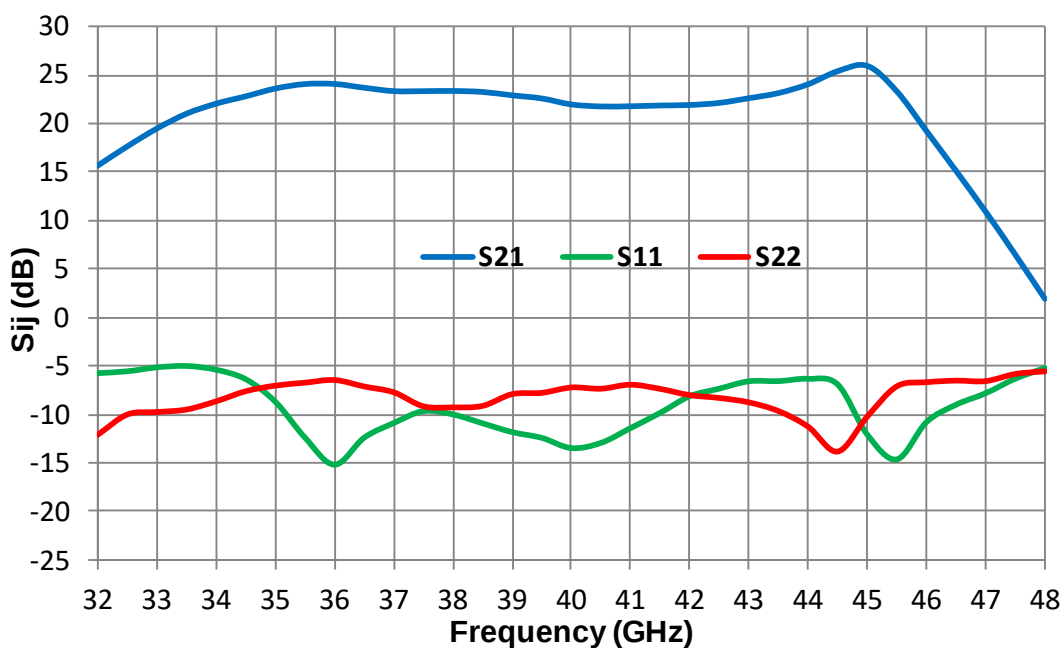
Gain & Return Losses versus Frequency

Vd = +6V, Idq = 800mA



Gain & Return Losses versus Frequency

Vd = +5V, Idq = 640mA

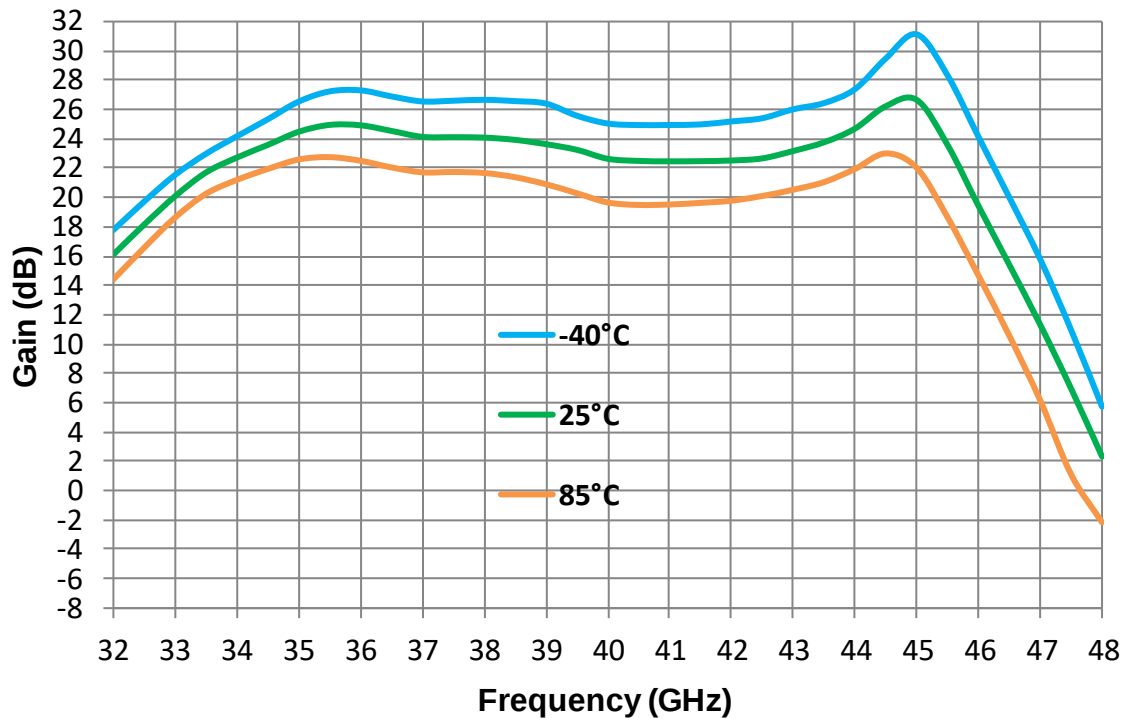


Typical Measurements on a probe compatible Board (CW)

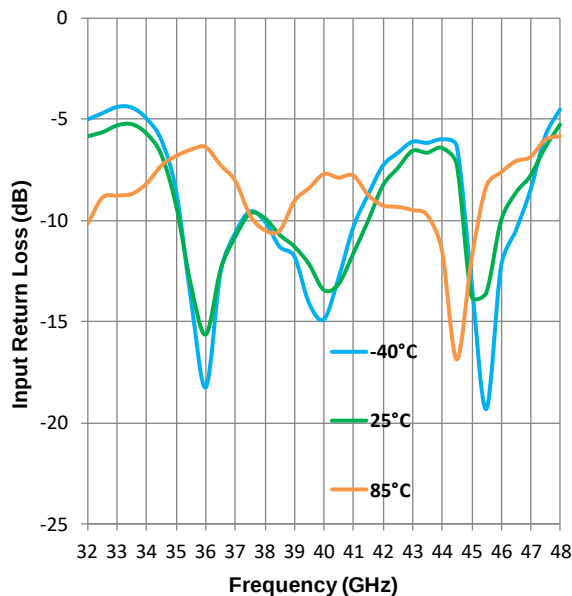
Tamb.= +25°C, Vd = +6.0V, Idq = 800mA

Measurement performed in the access plans of the die.

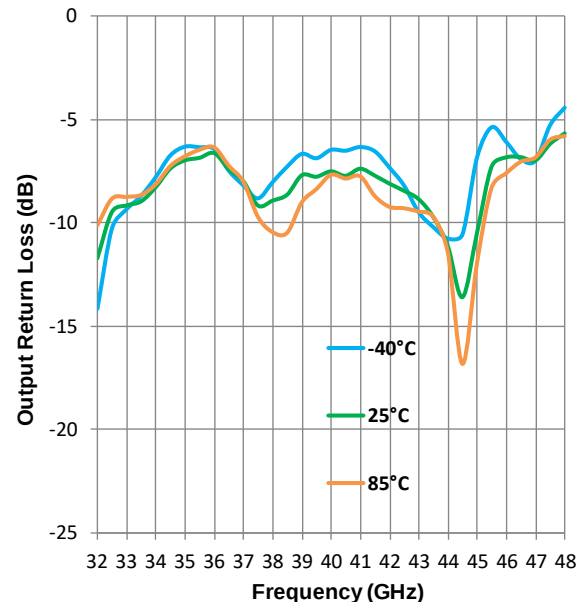
Gain versus Frequency in Temperature



Input Return Losses versus Frequency in Temperature



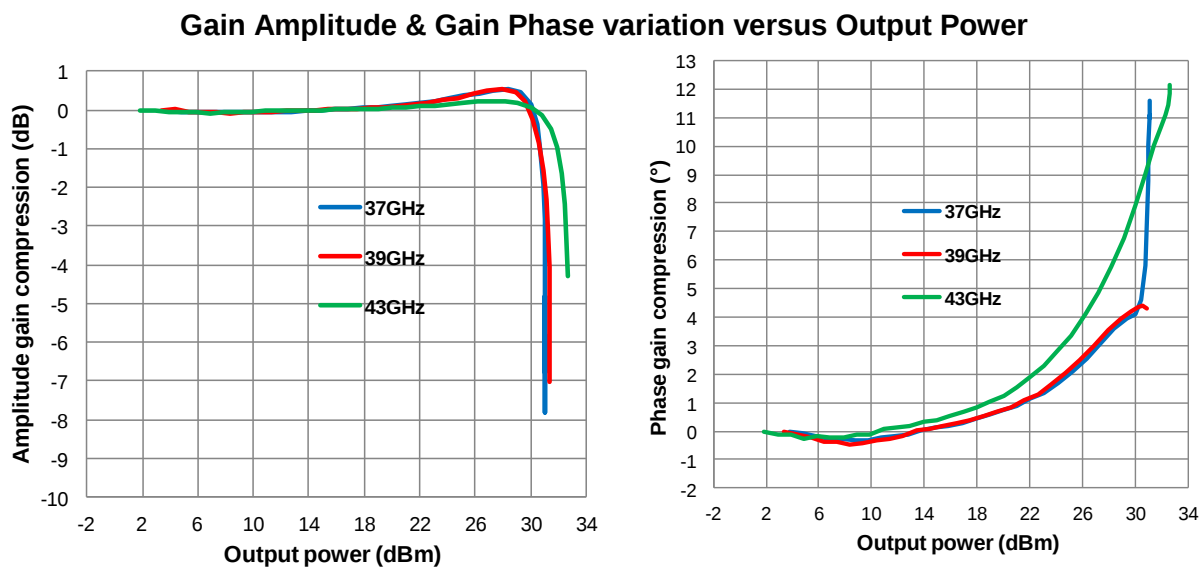
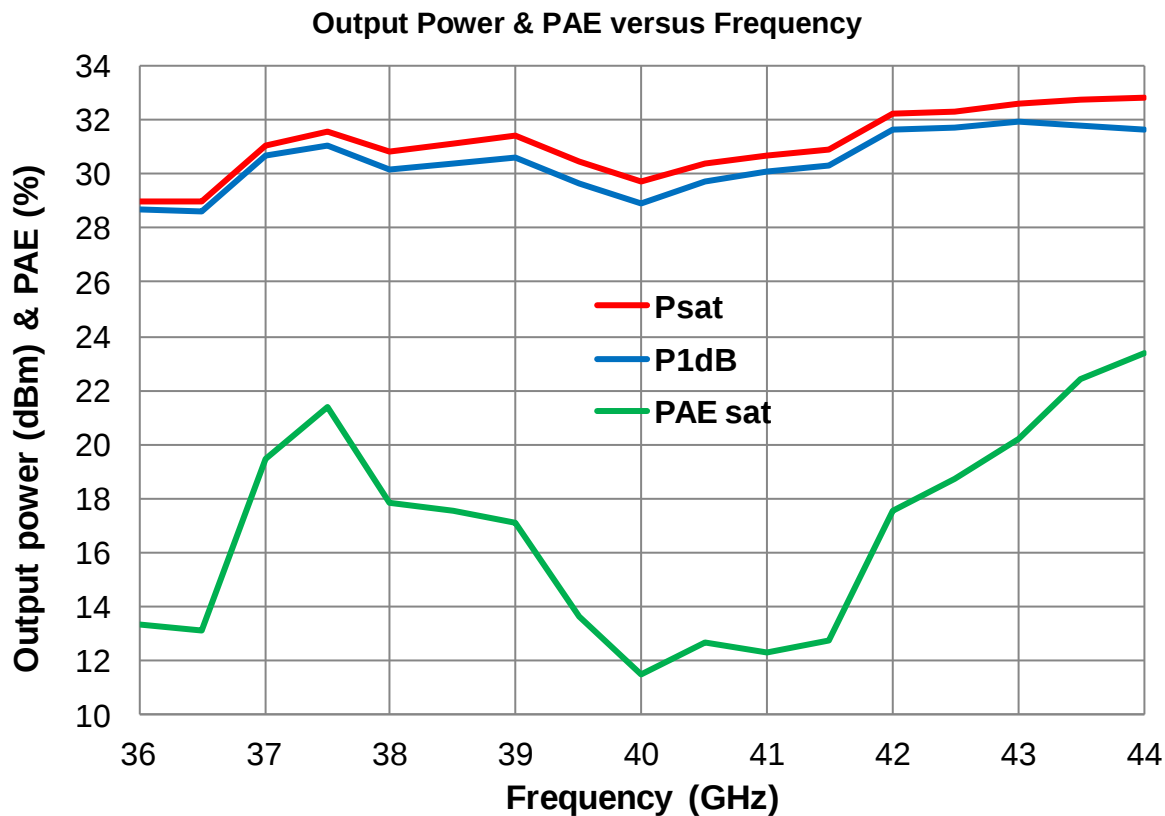
Output Return Losses versus Frequency in Temperature



Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 800mA

Measurement performed in the access plans of the die.

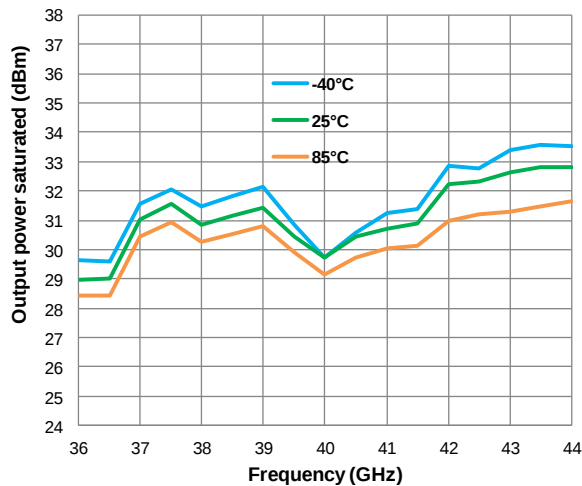


Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 800mA & Vd = +5V, Idq = 640mA

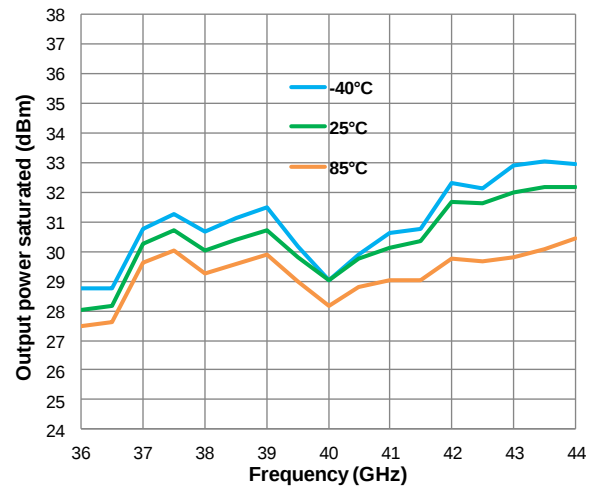
Saturated Power versus Frequency in Temperature

Vd = +6V, Idq = 800mA



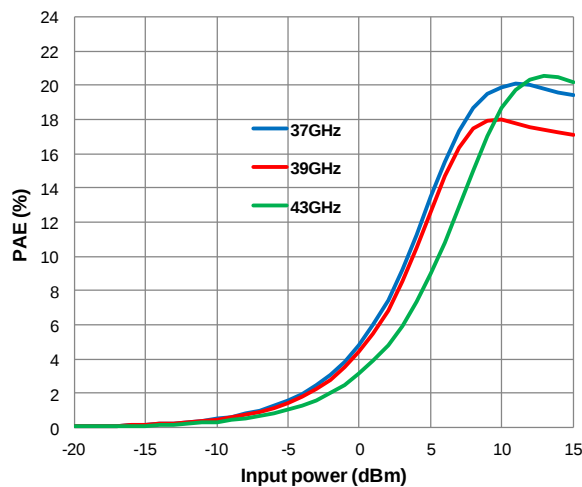
Saturated Power versus Frequency in Temperature

Vd = +5V, Idq = 640mA



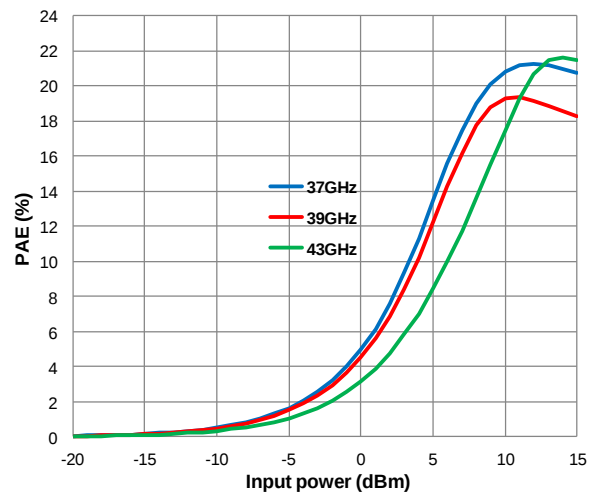
PAE versus Input Power

Vd = +6V, Idq = 800mA



PAE versus Input Power

Vd = +5V, Idq = 640mA



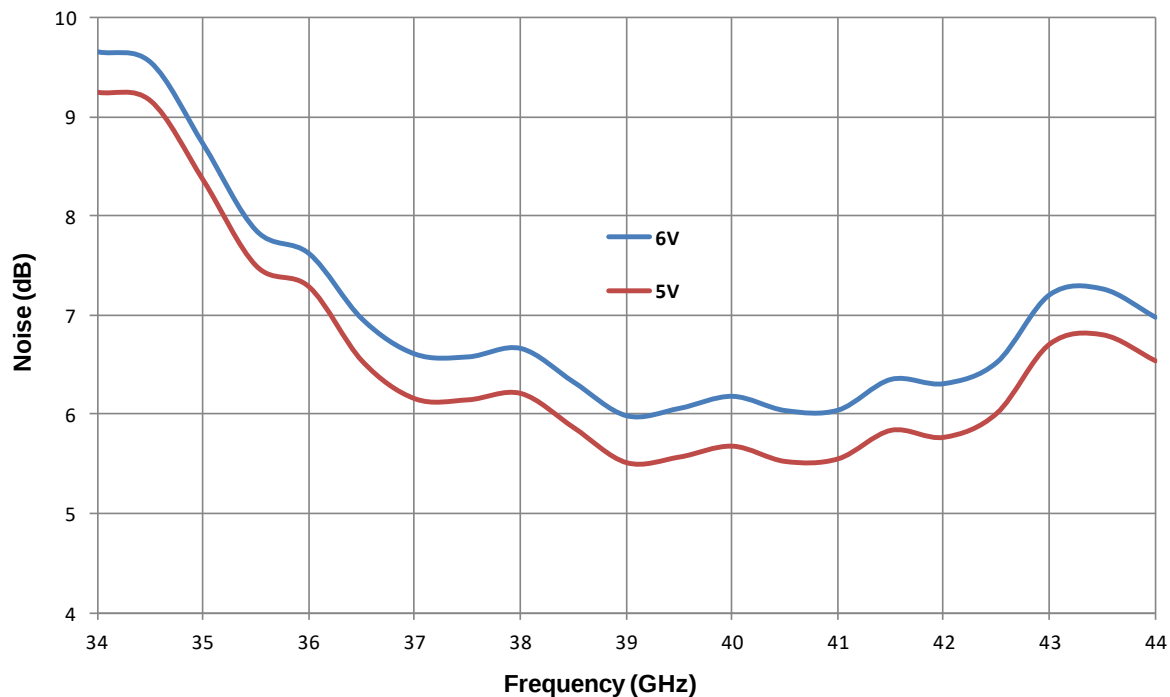
Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 800mA & Vd = +5V, Idq = 640mA

Noise Figure versus Frequency

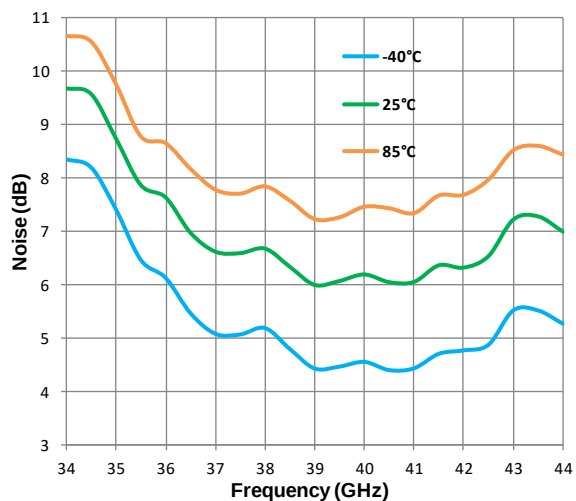
Vd = +6V, Idq = 800mA

Vd = +5V, Idq = 640mA



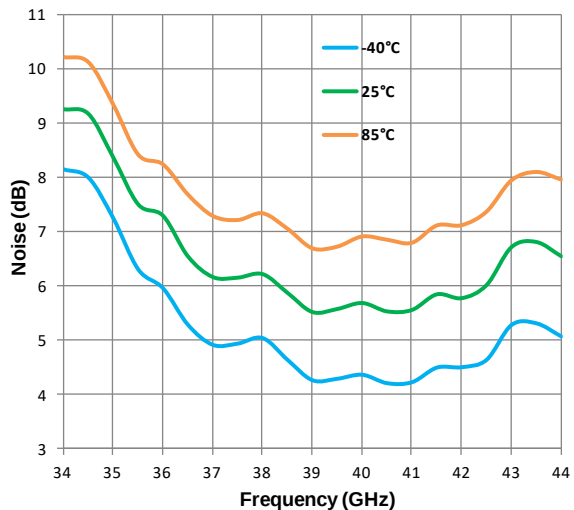
Noise Figure versus Frequency in Temperature

Vd = +6V, Idq = 800mA



Noise Figure versus Frequency in Temperature

Vd = +5V, Idq = 640mA

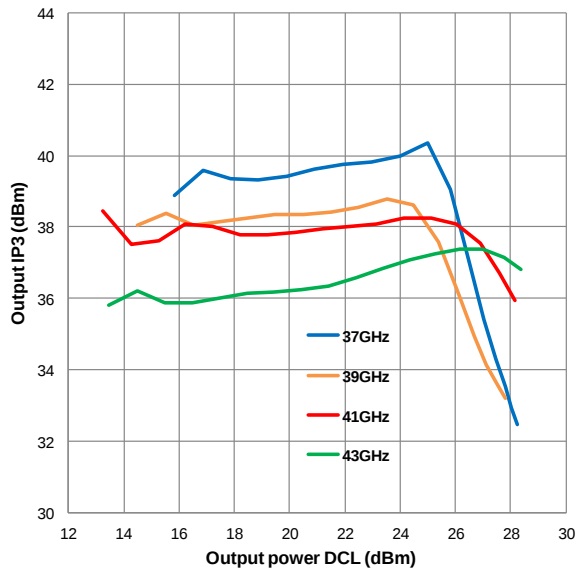


Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 800mA & Vd = +5V, Idq = 640mA

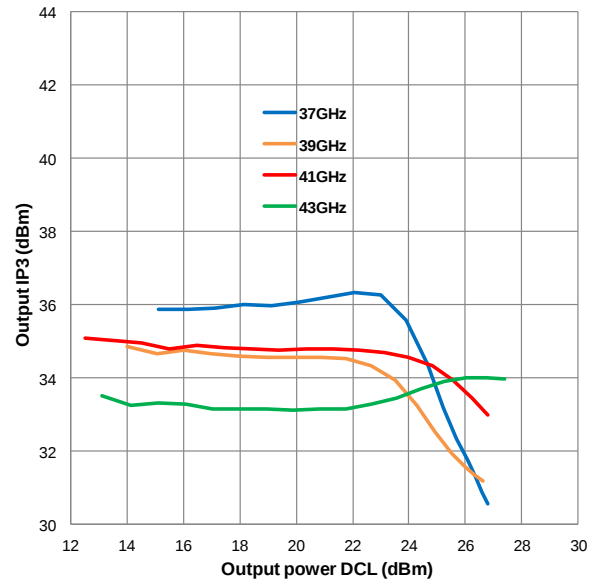
Output IP3 versus Output Power

Vd = +6V, Idq = 800mA



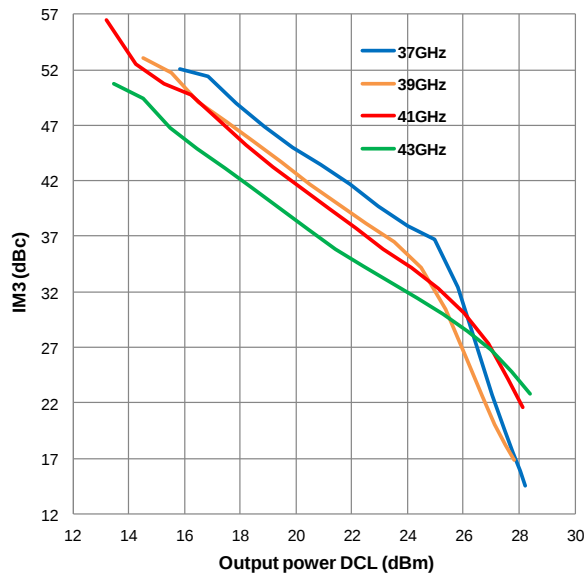
Output IP3 versus Output Power

Vd = +5V, Idq = 640mA



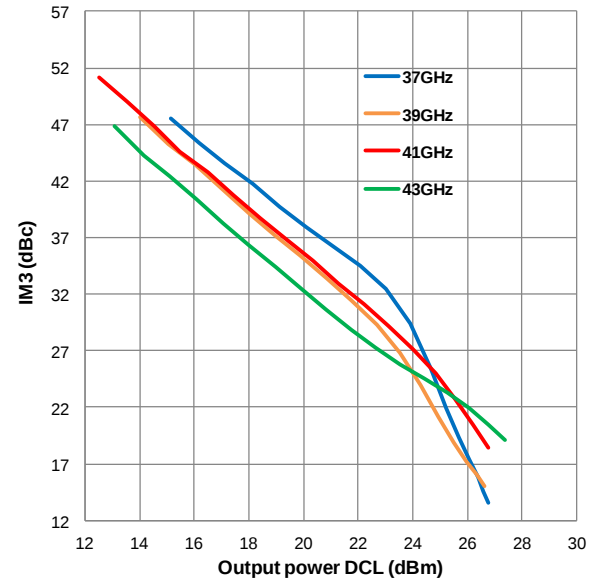
Output IM3 versus Output Power

Vd = +6V, Idq = 800mA



Output IM3 versus Output Power

Vd = +5V, Idq = 640mA

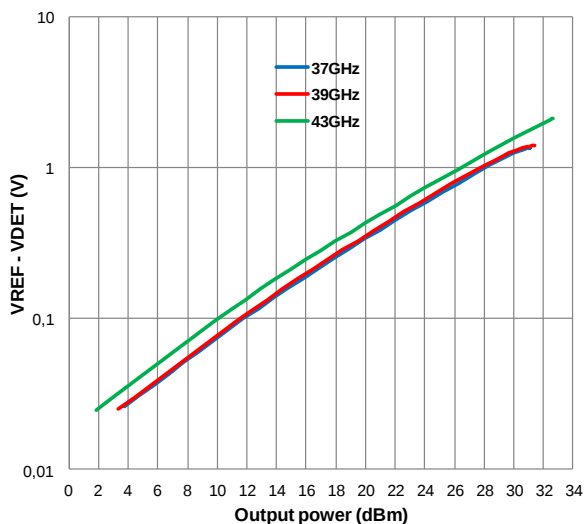


Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 800mA & Vd = +5V, Idq = 640mA

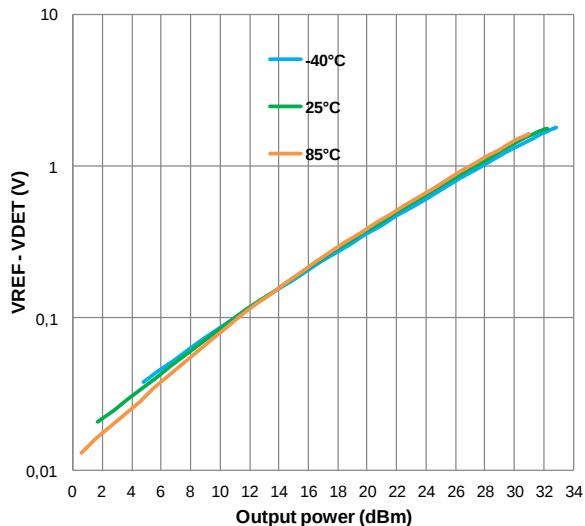
Power Detector versus Output Power

Vd = +6V, Idq = 800mA



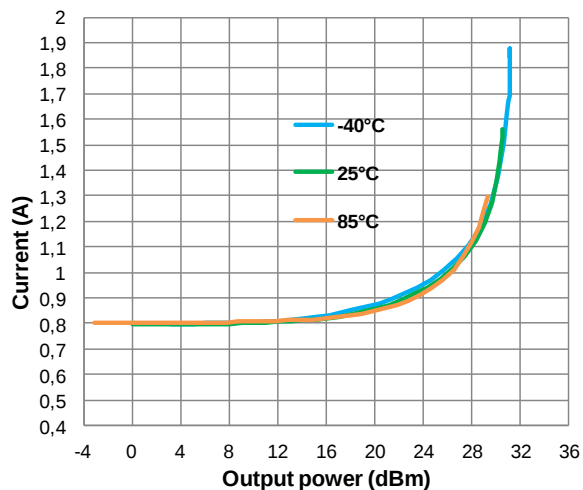
Power Detector versus Output Power & Temperature at 42GHz

Vd = +6V, Idq = 800mA



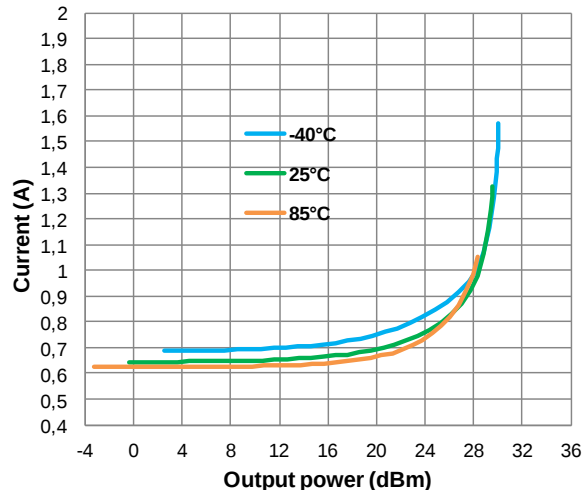
Total Drain Current versus Output Power at 42GHz

Vd = +6V, Idq = 800mA

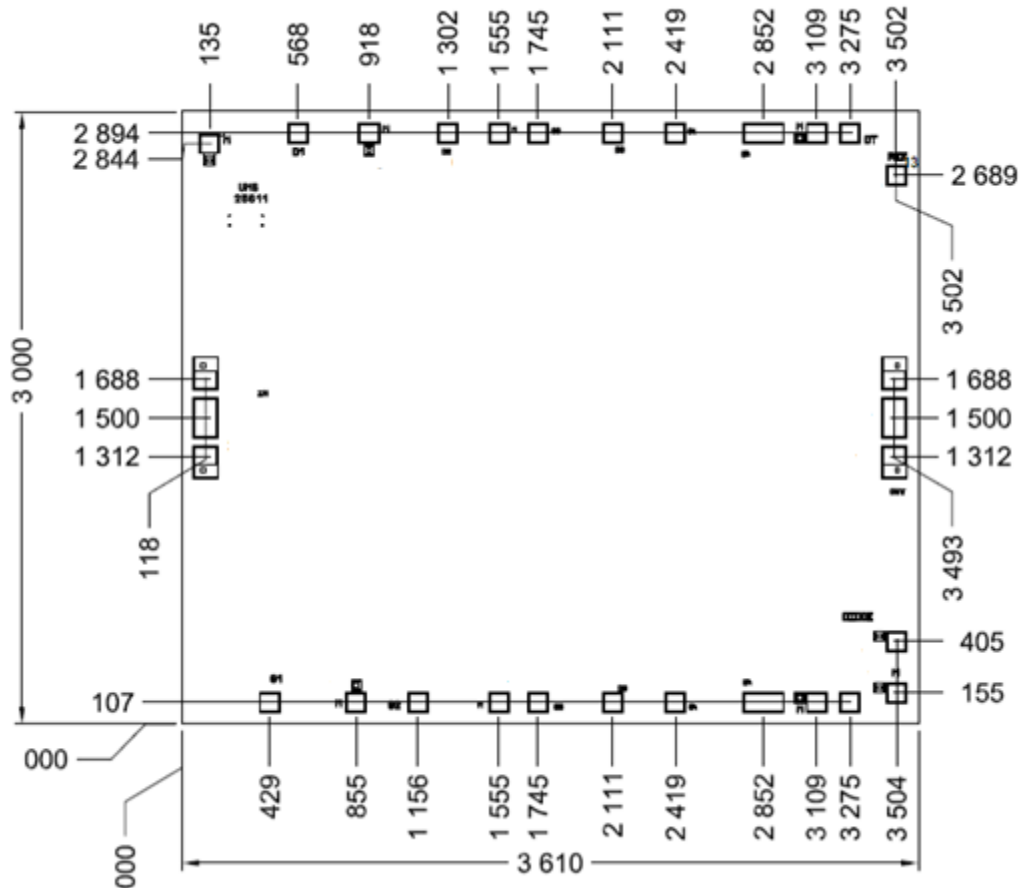


Total Drain Current versus Output Power at 42GHz

Vd = +5V, Idq = 640mA



Mechanical data



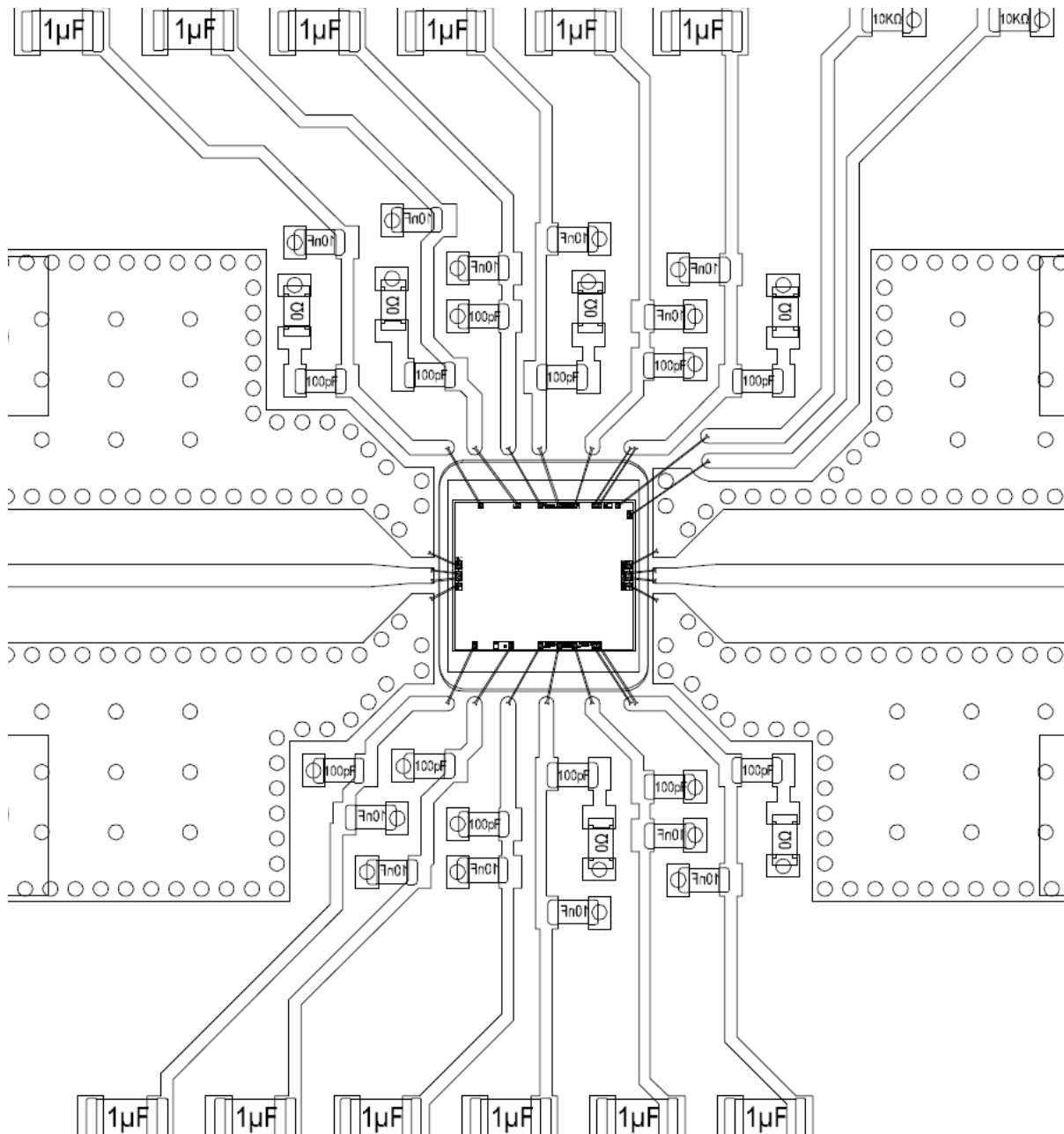
Chip thickness: 70 μ m.

All dimensions are in micrometers

DC pad size: 83 μ m x 83 μ m (BCB opening)

RF pad size: 105 μ m x 186 μ m (BCB opening)

Recommended assembly plan

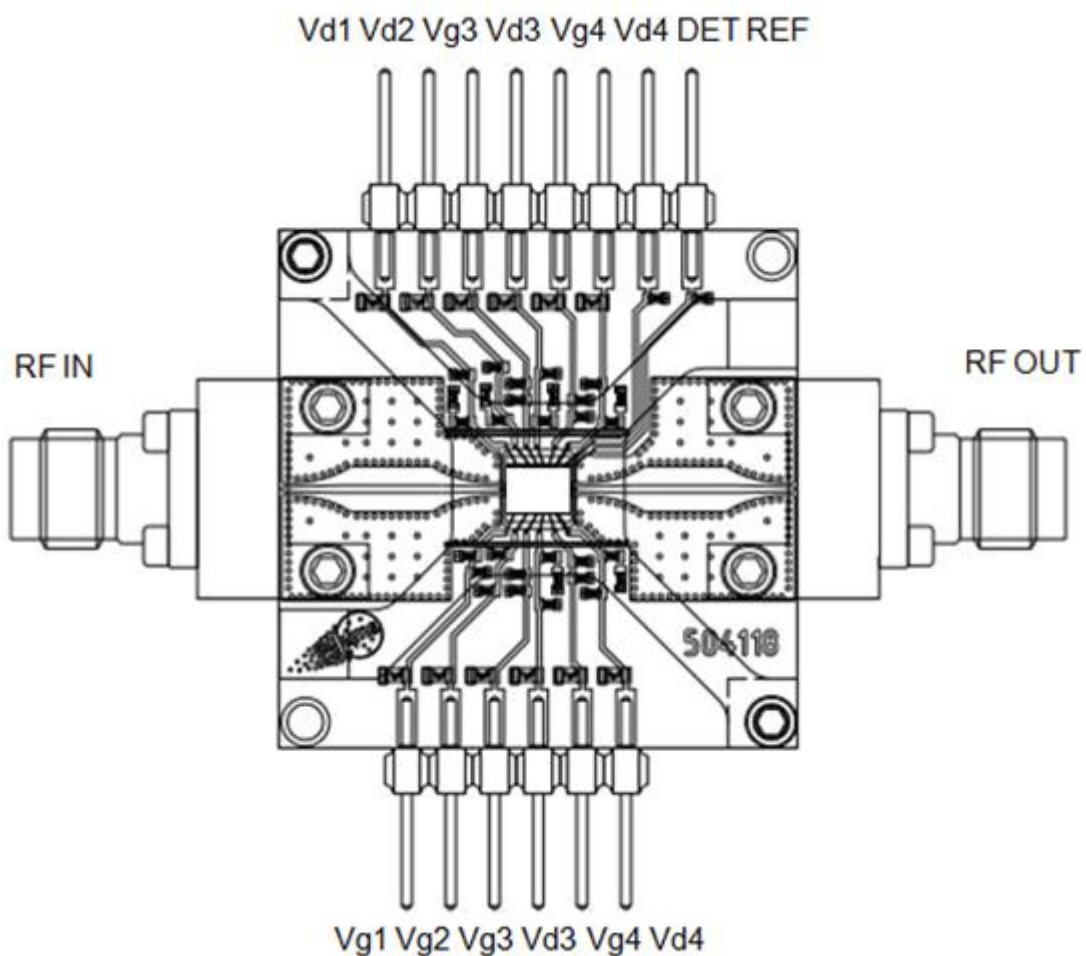


Decoupling capacitors: 100pF, 10nF & 1μF (on gate & drain access)

Note: Supply feed should be bypassed. 25μm diameter gold wire is to be preferred.

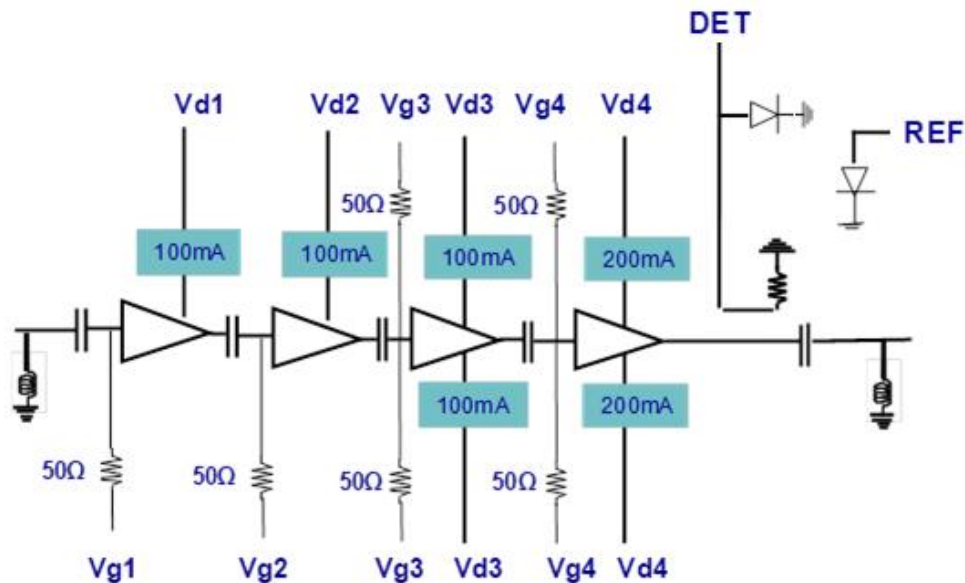
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically RF35P / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the chip.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF $\pm 5\%$, 10nF $\pm 10\%$ and 1 μ F $\pm 10\%$ are recommended for the gate and drain accesses.
- A 10K Ω resistor is recommended on VREF & VDET accesses for the detector
- Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



DC Schematic

HPA : 6V, 800mA



Biasing procedure

Device Power Up instructions:

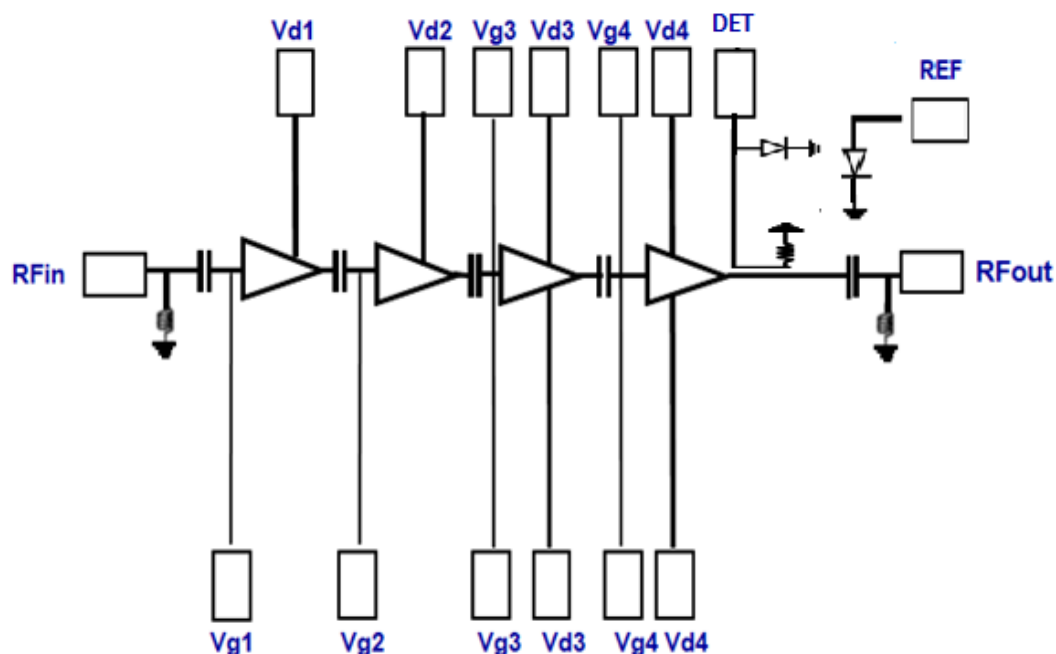
1. Ground the device
2. Bias HPA gate voltage at V_{gs} close to $V_{pinch-off}$ (example: $V_g \approx -2V$)
3. Apply V_{ds} quiescent bias voltage (Example: $V_d = 6V$)
4. Increase slowly V_{gs} up to quiescent bias drain current I_{dq} (pulsed applied on the gate)
5. Apply RF input power

Device Power Up instructions:

1. Remove RF input power
2. Decrease HPA gate voltage up to $V_{gs} -2V$
3. Decrease drain voltage up to 0V

Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage potentially present on the RF accesses.



Limited DC decoupling is implemented on chip. Additional external DC decoupling (100pF, 10nF, 1μF) on the PC Board, as close as possible to the bare die, is required.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

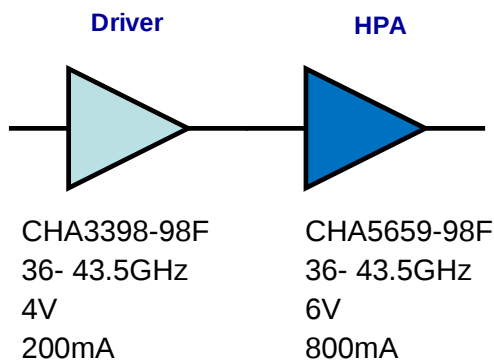
The circuit includes ESD protections on all RF and DC accesses.

Recommended UMS Power chain

The CHA3398-98F is recommended with the CHA5659-98F as driver.

Total Gain: 42dB

Gain control: 30dB with the both amplifiers.



Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Ordering Information

Chip form:

CHA5659-98F/00

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