

L-Band Low Noise Amplifier GaAs Monolithic Microwave IC

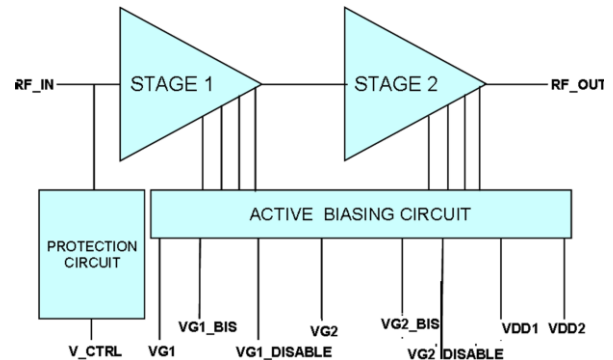
Description

The CHA3801-99F is an L-Band LNA monolithic circuit including an active bias network. Furthermore a protection network is included in order to allow high input power survivability.

The circuit is dedicated to space applications, and also well suited for a range of microwave applications and systems.

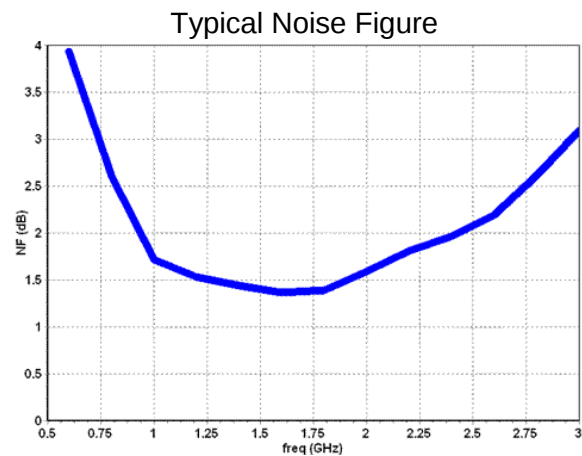
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- L-Band performances: 1-2GHz
- 1.45dB Noise Figure
- 28dB Linear Gain
- 17dBm Saturated Power
- 27dBm Output Third Order Intercept
- DC bias: Vd = 5Volt @ 70mA
- Chip size 1.6x1.4x0.1mm



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1		2	GHz
Gain	Linear Gain		28		dB
NF	Noise Figure		1.45		dB
Pout	Output Power @1dB comp.		15		dBm

Main Characteristics

T_{amb.} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F _{RF}	RF input frequency Range	1		2	GHz
G ⁽¹⁾	Gain		28		dB
-	Gain flatness ⁽¹⁾		0.5		dBp-p
S ₁₁	Input Return Loss		-15		dB
S ₂₂	Output Return Loss		-15		dB
NF **	Noise Figure		1.45		dB
S ₁₂	Reverse Isolation		40		dB
OIP3 **	Output Third order Intercept Point		27		dBm
OP1dB **	Output 1dB Compression Point		15		dBm
I _{d_1a}	Total drain current (mode 1a)		70		mA
I _{d_1b}	Total drain current (mode 1b)		90		mA
I _{d_1c}	Total drain current (mode 1c)		50		mA
V _d	Drain Voltage		5		V

⁽¹⁾ Under working mode 1a and input protection disabled

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

A bonding wire of typically 0.1 to 0.15nH will improve the matching at the accesses.

Working Modes

Mode	Description	PAD #3 PAD #6	PAD #4 PAD #7	PAD #5 PAD #8	PAD #9 PAD #10
1a	Nominal bias current (70mA)	-5V	n.c.*	n.c. *	+5V
1b	High bias current (+30%)	n.c.*	-5V	n.c. *	+5V
1c	Low bias current (-30%)	-5V	-5V	n.c. *	+5V

* not connected

Input protection state	PAD #2
enabled	GND
disabled	-5V

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage (Vg=-5V)	6.5	V
Vctrl	Control voltage	-6 to 0	V
Vg	Gate bias voltage (Vd=+5V)	-6 to 0	V
Pin	Protection switch enabled	+20	dBm
Pin	Protection switch disabled	+6	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Typical on-wafer Sij parameters

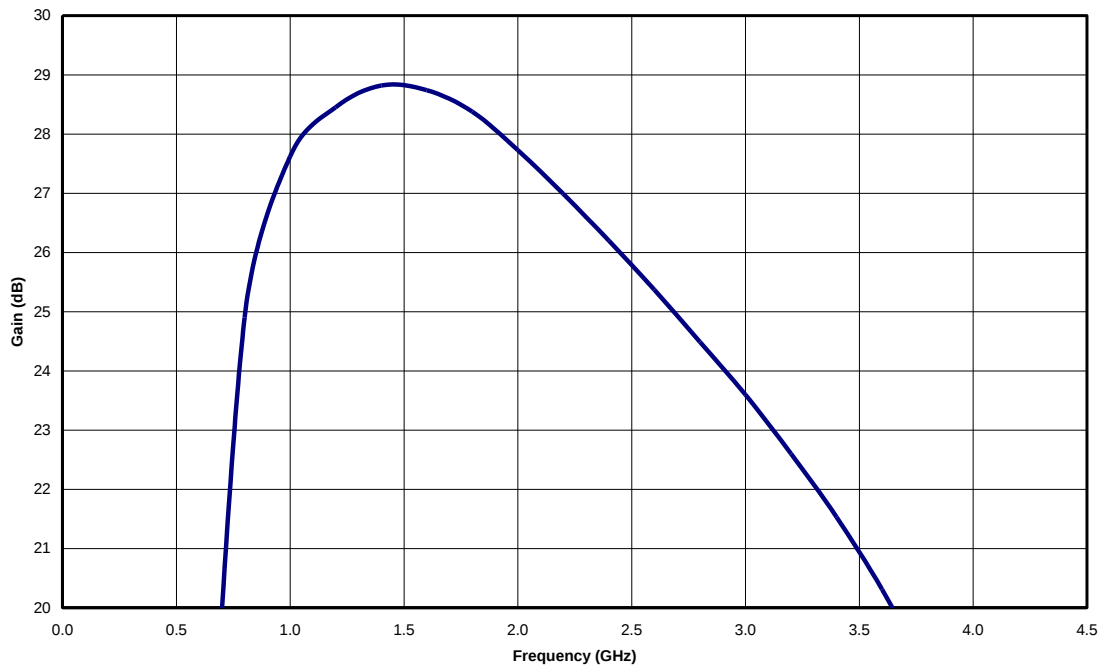
Tamb.= +25°C, Vd = +5V, Nominal bias current

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.2	-0.7363	-34.13	-54.05	63.29	-25.41	-139.5	-0.9557	-42.84
0.4	-1.232	-76.43	-56.62	112.00	-6.87	-20.58	-1.602	-89.75
0.6	-5.797	-147.5	-56.18	129.5	13.98	-134.00	-3.895	-147.6
0.8	-12.17	118.7	-69.11	0.9509	24.9	141.8	-15.53	147.8
1.0	-14.1	36.92	-56.16	-118.8	27.62	76.17	-22.07	-92.14
1.2	-15.93	4.04	-54.31	-127.1	28.45	31.2	-19.33	-107.1
1.4	-20.02	2.275	-50.91	-156.5	28.82	-6.376	-19.3	-101.00
1.6	-20.28	36.82	-48.07	176.2	28.74	-38.87	-17.64	-92.55
1.8	-16.18	50.27	-46.14	151.00	28.38	-67.66	-15.35	-96.02
2.0	-13.16	44.78	-45.74	125.2	27.73	-93.68	-14.35	-102.6
2.2	-11.58	37.8	-44.24	109.00	26.99	-116.9	-13.69	-109.2
2.4	-10.59	32.05	-44.33	92.94	26.2	-138.4	-13.4	-113.6
2.6	-9.907	28.51	-42.73	76.43	25.37	-158.6	-13.18	-116.00
2.8	-9.157	27.16	-41.75	62.9	24.49	-177.8	-12.83	-115.4
3.0	-8.175	26.17	-41.91	44.11	23.6	163.5	-12.06	-114.8
3.2	-6.95	24.36	-41.19	34.49	22.6	145.4	-10.98	-115.9
3.4	-5.646	20.49	-41.34	8.98	21.53	127.7	-9.788	-119.3
3.6	-4.456	14.89	-41.52	3.437	20.31	110.00	-8.732	-126.00
3.8	-3.43	8.087	-41.12	-12.47	18.89	93.67	-8.145	-133.9
4.0	-2.633	0.6992	-41.32	-25.8	17.4	78.74	-7.838	-140.5
4.2	-2.014	-6.844	-42.61	-40.22	15.87	64.99	-7.539	-146.9
4.4	-1.576	-14.11	-41.5	-48.33	14.31	52.42	-7.448	-153.1
4.6	-1.261	-20.93	-43.41	-58.21	12.78	41.09	-7.41	-158.1
4.8	-1.045	-27.5	-43.6	-60.29	11.31	30.13	-7.227	-164.2
5.0	-0.9556	-33.86	-42.22	-78.08	9.888	19.45	-7.018	-170.2
5.2	-1.182	-38.42	-42.29	-91.97	8.052	10.52	-7.657	-177.3
5.4	-0.7425	-41.62	-45.25	-106.5	6.816	3.948	-8.043	178.9
5.6	-0.578	-47.13	-46.64	-105.4	5.591	-3.491	-8.368	176.7
5.8	-0.4952	-51.86	-46.99	-112.9	4.417	-10.59	-8.558	174.4
6.0	-0.4492	-56.3	-47.28	-112.1	3.284	-17.47	-8.719	171.6
6.2	-0.4078	-60.46	-47.00	-114.6	2.226	-23.99	-8.905	169.00
6.4	-0.3896	-64.32	-48.25	-129.3	1.239	-30.16	-9.084	166.8
6.6	-0.3677	-68.06	-48.41	-134.2	0.3255	-36.53	-9.113	164.3
6.8	-0.3468	-71.64	-47.15	-127.4	-0.5797	-43.18	-9.131	159.2
7.0	-0.3351	-75.01	-46.72	-140.9	-1.536	-48.5	-9.809	155.2
7.2	-0.3236	-78.25	-47.18	-142.8	-2.243	-53.62	-10.31	154.2
7.4	-0.324	-81.39	-47.23	-147.9	-2.863	-59.15	-10.59	152.8
7.6	-0.3218	-84.5	-48.12	-146.2	-3.418	-64.74	-10.72	151.2
7.8	-0.3208	-87.49	-49.56	-145.00	-3.961	-70.13	-11.23	147.8
8.0	-0.3328	-90.33	-48.2	-148.4	-4.277	-75.94	-11.63	147.1
8.2	-0.3474	-93.23	-46.71	-143.7	-4.54	-82.03	-11.96	145.3
8.4	-0.3661	-96.02	-47.63	-168.6	-4.699	-88.35	-12.45	144.2
8.6	-0.3976	-98.76	-46.31	-164.6	-4.662	-95.49	-12.89	144.1
8.8	-0.3993	-101.7	-42.67	-172.8	-4.439	-103.6	-13.35	144.5
9.0	-0.5436	-104.5	-43.18	-178.3	-4.083	-114.00	-13.73	144.8

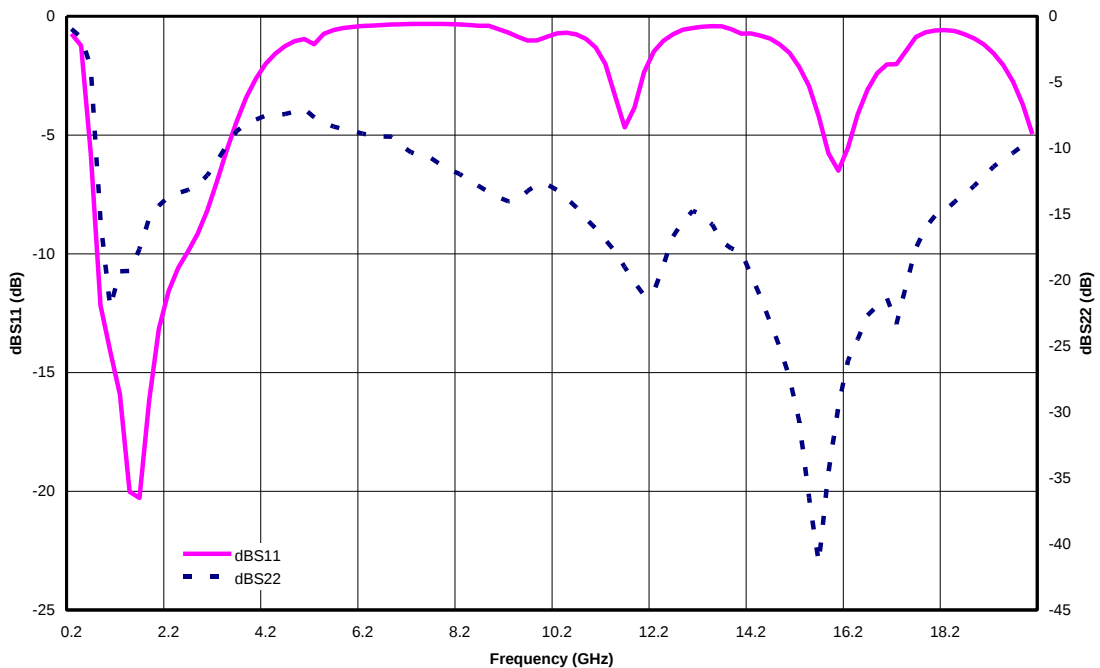
Typical on wafer Measurements

Tamb.= +25°C, Vd = +5V, working mode 1a with input protection disabled

Linear Gain versus Frequency



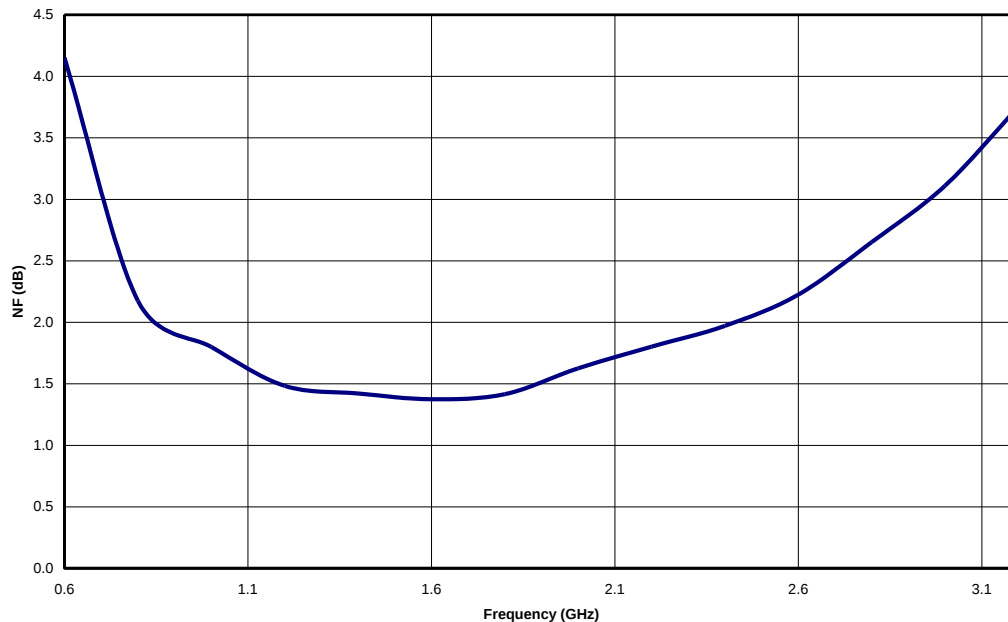
Input and Output Return Loss versus Frequency



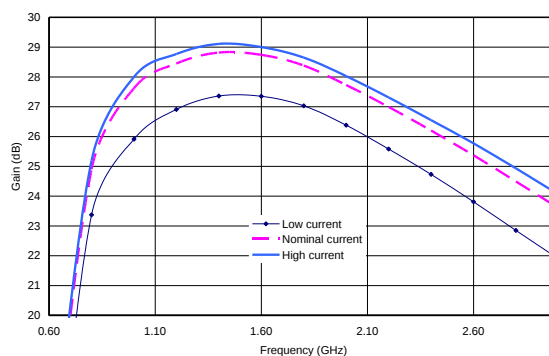
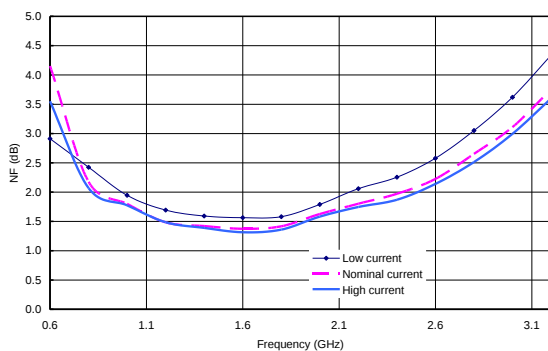
Typical on wafer Measurements

Tamb.= +25°C, Vd = +5V, working mode 1a with input protection disabled

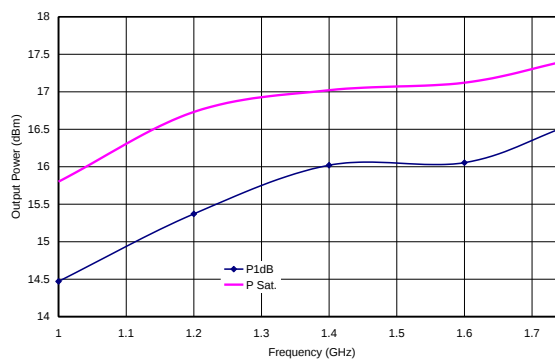
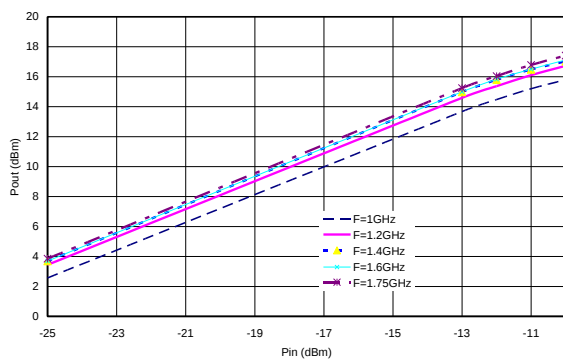
Noise Figure versus Frequency



Noise Figure and Gain vs Bias configuration



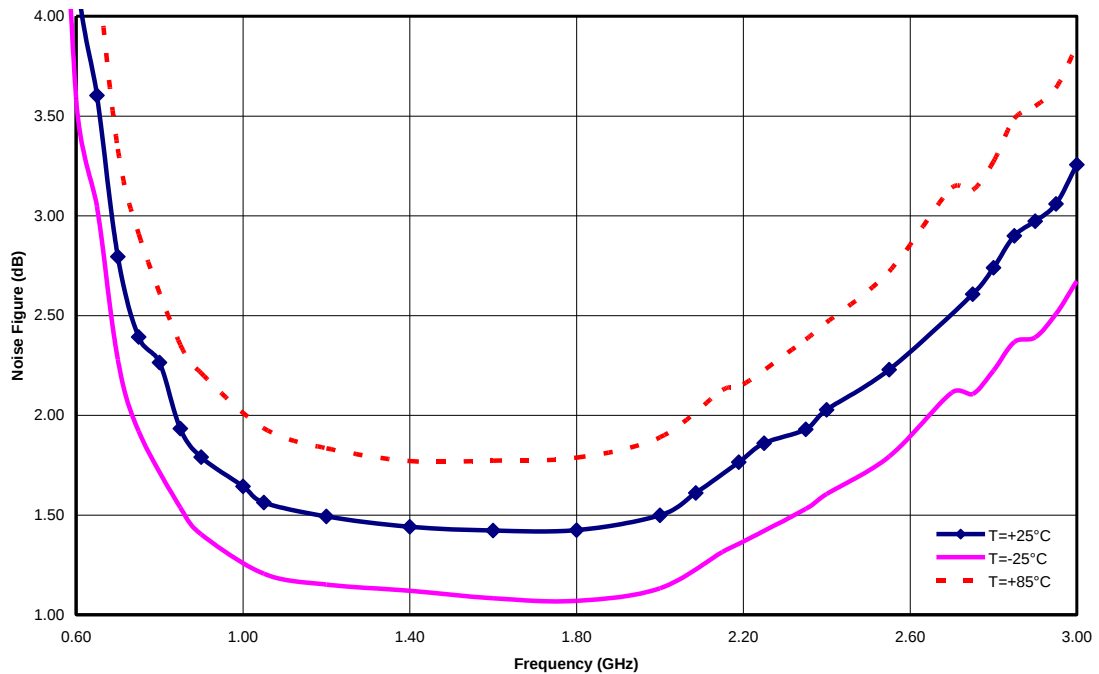
Output Power (F= 1 to 1.75GHz)



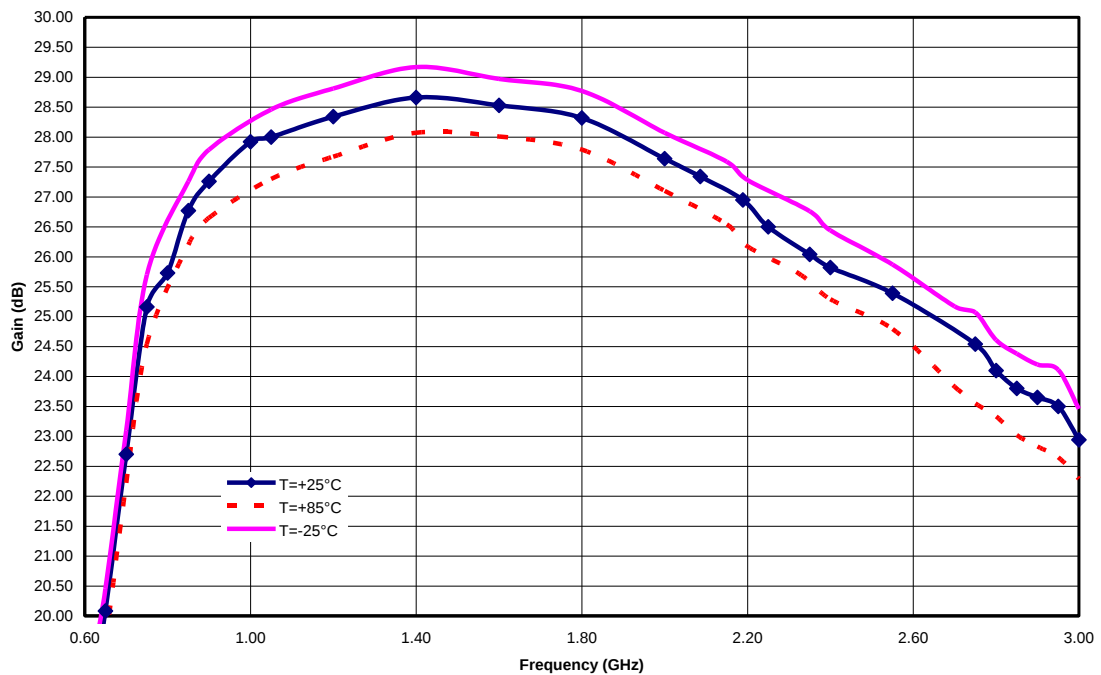
Typical Test Fixture Measurements

Tamb.= +25°C, Vd = +5V, Nominal bias current

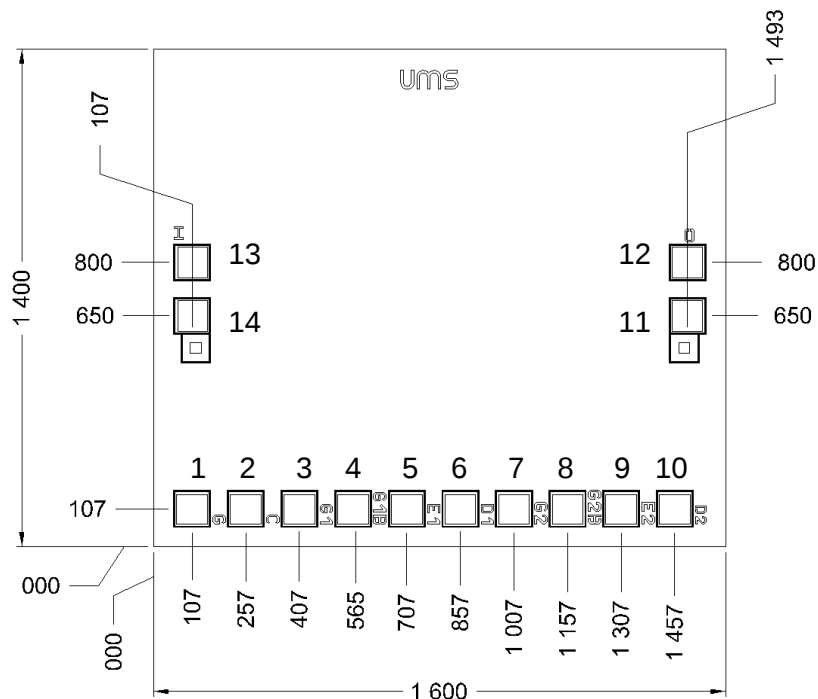
Noise Figure vs Frequency and Temperature



Gain vs Frequency and Temperature



Mechanical data



All dimensions are in micrometers

Chip thickness: 100µm.

Chip size: 1600*1400 ±35µm

RF pads = 100x100µm²

DC pads = 100x100µm²

PAD number	Description
1	Ground (no connection required)
2	Control voltage to be changed depending on input protection state, i.e. enabled or disabled
3	Gate supply voltage (stage 1)
4	Gate supply voltage bis (stage 1)
5	Active bias enable/disable voltage (stage 1)
6	Gate supply voltage (stage 2)
7	Gate supply voltage bis (stage 2)
8	Active bias enable/disable voltage (stage 2)
9	Drain voltage (stage 1)
10	Drain voltage (stage 2)
12	RF Output
13	RF Input
11	Ground pad for RF output
14	Ground pad for RF input

Note: pad information printed on chip is misleading for chip version 16051 available for sampling. Please refer only to the pad numbering shown above.

Notes

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Ordering Information

Chip form:

CHA3801-99F/00

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