CHA2441-QAG

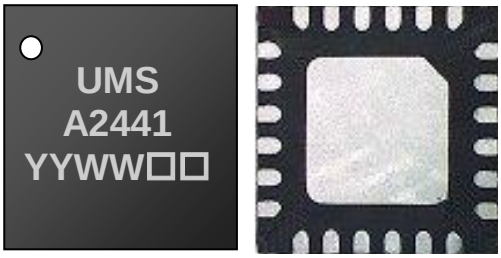
22-26GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

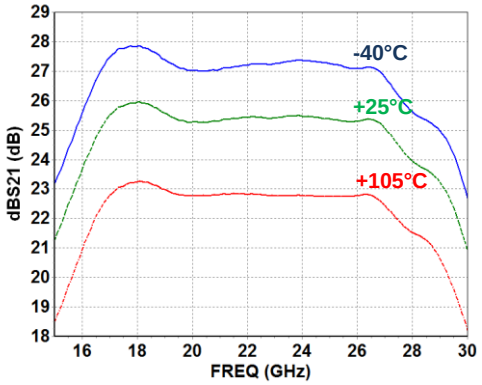
The CHA2441-QAG is a K-band low noise amplifier providing 25.5dB gain from a single bias supply +3.3V with a noise figure of 2.5dB. All the active devices are self biased on chip.

The circuit is manufactured with a pHEMT process 0.25µm.
It is supplied in RoHS compliant SMD package.



Main Features

- 22-26GHz Bandwith
- excellent 2.5dB Noise Figure
- 25.5dB Gain
- DC bias: Vd=3.3Volt@Id=50mA
- 16L-QFN3x3
- MSL1



S21 versus frequency and temperature

Main Electrical Characteristics

Tamb.= +25°C; Vd=+3.3V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	22		26	GHz
Gain	Linear Gain		25.5		dB
NF	Noise Figure		2.5		dB
Pin_{-1dB}	Input Power @1dB comp.		-14		dBm

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Electrical Characteristics

Full operating temperature range; **Vd=+3.3V**

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency Range	22		26	GHz
Gain	Small signal gain		25.5		dB
ΔG(T)	Small signal gain variation over temperature		+2/- 2.5		dB
NF	SSB Noise Figure		2.5		dB
S11/S22	Input/Output Return Loss		12		dB
Pin_{-1dB}	Input power at 1 dB gain compression		-14		dBm
IIP3	Input IP3		-4		dBm
Psat	Saturated output power @ 24.5 GHz			15	dBm
Id	Supply Current		50		mA
Top	Operating temperature range	-40	25	105	°C

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
+Vd	Maximum positive supply voltage	4.0	V
+I	Maximum positive supply current	70	mA
RFin	Maximum peak input power overdrive	-5.0	dBm
Top	Operating temperature range	-40 to 105	°C
Tstg	Storage temperature range	-55 to 150	°C
Tjmax	Maximum Junction Temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

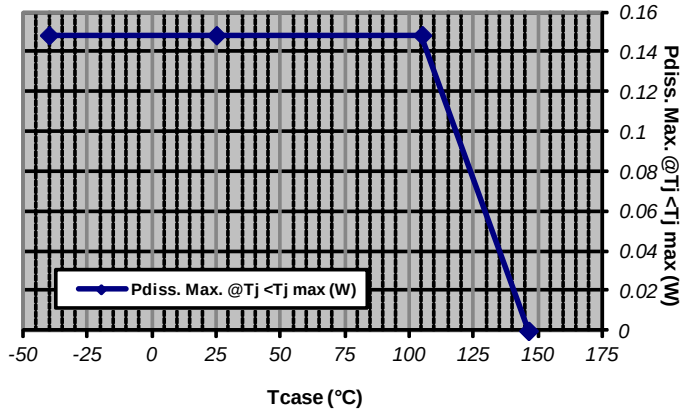
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

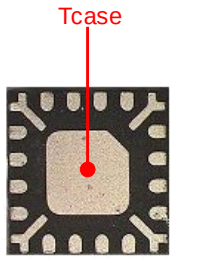
DEVICE THERMAL SPECIFICATION : CHA2441-QAG			
Recommended max. junction temperature (Tj max)	:	146	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	0.1	W
=> Pdiss. Max. derating above Tcase(1)= 105 °C	:	4	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<278	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	105	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the ***hottest junction*** *of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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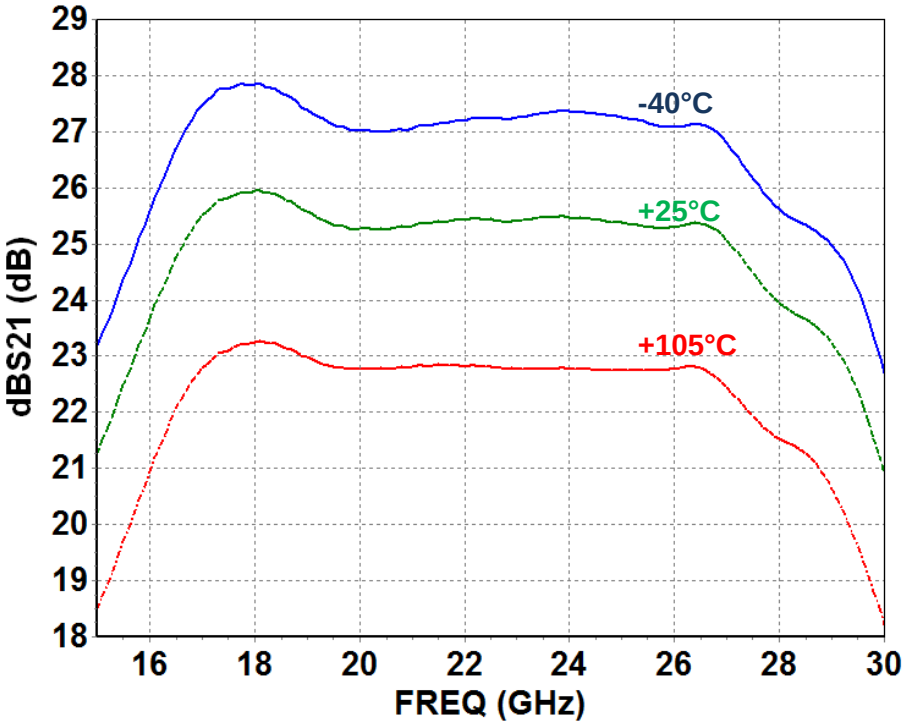
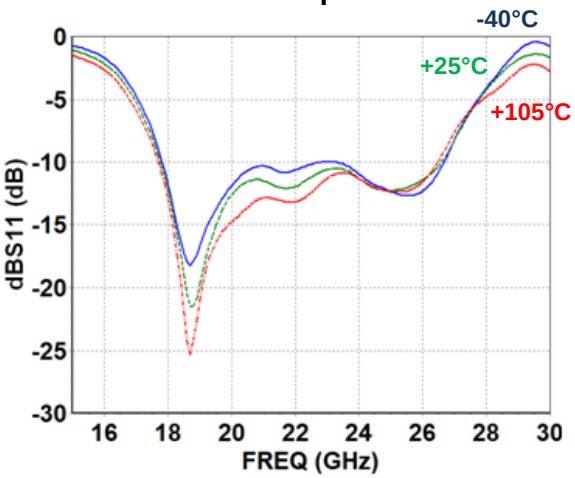
Typical Board Measurements

Vd = +3.3V

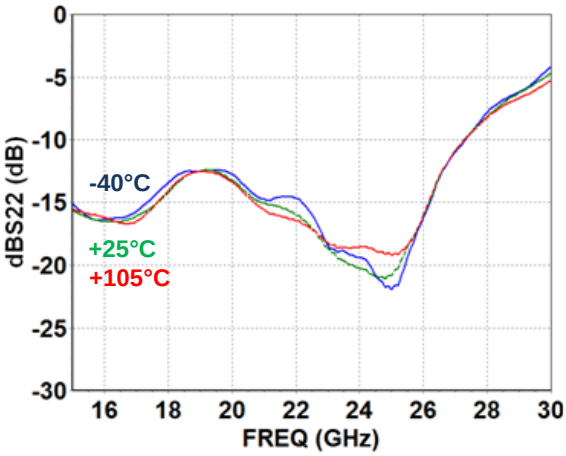
Linear Gain versus temperature



S11 versus temperature



S22 versus temperature



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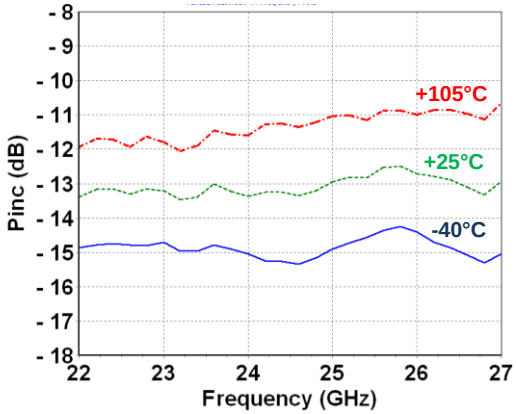
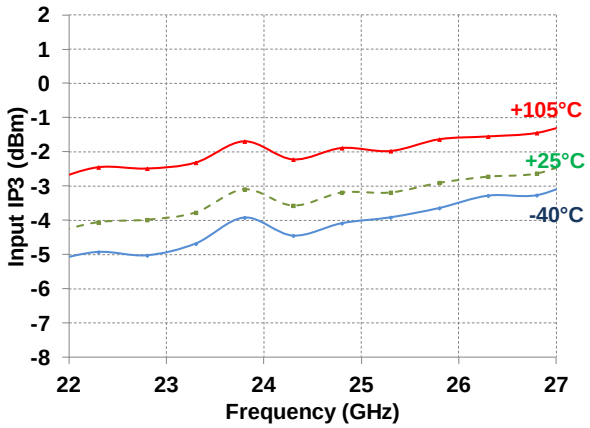
Typical Board Measurements

Vd = +3.3V

Input power at 1dB compression versus temperature



Input IP3 versus temperature



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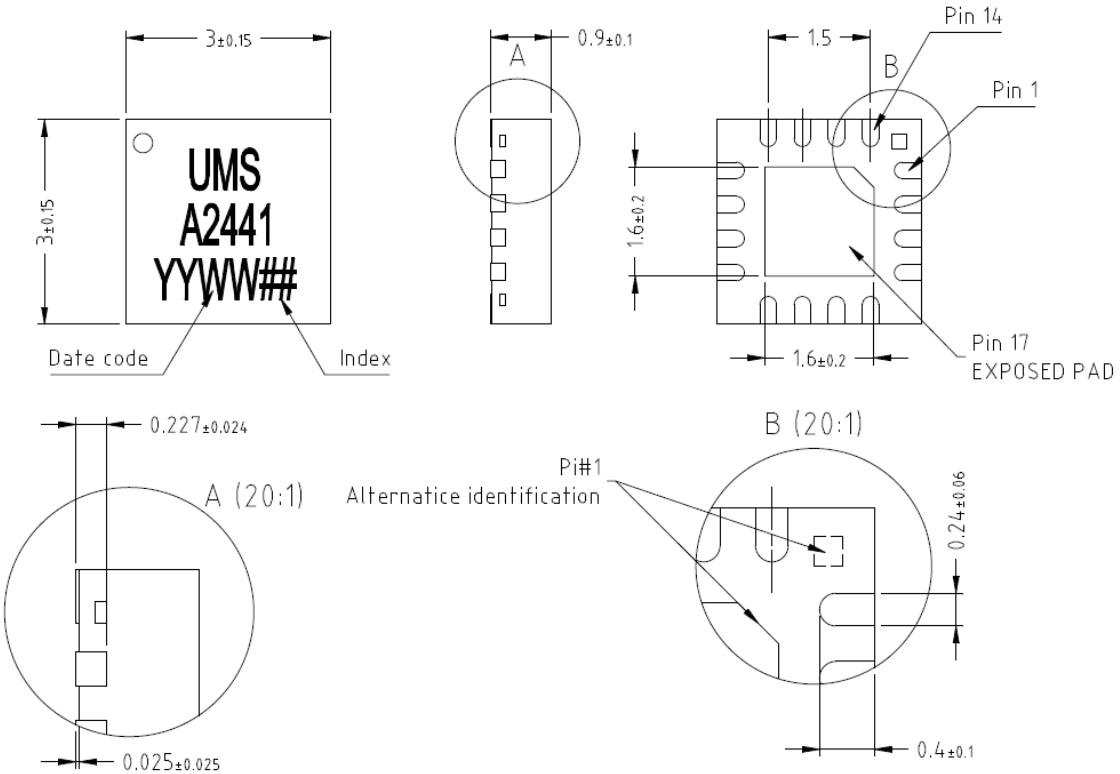
Package outline



Matt tin, Lead Free (Green)		1- Gnd(1)	7- Nc	13- Nc
Units : mm		2- Gnd(1)	8- Gnd(1)	14- VD
From the standard : JEDEC MO-220		3- RF in	9- Gnd(1)	15- Nc
	(VEED)	4- Gnd(1)	10- RF out	16- Nc
17- GND		5- Gnd(1)	11- Gnd(1)	
		6- Nc	12- Gnd(1)	

(1) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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ESD sensitivity

Standard	Value
MIL-STD-1686C	HBM Class 1 (<1000V)
ESD STM5.1-1998	HBM Class 0 (<250V)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte Sn
MSL Rating	MSL1

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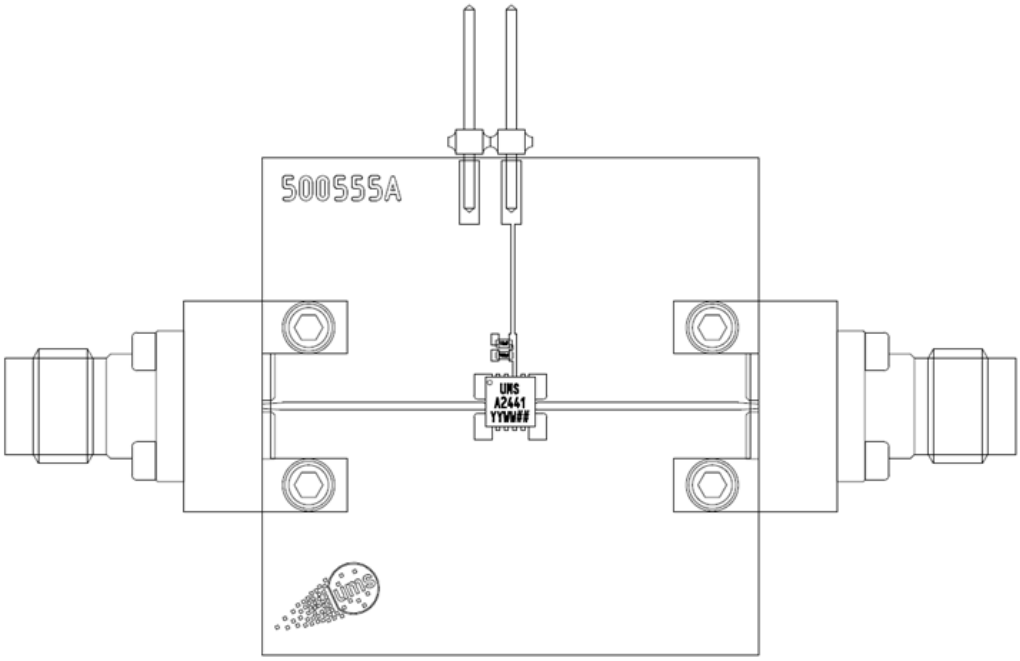
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5% and 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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Notes

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF + 10nF) on the PC board, as close as possible to the package.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 3x3 package:	CHA2441-QAG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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