18-27GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

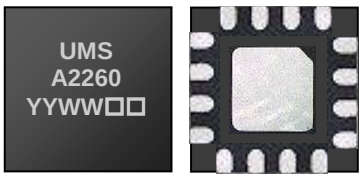
Description

The CHA2260-QAG is a low noise amplifier monolithic circuit, which integrates 3-stages self biased.

It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length.

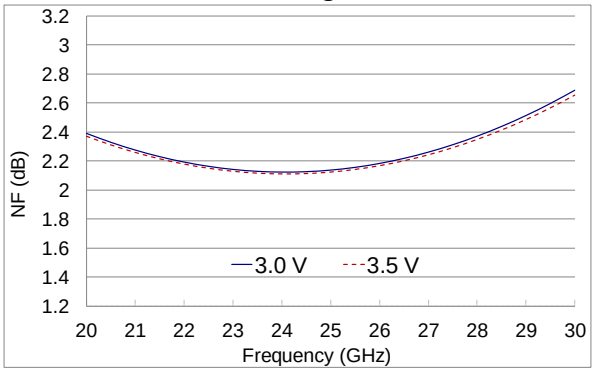
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performance: 18-27GHz
- 26dB Gain
- 2.2dB Noise Figure
- 13dBm Pout
- 23dBm Output IP3
- DC bias: Vd=3.5Volt@Id=65mA
- 16L-QFN3x3
- MSL1

Noise Figure



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	18		27	GHz
Gain	Linear Gain		26		dB
NF	Noise Figure		2.2		dB
Pout	Output Power @1dB comp.		13		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	18		27	GHz
Gain	Linear Gain		26		dB
ΔG	Gain variation in temperature		0.03		dB/°C
NF	Noise Figure in 18- 20.5GHz in 21- 27GHz		2.6 2.2		dB
RLin	Input Return Loss		10		dB
RLout	Output Return Loss		15		dB
OIP3	Output 3rd order intercept point		23		dBm
Pout	Output Power @ 1dB comp		13		dBm
Id	Drain current		65		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4V	V
Id	Drain bias current	85	mA
Pin	Maximum input power	6	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd	14	Drain bias voltage	3.5	V
Id	14	Drain current	65	mA

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below.

The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the PCB system must be designed to comply with this requirement.

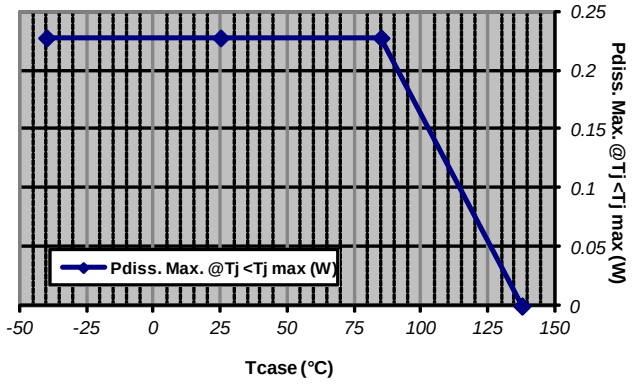
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

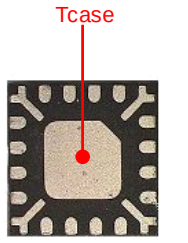
DEVICE THERMAL SPECIFICATION : CHA2260-QAG		
Recommended max. junction temperature (Tj max)	:	138 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power (Pdiss. Max.)	:	0.2 W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	4 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<231 °C/W
Minimum Tcase operating temperature(3)	:	-40 °C
Maximum Tcase operating temperature(3)	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the ***hottest junction*** *of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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Typical Package Sij parameters

Tamb.= +25°C, Vd = +3.5V, Id = 65mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
2.0	-0.783	-94.8	-41.140	50.6	-72.870	63.6	-0.089	-39.6
3.0	-0.886	-142.6	-45.210	0.5	-65.750	83.3	-0.134	-59.0
4.0	-1.038	170.9	-40.280	33.7	-62.620	69.3	-0.163	-78.5
5.0	-1.205	126.4	-36.350	24.0	-57.730	71.9	-0.189	-98.3
6.0	-1.606	85.0	-22.560	56.4	-52.860	42.3	-0.294	-119.0
7.0	-1.389	50.7	-11.010	10.6	-53.770	18.9	-0.542	-140.7
8.0	-1.120	14.8	-2.847	-40.9	-51.430	-2.5	-1.015	-164.3
9.0	-0.934	-18.1	2.941	-93.1	-50.070	-40.6	-1.652	170.7
10.0	-0.759	-49.4	7.445	-143.7	-51.100	-90.4	-2.520	145.0
11.0	-0.851	-81.9	11.550	168.7	-53.530	-128.2	-3.982	121.0
12.0	-0.842	-110.6	14.170	120.2	-60.960	-168.2	-6.060	85.0
13.0	-0.805	-135.9	16.150	79.1	-46.310	-137.8	-8.750	57.3
14.0	-0.869	-161.5	18.700	38.0	-48.360	163.5	-10.320	24.5
15.0	-0.883	171.0	21.370	-2.7	-48.220	125.0	-12.610	-6.2
16.0	-1.509	137.0	24.360	-46.4	-46.750	96.5	-14.010	-37.7
17.0	-4.175	89.7	26.590	-98.7	-46.120	52.5	-15.630	-87.5
18.0	-8.806	23.8	27.530	-155.1	-45.390	7.8	-15.460	-138.5
19.0	-12.470	-64.6	27.240	157.1	-55.140	-81.3	-20.700	175.7
20.0	-11.690	-123.2	27.020	113.4	-56.750	-74.6	-16.230	149.2
21.0	-11.030	-153.6	27.090	71.4	-53.770	-117.5	-16.070	114.6
22.0	-10.810	179.9	26.870	31.7	-46.900	-151.4	-17.630	109.1
23.0	-11.620	159.7	26.530	-7.9	-41.570	177.9	-17.350	106.9
24.0	-14.840	106.6	27.510	-49.4	-38.860	132.9	-14.790	39.2
25.0	-24.790	107.0	26.870	-92.3	-39.570	100.7	-23.190	-8.9
26.0	-20.330	127.9	27.040	-131.7	-37.130	87.7	-22.350	-4.1
27.0	-12.360	106.7	27.560	-177.6	-35.580	65.5	-14.470	-25.9
28.0	-5.208	66.5	27.610	127.0	-34.910	34.5	-7.773	-56.0
29.0	-2.699	16.8	24.660	70.6	-36.490	12.6	-4.174	-96.4
30.0	-1.827	-18.5	21.530	28.6	-38.480	1.9	-3.177	-122.0
31.0	-1.364	-53.6	18.530	-11.3	-41.020	6.5	-2.566	-141.3
32.0	-1.647	-88.1	15.410	-50.6	-38.520	14.0	-2.381	-158.2
33.0	-2.059	-119.6	11.850	-84.9	-35.390	1.4	-2.717	-169.5
34.0	-2.657	-148.9	8.204	-115.4	-35.590	-22.4	-3.052	-177.4
35.0	-3.079	-174.1	4.818	-141.9	-33.870	-47.2	-3.196	174.3
36.0	-3.223	165.9	1.690	-165.4	-34.220	-88.5	-3.221	165.8
37.0	-3.051	151.8	-1.060	173.8	-41.620	-117.0	-3.452	155.4
38.0	-2.587	138.3	-3.568	152.6	-41.800	-99.0	-3.799	145.3
39.0	-2.297	127.5	-5.777	131.9	-43.740	-95.8	-3.856	136.2
40.0	-2.145	117.2	-7.905	111.9	-47.990	-169.9	-3.758	122.7

The Sij measurement calibration planes are defined in the paragraph “Definition of the Sij reference planes”.

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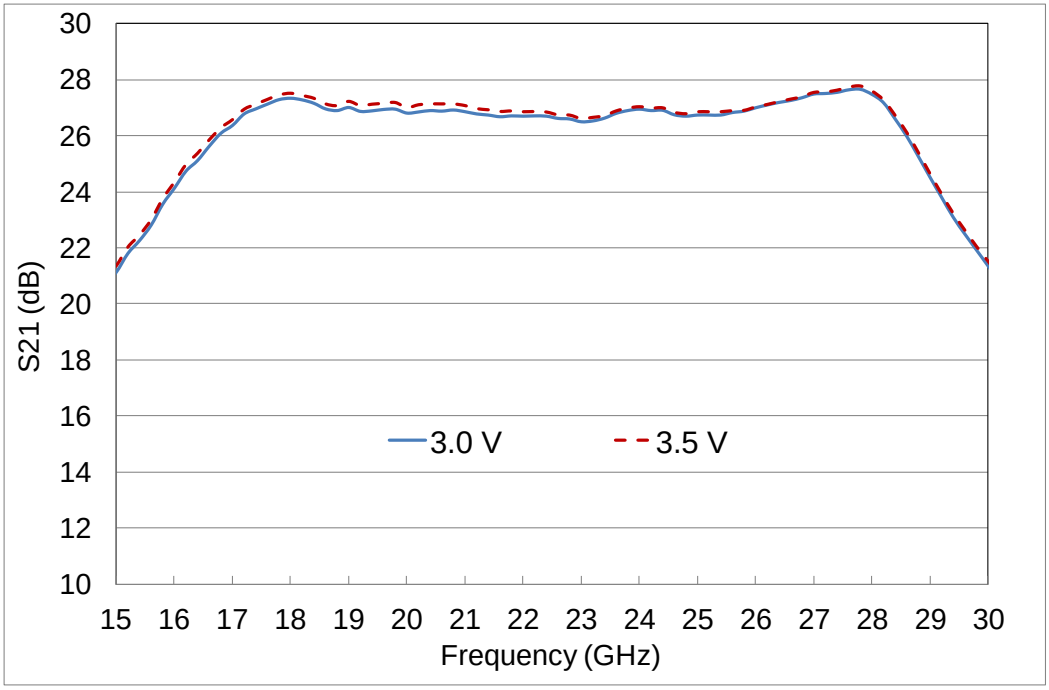
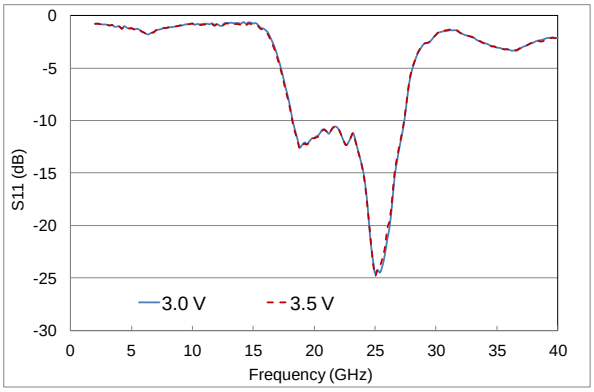
Typical Board Measurements

Tamb.= +25°C, Vd = +3.5V, Id = 65mA
These graphs are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".
Data are given in the QFN access planes

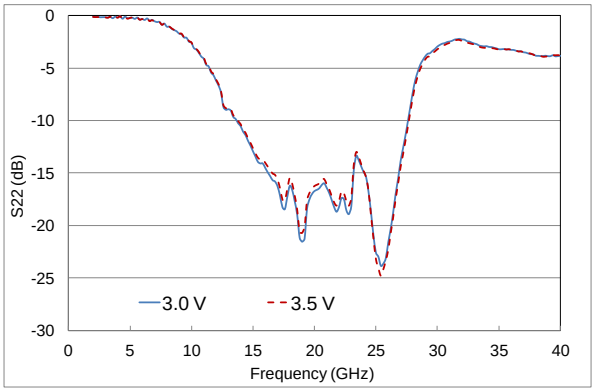
Gain versus Frequency



Input return loss versus Frequency



Output return loss versus Frequency



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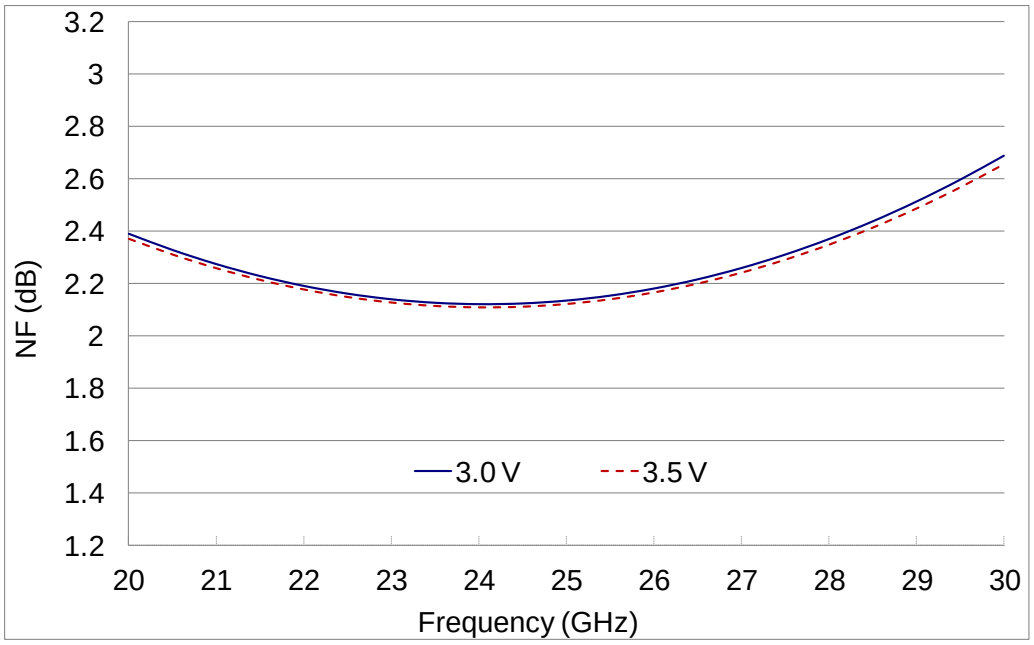
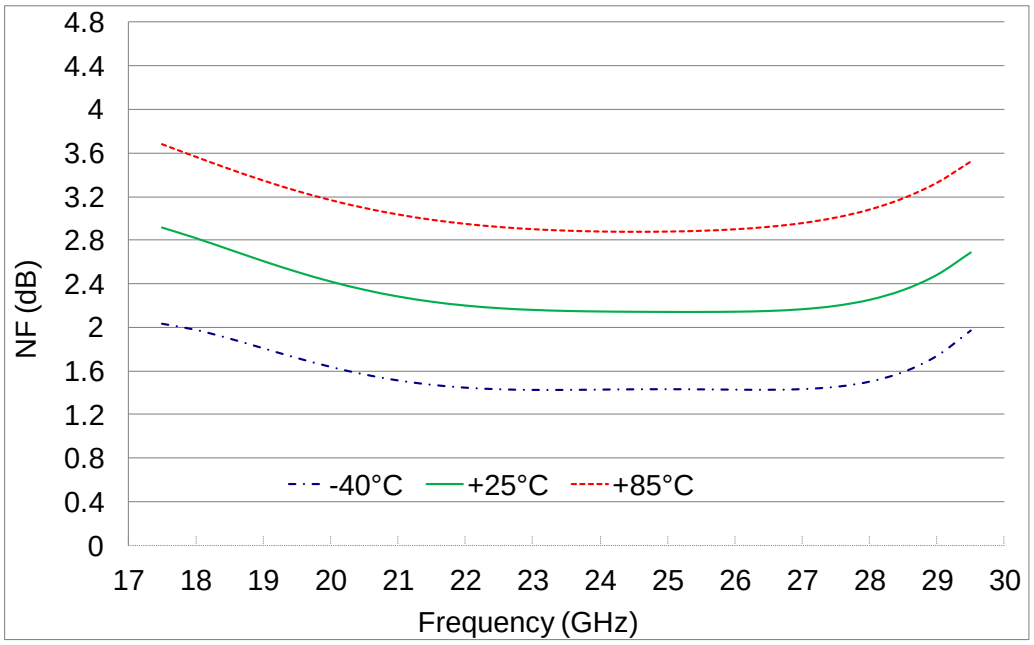
Typical Board Measurements

Tamb.= +25°C, Vd = +3.5V, Id = 65mA

Noise Figure versus Frequency and Drain Voltage



Noise Figure versus Frequency and Temperature



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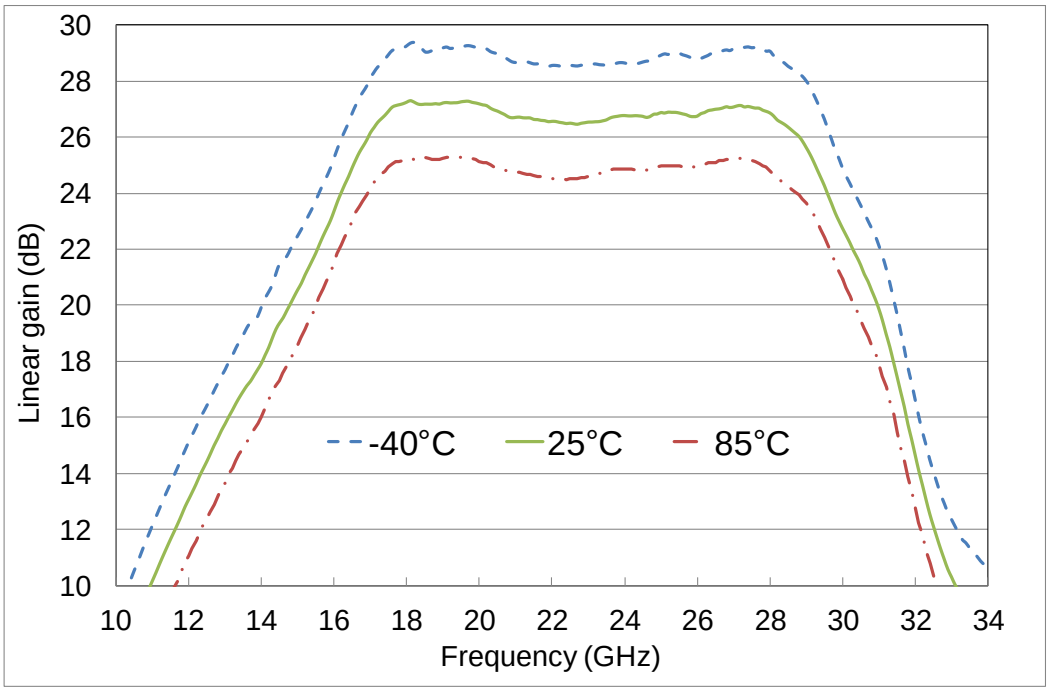
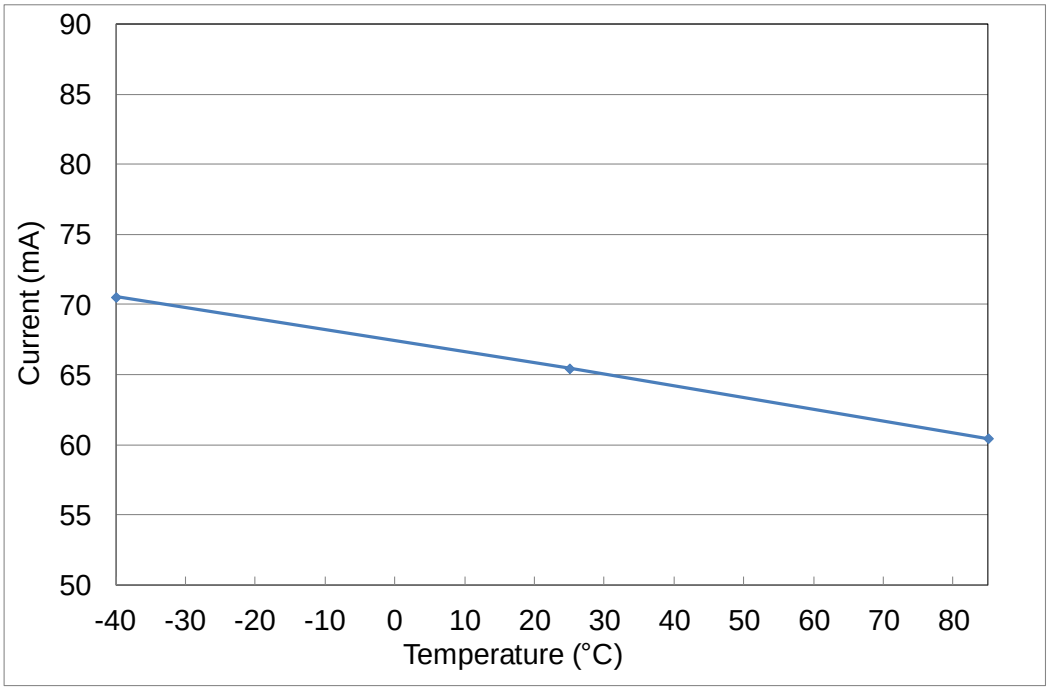
Typical Board Measurements

Tamb.= +25°C, Vd = +3.5V, Id = 65mA

Linear gain versus Frequency and Temperature



Current versus Temperature



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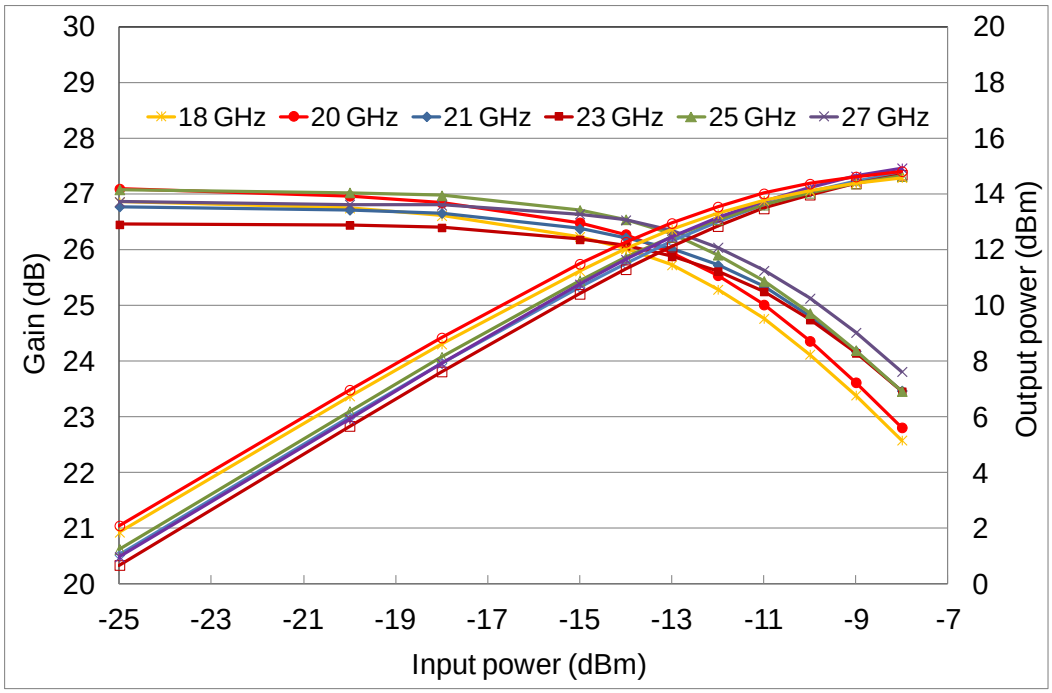
Typical Board Measurements

Tamb.= +25°C, Vd = +3.5V, Id = 65mA

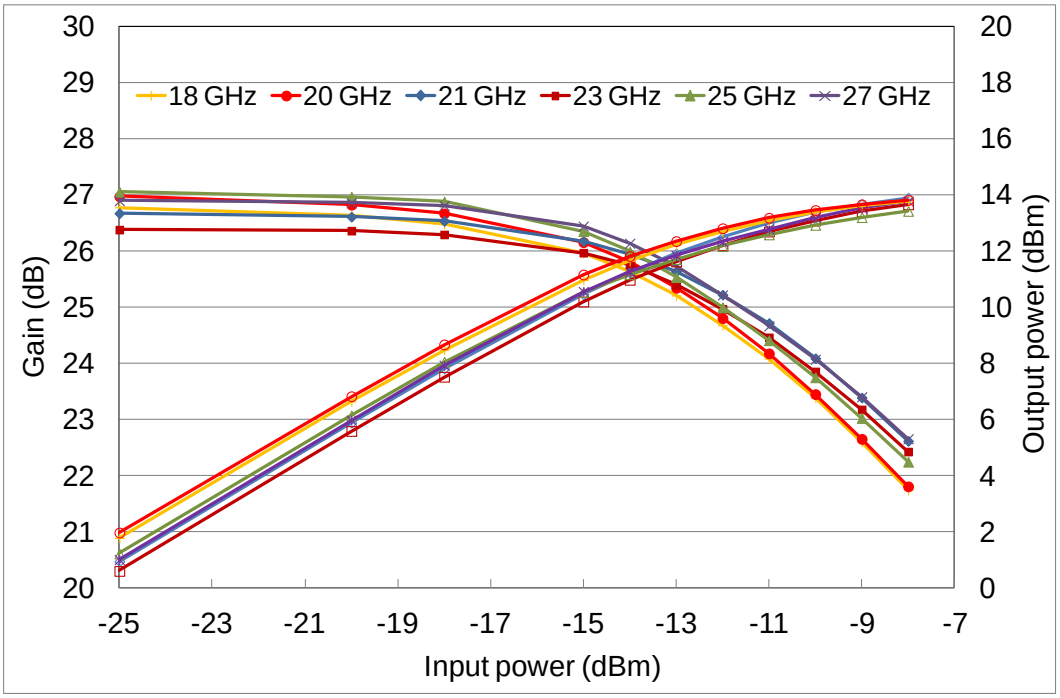
Gain and Output Power versus Input Power and Frequency

Vd= 3.5V



Gain and Output Power versus Input Power and Frequency

Vd= 3.0V



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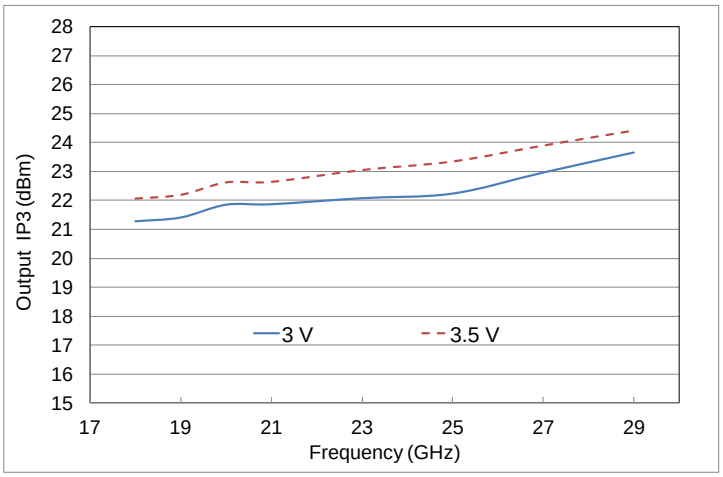
Typical Board Measurements

Tamb.= +25°C, Vd = +3.5V, Id = 65mA

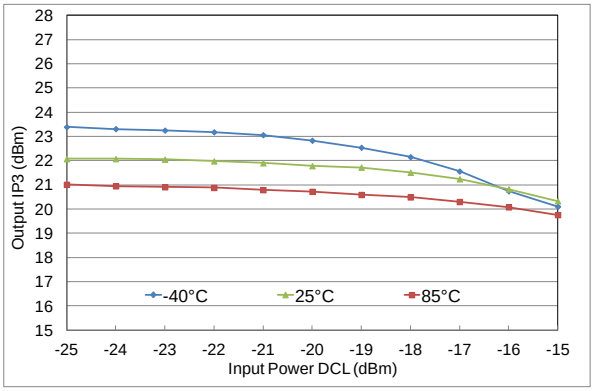
Output IP3 versus Frequency and Drain Voltage

Pin DCL= -23dBm



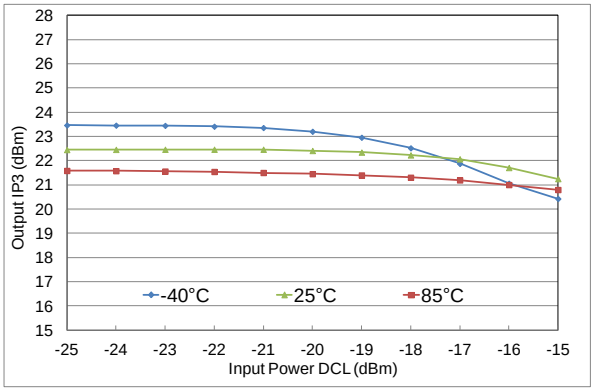
OIP3 versus Input Power & Temperature

Vd= 3.5V, Frequency= 18GHz



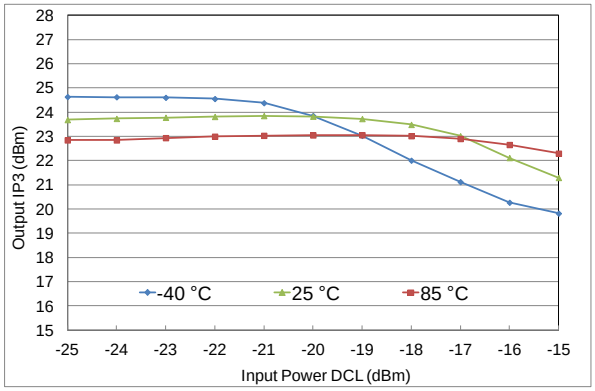
OIP3 versus Input Power & Temperature

Vd= 3.5V, Frequency= 21GHz



OIP3 versus Input Power & Temperature

Vd= 3.5V, Frequency= 27GHz



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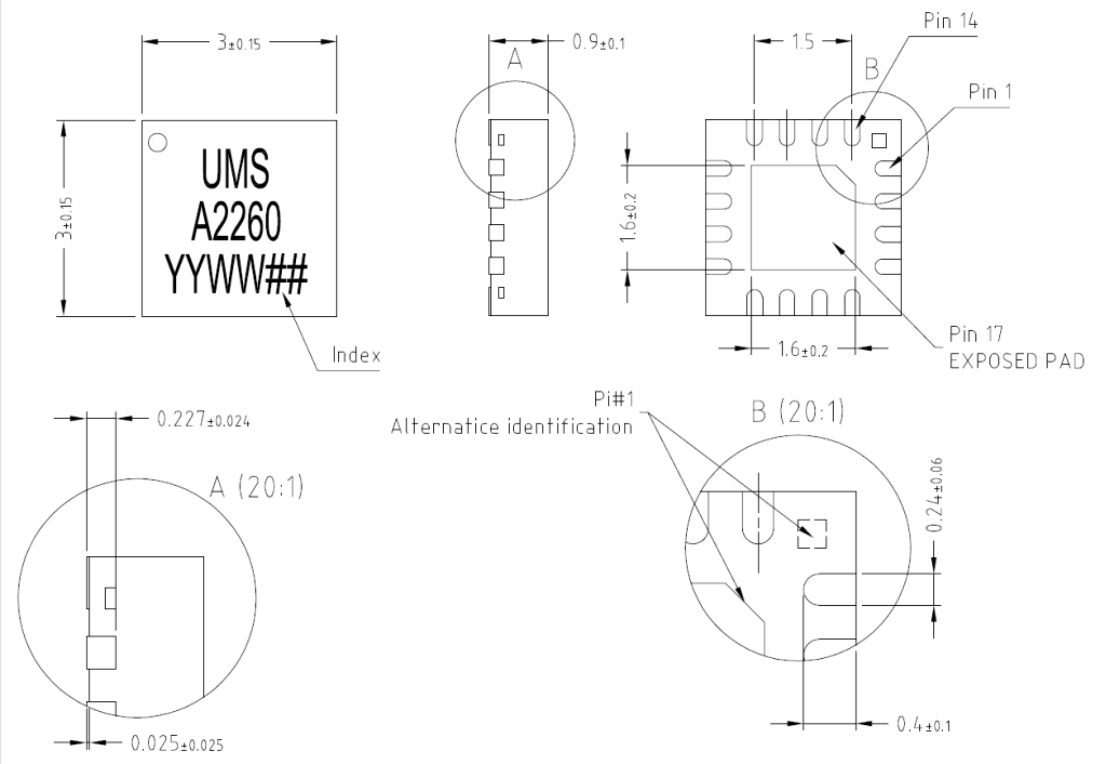
Package outline (1)



Matt tin, Lead Free (Green)		1- Gnd(2)	7- Nc	13- Nc
Units :	mm	2- Gnd(2)	8- Nc	14- Vd
From the standard :	JEDEC MO-220	3- RF in	9- Gnd(2)	15- Nc
	(VEED)	4- Gnd(2)	10- RF out	16- Gnd(2)
17- GND		5- Nc	11- Gnd(2)	
		6- Nc	12- Gnd(2)	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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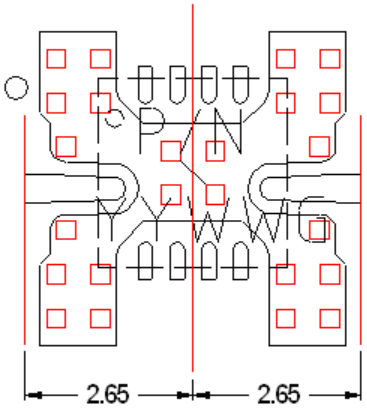
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 2.65mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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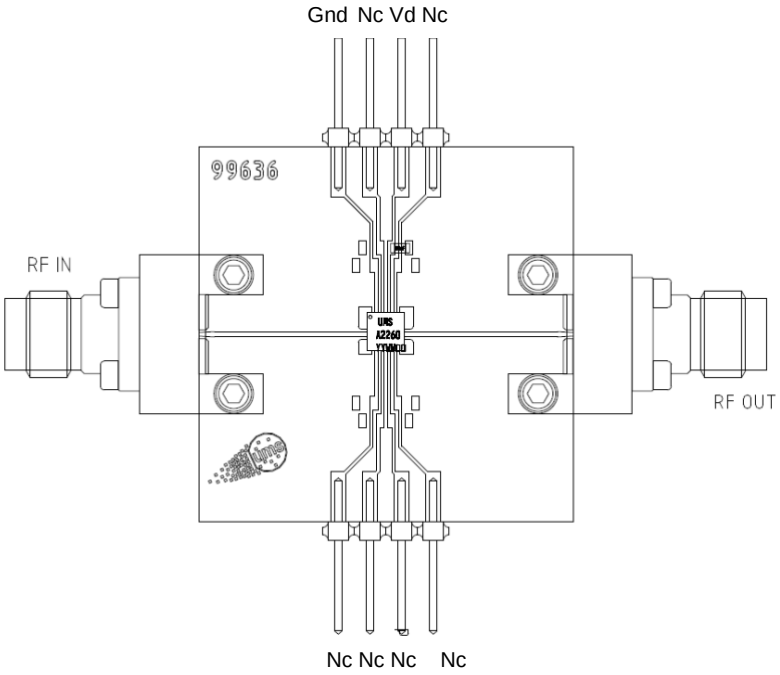
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitor of 10nF ±10% are recommended for all DC accesses.
- RF connectors 40GHz
- See application note AN0017 for details.



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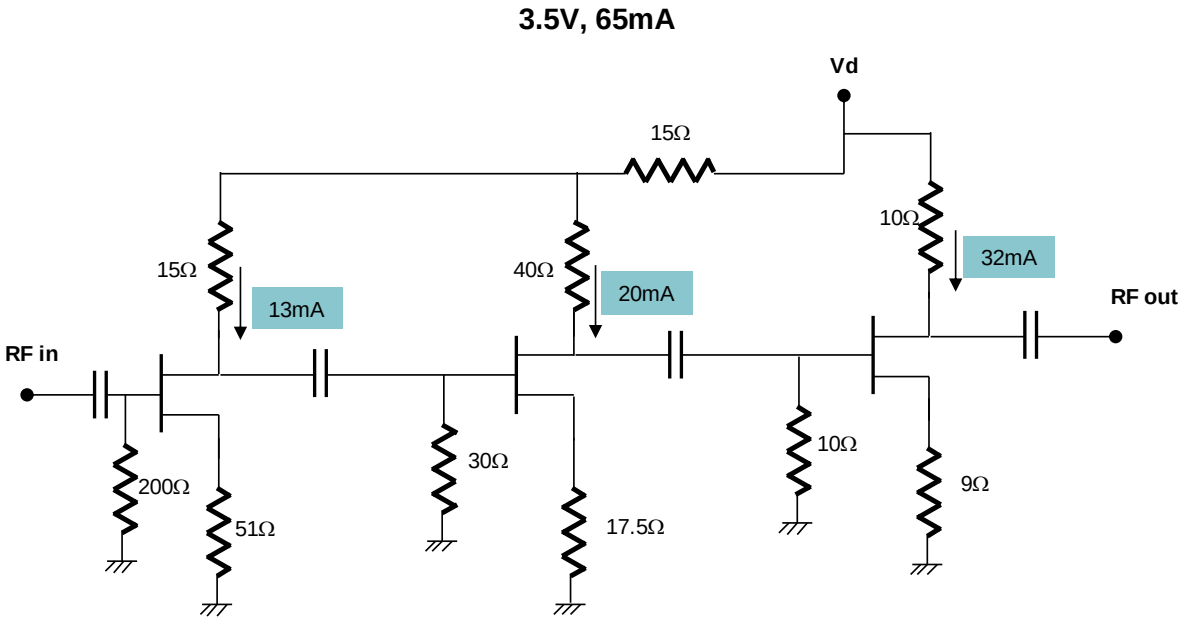
DC Schematic



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 3x3 package:	CHA2260-QAG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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