United Monolithic Semiconductors

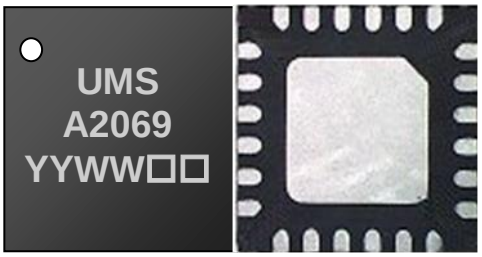
CHA2069-QDG

18-31GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA2069-QDG is a three-stage self-biased wide band monolithic low noise amplifier. Typical applications range from telecommunication (point to point, point to multi-point, VSAT) to ISM and military markets.



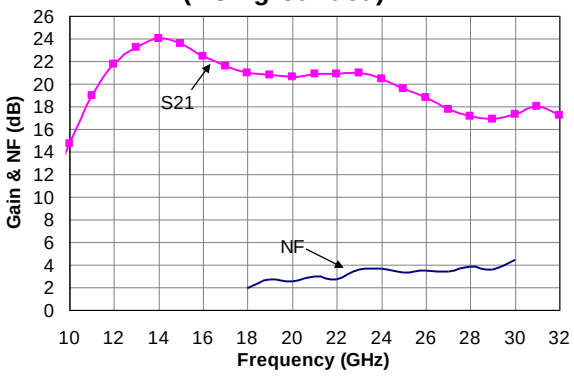
The circuit is manufactured with a standard pHEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in lead-free SMD package.

Main Features

- Broadband performance 18-31GHz
- 3dB noise figure
- 20dB gain
- 65mA low DC power consumption
- 20dBm 3rd order intercept point (high current configuration)
- 24L-QFN4x4 SMD package
- MSL Level: 1

Gain and NF @ high current configuration (BCF grounded)



Main Characteristics

Tamb = +25°C, Vd = +4,5V Pads: B, C, F = GND (High current configuration)

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise figure		3	4.5	dB
G	Gain	17	20		dB
IP3	3rd order intercept point (Pout/tone=-5dBm) 18-26GHz	18	20		dBm

ESD protections: electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics (low current configuration)

Tamb = +25°C, Vd = +4.5V, pads: B, D, E = GND

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	18		31	GHz
G	Gain	16.5	19.5		dB
ΔG	Gain flatness		±2	±2.5	dB
NF	Noise figure		3	4.5	dB
IS11I	Input return loss		-5	-2	dB
IS22I	Output return loss		-7	-2.5	dB
IP3	3rd order intercept point (Pout/tone=-5dBm) 18-26GHz	16.5	18.5		dBm
P1dB	Output power at 1dB gain compression	9.0	10.5		dBm
Id	Drain bias current		65		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Electrical Characteristics (high current configuration)

Tamb = +25°C, Vd = +4.5V, pads: B, C, F = GND

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	18		31	GHz
G	Gain	17	20		dB
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NF	Noise figure		3	4.5	dB
IS11I	Input return loss		-5	-2	dB
IS22I	Ouput return loss		-7	-2.5	dB
IP3	3rd order intercept point (Pout/tone=-5dBm) 18-26GHz	18	20		dBm
P1dB	Output power at 1dB gain compression	12	13.5		dBm
Id	Drain bias current		85		mA

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5	V
Pin	Maximum input power overdrive	+10	dBm
Rth_BDE	Thermal Resistance channel to ground paddle (2)	130	°C/W
Rth_BCF	Thermal Resistance channel to ground paddle (2)	120	°C/W
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Thermal Resistance for Tamb. = +85°C and a Tjmax = +175°C

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

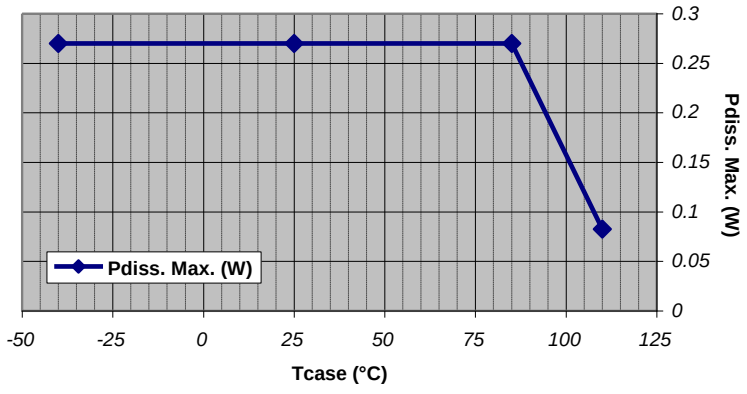
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

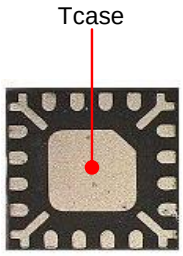
DEVICE THERMAL SPECIFICATION : CHA2069-QDG				
Recommended max. junction temperature (Tj max)			:	121 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power @ Tcase=	85	°C	:	0.27 W
=> Pdiss derating above Tcase(1)=	85	°C	:	8 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)			:	<133 °C/W
Min. package back side operating temperature(3)			:	-40 °C
Max. package back side operating temperature(3)			:	85 °C
Min. storage temperature			:	-55 °C
Max. storage temperature			:	125 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hottest junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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Typical Package Sij parameters for low current configuration

Tamb.= +25°C, Vd = +4.5V, Pads: B,D, E grounded

Freq (GHz)	S11 (dB)	S11 (°)	S12 (dB)	S12 (°)	S21 (dB)	S21 (°)	S22 (dB)	S22 (°)
2	-0.1	-58.7	-95.2	-85.6	-57.5	-2.4	-0.6	-148.4
3	-0.1	-89.3	-68.8	63.3	-77.6	-24.4	-0.9	157.1
4	-0.1	-123.5	-63.2	93.4	-52.9	62.8	-0.9	112.4
5	-0.2	-160.8	-62.9	47.1	-37.4	145.3	-1.3	72.0
6	-0.4	156.1	-58.1	11.4	-18.1	93.6	-1.7	39.9
7	-0.6	107.6	-67.5	-59.7	-4.4	28.0	-2.0	8.4
8	-1.2	58.9	-68.1	93.7	4.4	-52.1	-3.0	-20.2
9	-1.8	13.5	-61.6	-9.2	9.6	-122.4	-3.9	-38.6
10	-2.8	-26.1	-60.0	-42.6	14.7	176.1	-4.4	-69.5
11	-4.0	-58.0	-55.1	171.8	19.0	109.4	-8.3	-92.5
12	-5.7	-89.1	-53.4	87.2	21.7	41.3	-13.4	-92.8
13	-8.8	-122.0	-49.6	14.1	23.3	-24.1	-17.0	-67.1
14	-15.8	-173.9	-50.5	-42.8	24.0	-86.8	-12.6	-36.0
15	-17.4	24.9	-48.2	-120.3	23.5	-146.2	-8.3	-46.7
16	-10.9	-20.6	-48.3	171.6	22.4	162.0	-6.3	-65.3
17	-8.5	-47.1	-49.6	133.4	21.5	116.9	-5.9	-85.2
18	-7.0	-65.5	-47.3	121.9	20.9	75.8	-5.9	-99.8
19	-6.2	-82.8	-44.9	92.5	20.8	34.2	-6.1	-116.0
20	-5.8	-98.4	-42.5	57.3	20.7	-6.5	-7.2	-130.1
21	-4.9	-110.8	-43.2	20.1	20.9	-48.3	-7.9	-137.3
22	-4.7	-125.9	-45.3	14.9	20.9	-90.8	-9.2	-142.4
23	-4.3	-138.7	-43.3	-0.5	20.9	-135.3	-8.7	-139.3
24	-3.9	-152.2	-43.7	-14.8	20.4	178.7	-7.6	-141.9
25	-3.8	-163.2	-44.2	-36.7	19.6	135.8	-6.3	-148.5
26	-3.3	-173.7	-45.4	-48.5	18.8	92.8	-4.4	-156.9
27	-3.0	175.5	-46.5	-43.8	17.8	52.7	-3.7	-169.0
28	-2.5	166.4	-43.7	-45.2	17.1	13.2	-3.0	-179.9
29	-2.5	155.4	-43.2	-59.5	16.8	-26.3	-2.7	171.2
30	-2.8	146.3	-42.0	-81.7	17.3	-69.6	-2.7	161.4
31	-3.9	144.4	-46.4	-112.7	18.0	-123.9	-2.6	156.1
32	-2.8	154.3	-47.9	-148.6	17.2	168.4	-2.5	150.5

The Sij measurement calibration planes are defined in the paragraph “Definition of the Sij reference planes”.

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Typical Package Sij parameters for high current configuration

Tamb.= +25°C, Vd = +4.5V, Pads: B,D, E grounded

Freq (GHz)	S11 (dB)	S11 (°)	S12 (dB)	S12 (°)	S21 (dB)	S21 (°)	S22 (dB)	S22 (°)
2	-0.1	-58.5	-92.2	81.8	-57.9	0.4	-0.7	-146.6
3	-0.1	-88.9	-67.1	55.2	-69.1	-41.4	-1.1	159.3
4	-0.1	-122.6	-62.8	100.3	-51.5	77.3	-1.0	114.1
5	-0.2	-159.2	-63.0	51.4	-37.2	145.1	-1.5	73.0
6	-0.4	158.4	-56.6	15.4	-17.7	97.4	-1.9	40.1
7	-0.7	110.4	-64.5	-49.7	-3.8	31.4	-2.2	8.3
8	-1.3	60.8	-67.3	88.2	5.3	-49.4	-3.4	-21.8
9	-1.8	13.6	-61.5	-7.6	10.6	-120.9	-4.6	-40.0
10	-2.9	-27.8	-59.6	-45.7	15.6	177.2	-4.8	-68.3
11	-4.0	-60.9	-54.4	176.7	19.9	110.8	-8.5	-89.9
12	-5.6	-92.1	-53.9	99.3	22.7	43.0	-12.5	-90.4
13	-8.5	-123.1	-50.6	22.2	24.2	-22.2	-16.3	-76.8
14	-14.6	-169.0	-52.1	-32.8	25.1	-84.9	-13.8	-40.8
15	-19.5	26.2	-50.3	-120.6	24.8	-145.6	-8.9	-46.4
16	-11.3	-23.8	-49.4	165.3	23.6	161.3	-6.5	-65.0
17	-8.5	-49.1	-50.9	132.8	22.6	115.2	-6.0	-86.1
18	-6.9	-67.5	-46.9	122.6	21.8	73.8	-5.8	-101.6
19	-6.1	-83.9	-44.9	88.3	21.5	32.7	-6.1	-119.7
20	-5.6	-97.1	-43.0	53.7	21.2	-7.8	-7.0	-134.2
21	-4.6	-109.1	-44.1	21.4	21.3	-48.7	-7.6	-144.5
22	-4.4	-123.2	-45.4	19.8	21.3	-90.2	-9.0	-153.5
23	-4.1	-135.7	-43.9	7.2	21.4	-133.4	-9.4	-152.7
24	-3.7	-149.8	-43.4	-10.0	21.0	-178.9	-8.8	-151.9
25	-3.8	-162.0	-44.3	-34.6	20.3	138.4	-7.6	-155.6
26	-3.5	-173.4	-44.5	-42.2	19.7	94.7	-5.5	-161.7
27	-3.3	174.4	-47.4	-45.9	18.7	53.4	-4.5	-172.3
28	-3.0	164.8	-44.8	-39.0	18.0	12.8	-3.6	177.3
29	-2.9	153.8	-43.6	-43.1	17.6	-27.1	-3.0	168.4
30	-2.9	143.4	-41.7	-66.2	18.0	-70.8	-2.6	158.1
31	-3.8	138.2	-44.6	-91.4	18.4	-123.8	-2.6	150.7
32	-2.7	145.3	-49.9	-140.7	17.8	169.5	-2.6	144.6

The Sij measurement calibration planes are defined in the paragraph “Definition of the Sij reference planes”.

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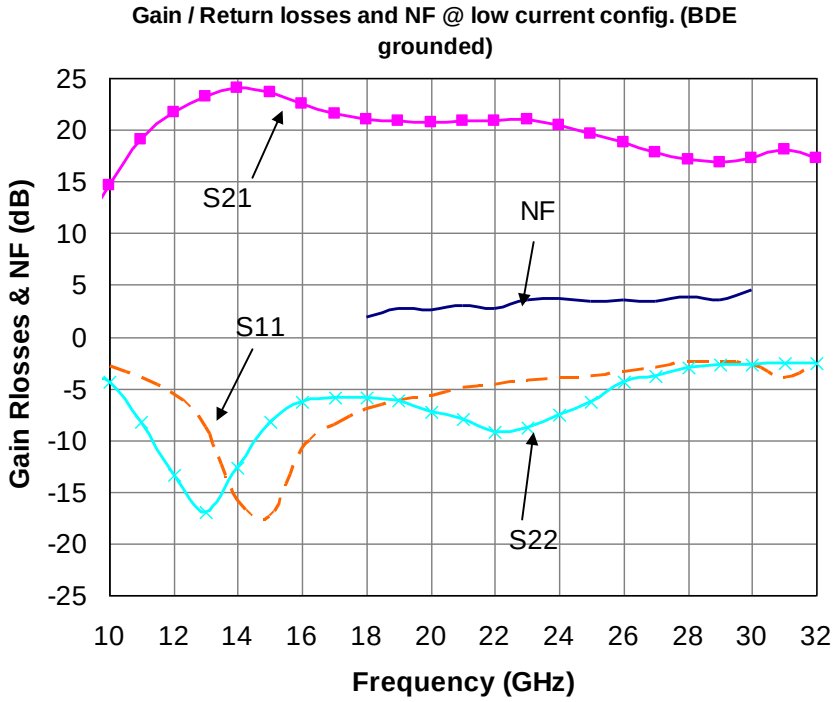
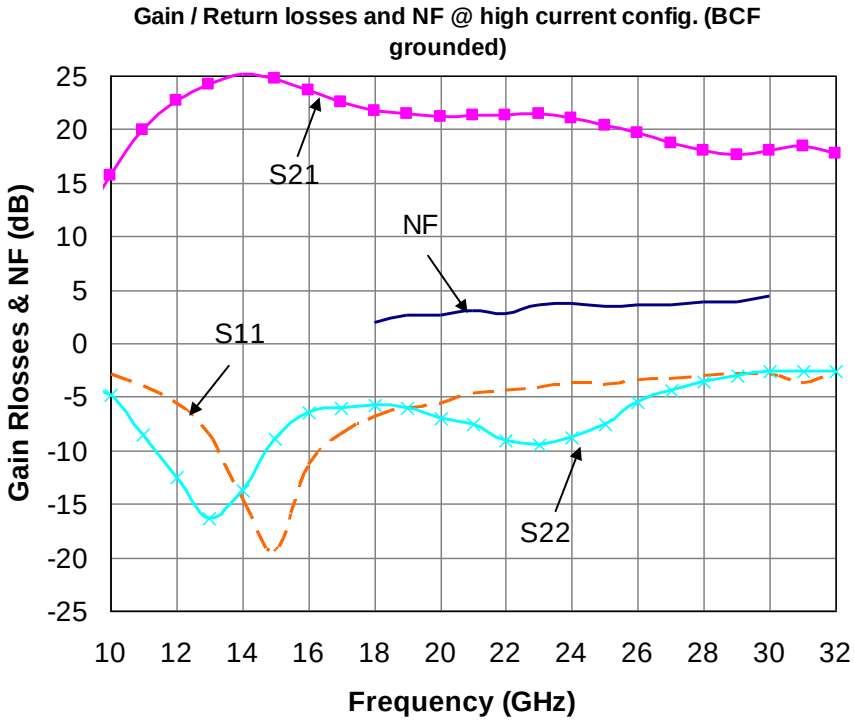
Typical on wafer Measurements

Tamb = +25°C, Vd = +4.5V

Measurements are given in the package access plans, using the proposed pattern and board given in the paragraph “Evaluation mother board:”.





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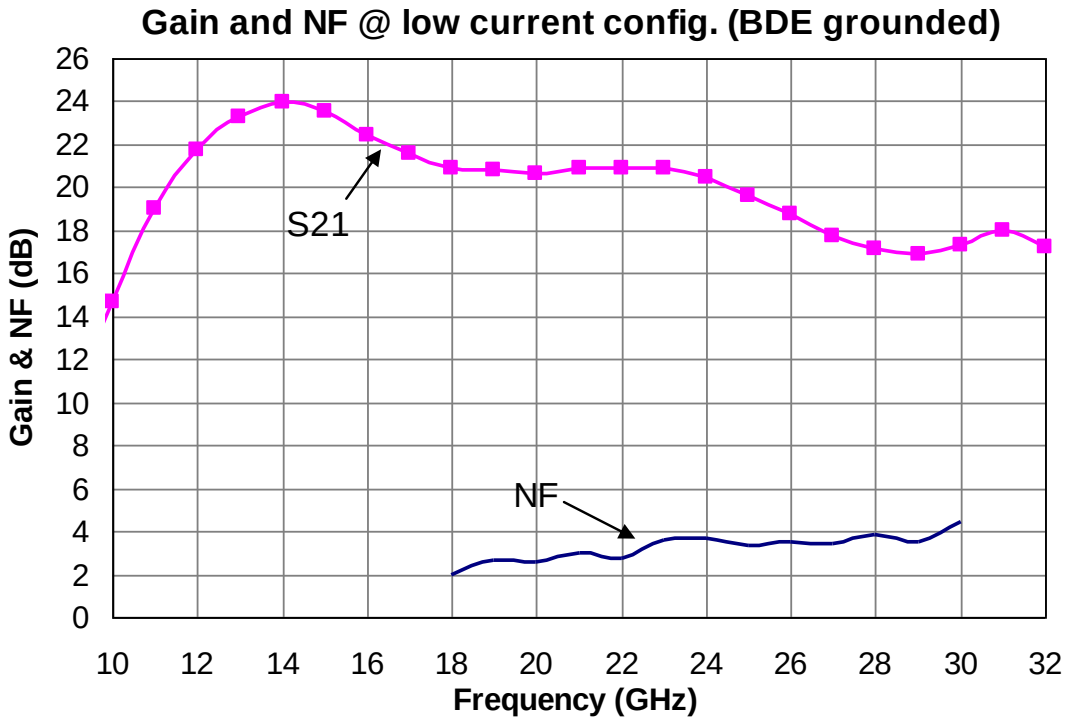

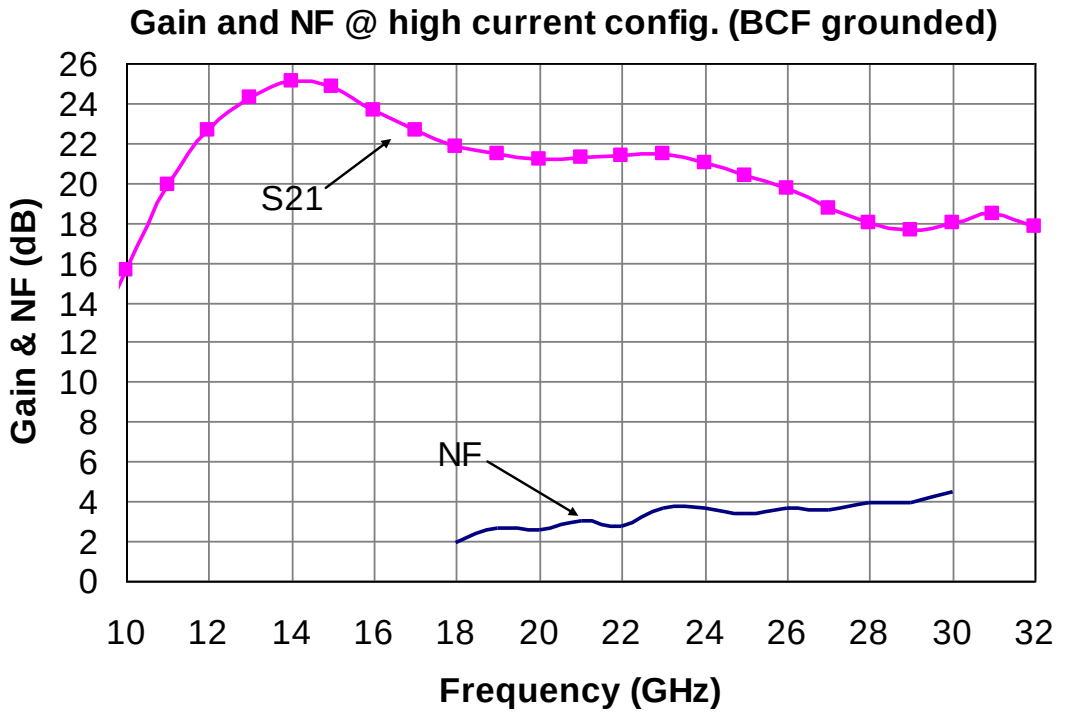

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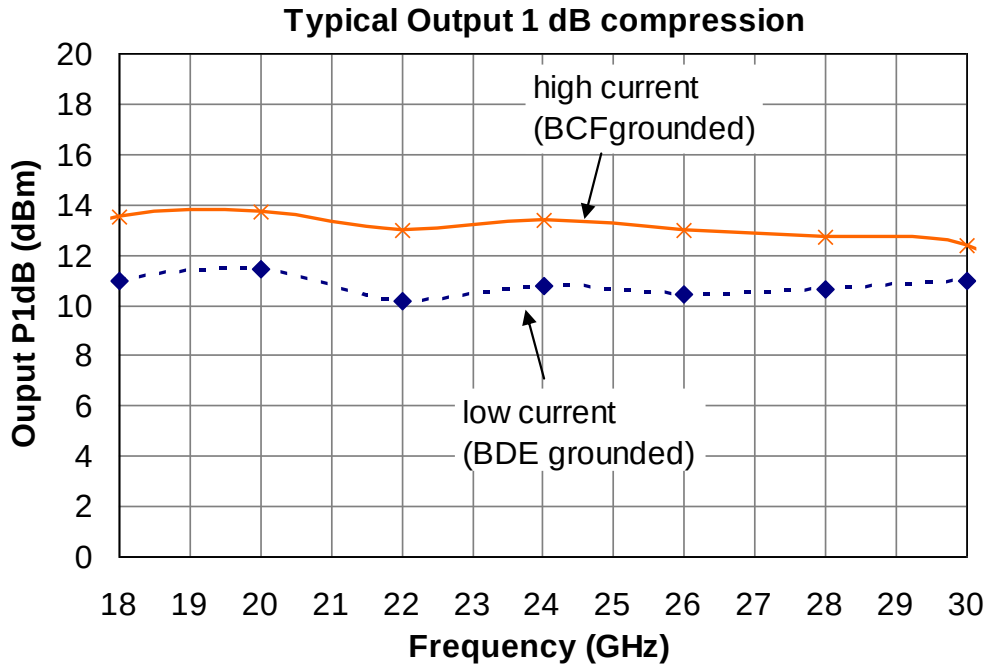
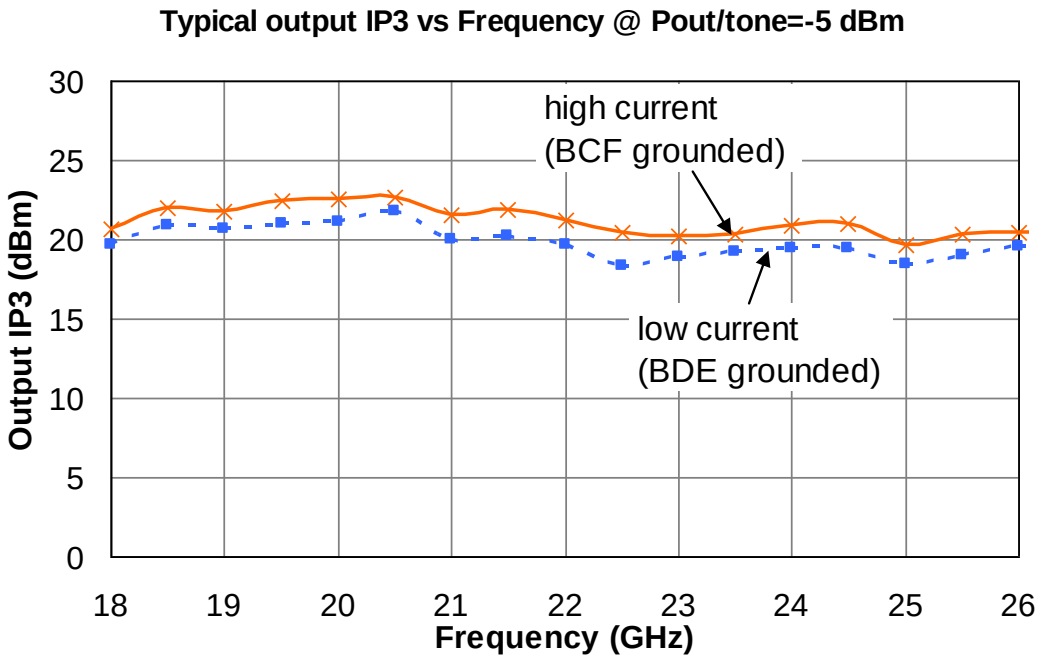
Typical on wafer Measurements

Tamb = +25°C, Vd = +4.5V
Measurements are given in the connectors' access plans, using the proposed land pattern and board given in the paragraph "Evaluation mother board".
For these measurements, losses due to board are not de-embedded.





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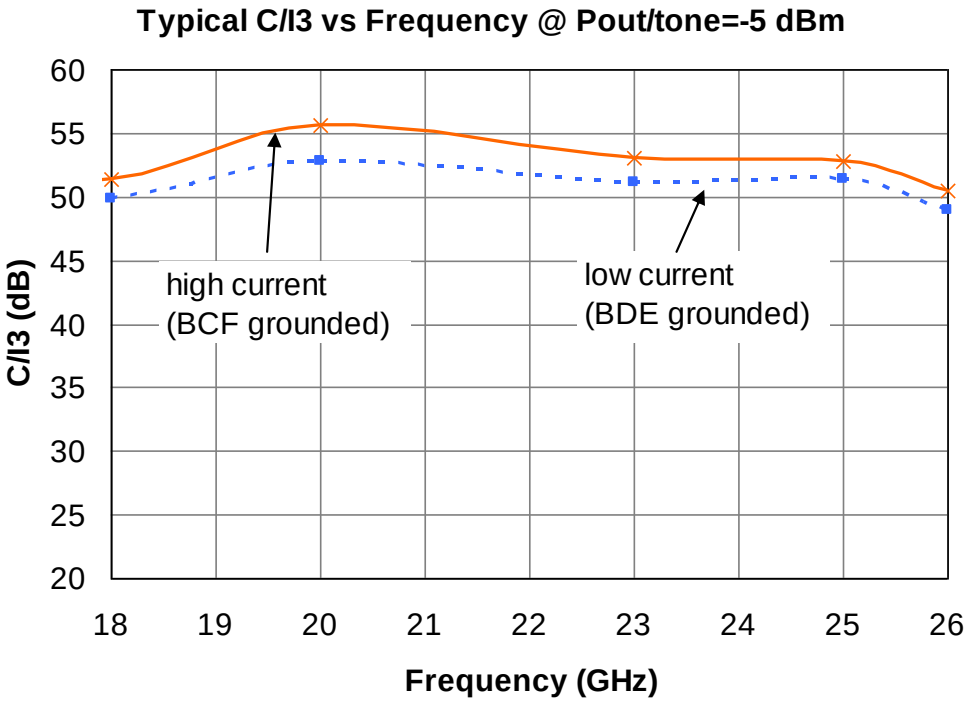
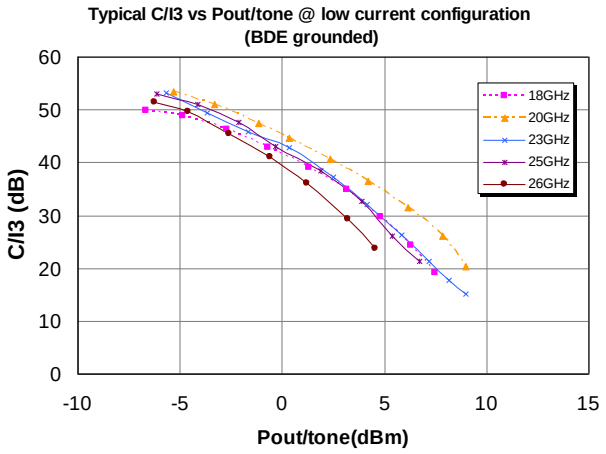
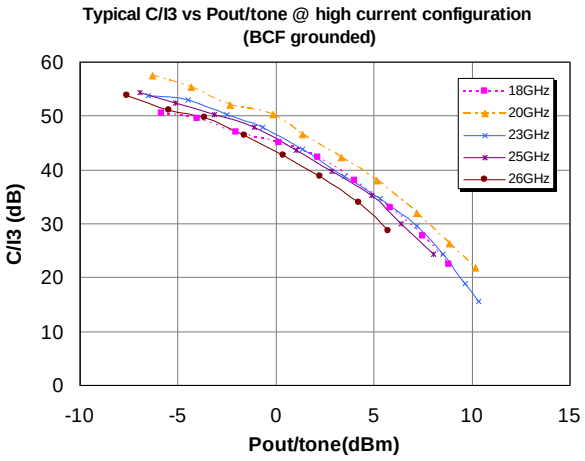
Typical on wafer Measurements

Tamb = +25°C, Vd = +4.5V







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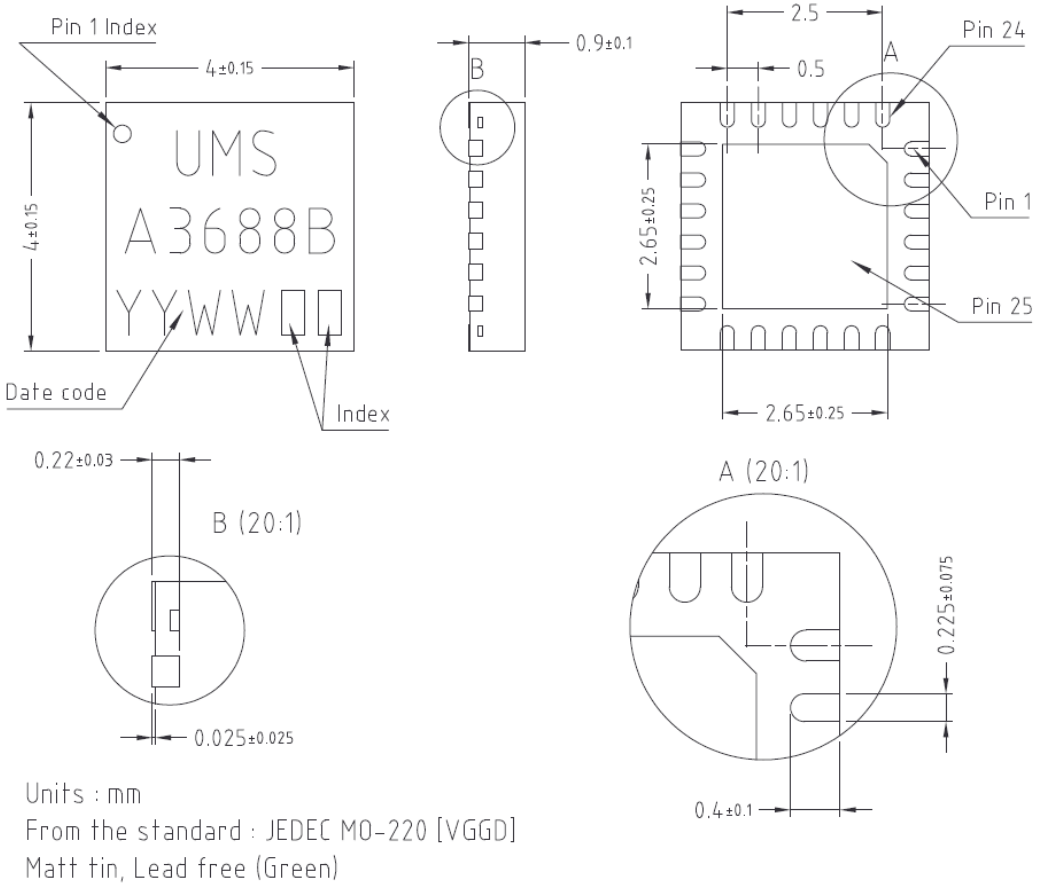
Package outline (1)



Matt tin, Lead Free	(Green)	1- Nc	13- Nc
Units	mm	2- Nc	14- Gnd
From the standard	JEDEC MO-220	3- Gnd	15- RF OUT
	(VGGD)	4- RF IN	16- Gnd
25- GND		5- Gnd	17- Nc
		6- Nc	18- Nc
		7- B	19- Vd
		8- C	20- Vd
		9- D	21- Vg3
		10- Nc	22- Vg2
		11- E	23- Vg1
		12- F	24- Nc

(1)The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 available at https://www.ums-rf.com for exact package dimensions. It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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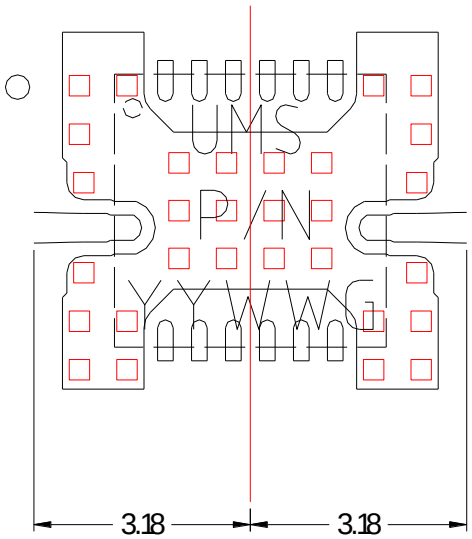
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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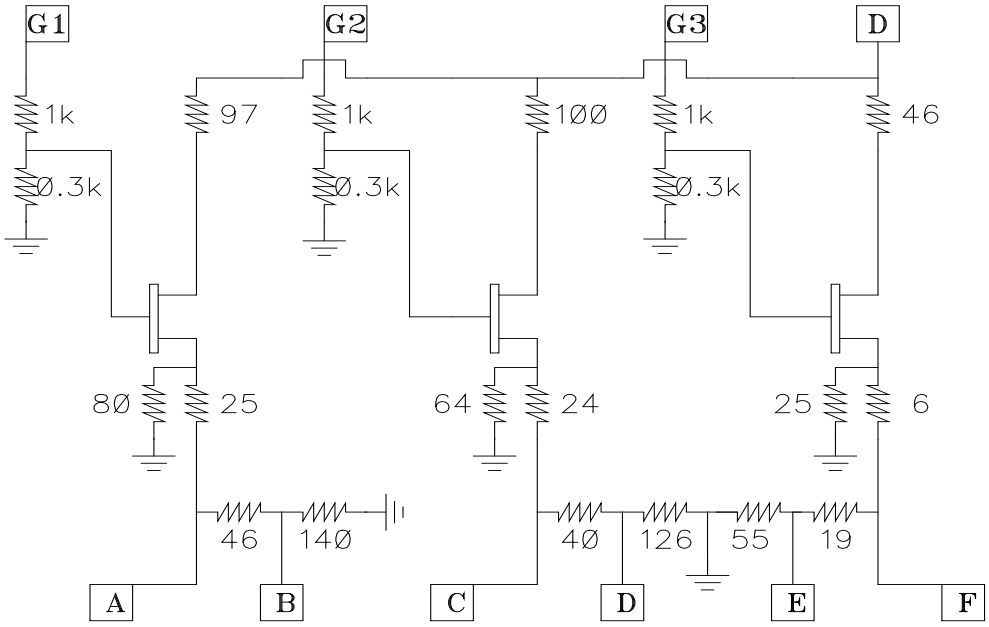
Packaged part biasing options

This circuit is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



The two requirements are:

N°1: Not exceed Vd = 3.5Volt (internal Drain to Source voltage).
N°2: Not biased in such a way that Vgs becomes positive. (Internal Gate to Source voltage)

We propose two standard biasing:

Low Noise and low consumption: Vd = 4.5V and B, D, E grounded.
All the other pads non connected (NC).
Id = 65mA & Pout-1dB = 10.5dBm Typical.
(Equivalent to B, C, D, E, F: non connected and Vd=4.5V; Vg1=Vg2=Vg3=+1.V).

Low Noise and higher output power Vd = 4.5V and B, C, F grounded.
All the other pads non connected (NC).
Id = 85mA & Pout-1dB = 13.5dBm Typical..

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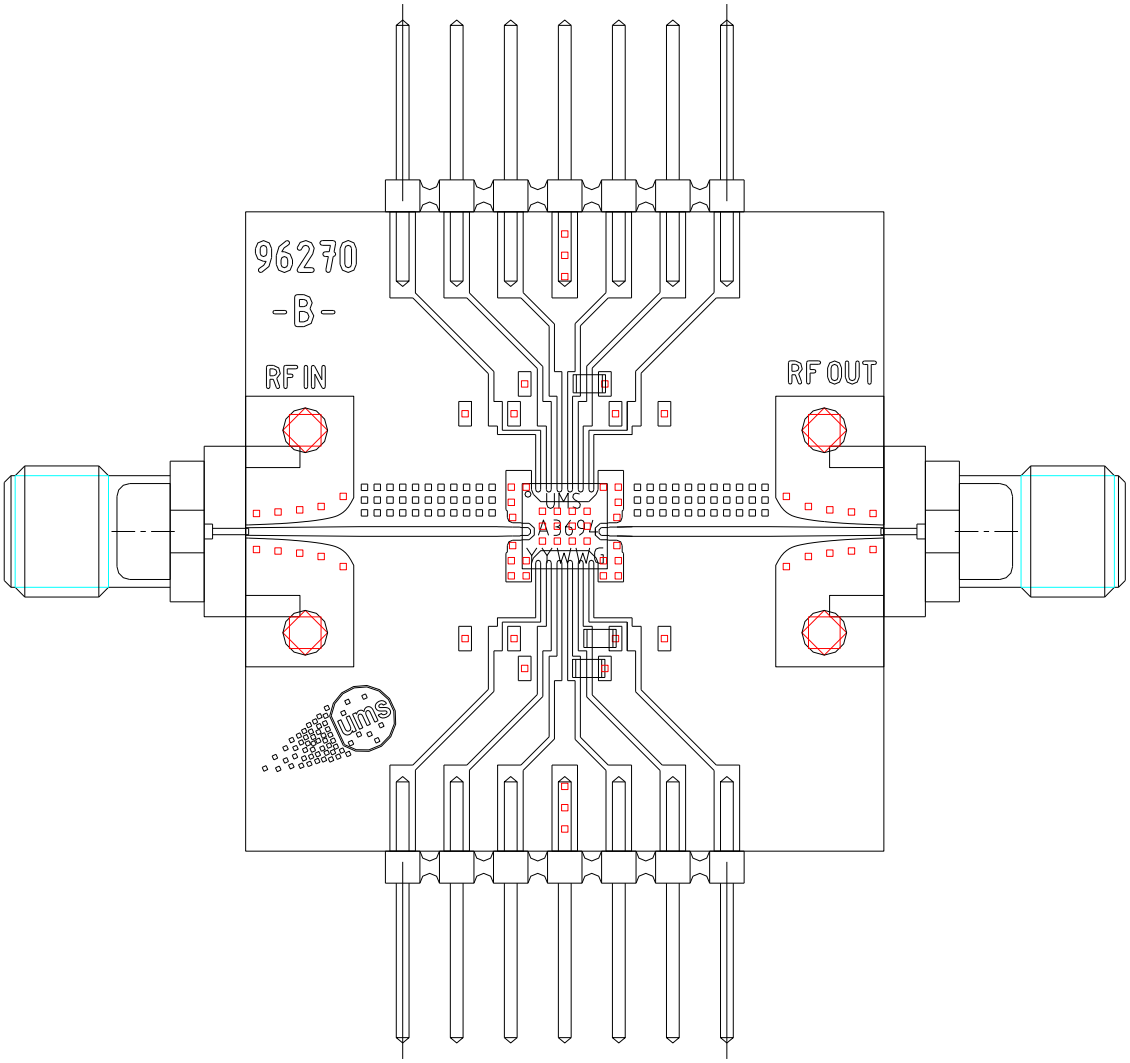
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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Notes

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

Recommended environmental management

Refer to the application note AN0019 available at https://www.ums-rf.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHA2069-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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