Chrontel CH7322B CEC

Features

- Complies with Consumer Electronic Control (CEC) version 1.3a
- Less than 10mA in full operation conditions
- Fully programmable through a two-wire serial port
- Programmable power management
- Auto Mode Technology † Supports mandatory CEC functions such as One Touch Play, Power Status etc. without software programming
- Capable of supporting full CEC features by accessing internal registers.
- Report CEC events through an interrupt and registers
- Flexible crystal frequency input between 4 and 50 MHz or external CMOS clock ranging from 1 to 100Mhz
- DDC master to obtain Physical Address
- Serial Port voltage supported from 1.8V to 5V
- Single 3.3V voltage supply
- Adjustable interrupt voltage level from 1.8V to 3.3V
- HBM up to 8KV ESD protection
- Offered in 16-pin, lead-free SSOP and QFN packages

Applications

- DVD Players
- DVD Recorders
- Digital Video Cameras
- Personal Computers
- A/V Receivers
- Digital Set-top Boxes

General Description

Chrontel's CH7322B is a low cost, low-power semiconductor device designed for HDMI systems to easily enable Consumer Electronic Control (CEC) features, which allow consumers to manage all of their HDMI CEC peripherals with just one remote control. The device's innovative approach for handling CEC message frame can help our customers to achieve their required HDMI-CEC features without programming complicated and time-consuming CEC functions using microcontroller.

To reduce CEC development complexity, the CH7322B incorporates a robust and powerful mechanism to process CEC message frames and execute some of the opcode commands. The device's advanced Auto Mode Technology† simply provides HDMI-CEC playback systems with the ability to accomplish three mandatory CEC functions – One Touch Play, Suspend and Resume without programming any of CH7322B registers. For example, when a HDMI-CEC DVD player is in standby mode and if the CEC "Set Stream Path" Opcode is received, the CH7322B will generate an interrupt signal to trigger the host controller to resume system normal operation.

More sophisticated CEC features like Deck Control, Tuner Control, Volume Adjustment and Recording Functions for AV devices can also be accomplished through programming CH7322B internal registers. Once the received CEC message frame is verified, the CH7322B will store the embedded CEC function opcode into register buffers and send an interrupt signal to notify the host controller. The system can then take an action according to the opcode command stored in the CH7322B register buffers.

The CH7322B has a master DDC interface and when the Hot Plug Signal is high, the CH7322B will automatically obtain its Physical Address in the EDID block of the HDMI Sink and keep it in the designated registers for future usage.

The CH7322B accepts a wide range of input clock frequencies that are generated from either a crystal or an external clock source for CEC command timing. This low-cost, power-saving and space-saving device is available in 16 pin lead-free SSOP and QFN packages.

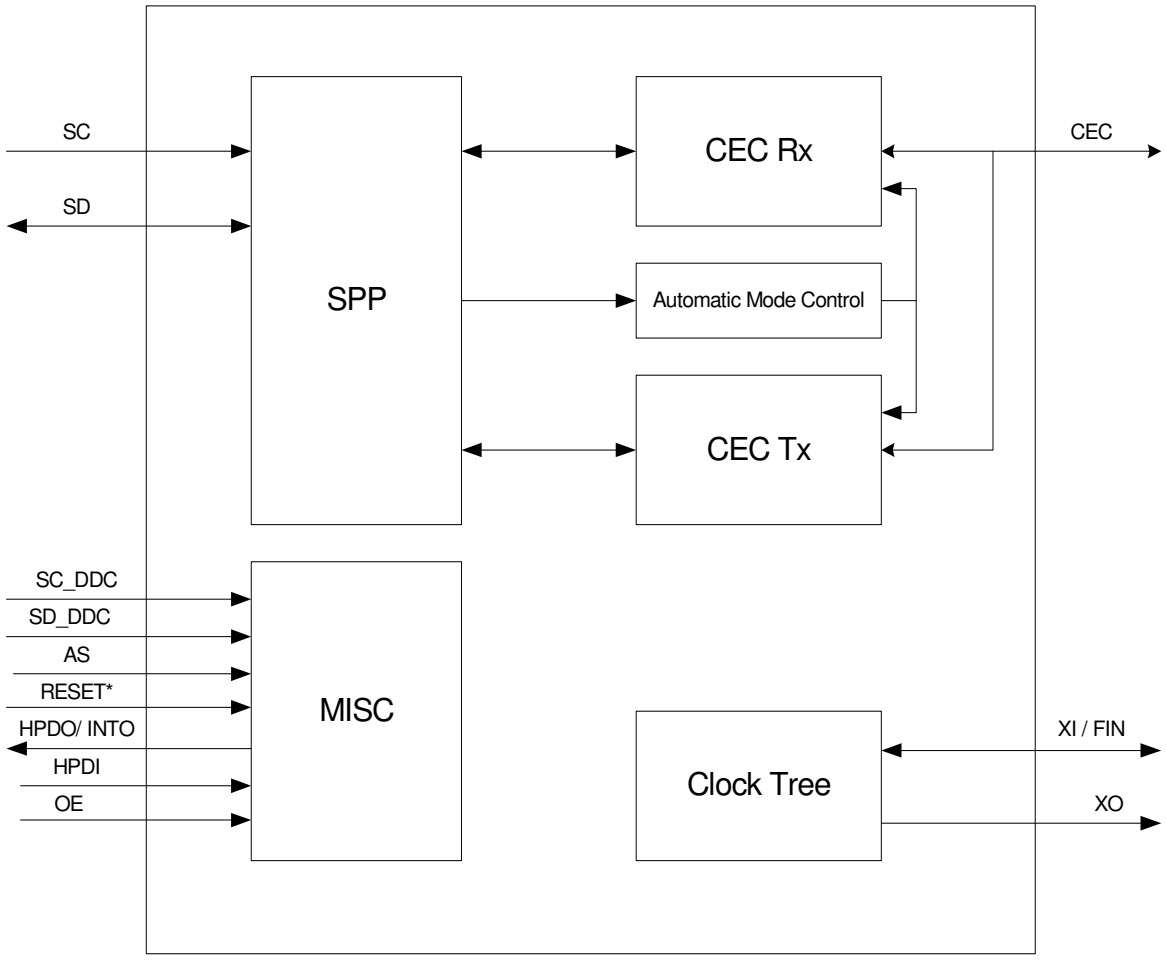

Figure 1: Functional Block Diagram

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1.0 Pin Description

Table 1: Pin Description

SSOP Pin #	QFN Pin #	Type	Symbol	Description
1	15	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (1,1,1,0,1,AS*, AS).
2	16	In	SC	**Serial Port Clock Input** This pin functions as the clock input of the serial port. This requires an external 2.2k ohm pull-up resistor. The voltage for logic 1 can be from 1.8V to 5V.
3	1	In/Out	SD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. This requires an external 2.2k ohm pull-up resistor. The voltage for logic 1 can be from 1.8V to 5V.
4	2	In	XI / FIN	**Crystal Input / External Reference Input** A parallel resonance crystal can be attached between this pin and XO. Crystal range is 4 to 50 MHz. However, an external clock can also drive the XI / FIN input and its range can be from 1 to 100 MHz.
5	3	Out	XO	**Crystal Output** A parallel resonance crystal can be attached between this pin and XI / FIN. Crystal range is 4 to 50 MHz. However, if an external CMOS clock is attached to XI / FIN, XO should be left open.
6	4	In	OE	**Output Enable (internal pull-up)** When this pin is low, it will put CH7322B into standby mode.
8	5	Out	HPDO / INTO	**Hot Plug Detect Output / Interrupt Output** This pin serves as an interrupt for device connection status. However this output pin can be programmed for other usage. Check Section 4.2 for more detail. Support CMOS logic level from 1.8V to 3.3V
10	6	In	HPDI	**Hot Plug Detect Input (internal pull-down)** This pin is used to monitor the Hot Plug detection signal. Refer to reference schematic for connectivity.
11	9	In/Out	SD_DDC	**Routed Serial Port Data to Port DDC** This pin attaches to DDC Data bus for obtaining the Physical Address from a receiver. Refer to reference schematic for connectivity.
12	10	In	SC_DDC	**Routed Serial Port Clock to Port DDC** This pin attaches to DDC Clock bus. Refer to reference schematic for connectivity.
13	11	In/Out	CEC	**CEC data Input / Output** This pin will output CEC message opcodes specified in HDMI Specification 1.3a.
14	12	In	ISET	**Current Set Resistor Input.** A 27K-ohm +/- 1% resistor should be connected between this pin and GND
15	13	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
7	7	NC	NC	**Not connect**
16	14	Power	VDD	**Supply Voltage (3.3V)**
9	8	GND	GND	**Ground**

2.0 Device Connection and General Usage

The CH7322B provides a low cost CEC solution for PCs and Consumer Electronic devices that support HDMI functions. The diagram (Figure 3) below is an example showing how CH7322B is interfacing with other components in the HDMI Source device.

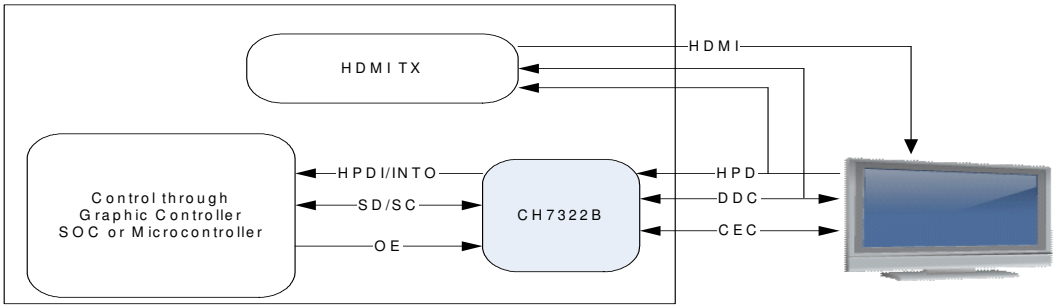

Figure 2: CH7322B Connection Block Diagram for HDMI Transmitter

When CH7322B is powered up and the Hot Plug Signal is detected, the device's DDC bus will obtain the assigned Physical Address located in the EDID block of the upstream HDMI Sink. This action will also be taken if each time the Hot Plug Signal is reasserted. To reduce the effort of CEC software developments using a microntroller, the CH7322B equips a special CEC message control mechanism to validate the incoming CEC message frame. Therefore the function opcode in the frame will be stored in the register buffers that allows system to perform the requested task. If the AV player requires only mandatory CEC functions (One Touch Play and Standby/Resume), a method called Auto Mode can be used to handle the received CEC message opcode and the CEC firmware coding may not be needed. For system manufactures prefer implementing more complicated CEC functions, the CH7322B can be switched to the Software Mode to provide a full control to all CEC function opcodes.

The devices' HPDI/INTO pin is used for generating an interrupt signal or a pulse if a CEC message frame is received and validated. This event is to notify the host controller (e.g. a SOC or a microcontroller) to retrieve the CEC function message from CH7322B's storage buffer and to execute the opcode command accordingly. Furthermore the system can return a CEC function opcode to the initiator by placing it in the CH7322B message buffer, which will be concatenated with the designation Physical Address upon the transmission.

The CH7322B can be designed into a HDMI Sink device, Figure 4 is an example of how CH7322B is connected to a HDMI Receiver. The method implemented by CH7322B for the HDMI transmitter to handle a CEC message frame can be applied to the HDMI Receiver as well. However using the Software Mode is recommended for interfacing with the HDMI Receiver. Notice the CH7322B's HPD and DDC pins do not need to be connected with a receiver chipset in this case.

The OE Pin serves as the system power status indicator. If CH7322B senses the pin is low, it will send the "Standby" message in respond to the Source Power State requested by the Sink.

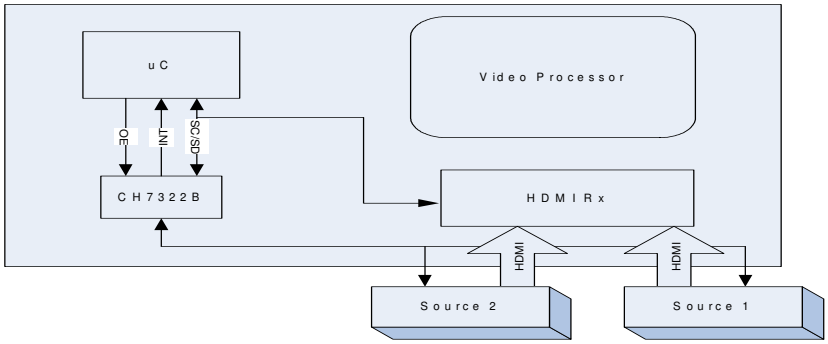

Figure 3: CH7322B HDMI Sink Connection Block Diagram

3.0 Functional Description

3.1 Overview

The CH7322B is a HDMI Consumer Electronic Control (CEC) device designed for products with HDMI capability. Common Applications include:

- Digital TV
- DVD Player
- Desktop/Portable PC
- AVR
- Set Top Box
- Game Consoles
- HDMI Switch

The CEC connection topology is assuming that a TV is the "root" of an up-side-down tree, and all AV sources are considered as "branch" or "leaf" being either directly or indirectly connected to the root. (Figure 5). The CH7322B provides an effective way to add Consumer Electronic Control (CEC) features for a global control of CEC-enabled devices in a HDMI network.

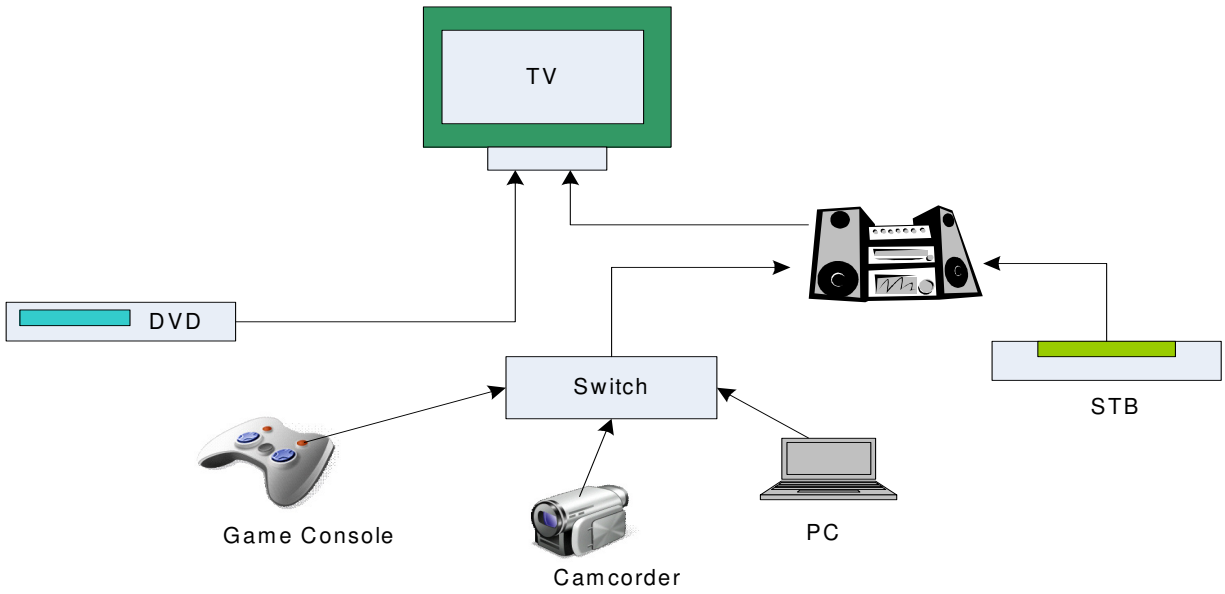

Figure 4: HDMI-CEC Network Connection

A dedicated bi-directional CEC pin on the CH7322B is used for receiving and transmitting CEC message opcodes defined in the HDMI Specification 1.3a. To handle mandatory CEC functions like the One Touch Play or the Standby/Resume , the CH7322B has incorporated a sophisticated algorithm for processing these CEC message opcodes to reduce the software development effort. The CH7322B has a register table that allows system manufactures to implement advanced CEC features, for example, controlling the TV tuner inside a HDMI Source or sending text string message to a HDMI display device that would normally require more complicated CEC message communication.

3.2 Interface Voltage Level

The CH7322B meets all electrical requirements specified in HDMI Specification 1.3a. For detail CEC bus electrical characteristic, please refer to HDMI Specification 1.3a, Supplement 1-CEC.

3.3 Hot Plug Detection and Interrupt

A HDMI receiver can be detected from the Hot Plug Signal through the HPDI pin. The HPD status will be reflected in the CH7322B register and can be retrieved through the serial port programming.

The HPDO/INTO pin, primarily served as an interrupt pin, can be programmed to support other functions:

1. In default mode, the HPDO/INTO pin is configured as the power control output. When CH7322B receives an opcode for enter/exit of standby mode, a pulse will be generated by the HPDO/INTO pin. This can be used as enter/exit global standby mode by the system.
2. The HPDO/INTO pin can be configured as a level-shifted version of the HPDI signal through programming CH7322B internal registers.
3. Through programming CH7322 registers, the HPDO/INTO pin can be configured to send an interrupt signal for detecting a Hot Plug event or receiving a new CEC opcode, etc. The interrupt signal can be a level signal that remains asserted until cleared through control registers. The interrupt signal can also be a pulse signal and the width can be modified through CH7322B registers.

The HPDO/INTO pin supports CMOS logic level from 1.8V to 3.3V. It can be programmed as active high or active low through control registers.

3.4 Power Saving

The CH7322B consumes very small amount of current and can be configured either as the normal operation mode or the power-down mode . These two modes can be switched by flipping the FPD bit on the Register 0x13.

3.5 System Power Status

One way to synchronize the power status between two connected HDMI devices is by the opcode communication through CEC line. The input pin (OE) is designed to allow the host controller to report the system's current power status. If the OE pin is low and the HDMI Sink sends an opcode to request the Source device's power state, the CH7322B in the Source will automatically reply with the "Standby" opcode.

3.6 Command Interface

The CH7322B has two sets of serial communication paths – SPP and DDC. The SPP has two wires, the SC (control clock) and SD (data) are used for controlling CH7322B internal registers. The DDC pins (SC_DDC and SD_DDC) is a master serial port interface which can be connected to an upstream Sink device for obtaining the assigned Physical Address in the Sink's EDID.

The SPP control bus is able to handle up to 1MHz when a host controller is accessing CH7322B internal registers, however a proper crystal/input clock frequency may be required. The CH7322B DDC bus serial is able to handle up to 100KHz and complies with HDMI specification 1.3a.

3.6.1 SPP

The CH7322B SPP lines, a two-wire serial bus, acting as a slave can be connected to a PC SMBus or a programmable serial port. For the SPP connecting to a SMBus on PC motherboard (Figure 12a), Chrontel has software driver to provid an access to CH7322B's register table. If the SPP is connected to a serial port of a PC grpahic controller (Figure 12b), programming CH7322B internal registers can be achieved by the software driver or the VBIOS written by a third party graphic controller vendor. In addition to PC platform, designing a CE application (12c) such as DVD/DVR or Display, the microcontoller's serial port can be used to communicate with CH7322B for enabling CEC functions. Please contact Chrontel for obtaining Chrontel for 8051 sample source codes.

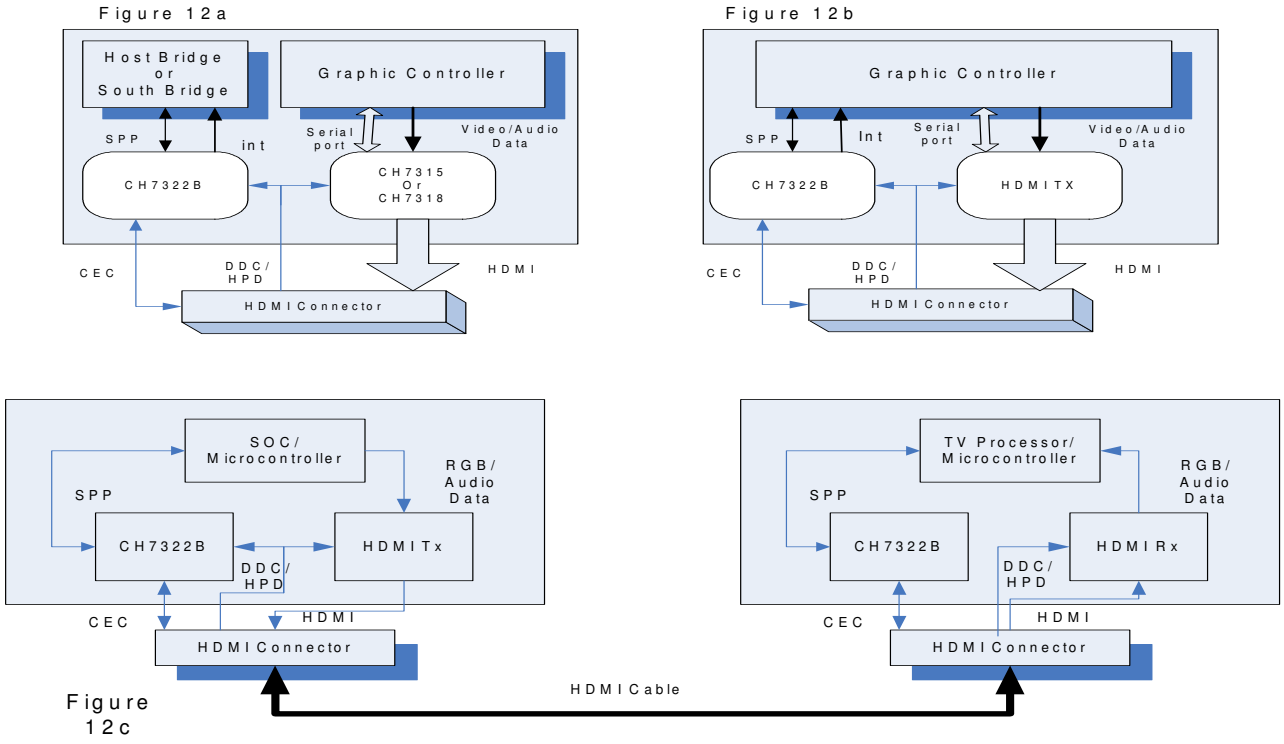

Figure 5: CH7322B SPP Connection Diagram

Because the CH7322B's SPP is designed only as slave serial interface and therefore, its serial clock line (SPC) is input only and is driven by the output buffer of the host. The serial port data line (SPD) is either input to or output from the CH7322B depending on the read/write status bit sent by the host. The Address Select (AS) pin with internal pull up is used to determine the device address of the CH7322B.

Figure 13 shows the connection of serial interface.

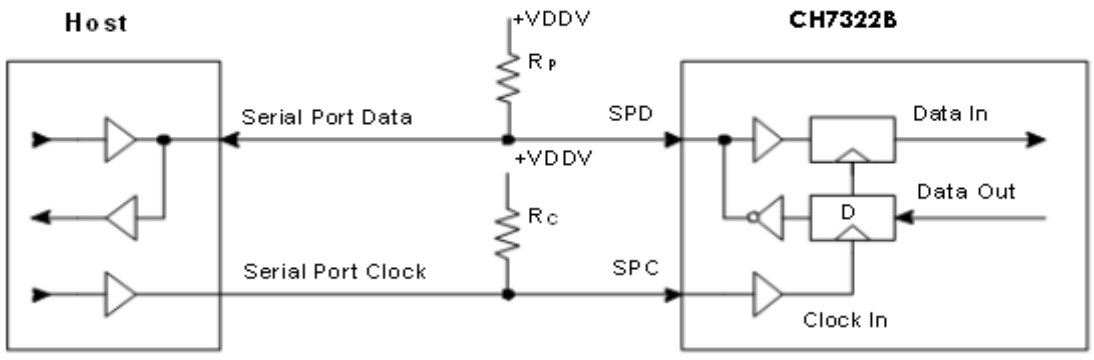

Figure 6: Serial Port Connection to a Controller

3.6.2 DDC

The CH7322B is DDC master which can read the EDID block to obtain the Physical Address assigned by the HDMI Sink (Figure 14). If the Physical Address is acquired, it will be stored in the CH7322B registers for the purpose of validating or transmitting CEC message frame. The CH7322B's SD_DDC and SC_DDC are 5V tolerant.

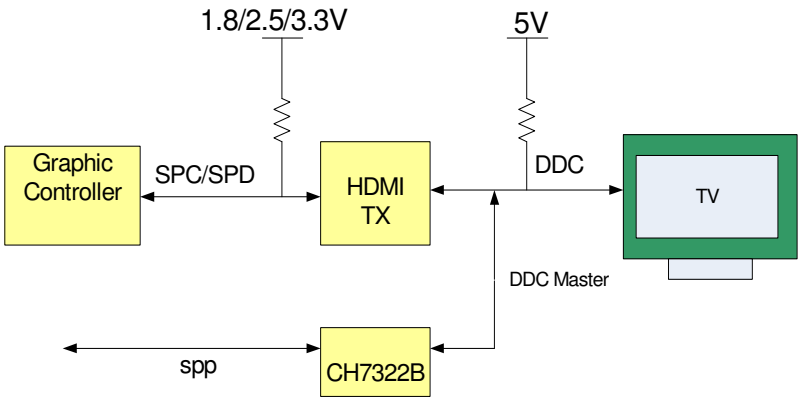

Figure 7: CH7322B DDC Bus Connection

3.7 Implementing CEC Features

Two CEC Control modes, the Auto Mode and the Software Control Mode in the CH7322B provide system vendors the flexibility to incorporate CEC feature into their design. By default, CH7322B is configured as the Auto Mode which only supports CEC mandatory features. A host controller does not need to toggle CH7322B registers for sending or responding mandatory CEC message opcodes (See Table 2), the CH7322B will acknowledge the initiator with the appropriated opcode command. However for implementing more advanced CEC functions, the Software Control Mode allows system designers to have a total control to all CEC message opcodes defined in the HDMI Specification 1.3a. The microcontroller or PC SMBus software retrieves the opcode command through the CH7322B SD/SC pins and execute it. If a system manufacture wishes to implement both CEC mandatory functions and some of CEC advanced features, the software can switch back and forth between Auto Mode and Software Mode at any time by toggling the "Software Overwrite" bit in the Register 0x5B

3.7.1 Full Auto Mode

If an AV playback device requires only mandatory CEC features, the Auto Mode is an effective solution because accessing CH7322B registers will not be necessary, therefore CH7322B's SPPs can be left open. When the AV playback device is in power-on state and the Hot Plug Signal is asserted, the CH7322B will obtain the assigned Physical Address and send the "One Touch Play" CEC message to the Sink device. In addition, the Auto Mode supports "Standby" CEC Opcode and "Set Stream Path" CEC Opcode broadcast by HDMI Receiver over the HDMI network. For details of implementing Auto Mode, please refer to Chrontel CH7322B Software Design Note.

3.7.2 Software Control Mode

Other advanced CEC features such as Deck Control, Menu Control, Remote Control Pass Through and On-screen Display can be accomplished by the Software Control Mode through programming CH7322B registers. By setting the Register 0x5B's "Software Overwrite" bit to "1", the device can be configured to allow system designers manually handling CEC message opcodes. The complexity of the software configuration will be system dependent. The detail of the register bit-mapping is listed in the Chrontel CH732B Software Design Note.

3.8 Software Support

Chrontel offers a CEC API Development Kit for software developers to incorporate partial or full CEC features into their products. Table 2 describes the CH7322B CEC control mechanism.

Table 2: CH7322B CEC Control Configuration

CEC Features	Full Auto (FA) Mode	Software Control (SC) Mode
Supported Logical Type	1 (Player Only)	Up to 6
One Touch Play	Can be triggered by re-read EDID or SPP register write	S/W generates and sends all CEC message sequences.
Routing Control	H/W response message	S/W generates and sends CEC message sequences for all Routing Control opcodes
Standby /Wakeup	H/W response message, generating power event signal	S/W can response standby and work with ACPI on PC system or uC in CE platform, H/W can also generate power event signal
General Protocol	H/W response message	S/W process CEC messages
System Information/Power Status	H/W response message	S/W process CEC message
Deck Control, Recording, User Menu Control, Remote Passthrough, Audio Control Timer, etc.	N/A	S/W read/write CEC message, and pass the remote control signal to hooked application

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	VDD power supply relative to GND	-0.5		5	V
	Input voltage of all digital pins	GND – 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 second)			260	°C
	Vapor phase soldering (11 second)			245	
	Vapor phase soldering (60 second)			225	

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VDD	Power supply voltage	3.0	3.3	3.6	V
T_{AMB}	Ambient operating temperature (Commercial / Automotive Grade 4)	0		70	°C

Electrical Specifications
(Operating Conditions: T_{AMB} = 0°C-70°C, VDD =3.3V+/- 0.3V, unless otherwise specified)

4.2.1 Supply

Symbol	Description	Min	Typ	Max	Units
I_{VDD}	Total supply current		1.9	2.2	mA
I_{PD}	Total Power Down Current		60		uA

4.2.2 DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
CEC						
C_{CEC}	CEC pin capacitance			30		pF
$I_{leak,CEC}$	CEC pin leakage when power removed				1.8	uA
$V_{OH,CEC}$	CEC output high voltage	Note 1,2,3	2.5	2.7	3.3	V
$V_{OL,CEC}$	CEC output low voltage	Note 1,2,3		0.2	0.6	V

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$V_{IH,CEC}$	CEC input high voltage threshold			1.5	2.0	V
$V_{IL,CEC}$	CEC input low voltage threshold		0.8	1.0		V
$V_{IN,hys,CEC}$	CEC input hysteresis			0.5		V
SPP (SD/SC), DDC (SD_DDC/SC_DDC, apply input specification only)						
$V_{PU,SPP}$	SPP pull up voltage		1.62		5.5	V
$V_{IH,SPP}$	SPP input high voltage threshold			1.25		V
$V_{IL,SPP}$	SPP input low voltage threshold			1.0		V
$V_{IN,hys,SPP}$	SPP input hysteresis		0.2	0.25		V
$V_{OL,SPP}$	SPP output low voltage	I_{OL}=3.0mA		0.2	0.3	V
$R_{PU,SPP}$	SPP external pull up resistor		1.1			K ohm
HPD						
$V_{MAX,HPD}$	Maximum voltage applicable to pin				5.5	V
$V_{IH,HPD}$	HPD input high voltage threshold		1.25	1.5	TBD	V
$V_{IL,HPD}$	HPD input low voltage threshold		0.9	1.1	TBD	V
$V_{IN,hys,HPD}$	HPD input hysteresis			0.4		V
$R_{PD,HPD}$	HPD internal pull down resistor			120		K ohm
HPDO/INTO						
C_L	External load Capacitance				100	pF
AS						
$V_{IH,AS}$	AS input high voltage			0.8*VDD		V
$V_{IL,AS}$	AS input low voltage			0.25*VDD		V
RESET*						
$V_{IH,RES}$	RESET* input high voltage threshold		1.2	1.5	TBD	V
$V_{IL,RES}$	RESET* input low voltage threshold		0.9	1.1	TBD	V
$V_{IN,hys,RES}$	RESET* input hysteresis			0.4		V
ISET						
R_{ISET}	External ISET resistor			27		K ohm
V_{ISET}	ISET pin voltage output			1.25		V
OE (if applicable)						
$V_{IH,OE}$	OE input high voltage threshold		1.25	1.5	TBD	V
$V_{IL,OE}$	OE input low voltage threshold		0.9	1.1	TBD	V
$V_{IN,hys,OE}$	OE input hysteresis			0.4		V

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$I_{L,OE}$	OE input low leakage current			-4		uA

Note 1: CEC pin connected to 3.3V via 27Kohm resistor. VDD=3.3V.

Note 2: CEC pin connected to 3.3V via 3Kohm resistor. VDD=3.3V.

Note 3: CEC pin connected to ground via 150Kohm resistor. VDD=3.3V.

4.2.3 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
CEC						
$t_{r,CEC}$	CEC output rise time, 10% to 90%	Note 1,2,3		50	250	uS
$t_{f,CEC}$	CEC output fall time, 90% to 10%	Note 1,2,3		3	50	uS
SPP (SD/SC), DDC (SD_DDC/SC_DDC, apply input specification only)						
t_{glitch}	Maximum pulse width for SPP input glitch suppression		50			nS
XI, XO						
f_{OSC}	Crystal Oscillator Frequency		4		50	MHz
	External Input Clock Frequency		1		100	MHz

Note 1: CEC pin connected to 3.3V via 27Kohm resistor and external 1500pF capacitor to ground. VDD=3.3V.

Note 2: CEC pin connected to 3.3V via 3Kohm resistor and external 7200pF capacitor to ground. VDD=3.3V.

Note 3: CEC pin connected to external 150pF capacitor to ground. VDD=3.3V.

5.0 Package Dimensions

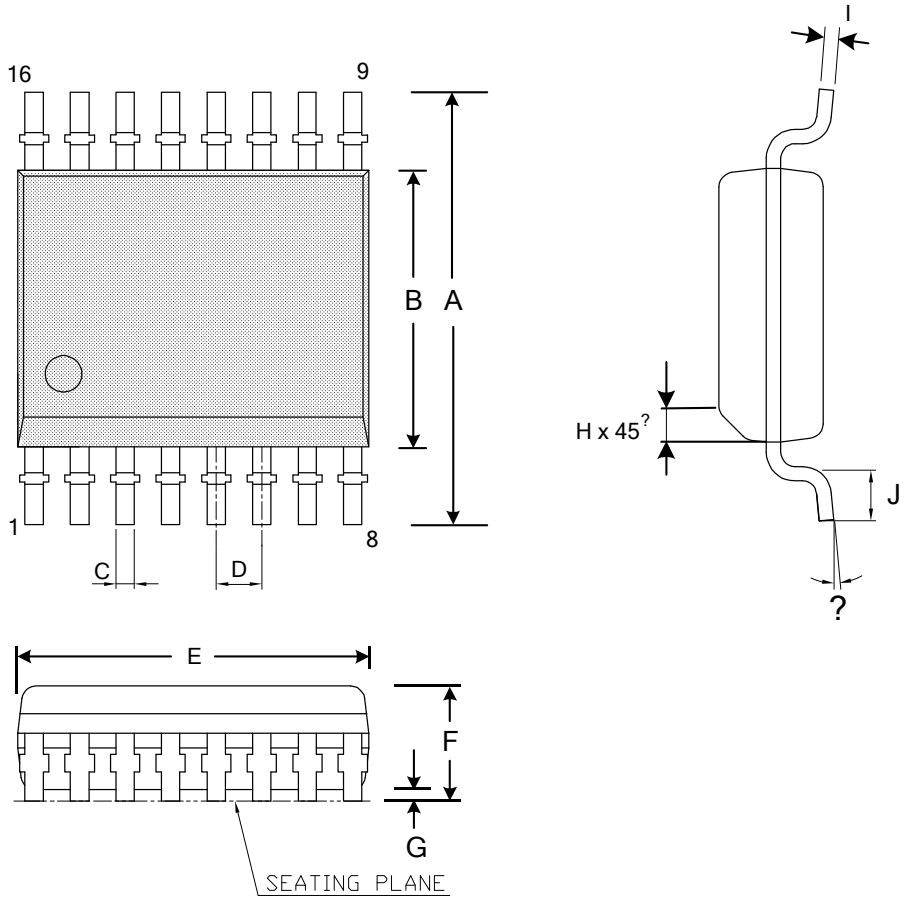

Figure 8: 16-Pin SSOP Package

Table of Dimensions

No. of Leads		SYMBOL										
16		A	B	C	D	E	F	G	H	I	J	ϕ
Milli-meters	MIN	5.80	3.80	0.20	0.635	4.70	1.35	0.10	0.25	0.18	0.40	0°
	MAX	6.20	4.00	0.30		5.10	1.75	0.25	0.50	0.25	1.27	8°

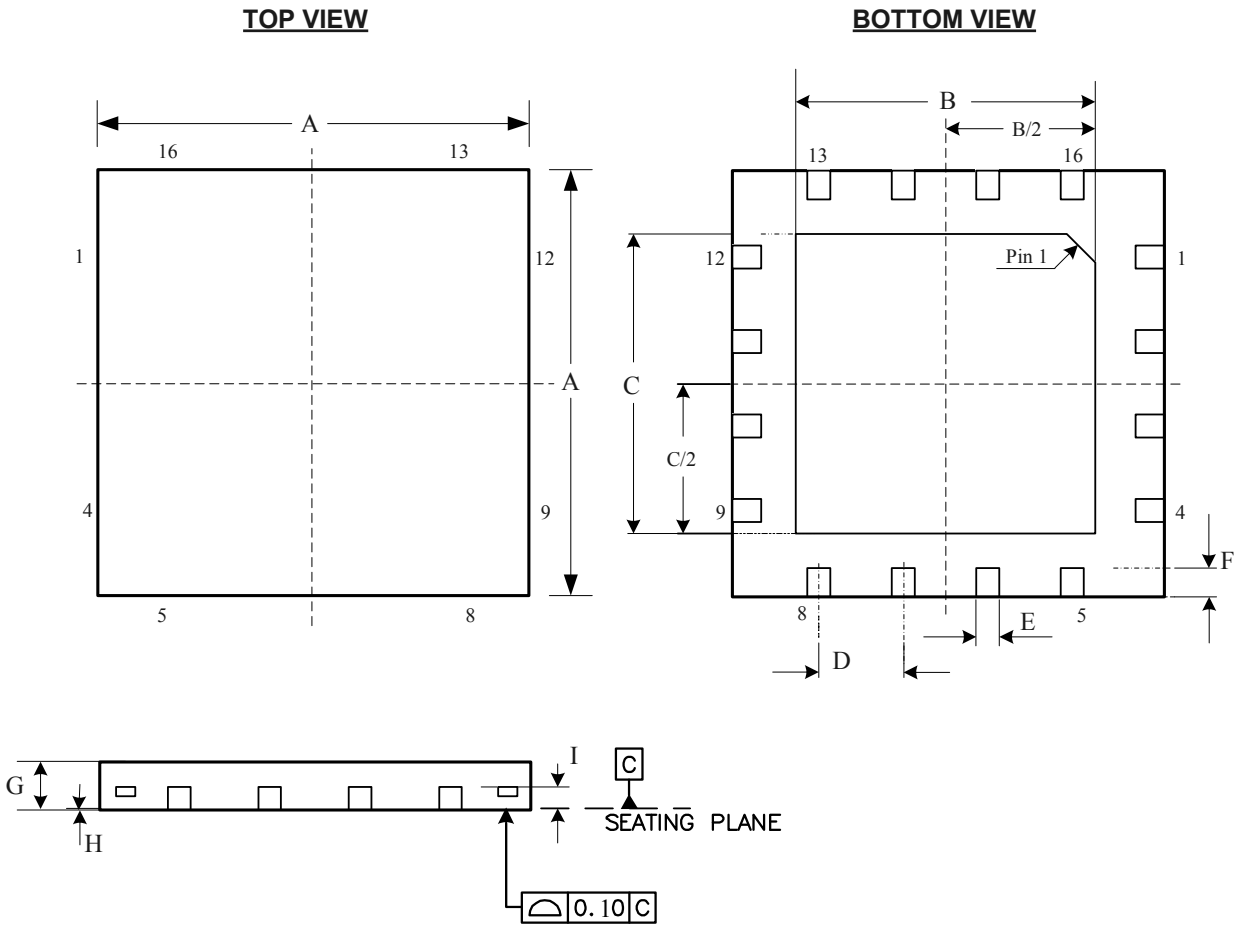

Figure 9: 16 Pin QFN Package (4 x 4 mm)

Table of Dimensions

No. of Leads		SYMBOL								
16 (4 X 4 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	3.90	2.40	2.40	0.65	0.25	0.30	0.70	0	0.203
	MAX	4.10	2.60	2.60		0.35	0.50	0.80	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

6.0 Revision History

Table 3: Revision History

Rev. #	Date	Section	Description
1.1	2/24/2009	All	Official release.
1.2	6/29/2009	Features	8KV ESD protection spec added
1.3	12/17/2009	4.2.1	I_{VDD} updated
1.4	4/11/2013	4.2.1	I_{VDD} and IP_D updated
1.5	1/7/2014	4.2	The maximum value of T_{AMB} from 85°C to 70°C.
1.6	1/15/2014	4.2	Operating Conditions for T_{AMB} corrected
2.0	9/10/2015	1.2, 5.0	QFN Package added

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ORDERING INFORMATION

Part Number	Package Type	Number of Pins	Voltage Supply
7322BMF	Lead Free SSOP	16	3.3V
7322BMF-TR	Lead Free SSOP in Tape & Reel	16	3.3V
7322BBF	Lead Free QFN	16	3.3V
7322BBF-TR	Lead Free QFN in Tape & Reel	16	3.3V

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