Chrontel

CH7214A USB Type C Logic Controller

FEATURES

- Compliant with USB Type-C Cable and Connector Specification Revision 1.2
- Compliant with the latest Power Delivery Specification Revision 2.0, Version 1.1
- Supports VESA DisplayPort Alt. Mode 1.0a
- Bi-directional conversion between the HPD signal and Power Delivery VDM
- Support DisplayPort AUX CH DC voltage level detection
- USB Type-C SBU and DisplayPort AUX CH Switch integrated
- Configurable USB Type-C Ports. Device can be designed with Type-C plug or Type-C receptacle connector. CC logic and Power Delivery protocol support one sink port and one charging port
- Rp and Rd resistors for DFP/UFP/DRP integrated together with the Ra termination resistor for VCONN Powered Accessory
- Support up to 5V@3A USB Type-C Current and Source Power Rules defined in USB PD Specification Revision 2.0, Version 1.2 in Source role.
- Support Dead Battery
- Support CDP and DCP mode of Battery Charging Specification Revision 1.2
- Support Type-C plug orientation detection
- Integrated USB Billboard Class, Version 1.21 for supporting USB Type-C Alt. Mode
- GPIO/I2C/SPI/UART control interface with external component.
- VCONN power supply supported, with 5V to 3.3V and 3.3V to 1.2V Regulator integrated to save the BOM cost
- Power charging control output support
- Embedded MCU to handle the control logic
- Support device boot up by loading firmware from On Chip Flash automatically
- IIC slave interface and USB 2.0 interface are available for firmware update and debug
- Crystal free
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 40-Pin QFN (5 x 5 mm)

APPLICATION

- USB Type-C Docking Device
- USB Type-C to Multi-video adapter
- USB Power Charge Controller

GENERAL DESCRIPTION

Chrontel's CH7214A is a low cost USB Type-C logic controller. The device is targeted for system designers implementing USB Type-C devices with DisplayPort capabilities and USB Power Delivery 2.0 support. The CH7214A integrates the USB Type-C plug orientation and attached detection mechanism on the CC (Channel Communication) pins. Its robust Power Delivery 2.0 module using the BMC protocol can enable USB Type-C devices operating in various power management roles including Consumer, Provider and Power Role Swap. CH7214A also supports the battery charging with specification revision 1.2.

The DisplayPort Alt. mode is another alternative interface supported in the CH7214A. A built-in Billboard Class can be automatically exposed to the USB 2.0 D+/- bus if a Type-C PD Source (DFP) does not equip USB Type-C Alt. Mode features that support DisplayPort signal transmission. The CH7214A's bi-directional signal converter for the DisplayPort HPD (hot plug detection) and VDM (Vendor Defined Message) is capable of translating the HPD to the appropriated VDM to Type-C DP device and vice versa. In addition to hardware support of PHY and Link layers, the CH7214A has an internal microprocessor to handle the cable logic communication and can be programmed for customization according to the application of USB Type-C platforms

In order to save the BOM cost of the end product such as cable, the CH7214A also integrates all necessary components and circuits, such as LDO, clock generation, isolation circuit, R_a, R_d and R_p etc.
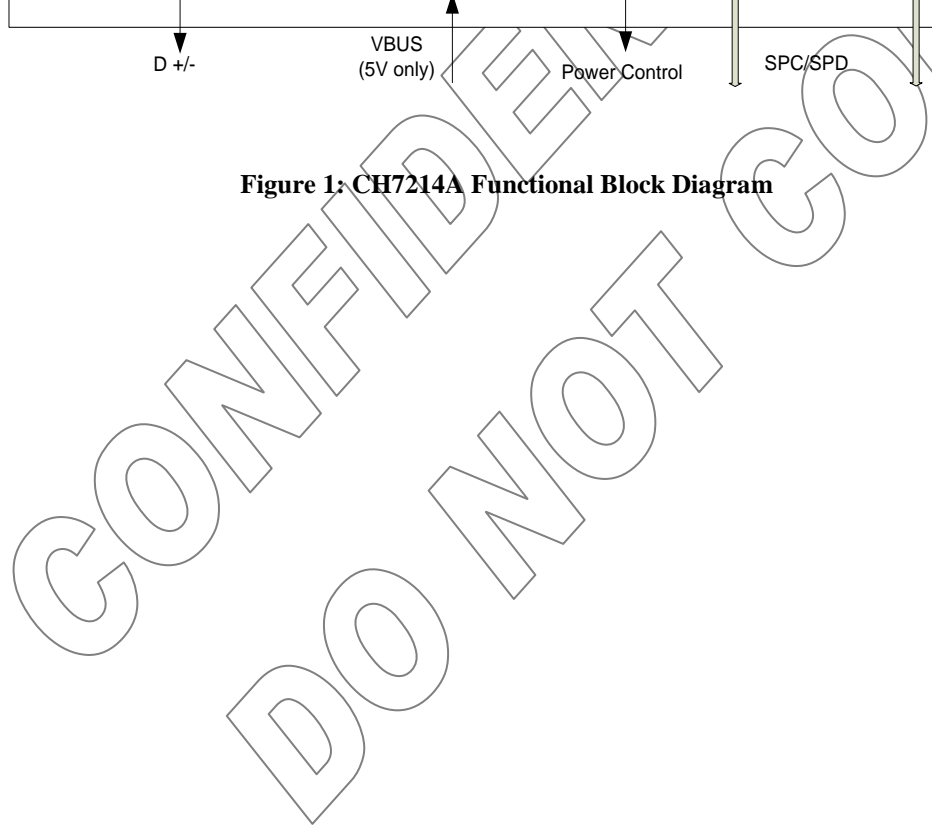
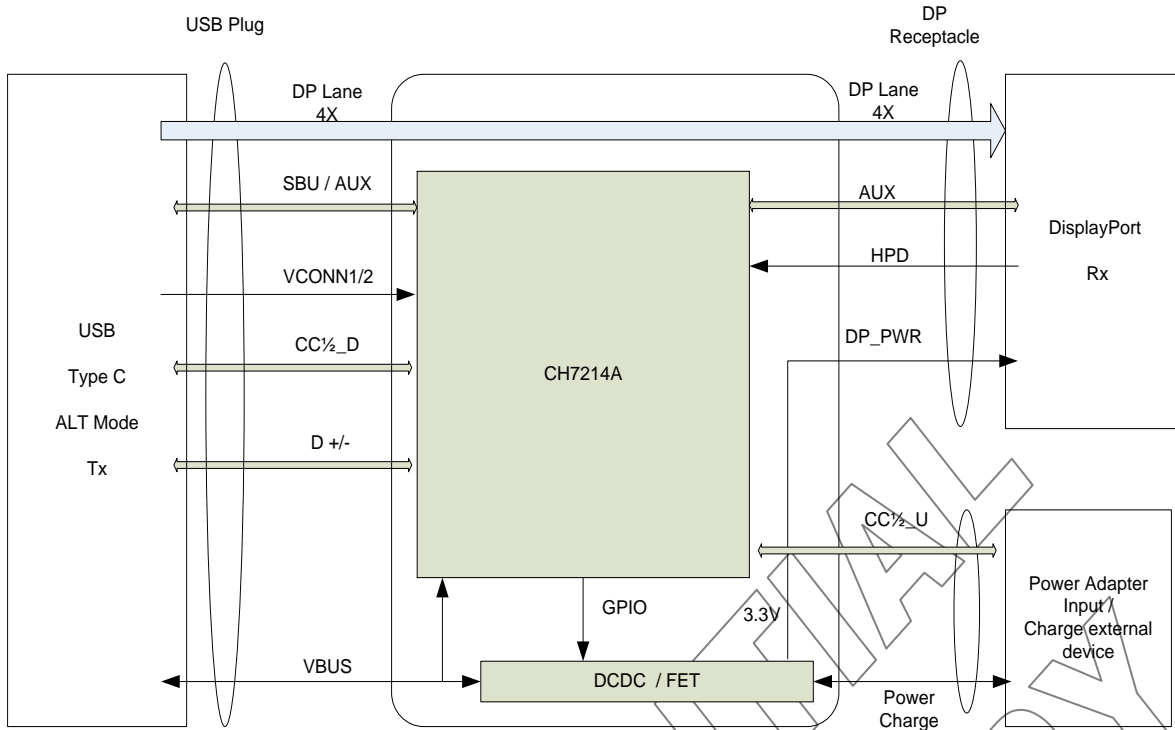**Figure 1: CH7214A Functional Block Diagram**

Figure 2: CH7214A USB to DP + Power Charge Docking Station Block Diagram
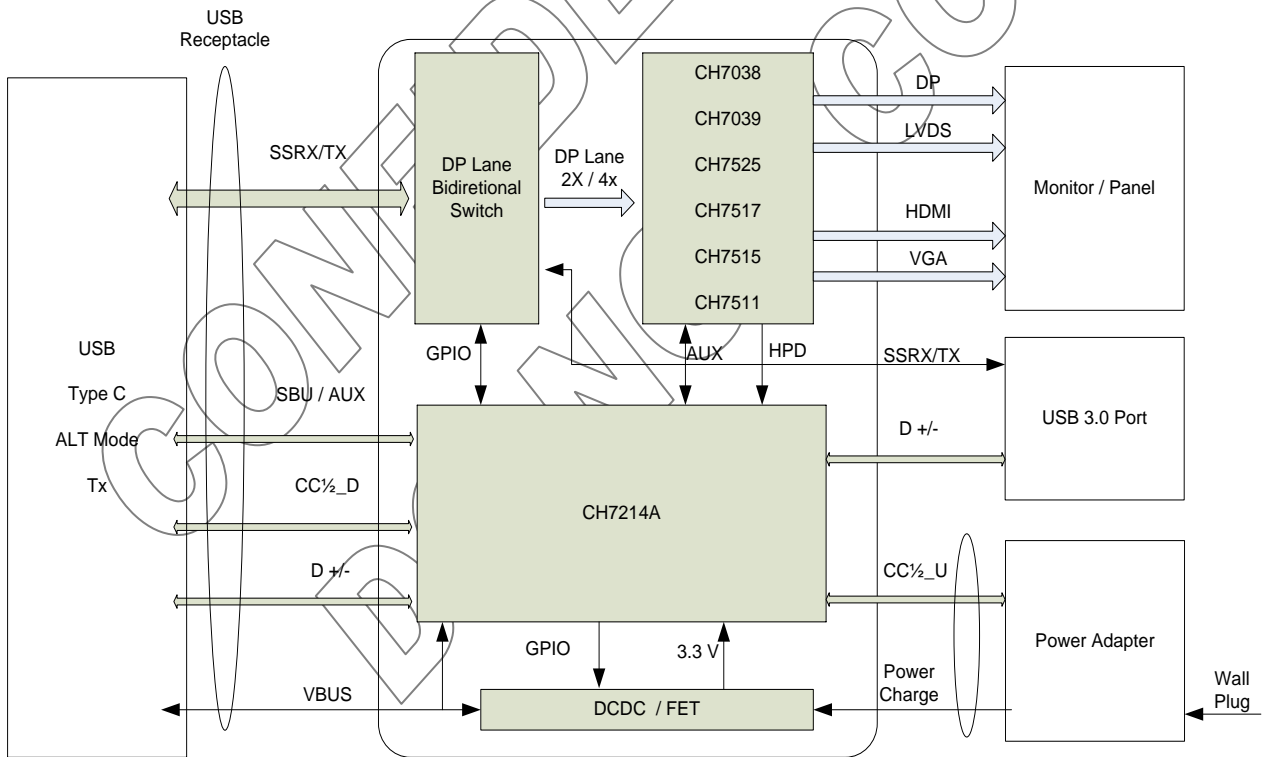

Figure 3: CH7214A USB to Multi-video interfaces + U3 + Power Charge Station Block Diagram
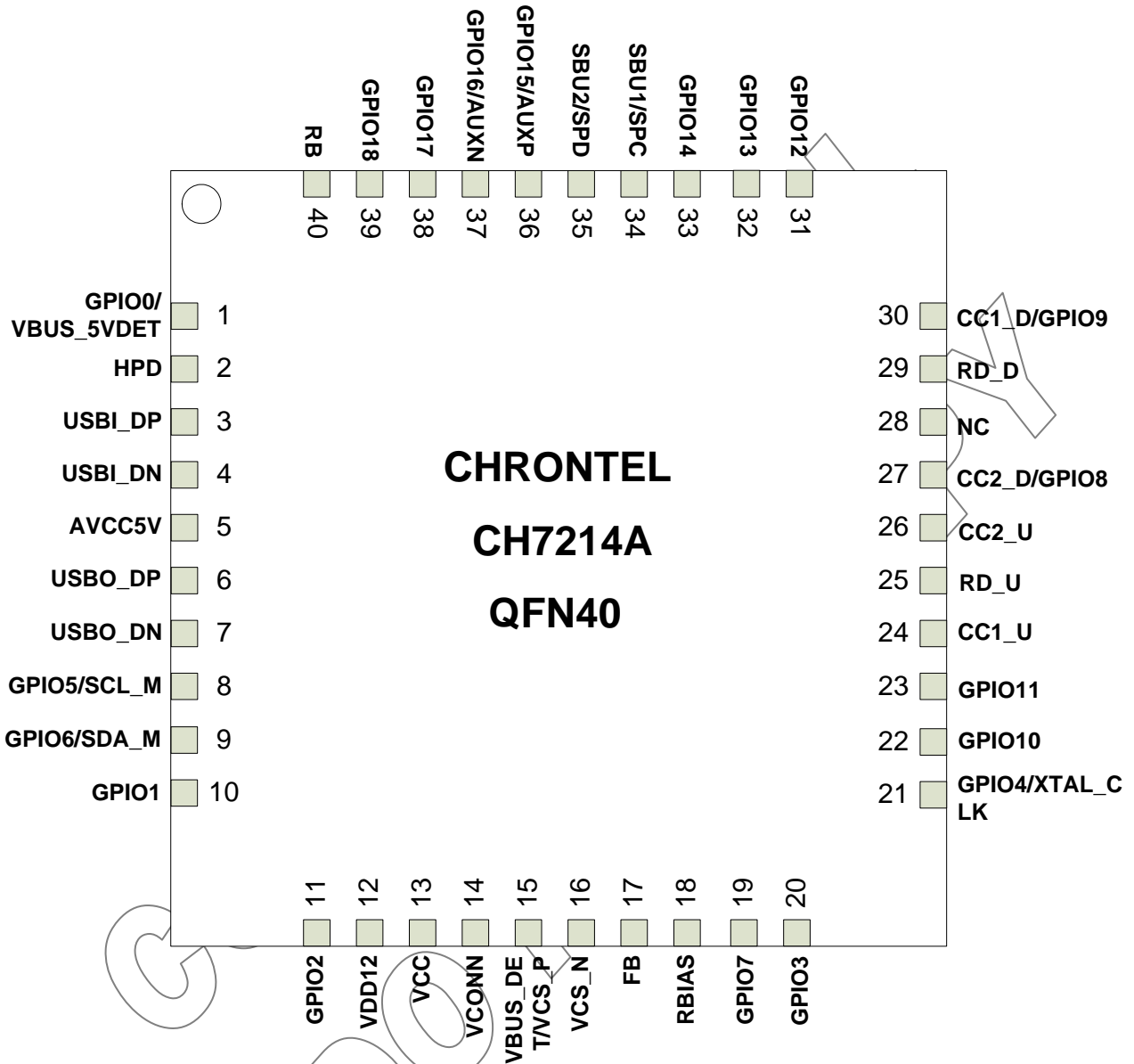
1.0 PIN-OUT

1.1 Package Diagram

Figure 4: CH7214A 40 pin QFN Pin Out

1.2   Pin Description

Table 1: QFN 40 Pin Description

Pin #	Type	Symbol	Description
1	I/O	GPIO0	**General Purpose Input/Output**
	I	VBUS_5VDET	**5V-only VBUS Detection**
2	I/O	HPD	**DisplayPort HPD**
3	I/O	USB_DP	**USB Billboard Positive Data Line**
4	I/O	USB_DN	**USB Billboard Negative Data Line**
5	I/O	USBO_DP	**USB Switch Positive Data Line**
6	I/O	USBO_DN	**USB Switch Negative Data Line**
8	I/O	GPIO5	**General Purpose Input/Output**
	O	SCL_M	**I2C Master Serial Port Clock** This pin requires a pull-up 1.8kΩ Resistor to the desired voltage level.
9	I/O	GPIO6	**General Purpose Input/Output**
	I/O	SDA_M	**I2C Master Serial Port Data** This pin requires a pull-up 1.8kΩ Resistor to the desired voltage level.
10,11,19,20,22,23,31,32,33,38,39	I/O	GPIO[3:1],GPIO7,GPIO[14:10],GPIO18,GPIO19	**General Purpose Input/Output**
15	I	VBUS_DET	**Scaled Input for VBUS Voltage Level Detection**
	I	VCS_P	**Scaled Input for VBUS Current Sense**
16	I	VCS_N	**Scaled Input for VBUS Current Sense**
17	O	FB	**Feedback Control to External DC-DC**
18	I	RBIAS	**Analog Reference Resistor** External resistor is 10K with 1% accuracy
21	I/O	GPIO4	**General Purpose Input/Output**
	I	XTAL_CLK	**27MHz Clock Input for LC Production Trimming**
24	I/O	CC1_U	**Upstream Type-C Port Configuration Channel 1**
25	I	RD_U	**Upstream Type-C Port CC1_U Rd Connection;**
26	I/O	CC2_U	**Upstream Type-C Port Configuration Channel 2**
27	I/O	GPIO8	**General Purpose Input/Output**
	I/O	CC2_D	**Downstream Type-C Port Configuration Channel 2**
28	NC	NC	**Not Connected**
29	I	RD_D	**Downstream Type-C Port CC1_D Rd Connection;**
30	I/O	GPIO9	**General Purpose Input/Output**
	I/O	CC1_D	**Downstream Type-C Port Configuration Channel 1**
34	I	SPC	**I2C Slave Serial Port Clock Input** External pull-up 6.8 kΩ Resistor is required.
	I/O	SBU1	**USB Type-C Sideband Use 1**
35	I/O	SPD	**I2C Slave Serial Port Data Input / Output** External pull-up 6.8 kΩ Resistor is required.
	I/O	SBU2	**USB Type-C Sideband Use 2**

| 36	I	AUXP	**DisplayPort Positive AUX CH**
	I/O	GPIO15	**General Purpose Input/Output**
37	I	AUXN	**DisplayPort Negative AUX CH**
	I/O	GPIO16	**General Purpose Input/Output**
40	I	RB	**Chip Reset** Low to 0V for reset. Typical High level is 3.3V
7	PWR	AVCC5V	**5V Power Supply for USB**
12	PWR	VDD12	**Digital Power Supply(1.2V)**
13	PWR	VCC	**3.3V Power Supply**
14	PWR	VCONN	**Vconn Power Supply** These pins connect to VCONN of the plug on the other side of the USB Type-C cable. (2.7 V to 5.5 V)
thermal pad		AVSS	**Ground**

2.0 PACKAGE DIMENSION

TOP VIEW   **BOTTOM VIEW**
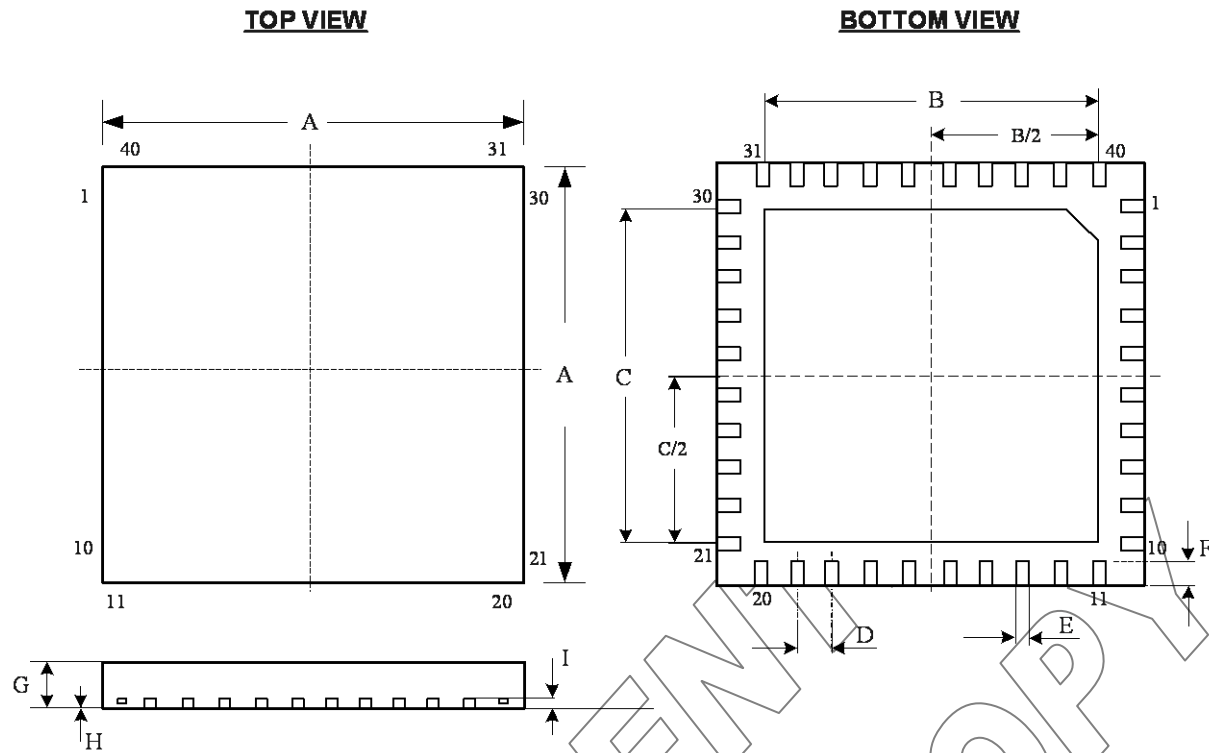
Figure 5: 40 Pin VQFN Package

Table 4: Table of Dimensions

No. of Leads		SYMBOL								
40 (5 X 5 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	4.90	3.20	3.20	0.4	0.15	0.35	0.70	0	0.203
	MAX	5.10	3.40	3.40		0.25	0.45	0.80	0.05	REF

Notes:
1. Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7214A-BF	40 QFN, Lead-free	Commercial : 0 to 70°C	**490/Tray**

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