# 8 Enhanced USB single-chip CH552, CH551

Manual

Version: 1

http://wch.cn

## 1 Overview

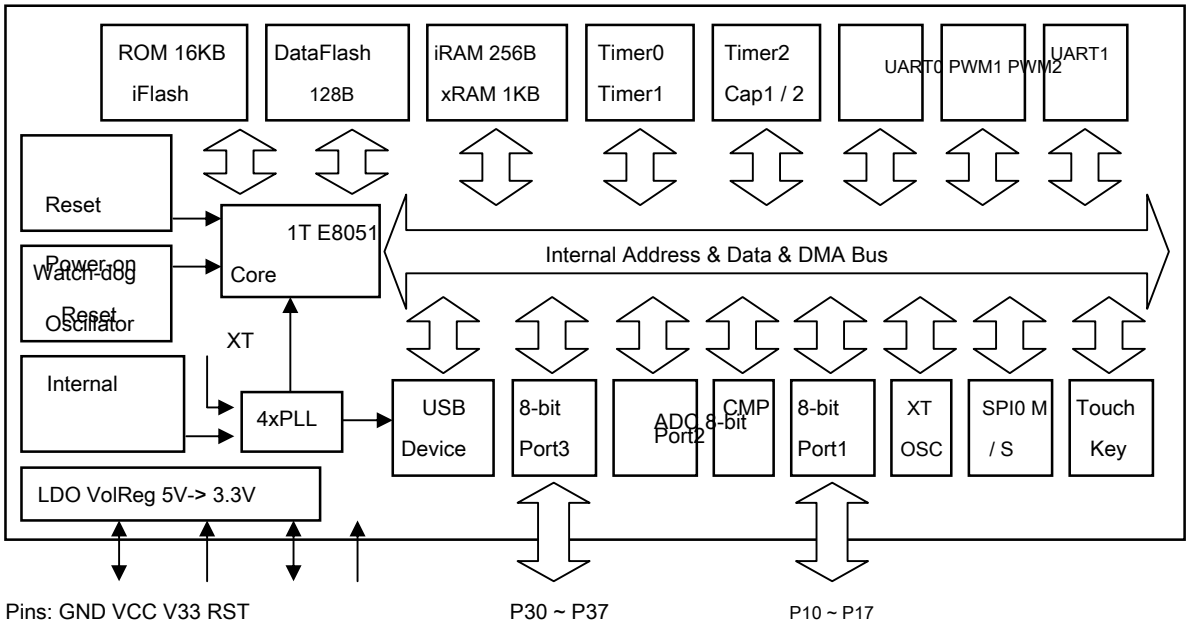
CH552 chip is a microcontroller core E8051 compatible MCS51 enhanced instruction set that 79% of single-byte instructions are single cycle instructions, instruction average velocity MCS51 8 to 15 times faster than the standard.

CH552 system supports up to 32MHz frequency, built 16K bytes of program memory ROM and 256 bytes of internal iRAM 1K and the inner sheet xRAM, xRAM supports direct memory access DMA.

CH552 built ADC analog to digital converter, a capacitance detection touch key, group 3 and the PWM signal acquisition and timers, dual asynchronous serial interface, SPI, USB full-speed device controller and transceiver function modules.

CH551 to CH552 is a simplified version, only program memory ROM 10K, the sheet xRAM only 512 bytes, only asynchronous serial UART0 provided, only SOP16 package, and removes the ADC analog to digital conversion module and a USB type-C module in addition addition to the above difference with the same CH552, CH552 direct reference manuals and information.

The following is an internal block diagram CH552 for reference purposes only.




## 2. Features

- Core: Enhanced E8051 core MCS51 compatible instruction set which 79% of single-byte instructions are single cycle instructions, instruction average Faster than standard MCS51 8 ~ 15 times, specific data XRAM fast copy instruction, dual DPTR pointer.
- ROM: 16KB capacity reprogrammable non-volatile memory ROM, may all be used to program memory space; or may be divided And a program storage area for the 2KB 14KB boot code BootLoader / ISP program area.
- DataFlash: 128 bytes of data can be repeatedly rewritable nonvolatile memory, support rewriting data in bytes.
- RAM: 256 bytes of internal iRAM, can be used for temporary storage and fast data stack; 1KB inner sheet xRAM, may be used in large amounts According to scratch and DMA Direct Memory Access.
- USB: Embedded USB transceiver and the USB controller support the USB-Device device mode, supports USB type-C master-slave detection, Support USB 2.0 full-speed 12Mbps or low-speed 1.5Mbps. Supports up to 64-byte packets, the FIFO built, support DMA.
- Timer: 3 sets a timer, T0 / T1 / T2 standard MCS51 timer.

l Capture: Timer T2 extended to support 2-channel signal capture.

l PWM: PWM outputs 2, PWM1 / PWM2 2 8-bit PWM output.

l UART: 2 groups of asynchronous serial ports, support higher baud rate, UART0 standard MCS51 serial port.

l SPI: SPI controller built-in the FIFO, up to half the clock frequency of the system frequency Fsys with serial data input and output

Simplex multiplexing, supports Master / Slave mode from the master.

l ADC: 4 channel 8-bit A / D analog-digital converter, a voltage comparator support.

l Touch-Key: 6-channel capacitive sensing, supports up to 15 touch keys, support independent timer interrupt.

l GPIO: GPIO pins support up to 17 (inclusive XI / XO and RST signal pins and USB).

l Interrupt: Support group interrupt signal source 14, including a standard group 6 MCS51 compatible interrupt (INT0, T0, INT1, T1,

UART0, T2), and an extended set of 8 interrupt (SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG), wherein the GPIO interrupts may be selected from seven pins.

l Watch-Dog: 8-bit watchdog timer preset WDOG, support the timer interrupt.

l Reset: reset signal supports four source, and internal power-on reset, reset and watchdog timeout support software reset, optional outer pin

Reset input unit.

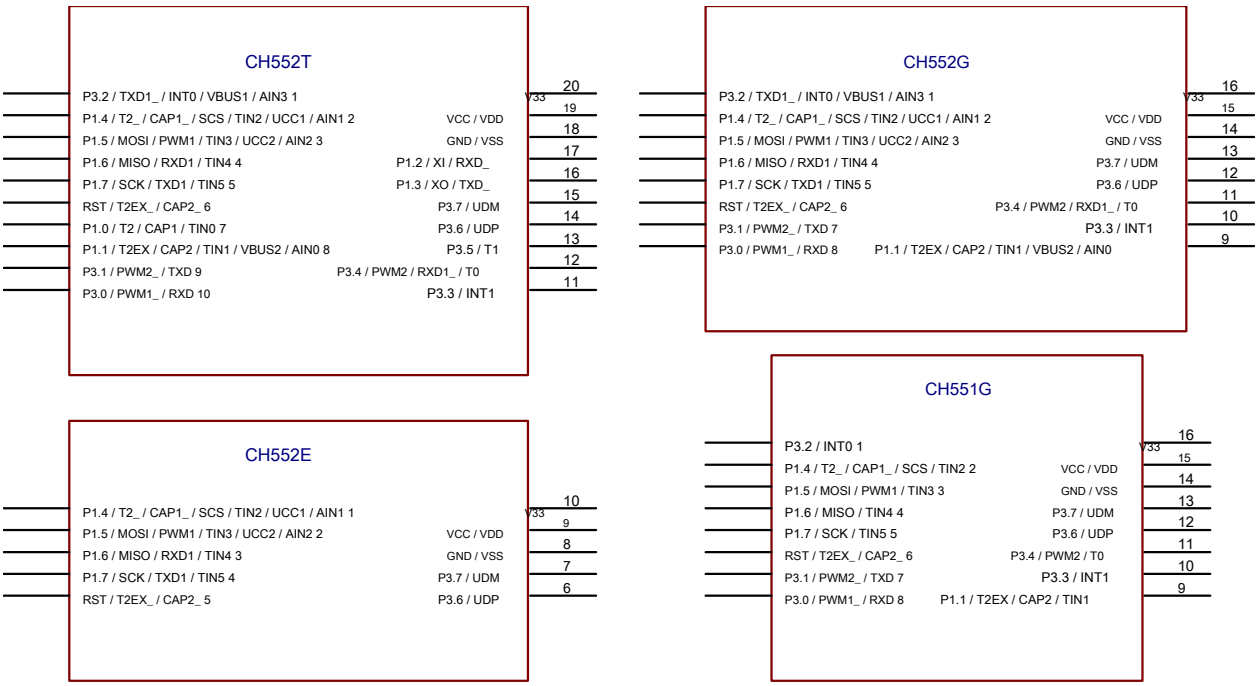
l Clock: Built 24MHz clock source, may be supported by multiplexing GPIO pin external crystal.

l Power: low-dropout voltage regulator 5V to 3.3V, 3.3V, or even support 2.8V 5V supply voltage. Support low power

Loss of sleep, support for USB, UART0, UART1, SPI0 as well as some external GPIO wake.

l Chip built a unique ID number.

## 3, the package




| Package | Width of plastic | | Lead pitch | | Package Description | Ordering |
|---|---|---|---|---|---|---|
| TSSOP-20 | 4.40mm | 173mil | 0.65mm | 25mil thin compact 20-pin SMD CH552T | | |
| SOP-16 | 3.9mm | 150mil | 1.27mm | 50mil | Standard 16-pin SMD | CH552G |
| MSOP-10 | 3.0mm | 118mil | 0.50mm | 19.7mil Miniature 10-pin SMD CH552E | | |
| SOP-16 | 3.9mm | 150mil | 1.27mm | 50mil | Standard 16-pin SMD | CH551G |

## 4 pin

| lead Pin number | | | Pin | Other features Name | Other Functional Description |
|---|---|---|---|---|---|
| TSSOP20 | SOP16 | MSOP10 | name | (Left function priority) | |
| 19 | 15 | 9 | VCC | VDD | Power input, requires an external power supply decoupling capacitor 0.1uF. |
| 20 | 16 | 10 | V33 | | USB internal regulator power output and the internal USB power input, when the power supply is connected the VCC input voltage is less than 3.6V external power supply, external power supply decoupling capacitor 0.1uF when the supply voltage is greater than 3.6V |
| 18 | 14 | 8 | GND | VSS | Common ground. |
| 6 | 6 | 5 | RST | RST / T2EX_ / CAP2_ Suffix underlined pin mapping of the same name is not underlined pins. | RST pin pull-down resistor; other GPIO default pull-up resistor. RST reset input. T2: timer / counter external count input / output 2 clocks. T2EX: timer / counter reload 2 / capture input. CAP1, CAP2: timer / counter 1 input 2 capture. TIN0 ~ TIN5: 0 # ~ 5 # capacitance detection touch key input channel. AIN0 ~ AIN3: 0 # ~ 3 # channel ADC analog signal input. UCC1, UCC2: USB type-C two-way channel configuration. VBUS1, VBUS2: USB type-C bus voltage sense input. XI, XO: external crystal oscillator input terminal, an inverting output terminal. RXD, TXD: UART0 serial data input and serial data output. SCS, MOSI, MISO, SCK: SPI0 interfaces, SCS is the chip select input, MOSI output host / slave input, MISO host input / output slave, SCK is a serial clock. PWM1, PWM2: PWM1 output, PWM2 output. RXD1, TXD1: UART1 serial data input and serial data output. INT0, INT1: External Interrupt 0, external interrupt 1 input. T0, T1: timer 0, timer 1 external input. UDM, UDP: D-, D + signal terminal of the USB device. Note: P3.6 and P3.7 V33 as the internal I / O power supply, the high level only to the input and output voltage V33 does not support 5V |
| 7 | - | - | P1.0 | T2 / CAP1 / TIN0 | |
| 8 | 9 | - | P1.1 | T2EX / CAP2 / TIN1 / VBUS2 / AIN0 | |
| 17 | - | - | P1.2 | XI / RXD_ | |
| 16 | - | - | P1.3 | XO / TXD_ | |
| 2 | 2 | 1 | P1.4 | T2_ / CAP1_ / SCS / TIN2 / UCC1 / AIN1 | |
| 3 | 3 | 2 | P1.5 | MOSI / PWM1 / TIN3 / UCC2 / AIN2 | |
| 4 | 4 | 3 | P1.6 | MISO / RXD1 / TIN4 | |
| 5 | 5 | 4 | P1.7 | SCK / TXD1 / TIN5 | |
| 10 | 8 | - | P3.0 | PWM1_ / RXD | |
| 9 | 7 | - | P3.1 | PWM2_ / TXD | |
| 1 | 1 | - | P3.2 | TXD1_ / INT0 / VBUS1 / AIN3 | |
| 11 | 10 | - | P3.3 | INT1 | |
| 12 | 11 | - | P3.4 | PWM2 / RXD1_ / T0 | |
| 13 | - | - | P3.5 | T1 | |
| 14 | 12 | 6 | P3.6 | UDP | |
| 15 | 13 | 7 | P3.7 | UDM | |

## 5, the SFR

In this manual The register is described The following abbreviations may be used later when:

| abbreviation | description |
|---|---|
| RO | It represents the type of access: Read-only |
| WO | Represents Access Type: Write-only, read values are invalid |
| RW | It represents Access Type: readable and |
| writable H | Its end represents a hexadecimal number B |
| | Its end represents a binary number |

About 5.1 SFR and address distribution

CH552 using the SFR control, management device, and set the operating mode.

80h-FFh occupied SFR address range of the internal data memory space, accessible only via a direct address instruction mode. Wherein the address register x0h or x8h is bit addressable, so as to avoid access to a specific bit value of bits sometimes modify other; other non-multiple of 8 address registers can only be accessed by byte.

Data can be written only SFR portion in safe mode, while in non-secure mode is read-only status, for example: GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL.

SFR portion having one or more aliases, for example: SPI0_CK_SE / SPI0_S_PRE. Part of the address corresponding to a plurality of individual SFR, for example: SAFE_MOD / CHIP_ID, ROM_CTRL / ROM_STATUS. CH552 comprising standard SFR registers 8051, while increasing the other control registers. Specific SFR in the table below.

table 5 .1 Special Function can Register Table

| SFR | 0,8 | 1,9 | 2, A | 3, B | 4, C | 5, D | 6, E | 7, F |
|---|---|---|---|---|---|---|---|---|
| 0xF8 | SPI0_STAT | SPI0_DATA | SPI0_CTRL | SPI0_CK_SE SPI0_SETUP | SPI0_S_PRE | | RESET_KEEP | WDOG_COUNT |
| 0xF0 | B | | | | | | | |
| 0xE8 | IE_EX | IP_EX | UEP4_1_MOD | UEP2_3_MOD | UEP0_DMA_L | UEP0_DMA_H | UEP1_DMA_L | UEP1_DMA_H |
| 0xE0 | ACC | USB_INT_EN | USB_CTRL | USB_DEV_AD | UEP2_DMA_L | UEP2_DMA_H | UEP3_DMA_L | UEP3_DMA_H |
| 0xD8 | USB_INT_FG | USB_INT_ST | USB_MIS_ST | USB_RX_LEN | | UEP0_CTRL | UEP0_T_LEN | UEP4_CTRL | UEP4_T_LEN |
| 0xD0 | PSW | UDEV_CTRL | UEP1_CTRL | UEP1_T_LEN | UEP2_CTRL | UEP2_T_LEN | UEP3_CTRL | UEP3_T_LEN |
| 0xC8 | T2CON | T2MOD | RCAP2L | RCAP2L | TL2 | TH2 | T2CAP1L | T2CAP1H |
| 0xC0 | SCON1 | SBUF1 | SBAUD1 | TKEY_CTRL | TKEY_DATL | TKEY_DATH | PIN_FUNC | GPIO_IE |
| 0xB8 | IP | CLOCK_CFG | | | | | | |
| 0xB0 | P3 | GLOBAL_CFG | | | | | | |
| 0xA8 | IE | WAKE_CTRL | | | | | | |
| 0xA0 | P2 | SAFE_MOD<br>CHIP_ID | XBUS_AUX | | | | | |
| 0x98 | SCON | SBUF | ADC_CFG | PWM_DATA2 | PWM_DATA1 | PWM_CTRL | PWM_CK_SE | ADC_DATA |
| 0x90 | P1 | USB_C_CTRL | P1_MOD_OC | P1_DIR_PU | | | P3_MOD_OC | P3_DIR_PU |
| 0x88 | TCON | TMOD | TL0 | TL1 | TH0 | TH1 | ROM_DATA_L | ROM_DATA_H |
| 0x80 | ADC_CTRL | SP | DPL | DPH | ROM_ADDR_L | ROM_ADDR_H | ROM_CTRL<br>ROM_STATUS | PCON |

Remarks :( 1), red text Representative bit addressable; (2), the following is a description corresponding to the color box

| | |
|---|---|
| | ADC register address register associated SPI0 |
| | relevant register Touch-Key USB registers |
| | relevant register associated timer / counter |
| | register 2 associated port registers associated |
| | PWM1 and PWM2 associated registers |
| | relevant register UART1 associated registers |
| | Flash-ROM |
| | |
| | |
| | |

## 5.2 SFR reset values and classification

Table 5.2 SFR and reset values described

| Functional Classification | name | address | description | Reset value |
|---|---|---|---|---|
| System Settings | B | F0h | B register | 0000 0000b |
| Related register | ACC | E0h | accumulator | 0000 0000b |

| | | | | |
|---|---|---|---|---|
| | PSW | D0h | Program Status Register | 0000 0000b |
| | GLOBAL_CFG | B1h | Global configuration register (the bootstrap state CH552) | 1010 0000b |
| | | | Global configuration register (the application state CH552) | 1000 0000b |
| | | | Global configuration register (CH551 guided program status) | 1110 0000b |
| | | | Global configuration register (the application state CH551) | 1100 0000b |
| | CHIP_ID | A1h | CH552 chip identification code ID (read only) | 0101 0010b |
| | | | CH551 chip identification code ID (read only) | 0101 0001b |
| | SAFE_MOD | A1h | Security Mode Control Register (write only) | 0000 0000b |
| | DPH | 83h | Data Address Pointer High 8 | 0000 0000b |
| | DPL | 82h | Data Address Pointer Low 8 | 0000 0000b |
| | DPTR | 82h | DPL and DPH composed of 16 SFR | 0000h |
| | SP | 81h | Stack Pointer | 0000 0111b |
| Clock, sleep and power control associated registers | WDOG_COUNT | FFh | Watchdog Count Register | 0000 0000b |
| | RESET_KEEP | FEh | Reset the holding registers (the power-on reset state) | 0000 0000b |
| | CLOCK_CFG | B9h | System clock configuration register | 1000 0011b |
| | WAKE_CTRL | A9h | Sleep wakeup control register | 0000 0000b |
| | PCON | 87h | Power control register (on the lower reset state) | 0001 0000b |
| Related interrupt control register | IP_EX | E9h | Extended Interrupt Priority Control Register | 0000 0000b |
| | IE_EX | E8h | Extended Interrupt Enable Register | 0000 0000b |
| | GPIO_IE | C7h | GPIO interrupt enable register | 0000 0000b |
| | IP | B8h | Interrupt Priority Control Register | 0000 0000b |
| | IE | A8h | Interrupt enable register | 0000 0000b |
| Flash-ROM associated registers | ROM_DATA_H | 8Fh | flash-ROM data register high byte | xxxx xxxxb |
| | ROM_DATA_L | 8Eh | flash-ROM Data Register Low Byte | xxxx xxxxb |
| | ROM_DATA | 8Eh | ROM_DATA_L and ROM_DATA_H composed of 16 SFR | xxxxh |
| | ROM_STATUS | 86h | flash-ROM status register (read only) | 0000 0000b |
| | ROM_CTRL | 86h | flash-ROM control register (write only) | 0000 0000b |
| | ROM_ADDR_H | 85h | flash-ROM Address Register High Byte | xxxx xxxxb |
| | ROM_ADDR_L | 84h | flash-ROM Address Register Low Byte | xxxx xxxxb |
| | ROM_ADDR | 84h | ROM_ADDR_L and ROM_ADDR_H composed of 16 SFR | xxxxh |
| Port-related registers | PIN_FUNC | C6h | Pin Function Select Register | 1000 0000b |
| | XBUS_AUX | A2h | Auxiliary external bus setting register | 0000 0000b |
| | P3_DIR_PU | 97h | P3 port direction control and the pullup enable register | 1111 1111b |
| | P3_MOD_OC | 96h | Port P3 output mode register | 1111 1111b |
| | P1_DIR_PU | 93h | P1 and pull-directional control port enable register | 1111 1111b |
| | P1_MOD_OC | 92h | Port output mode register P1 | 1111 1111b |
| | P3 | B0h | Register input and output ports P3 | 1111 1111b |
| | P2 | A0h | P2 port output register | 1111 1111b |
| | P1 | 90h | Input and output ports P1 register | 1111 1111b |
| Timer / Counter Associated registers 0 and 1 | TH1 | 8Dh | Timer1 high byte count | xxxx xxxxb |
| | TH0 | 8Ch | Timer0 high byte count | xxxx xxxxb |
| | TL1 | 8Bh | Timer1 counter low byte | xxxx xxxxb |
| | TL0 | 8Ah | Low byte count Timer0 | xxxx xxxxb |

| | | | | |
|---|---|---|---|---|
| | TMOD | 89h | Timer0 / 1 mode register | 0000 0000b |
| | TCON | 88h | Timer0 / 1 Control Register | 0000 0000b |
| UART0 Related register | SBUF | 99h | UART0 data register | xxxx xxxxb |
| | SCON | 98h | Control Register UART0 | 0000 0000b |
| Timer / Counter related registers 2 | T2CAP1H | CFh | Timer2 capture a high byte data (read-only) | xxxx xxxxb |
| | T2CAP1L | CEh | Timer2 capture a low-byte data (read only) | xxxx xxxxb |
| | T2CAP1 | CEh | T2CAP1L and T2CAP1H composed of 16 SFR | xxxxh |
| | TH2 | CDh | Timer2 counter high byte | 0000 0000b |
| | TL2 | CCh | Timer2 Counter Low | 0000 0000b |
| | T2COUNT | CCh | TL2 and TH2 composed of 16 SFR | 0000h |
| | RCAP2H | CBh | Reload count / capture data register 2 high byte | 0000 0000b |
| | RCAP2L | CAh | Reload count / capture data register 2 low byte | 0000 0000b |
| | RCAP2 | CAh | RCAP2L and RCAP2H composed of 16 SFR | 0000h |
| | T2MOD | C9h | Timer2 mode register | 0000 0000b |
| | T2CON | C8h | Timer2 Control Register | 0000 0000b |
| PWM1 and PWM2 associated registers | PWM_CK_SE | 9Eh | Clock Divider PWM setting register | 0000 0000b |
| | PWM_CTRL | 9Dh | PWM Control Register | 0000 0010b |
| | PWM_DATA1 | 9Ch | PWM1 data register | xxxx xxxxb |
| | PWM_DATA2 | 9Bh | PWM2 data register | xxxx xxxxb |
| SPI0 relevant register | SPI0_SETUP | FCh | SPI0 setting register | 0000 0000b |
| | SPI0_S_PRE | FBh | SPI0 slave mode preset data register | 0010 0000b |
| | SPI0_CK_SE | FBh | SPI0 clock divider setting register | 0010 0000b |
| | SPI0_CTRL | FAh | Control Register SPI0 | 0000 0010b |
| | SPI0_DATA | F9h | SPI0 data transceiver register | xxxx xxxxb |
| | SPI0_STAT | F8h | Status Register SPI0 | 0000 1000b |
| UART1 associated registers | SBAUD1 | C2h | UART1 baud rate setting register | xxxx xxxxb |
| | SBUF1 | C1h | UART1 data register | xxxx xxxxb |
| | SCON1 | C0h | Control Register UART1 | 0100 0000b |
| ADC relevant register | ADC_DATA | 9Fh | ADC data register | xxxx xxxxb |
| | ADC_CFG | 9Ah | ADC configuration register | 0000 0000b |
| | ADC_CTRL | 80h | ADC Control Register | x000 0000b |
| Touch-Key associated registers | TKEY_DATH | C5h | Touch-Key high byte data (read-only) | 0000 0000b |
| | TKEY_DATL | C4h | Touch-Key low-byte data (read only) | xxxx xxxxb |
| | TKEY_DAT | C4h | TKEY_DATL and TKEY_DATH composed of 16 SFR | 00xxh |
| | TKEY_CTRL | C3h | Touch-Key Control Register | x000 0000b |
| USB related registers | UEP1_DMA_H | EFh | Endpoint 1 buffer start address high byte | 0000 00xxb |
| | UEP1_DMA_L | EEh | Endpoint 1 buffer start address low byte | xxxx xxxxb |
| | UEP1_DMA | EEh | UEP1_DMA_L and UEP1_DMA_H composed of 16 SFR | 0xxxh |
| | UEP0_DMA_H | EDh | Endpoint 0 and 4 buffer start address high byte | 0000 00xxb |
| | UEP0_DMA_L | ECh | Endpoint 0 and 4 buffer start address low byte | xxxx xxxxb |
| | UEP0_DMA | ECh | UEP0_DMA_L and UEP0_DMA_H composed of 16 SFR | 0xxxh |
| | UEP2_3_MOD | EBh | Endpoint mode control register 3 | 0000 0000b |
| | UEP4_1_MOD | EAh | Endpoint Control Register Mode 4 | 0000 0000b |

| | | | | |
|---|---|---|---|---|
| | UEP3_DMA_H | E7h | Endpoint buffer start address high byte 3 | 0000 00xxb |
| | UEP3_DMA_L | E6h | Endpoint buffer start address low byte 3 | xxxx xxxxb |
| | UEP3_DMA | E6h | UEP3_DMA_L and UEP3_DMA_H composed of 16 SFR | 0xxxh |
| | UEP2_DMA_H | E5h | Endpoint buffer start address high byte | 0000 00xxb |
| | UEP2_DMA_L | E4h | Endpoint 2 buffer start address low byte | xxxx xxxxb |
| | UEP2_DMA | E4h | UEP2_DMA_L and UEP2_DMA_H composed of 16 SFR | 0xxxh |
| | USB_DEV_AD | E3h | USB Device Address Register | 0000 0000b |
| | USB_CTRL | E2h | USB control register | 0000 0110b |
| | USB_INT_EN | E1h | USB interrupt enable register | 0000 0000b |
| | UEP4_T_LEN | DFh | Endpoint transmit length register 4 | 0xxx xxxxb |
| | UEP4_CTRL | DEh | Endpoint Control register 4 | 0000 0000b |
| | UEP0_T_LEN | DDh | Endpoint transmit length register 0 | 0xxx xxxxb |
| | UEP0_CTRL | DCh | Endpoint Control Register 0 | 0000 0000b |
| | USB_RX_LEN | DBh | Receiving USB length register (read only) | 0xxx xxxxb |
| | USB_MIS_ST | DAh | Miscellaneous USB status register (read only) | xx10 1000b |
| | USB_INT_ST | D9h | USB Interrupt Status Register (read only) | 00xx xxxxb |
| | USB_INT_FG | D8h | USB interrupt flag register | 0010 0000b |
| | UEP3_T_LEN | D7h | Endpoint transmit length register 3 | 0xxx xxxxb |
| | UEP3_CTRL | D6h | Endpoint Control Register 3 | 0000 0000b |
| | UEP2_T_LEN | D5h | Endpoint transmit length register 2 | 0000 0000b |
| | UEP2_CTRL | D4h | Endpoint Control Register 2 | 0000 0000b |
| | UEP1_T_LEN | D3h | Endpoint 1 transmits length register | 0xxx xxxxb |
| | UEP1_CTRL | D2h | Endpoint Control register 1 | 0000 0000b |
| | UDEV_CTRL | D1h | USB device port control register | 10xx 0000b |
| | USB_C_CTRL | 91h | USB type-C channel control registers configured | 0000 0000b |

5.3 General registers 8051

Table 5.3.1 general register list 8051

| name | address | description | Reset value |
|---|---|---|---|
| B | F0h | B register | 00h |
| A, ACC | E0h | accumulator | 00h |
| PSW | D0h | Program Status Register | 00h |
| GLOBAL_CFG | B1h | Global configuration register (the bootstrap state CH552) | A0h |
| | | Global configuration register (the application state CH552) | 80h |
| | | Global configuration register (CH551 guided program status) | E0h |
| | | Global configuration register (the application state CH551) | C0h |
| CHIP_ID | A1h | CH552 chip identification code ID (read only) | 52h |
| | | CH551 chip identification code ID (read only) | 51h |
| SAFE_MOD | A1h | Security Mode Control Register (write only) | 00h |
| PCON | 87h | Power control register (on the lower reset state) | 10h |
| DPH | 83h | Data Address Pointer High 8 | 00h |
| DPL | 82h | Data Address Pointer Low 8 | 00h |
| DPTR | 82h | DPL and DPH composed of 16 SFR | 0000h |

| | | | |
|---|---|---|---|
| SP | 81h | Stack Pointer | 07h |

B register (B):

| Bit | Name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | B | RW | arithmetic registers, mainly for multiplication and division, can be bit addressing | 00h |

A accumulator ( A, ACC):

| Bit | Name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | A / ACC | RW | accumulator arithmetic operation, bit addressing can be | 00h |

program shape State Storage Device (PSW) :

| Bit | Name | Access | description | Reset value |
|---|---|---|---|---|
| 7 | CY | RW | Carry flag: when performing arithmetic and logic operation instruction for recording the most significant bit carry or borrow bit; when 8-bit adder, the Most Significant bit, the bit is cleared otherwise; 8-bit subtraction when If the borrow bit, the bit is cleared otherwise; logic instructions may cause the position or cleared | 0 |
| 6 | AC | RW | auxiliary carry flag: addition or subtraction recording, lower 4 bits to the high 4 there is a carry or borrow Position, AC set, otherwise cleared | 0 |
| 5 | F0 | RW | purpose flag bit addressing can be 0: Users can define their own, may be set or cleared by software | 0 |
| 4 | RS1 | RW | upper register bank select bits | 0 |
| 3 | RS0 | RW | lower register bank select bits | 0 |
| 2 | OV | RW | overflow flag: when addition or subtraction, the calculation result exceeds 8-bit binary numbers, the set OV 1, the overflow flag, otherwise cleared | 0 |
| 1 | F1 | GM | flag 1 bit addressing can be RW: Users can define their own, may be set or cleared by software | 0 |
| 0 | P | RO | Parity Flag: recording the instruction is executed in the accumulator A of a parity, an odd P Set, an even number of clearing the P | 0 |

State of the processor status register is stored in the PSW, PSW bit addressing support. Status word includes a carry flag, an auxiliary carry flag BCD code processing, the parity flag, overflow flag, and RS0 and RS1 for the selected register bank. Region where the register bank can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 RS1 register bank selection table

| | RS0 | Working Register Group |
|---|---|---|
| 0 | 0 | Group 0 (00h-07h) |
| 0 | 1 | Group 1 (08h-0Fh) |
| 1 | 0 | Group 2 (10h-17h) |
| 1 | 1 | Group 3 (18h-1Fh) |

table 5. 1.3 impact mark Mark Bit operating (X Flag represents versus Operating Results turn off)

| operating | CY | OV | AC | operating | CY | OV | AC |
|---|---|---|---|---|---|---|---|
| ADD | X | X | X | SETB C | 1 | | |
| ADDC | X | X | X | CLR C | 0 | | |
| SUBB | X | X | X | CPL C | X | | |
| MUL | 0 | X | | MOV C, bit | X | | |
| DIV | 0 | X | | ANL C, bit | X | | |
| DA A | X | | | ANL C, / bit | X | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| RRC A | X | | | ORL C, bit | X | | |
| RLC A | X | | | ORL C, / bit | X | | |
| CJNE | X | | | | | | |

Address data Finger Needle (DPTR) :

| Place | name access | description | Reset value |
|---|---|---|---|
| [7: 0] | DPL | Low Byte Data Pointer RW | 00h |
| [7: 0] | DPH | High Byte Data Pointer RW | 00h |

DPL and DPH composed of 16-bit data pointer DPTR, for accessing xRAM data memory or program memory, 16-bit data corresponding to the actual DPTR pointer on the two physical DPTR1 DPTR0 and by the DPS XBUS_AUX dynamically selected.

Stack Pointer (SP):

| Place | name access | description | Reset value |
|---|---|---|---|
| [7: 0] | SP | RW Stack Pointer, mainly for calls and interrupt calls and data in and out of the stack | 07h |

Stack specific function: to protect endpoints and protect the scene, managed according to the principle of first in, last out. When SP stack pointer is automatically incremented by 1, or data stored breakpoint information; SP pointers to data taken when the stack unit, SP pointer is decremented. SP is reset at the initial value after 07h, stack stores corresponding default start 08h.

## 5.4 unique register

Global Configuration send Register (GLOBAL _CFG), Can only be written in Safe Mode:

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 6] | Retention | RO to CH552, a fixed value 10 | | 10b |
| [7: 6] | Retention | RO to CH551, a fixed value 11 | | 11b |
| 5 | bBOOT_LOAD | RO | Boot loader status bit for distinguishing ISP bootstrap status or an application status: set the power is on, software reset cleared. For chip ISP boot program, the bit is reset to a software had never been described, usually ISP boot program after power run state; 0 indicates the bit is reset through software has usually application state | 1 |
| 4 | bSW_RESET | RW software reset control bit: 1 cause a software reset is set, the hardware automatically cleared | | 0 |
| 3 | bCODE_WE | RW | Flash-ROM and write permit bits DataFlash: the write protect bit is 0; as a Flash-ROM and rewritable Data | 0 |
| 2 | bDATA_WE | RW | DataFlash region Flash-ROM write enable bit: This bit is 0, the write protection; DataFlash region is a rewritable | 0 |
| 1 | bLDO3V3_OFF | RW | USB power LDO regulator disable control bits: Bit 0 allows the LDO, may be generated by USB 5V supply voltage for the 3.3V and the internal clock oscillator;<br>To disable an LDO, V33 pin must be input 3.3V power supply | 0 |
| 0 | bWDOG_EN | RW watchdog reset enable bit: This bit is used only for the watchdog timer 0; this bit Watchdog reset is generated when a timer overflow to allow | | 0 |

Chip identification ID Do not code (CHIP_ID ):

| Place | name access | description | Reset value |
|---|---|---|---|
| [7: 0] | CHIP_ID | RO to CH552, is a fixed value 52h, for identifying a chip | 52h |

| | | | |
|---|---|---|---|
| [7: 0] | CHIP_ID | RO to CH551, is a fixed value 51h, for identifying a chip | 51h |

Safe Mode control Register system (S A FE_MOD ): Bit

| | name access | | description | Reset value |
|---|---|---|---|---|
| [7: 0] | SAFE_MOD | WO safe mode for entering or terminate | | 00h |

Data can be written only part of SFR in safe mode, but in non-secure mode is always read-only. Step into safe mode: (1), write to this register 55h; (2), followed by an AAh this register;

(3), after about 13-23 cycles the system frequency in a safe mode, the period can be rewritten within one or more security classes SFR SFR or normal;

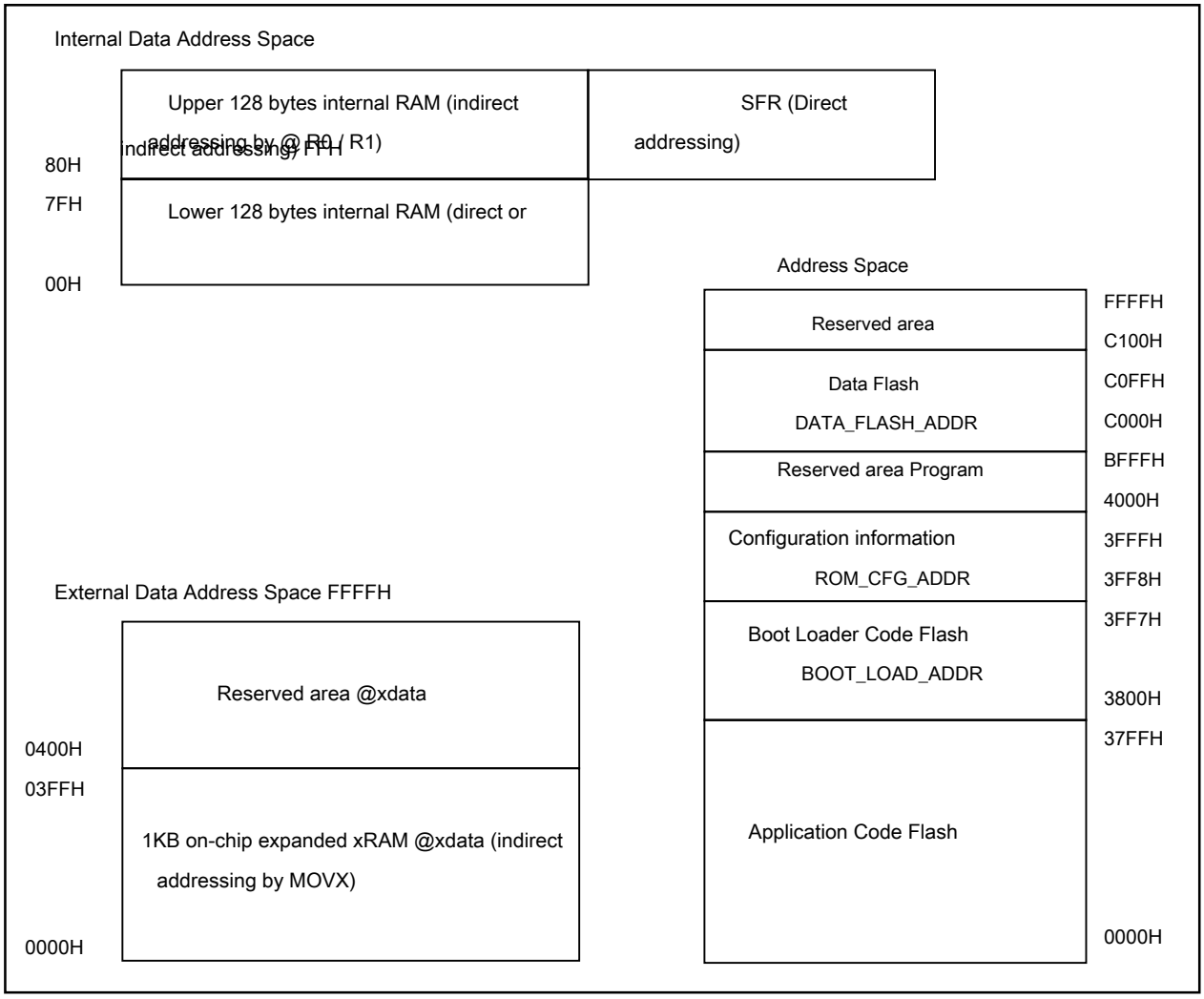
(4), beyond the above period after the security mode automatically terminated; (5), or any value register write again the safe mode can be terminated early.

## 6, the memory structure

### 6.1 memory space

CH552 address space is divided into program memory space, the internal data memory space, the external data memory space.

Figure 6.1 the memory structure of FIG.




### 6.2 program memory space

64KB altogether program memory space, shown in Figure 6.1, wherein a 16KB ROM, including Code Flash Configuration Information area and configuration information region for storing instruction codes.

Code Flash application comprises program code and boot code region of the high address lower address region, these two regions may also be combined to hold a single application code.

**For the application code area CH551, Code Flash only 10KB. ROM is iFlash ™ Process for the finished blank after the official ROM package, may be about 200 times** programmed 5V supply. Data Flash address range to C0FFH .The to C000h (only even address is valid, there is actually a byte of every other storage unit), only support a single byte (8 bits) read and write operations, the data remain unchanged after the chip is powered down. Data Flash support about 1 million Write.

Configuration Information configuration information comprises four sets of 16-bit data to 3FFFH 3FF8H address, the read-only three units, to provide a chip ID. Located 3FF8H address configuration data set as desired by the programmer, with reference to Table 6.2.

Table 6.2 flash-ROM configuration described

| Bit address | Bit Name | Explanation | suggested value |
|---|---|---|---|
| 15 | Code_Protect flash-ROM code and data protection mode: | 0- inhibit programming read out, program secrecy; 1- permissible reading | 0/1 |
| 14 | No_Boot_Load | BootLoader boot code enabling startup mode: 0 from an application start address 0000h; 1- boot program from the boot address 3800h | 1 |
| 13 | En_Long_Reset the additional delay can be reset during power-on reset: | 0- standard short reset; 1- wide reset, the reset time additional 44mS | 0 |
| 12 | En_RST_RESET RST pin is enabled as a manual reset input pin: 0- disabled; 1 - enables RST | | 0 |
| [11:10] | Retention | (As required by the programmer automatically set to 00) | 00 |
| 9 | Must_1 | (As required by the programmer automatically set to 1) | 1 |
| 8 | Must_0 | (As required by the programmer automatically set to 0) | 0 |
| [7: 0] | All_1 | (Automatically set by the programmer needed to FFh) | FFh |

### 6.3 Data storage space

Internal data memory space 256 bytes shown in Figure 6.1, and have been used in SFR iRAM, wherein iRAM for temporary data stack and fast, can be subdivided as working registers R0-R7, BDATA variable bits, bytes variable data, idata and so on.

64KB altogether external data memory, shown in Figure 6.1, the expansion part for the 1KB xRAM sheet, the remaining area is reserved. For CH551, only 512 bytes xRAM expansion chip.

## 6.4 flash-ROM register

Table 6.4 Register list operations flash-ROM

| name | address | description | Reset value |
|---|---|---|---|
| ROM_DATA_H | 8Fh | flash-ROM data register high byte | xxh |
| ROM_DATA_L | 8Eh | flash-ROM Data Register Low Byte | xxh |
| ROM_DATA | 8Eh | ROM_DATA_L and ROM_DATA_H composed of 16 SFR | xxxxh |
| ROM_STATUS | 86h | flash-ROM status register (read only) | 00h |
| ROM_CTRL | 86h | flash-ROM control register (write only) | 00h |
| ROM_ADDR_H | 85h | flash-ROM Address Register High Byte | xxh |
| ROM_ADDR_L | 84h | flash-ROM Address Register Low Byte | xxh |
| ROM_ADDR | 84h | ROM_ADDR_L and ROM_ADDR_H composed of 16 SFR | xxxxh |

flash-ROM Address Register (ROM_ADDR):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | ROM_ADDR_H | RW | flash-ROM address high byte | xxh |
| [7: 0] | ROM_ADDR_L | RW | flash-ROM address low byte, supports only even address for Data Flash, the actual offset must be left address 00H-7FH becomes an even address 00H / 02H / 04H ... ~ FEH and then placed | xxh |

**flash-RO M Data register (ROM _ DATA) :**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | ROM_DATA_H | RW | flash-ROM data to be written high byte | xxh |
| [7: 0] | ROM_DATA_L | RW | flash-ROM low byte of data to be written, For DataFlash, data byte is to be written or read out data bytes | xxh |

**flash-RO M Control Register (ROM _ CTRL) :**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | ROM_CTRL | WO | flash-ROM control register | 00h |

**flash-RO M Status Register (ROM _ STATUS ): Bit**

| | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | Retention | RO reserved. | | 0 |
| 6 | bROM_ADDR_OK | RO | flash-ROM write address is valid status bit: This bit indicates an invalid parameter 0; 1 indicates the effective address | 0 |
| [5: 2] | Retention | RO reserved. | | 0000b |
| 1 | bROM_CMD_ERR | RO | flash-ROM Operation Command Error Status Bit: This bit is a 0 indicates a valid command; 1 indicates the command is unknown | 0 |
| 0 | Retention | RO reserved. | | 0 |

## 6.5 flash-ROM Procedure

1, flash-ROM write code region, double-byte data is written to the target address: (1), if the flash-ROM need to write the code, you must select the 5V supply voltage; (2), the security mode is enabled, SAFE_MOD = 55h ; SAFE_MOD = 0AAh;

(3), the configuration register to set the global write enable GLOBAL_CFG opening (bCODE_WE bDATA_WE or the corresponding code or data); (4), provided the ROM_ADDR address registers, write 16-bit target address (the least significant bit is always 0); (5), data register settings ROM_DATA, 16-bit write data to be written, step (4), (5) the sequence may be reversed; (6), provided for the operation control register ROM_CTRL 09Ah, a write operation, during the operation of automatically pauses; (7), the program resumes after the operation is completed, then check the status register ROM_STATUS can view the operating status; if

A plurality of write data, the loop (4), (5), (6), (7) a step; (8), re-enter the safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh; (9), set the global configuration register GLOBAL_CFG open write-protected (bCODE_WE = 0, bDATA_WE = 0).

2, the write data area Data Flash, single byte data is written to the target address: (1), the security mode is enabled, SAFE_MOD = 55h; SAFE_MOD = 0AAh; (2), set the global configuration register GLOBAL_CFG Open Write Enable (bDATA_WE corresponding to data); (3), provided the ROM_ADDR address registers, write 16-bit target address, address 00H-7FH actual offset must be changed to a left

**Even address 00H / 02H / 04H ... ~ FEH then placed, followed by final address C000H / C002H / C004 ... ;**

(4), the data register settings ROM_DATA_L, write 8-bit data to be written, step (3), (4) sequence can be reversed; (5), provided for the operation control register ROM_CTRL 09Ah, a write operation, during the operation of the program automatically suspended operation; (6), the program resumes after the operation is completed, then check the status register ROM_STATUS can view the operating status; if

A plurality of write data, the loop (3), (4), (5), (6) a step; (7), re-enter the safe mode, SAFE_MOD = 55h; SAFE_MOD = 0AAh; (8), set the global configuration register GLOBAL_CFG open write-protected (bCODE_WE = 0, bDATA_WE = 0).

3, the read data area Data Flash, single byte data read from the target address:

(1), provided the ROM_ADDR address registers, write 16-bit target address, address 00H-7FH actual offset must be changed to a left

**Even address, followed by a final address C000H / C002H / C004 ... ;**

(2), provided for the operation control register ROM_CTRL 08Eh, read operation is performed automatically during operation pauses; (3), the program resumes the operation is completed, the status register ROM_STATUS case the query can view this bROM_CMD_ERR

Secondary operating state; if the command is valid, then the 8-bit data stored in the read data register ROM_DATA_L; and (4), if a plurality of data to be read, the loop (1), (2), (3) step.

4, reads flash-ROM:

MOVC instruction directly, or through a pointer points to the memory space, or code data read destination address.

## 6.6 On-board programming and ISP download

When the configuration information Code_Protect = 1, the data in the flash-ROM chip CH552 code and Data Flash may be by an external programmer by a synchronous serial interface to read; = 0 when the configuration information Code_Protect, flash-ROM code and data in the data Flash is protected and can not read, but can be erased and re-power after erasing code protection is canceled.

When CH552 chip is preset BootLoader boot program, CH552 can support multiple USB ISP to download an asynchronous serial interface, or loading an application; however, in no case where the boot program, CH552 can be written by a programmer external dedicated boot program or an application. In order to support on-board programming, it must be temporarily 5V supply voltage, to be reserved and the circuit 4 is connected between the pin CH552 programmer, is the minimum necessary connection pin 3: P1.4, P1.6, P1.7.

Table 6.6.1 and the connection pins between the programmer

| Pin | GPIO | Pin Description |
|---|---|---|
| RST | RST reset in | the programmed state control pin, allowing access to high programmed state SCS |
| | Chip select | input pin (required), the default high, active low SCK in the programmed state P1.4 |
| | Clock Input | Pins P1.7 programmed state (necessary) the MISO |
| | Data output | pins (if necessary) in a programmed state P1.6 |

Note: Whether or on-board programming through the serial port or USB download, must be temporarily used 5V supply voltage.

## 6.7 chip unique ID number

Each MCU has a unique ID number at the factory, that is, the chip identification number. The ID data of 5 bytes, is stored in the address information arranged 3FFAH to 3FFFH Configuration Information area. Wherein 3FFBH address holding unit, and 8-bit data 3FFCH 3FFEH two 16-bit addresses and data 40 combined 3FFAH address bit chip ID data.

| Program Space Address | ID Data Description |
|---|---|
| 3FFAh, 3FFBh | Last word ID data, 40 is the highest order byte ID number, a reserved byte |
| 3FFCh, 3FFDh | ID data first word, followed by the least significant byte ID number, the second lowest byte |
| 3FFEh, 3FFFh | ID data sub-word, followed by high byte, high-byte ID number |

The ID data can be acquired by reading Code Flash manner. ID numbers can be downloaded with the program means for encrypting the target, the general application, just before the use of 32-bit ID number, i.e., 8-bit data can be ignored 3FFAH address.

## 7, power management, sleep and reset

### External power input 7.1

CH552-chip low dropout voltage regulator 5V to 3.3V, 3.3V, or even support external 2.8V 5V supply voltage input

The two supply voltage input Mode into the following table.

| External power supply voltage | VCC pin voltage: 3V ~ 5V external voltage | V33 pin voltage: 3.3V internal voltage |
|---|---|---|
| Comprising less than 3.6V 3.3V or 3V | External 3.3V voltage input to the voltage regulator, must be connected to no less than 0.1uF decoupling capacitance | External input 3.3V as the internal power supply, must be connected to the decoupling capacitance not less than 0.1uF |
| Is greater than 5V 3.6V comprising | Input 5V voltage to a voltage regulator, must be connected to no less than 0.1uF decoupling capacitance | The internal voltage regulator 3.3V and 3.3V output internal working power input must be connected to no less than 0.1uF decoupling capacitance |

After the power supply or system reset, CH552 default is running. Under the premise to meet the requirements of performance, due to lower system frequency can reduce power consumption during operation. When CH552 completely without running, can be provided in the PD PCON enter the sleep state, the sleep state can be selected by an external wake USB, UART0, UART1, SPI0 and some GPIO.

### 7.2 Power and Sleep Control Register

Table 7.2.1 Power and Sleep Control Register List

| name | address | description | Reset value |
|---|---|---|---|
| WDOG_COUNT | FFh | watchdog count register | 00h |
| RESET_KEEP | FEh | reset the holding registers | 00h |
| WAKE_CTRL | A9h | sleep wakeup control register | 00h |
| PCON | | Power control register 87h | 10h |

**Watchdog meter number Register (the WDOG _ COUNT) :**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | WDOG_COUNT | RW | watchdog current count, overflow expiration 0FFh steering 00h, overflow from Automatically sets the interrupt flag bWDOG_IF_TO 1 | 00h |

**Reset Hold send Register (RESET_ K EEP):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | RESET_KEEP | RW | reset the holding register values can be artificially modified, in addition to power-on reset may be Than it is cleared, any other reset does not affect the value | 00h |

**Sleeping Call Wake up control register (WA K E_ CTRL ), Can be written only in safe mode:**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bWAK_BY_USB | RW | Enable USB Wake event, this bit disables wake 0 | 0 |
| 6 | bWAK_RXD1_LO | RW | UART1 receiving wake-up enable input low, the wake-up prohibition bit is 0. The bUART1_PIN_X = 0/1 to select or RXD1_ pin RXD1 | 0 |
| 5 | bWAK_P1_5_LO | RW | P1.5 low wakeup enable, 0 to disable wake | 0 |
| 4 | bWAK_P1_4_LO | RW | P1.4 low wakeup enable, 0 to disable wake | 0 |
| 3 | bWAK_P1_3_LO | RW | P1.3 low wakeup enable, 0 to disable wake | 0 |
| 2 | bWAK_RST_HI | RW | RST high wakeup enable, 0 to disable wake | 0 |
| 1 | bWAK_P3_2E_3L | RW | P3.2 and P3.3 low edge transition enable wake, wake-up is prohibited 0 | 0 |
| 0 | bWAK_RXD0_LO | RW | UART0 receiving wake-up enable input low, 0 to disable wake. | 0 |

| | | | | |
|---|---|---|---|---|
| | | | The select pin RXD0 or RXD0_ bUART0_PIN_X = 0/1 | |

power supply control System register (PCON) :

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | SMOD | When RW is generated when UART0 baud rate timer 1, a mode selection UART0, | 2,3 baud rate: 0 slow mode; 1- Quick mode | 0 |
| 6 | Retention | RO reserved. | | 0 |
| 5 | bRST_FLAG1 | R0 chip last reset flag high | | 0 |
| 4 | bRST_FLAG0 | R0 chip low last reset flag | | 1 |
| 3 | GF1 | RW purpose flag 1: Users can define their own, can be set or cleared by software | | 0 |
| 2 | GF0 | RW common flag 0: Users can define their own, can be set or cleared by software | | 0 |
| 1 | PD | RW sleep mode is enabled, set after sleep, the hardware is automatically cleared after wake | | 0 |
| 0 | Retention | RO reserved. | | 0 |

Table 7.2.2 chip reset flag described in a recent

| bRST_FLAG1 | bRST_FLAG0 | Reset flag description |
|---|---|---|
| 0 | 0 | Software reset, Source: bSW_RESET = 1 and (bBOOT_LOAD = 0 or bWDOG_EN = 1) |
| 0 | 1 | Power reset on power sources: VCC pin voltage is below the detection level |
| 1 | 0 | Watchdog reset, Source: bWDOG_EN = 1 and the watchdog timeout |
| 1 | 1 | External reset pin manually, Source: En_RST_RESET = 1 and the RST input high |

## 7.3 Reset Control

CH552 has four sources of reset: power-on reset, external reset, software reset, a watchdog reset, three belonging to the warm reset.

### 7.3.1 Power-On Reset

POR power-on reset is generated by on-chip voltage detecting circuit. POR circuit continuously monitors the power supply voltage VCC pin, a power-on reset VPOT below the detection level, automatic delay Tpor by hardware to maintain the reset state, after the operation delay CH552.

Only power-on reset only the CH552 reload the configuration information and clear RESET_KEEP, warm reset does not affect the other.

### 7.3.2 External reset

Applied to a high level by the external reset pin RST is generated. When configuration information En_RST_RESET 1, and the duration of the high level on the reset procedure is triggered when the RST pin is greater than Trst. When the high level signal is applied to withdraw, automatic delay Trdl hardware to maintain the reset state, CH552 When the time delay started from the 0 address.

### 7.3.3 Software Reset

CH552 supports internal software reset, so that no external intervention initiative to reset the CPU state and rerun. GLOBAL_CFG set global configuration register is bSW_RESET 1, the software can be reset and the automatic delay Trdl to maintain the reset state, CH552 When the time delay started from the address 0, bSW_RESET bit is automatically cleared by hardware.

When bSW_RESET set to 1, if bBOOT_LOAD = 0 or bWDOG_EN = 1, then the reset bRST_FLAG1 / 0 indicating a software reset; if 1, if bBOOT_LOAD = 1 and bWDOG_EN = 0, then bRST_FLAG1 / 0 will not generate bSW_RESET set new the reset flag, once reset flag before but remains unchanged.

For the latter with a power-on reset chip ISP boot program, the power to run the boot program, the software program needed to reset the chip to switch the state of the application, the software reset only cause bBOOT_LOAD cleared state does not affect bRST_FLAG1 / 0 of (Since the pre-reset bBOOT_LOAD = 1), when the state is switched to the application, bRST_FLAG1 / 0 is still indicated as POR state.

### 7.3.4 Watchdog Reset

The watchdog reset occurs from the watchdog timer timeout. The watchdog timer is an 8-bit counter, which counts the clock frequency of the system frequency Fsys / 65536, an overflow signal when the count is full 0FFh steering 00h.

Watchdog timer overflow signal triggers the interrupt flag bWDOG_IF_TO to 1, the interrupt flag when reloaded WDOG_COUNT or enter the corresponding is automatically cleared when the interrupt service routine.

By writing an initial value to the different counting WDOG_COUNT, in order to achieve different timing periods Twdc. In frequency 6MHz, watchdog timing cycle time of writing 00h Twdc about 2.8 seconds, about 1.4 seconds writing 80h. While halved 12MHz clock speed.

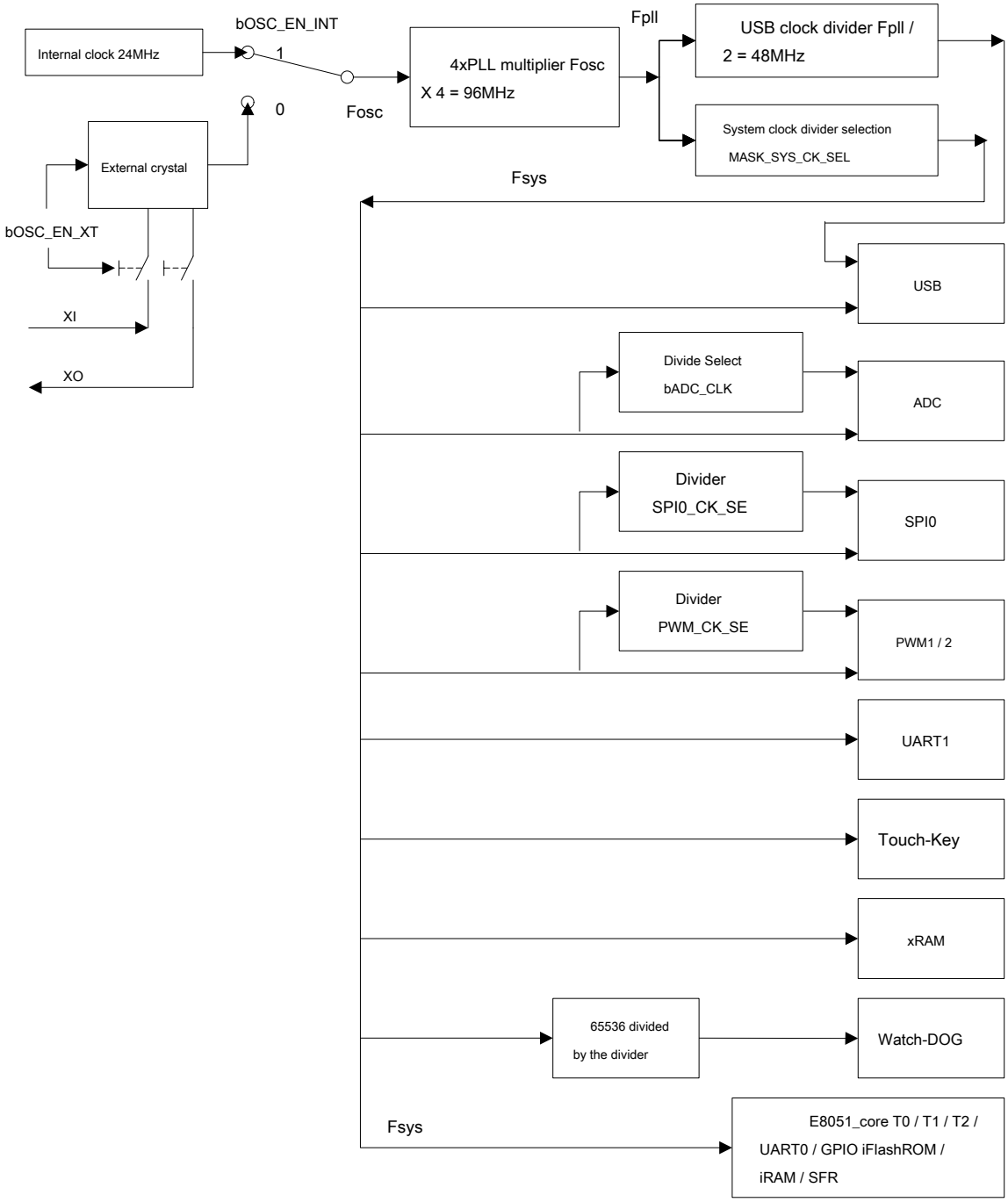
If the watchdog timer overflow bWDOG_EN = 1, then the watchdog reset is generated, and the automatic delay Trdl to maintain the reset state, CH552 When the time delay started from the 0 address.

When bWDOG_EN = 1 In order to avoid a watchdog reset, reset must be timely WDOG_COUNT, avoid overflow.

## 8, the system clock

### 8.1 a block diagram of a clock

And FIG clock system configuration diagram 8.1.1




Internal or external clock as a second election after Fosc original clock, generating the high frequency clock and then after Fpll 4xPLL frequency, and finally through two clock divider respectively Fsys Fusb4x system clock and the USB module. The system clock is directly supplied to each module Fsys of CH552.

## 8.2 Register Description

Clock Control Register List Table 8.2.1

| name | address | description | Reset value |
|---|---|---|---|
| CLOCK_CFG | B9h system | clock configuration register | 83h |

**System Clock Match Configuration registers (CLOCK_C FG), Can only be written in Safe Mode:**

| Place | name | access | description | Reset value |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 7 | bOSC_EN_INT | RW | The internal clock oscillator is enabled, this bit enables the internal clock oscillator 1 and the internal clock selection; selection of the external crystal oscillator provides a clock bit is turned off and the internal clock oscillator 0 | 1 |
| 6 | bOSC_EN_XT | RW | External crystal oscillator is enabled, the bit is 1 P1.2 / P1.3 pin as XI / XO and enable the oscillator, an external quartz crystal or ceramic resonator between the XO and XI; the bit is 0 Close external oscillator | 0 |
| 5 | bWDOG_IF_TO | RO | Watchdog timer interrupt flag bit, which is 1 means interrupt, triggered by a timer overflow signal; the bit is 0 for no interruptions. When the bit count register WDOG_COUNT watchdog reloaded into the respective automatically cleared or the interrupt service routine | 0 |
| 4 | bROM_CLK_FAST | RW | flash-ROM reference clock frequency selection: 0-normal (if Fosc> = 16MHz); 1- accelerate (if Fosc <16MHz) | 0 |
| 3 | bRST | R0 | RST bit input pin state | 0 |
| [2: 0] MASK_SYS_CK_SEL | | RW select the system clock frequency, the reference to Table 8.2.2 | | 011b |

Table 8.2.2 system frequency selection table

| MASK_SYS_CK_SEL Fsys the system frequency when the crystal frequency Fosc Fsys 24MHz Fxt relationship when = | | | |
|---|---|---|---|
| 000 | Fpll / 512 | Fxt / 128 | 187.5KHz |
| 001 | Fpll / 128 | Fxt / 32 | 750KHz |
| 010 | Fpll / 32 | Fxt / 8 | 3MHz |
| 011 | Fpll / 16 | Fxt / 4 | 6MHz |
| 100 | Fpll / 8 | Fxt / 2 | 12MHz |
| 101 | Fpll / 6 | Fxt / 1.5 | 16MHz |
| 110 | Fpll / 4 | Fxt / 1 | 24MHz |
| 111 | Fpll / 3 | Fxt / 0.75 | 32MHz |

8.3 Configuration Clock

After power on CH552 default using the internal clock, the internal clock frequency is 24MHz. May be selected internal clock or external clock by a crystal oscillator CLOCK_CFG, if you turn off the external crystal oscillator, the XO and XI pins P1.2 and P1.3 can be used as normal I / O port. If an external crystal oscillator clock, you should jumper crystal, and XO and XI respectively to GND pin capacitance connected between the pin XO and XI; if the input clock signal directly from the outside, it should lead from XI pin input, XO pin floating.

Original clock frequency Fosc = bOSC_EN_INT 24MHz:? Fxt PLL frequency Fpll =
Fosc * 4 = 96MHz USB clock frequency Fusb4x = Fpll / 2 = 48MHz system
frequency reference table 8.2.2 Fsys by the frequency-dividing Fpll

The default state after reset, Fosc = 24MHz, Fpll = 96MHz, Fusb4x = 48MHz, Fsys = 6MHz.

To switch to an external crystal oscillator clock as follows:

(1), into safe mode, a step SAFE_MOD = 55h; Step two SAFE_MOD = AAh;

(2), using "bit or" operation set bOSC_EN_XT CLOCK_CFG 1, the other bits are left unchanged, a crystal oscillator is enabled; (3), the number of milliseconds delay, typically 5mS ~ 10mS, waiting for a stable crystal oscillator; (4), re-enter the safe mode, a step SAFE_MOD = 55h; step two SAFE_MOD = AAh; (5), with "bits and" operation in bOSC_EN_INT CLOCK_CFG cleared, other bits remain unchanged from the external clock;

(6), the safety off mode, an arbitrary value is written to the secure mode SAFE_MOD early termination.

The step of modifying the system frequency is as follows:

(1), into safe mode, a step SAFE_MOD = 55h; Step two SAFE_MOD = AAh; (2), to write the new value CLOCK_CFG;

(3), the safety off mode, an arbitrary value is written to the secure mode SAFE_MOD early termination.

Remarks:

(1), if the USB module, it must be Fusb4x 48MHz; and when full speed USB, not lower than the system frequency Fsys 6MHz; at low speed USB, the system frequency Fsys not less than 1.5MHz.

(2), a lower priority to the Fsys system clock frequency, thereby reducing the dynamic power system, and the operating temperature range is widened. (3), the internal clock oscillator of the power supply V33, the voltage V33 so that the low voltage variations will affect the particular internal clock frequency.

## 9, interrupted

CH552 chip supports 14 set of interrupt signal sources, including standard MCS51 compatible 6 set of interrupt: INT0, T0, INT1, T1, UART0, T2, and 8 groups interrupted extension: SPI0, TKEY, USB, ADC, UART1, PWMX, GPIO, WDOG, wherein the GPIO interrupts may be selected from seven I / O pins.

### 9.1 Register Description

Table 9.1.1 Interrupt Vector Table

| Interrupt Source | Entry address | interrupt number | description | The default priority order |
|---|---|---|---|---|
| INT_NO_INT0 | 0x0003 | 0 | External Interrupt 0 | High priority |
| INT_NO_TMR0 | 0x000B | 1 | Timer 0 interrupt | ↓ |
| INT_NO_INT1 | 0x0013 | 2 | External interrupt 1 | ↓ |
| INT_NO_TMR1 | 0x001B | 3 | Timer 1 interrupt | ↓ |
| INT_NO_UART0 | 0x0023 | 4 | UART0 interrupt | ↓ |
| INT_NO_TMR2 | 0x002B | 5 | Timer 2 interrupt | ↓ |
| INT_NO_SPI0 | 0x0033 | 6 | SPI0 interrupt | ↓ |
| INT_NO_TKEY | 0x003B | 7 | Touch Key timer interrupt | ↓ |
| INT_NO_USB | 0x0043 | 8 | USB interrupt | ↓ |
| INT_NO_ADC | 0x004B | 9 | ADC interrupt | ↓ |
| INT_NO_UART1 | 0x0053 | 10 | UART1 interrupt | ↓ |
| INT_NO_PWMX | 0x005B | 11 | PWM1 / PWM2 interrupt | ↓ |
| INT_NO_GPIO | 0x0063 | 12 | GPIO interrupt | ↓ |
| INT_NO_WDOG | 0x006B | 13 | Watchdog Timer | Low Priority |

Table 9.1.2 Interrupt related register list

| name | address | description | Reset value |
|---|---|---|---|
| IP_EX | E9h | Extended Interrupt Priority Control Register | 00h |
| IE_EX | E8h | Extended Interrupt Enable Register | 00h |
| GPIO_IE | C7h | GPIO interrupt enable register | 00h |
| IP | B8h | Interrupt Priority Control Register | 00h |
| IE | A8h | Interrupt enable register | 00h |

**Interrupt Make Register ( IE): Bit name**

| access | | | description | Reset value |
|---|---|---|---|---|
| 7 | EA | RW | global interrupt enable control bit, the bit is 1 and 0 to allow interrupt E_DIS; the Bit 0 mask all interrupt requests | 0 |
| 6 | E_DIS | RW | Global interrupt disable control bit, the bit is a mask all interrupt requests; the EA bit is 0 and 1 allows to interrupt. It is typically used to temporarily disable interrupts during operation of the flash-ROM bit | 0 |
| 5 | ET2 | RW | timer 2 interrupt enable bit, which allows the T2 interrupt is 1; 0 shield | 0 |
| 4 | ES | 0 RW | asynchronous serial port interrupt enable bit, this bit to 1 to allow UART0 interrupt; 0 shield | 0 |
| 3 | ET1 | RW | timer 1 interrupt enable bit, this bit to 1 to allow T1 interrupt; 0 shield | 0 |
| 2 | EX1 | | External interrupt enable bit RW 1, this bit to 1 to allow interrupt INT1; 0 shield | 0 |
| 1 | ET0 | RW | timer 0 interrupt enable bit, this bit to 1 to allow T0 interrupt; 0 shield | 0 |
| 0 | EX0 | | External Interrupt 0 RW enable bit, this bit to 1 to allow INT0 interrupt; 0 shield | 0 |

**Spread in Enable send-off Deposit Is (IE _EX):**

| Place name access | | | description | Reset value |
|---|---|---|---|---|
| 7 | IE_WDOG | RW | watchdog timer interrupt enable bit, this bit to 1 to allow WDOG interrupt; 0 shield | 0 |
| 6 | IE_GPIO | RW | GPIO interrupt enable bit, this bit allows the interrupts enabled in GPIO_IE 1; 0 masking all interrupts GPIO_IE | 0 |
| 5 | IE_PWMX | RW | PWM1 / PWM2 interrupt enable bit, this bit to 1 to allow PWM1 / 2 interrupt; 0 shield | 0 |
| 4 | IE_UART1 | RW 1 | asynchronous serial port interrupt enable bit, this bit to 1 to allow UART1 interrupt; 0 shield | 0 |
| 3 | IE_ADC | RW | ADC analog to digital conversion interrupt enable bit, this bit to 1 to allow ADC interrupt; 0 shield | 0 |
| 2 | IE_USB | RW | USB interrupt enable bit, this bit to 1 to allow a USB interrupt; 0 shield | 0 |
| 1 | IE_TKEY | RW | key touch timer interrupt enable bit, this bit allows a timer interrupt; 0 shield | 0 |
| 0 | IE_SPI0 | RW | SPI0 interrupt enable bit, this bit to 1 to allow interrupt SPI0; 0 shield | 0 |

**GPIO Interrupt enable register ( GPIO_I E):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bIE_IO_EDGE | RW | GPIO edge interrupt mode enable:<br>The bit selection level 0 interrupt mode, GPIO pin bIO_INT_ACT to the active level 1 and has an interrupt request, GPIO bIO_INT_ACT invalid input level is 0 and cancels the interrupt request;<br>The 1 bit is selected edge interrupt mode, an interrupt request and the interrupt flag bIO_INT_ACT GPIO pin valid edge, the software interrupt flag is not cleared, or reset only when level interrupt mode or into the corresponding interrupt service routine when it is automatically cleared | 0 |
| 6 | bIE_RXD1_LO | RW | This bit to 1 enables UART1 receive interrupt pin (active low level mode, falling edge active mode); the bit 0 is prohibited. The bUART1_PIN_X = 0/1 to select or RXD1_ pin RXD1 | 0 |
| 5 | bIE_P1_5_LO | RW | This bit is set to 1 to enable interrupts P1.5 active low (level pattern, edge patterns Falling edge active); the bit is 0 prohibition | 0 |
| 4 | bIE_P1_4_LO | RW | This bit is set to 1 to enable interrupts P1.4 active low (level pattern, edge patterns Falling edge active); the bit is 0 prohibition | 0 |

| | | | | |
|---|---|---|---|---|
| 3 | bIE_P1_3_LO | RW | This bit is set to 1 to enable interrupts P1.3 active low (level pattern, edge patterns Falling edge active); the bit is 0 prohibition | 0 |
| 2 | bIE_RST_HI | RW | This bit is a 1 on the RST interrupt enable (active high level mode, edge pattern Rising edge active); the bit is 0 prohibition | 0 |
| 1 | bIE_P3_1_LO | RW | This bit is set to 1 to enable interrupts P3.1 active low (level pattern, edge patterns Falling edge active); the bit is 0 prohibition | 0 |
| 0 | bIE_RXD0_LO | RW | This bit to 1 enables an interrupt UART0 receive pin (active low level mode, falling edge active mode); the bit 0 is prohibited. The select pin RXD0 or RXD0_ bUART0_PIN_X = 0/1 | 0 |

**Interrupt excellent Priority control register Device (IP) :**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | PH_FLAG | RO | high priority interrupt executing flag | 0 |
| 6 | PL_FLAG | RO | is performing low-priority interrupt flag | 0 |
| 5 | PT2 | RW | Timer 2 interrupt priority control bits | 0 |
| 4 | PS | RW | UART0 interrupt priority control bits | 0 |
| 3 | PT1 | RW | Timer 1 interrupt priority control bits | 0 |
| 2 | PX1 | RW | External Interrupt 1 Priority Control | 0 |
| 1 | PT0 | RW | Timer 0 interrupt priority control bits | 0 |
| 0 | PX0 | RW | External Interrupt 0 interrupt priority control bits | 0 |

**Spread in Interrupt priority control send Register ( IP_EX):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bIP_LEVEL | RO | nesting level of the current interrupt flag bit, which is 0 for no interruption or nesting Level 2 interrupt; the bit is 1, it indicates the current nesting level 1 interrupts | 0 |
| 6 | bIP_GPIO | RW | GPIO interrupt priority control bits | 0 |
| 5 | bIP_PWMX | RW | PWM1 / PWM2 interrupt priority control bits | 0 |
| 4 | bIP_UART1 | RW | UART1 interrupt priority control bits | 0 |
| 3 | bIP_ADC | RW | ADC interrupt priority control bits | 0 |
| 2 | bIP_USB | RW | USB interrupt priority control bits | 0 |
| 1 | bIP_TKEY | RW | touch button timer interrupt priority control bits | 0 |
| 0 | bIP_SPI0 | RW | SPI0 interrupt priority control bits | 0 |

IP_EX and IP registers for setting the interrupt priority level, if a bit is set, the corresponding interrupt source is set to a high priority; if a bit is cleared, the corresponding interrupt source is set to a low priority . For the same level interrupt sources, the system has a default priority order, the default order of priority electrode as shown in Table 9.1.1. Which PH_FLAG and PL_FLAG combination indicates the priority of the current interrupt.

Table 9.1.3 Current Interrupt priority status indication

| PH_FLAG | PL_FLAG | The current interrupt priority status |
|---|---|---|
| 0 | 0 | There are currently no interruption |
| 0 | 1 | Currently performing low-priority interrupt |
| 1 | 0 | Currently executing high priority interrupt |
| 1 | 1 | Unexpected state, unknown error |

# 10, I / O ports

## About 10.1 GPIO

CH552 provides up to 17 I / O pins, some pins having multiplexed functions. Wherein the input and output ports P1 and P3 are bit addressable. Port P2 is an internal port, only with R0 or R1 when p is selected xRAM MOVX access.

If the pin is not configured to multiplex function, the default is the general purpose I / O pin state. As a general purpose digital I / O Usage, all I / O ports have true "reading - modification - writing" function, support SETB or CLR bit operation instructions and the like independently changing the direction of some of the pin or the port electrically equal.

## 10.2 GPIO register

This section and all bits of the registers in general form: lower case "n" represents the port number (n = 1 or 3), while the number of the lowercase "x" represents the bit number (x = 0,1,2,3, 4,5,6,7).

Table 10.2.1 GPIO register list

| name | address | description | Reset value |
|---|---|---|---|
| P1 | 90h | Input and output ports P1 register | FFh |
| P1_MOD_OC | 92h | Port output mode register P1 | FFh |
| P1_DIR_PU | 93h | P1 and pull-directional control port enable register | FFh |
| P2 | A0h | P2 port output register | FFh |
| P3 | B0h | Register input and output ports P3 | FFh |
| P3_MOD_OC | 96h | Port P3 output mode register | FFh |
| P3_DIR_PU | 97h | P3 port direction control and the pullup enable register | FFh |
| PIN_FUNC | C6h | Pin Function Select Register | 80h |
| XBUS_AUX | A2h | Auxiliary bus setting register | 00h |

**Pn output port The output register (Pn ): Bit**

| | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | Pn.0 ~ Pn.7 | RW | Pn.x input and data output pin state bits, bit addressable | FFh |

**Pn output port A mode register (Pn _MOD_OC ): Bit**

| | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | Pn_MOD_OC | RW | Pn.x pin output mode setting: 0 pull output; open drain output 1- | FFh |

**Pn port side So that the control and pull can register (Pn_DIR_PU):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | Pn_DIR_PU | RW | Pn.x pin direction is controlled in push-pull mode:<br>0- input; 1- outputs;<br>In the open drain output mode is Pn.x pull pin resistor enable: 0- pullup disabled;<br>1 - enables pull-up resistor | FFh |

A Pn_MOD_OC [x] and Pn_DIR_PU [x] Related Pn port combination thereof, as follows.

Table 10.2.2 compositions port configuration register

| Pn_MOD_OC | Pn_DIR_PU | Operating modes are described |
|---|---|---|
| 0 | 0 | High impedance input mode, pins does not pull |
| 0 | 1 | Push-pull mode with a symmetrical drive capability, output, or can absorb a large current |

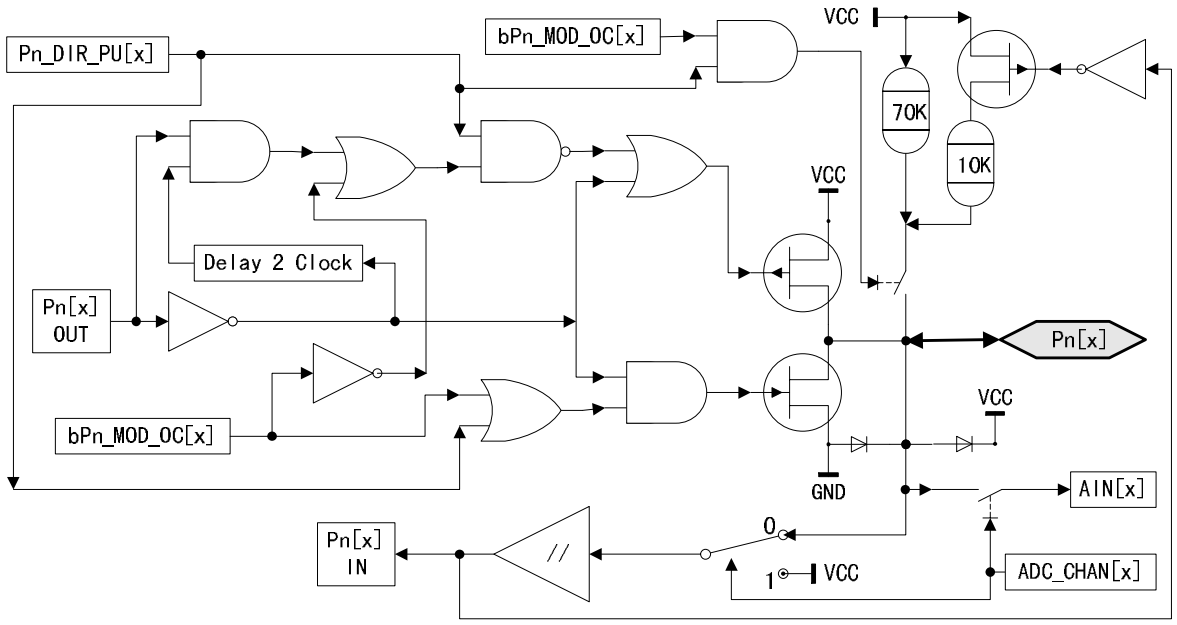
| | | |
|---|---|---|
| 1 | 0 | Open drain, high impedance input support pin does not pull |
| 1 | 1 | Quasi-bidirectional mode (standard 8051), open-drain output, input support pin pull-up resistor, a high level when the output from the low rotation automatically driven high for two clock cycles to speed up the conversion |

P1 and P3 input ports support a pure or quasi-push-pull output and bidirectional modes. Pull-up resistor inside each pin has freely controlled, and the protection diode are connected to the VCC and GND.

FIG 10.2.1 P1.x is equivalent diagram pins P1 port, after removing the AIN may be adapted to the port P3. FIG V33 to VCC after suitable P3.6 and P3.7, P3.6 and P3.7 i.e. the pull or only to the input or the output high voltage V33.

P3.6 and P3.7 optionally standard pull-up resistor (to V33), 15KΩ pull-down resistor, in which a pin, or providing a strong pull-up resistor 1.5KΩ (to V33). Standard pull-up resistor that is only bUSB_IO_EN = 0 GPIO mode active, controlled by bits 7 6 P3_DIR_PU; a pull-down resistor when the bUD_PD_DIS bUC_RESET_SIE = 0 control, regardless of bUSB_IO_EN; pull-up resistor to the pull-down resistor 1.5KΩ precedence strong, in bUC_DEV_PU_EN bUC_RESET_SIE = 0 when the control, regardless of bUSB_IO_EN.

FIG 10.2.1 I / O Pin Equivalent Schematic




10.4 GPIO multiplexing and mapping

CH552 portion I / O pins having multiplexed functions after power-on default are general-purpose I / O pins, after enabling different functional modules, the respective pins are configured as respective functions of the function corresponding to the module pins.

**Pin Gong Can select register (PIN_FU NC):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUSB_IO_EN | RW | USB UDP / UDM pin enable bit, this bit is 0 P3.6 / P3.7 to the GPIO, pull-up resistor control P3_DIR_PU support, support P3_MOD_OC; this bit is 1, P3.6 / P3.7 for UDP / UDM, controlled by the USB module, P3_DIR_PU and P3_MOD_OC its invalid | 1 |
| 6 | bIO_INT_ACT | R0 | GPIO interrupt request active:<br>When bIE_IO_EDGE = 0, the bit is 1, the GPIO input active level, the interrupt request as a level 0 indicates that the input is invalid; when bIE_IO_EDGE = 1, the interrupt flag bit as an edge, showing the subject 1<br>Measured valid edge, the bit can not be cleared by software, only when the level of the reset or | 0 |

| | | | | |
|---|---|---|---|---|
| | | | Off mode, or enter the corresponding is automatically cleared when the interrupt service routine | |
| 5 | bUART1_PIN_X | RW | Pin Mapping UART1 enable bit, this bit is 0 RXD1 / TXD1 use P1.6 / P1.7; the bit is a RXD1 / TXD1 use P3.4 / P3.2 | 0 |
| 4 | bUART0_PIN_X | RW | UART0 Pin Mapping enable bit, this bit using P3.0 / P3.1 is 0 RXD0 / TXD0; the bit is a RXD0 / TXD0 use P1.2 / P1.3 | 0 |
| 3 | bPWM2_PIN_X | RW | Pin Mapping PWM2 enable bit, this bit is 0 PWM2 used on P3.4; the bit is 1 P3.1 using PWM2 | 0 |
| 2 | bPWM1_PIN_X | RW | Pin Mapping PWM1 enable bit, this bit is 0 PWM1 use P1.5; PWM1 this bit is 1, use P3.0 | 0 |
| 1 | bT2EX_PIN_X | RW | T2EX / CAP2 Pin Mapping Enable bit, which is used P1.1 0 T2EX / CAP2; using the RST bit of a T2EX / CAP2 | 0 |
| 0 | bT2_PIN_X | RW | T2 / CAP1 Pin Mapping Enable bit, which is used P1.0 0 T2 / CAP1; this bit is 1, T2 / CAP1 use P1.4 | 0 |

Table 10.4.1 GPIO pin multiplexing function list

| GPIO | Other features: the priority order from left to right |
|---|---|
| RST | RST, bT2EX_, bCAP2_, bRST |
| P1 [0] | T2 / bT2, CAP1 / bCAP1, TIN0, P1.0 |
| P1 [1] | T2EX / bT2EX, CAP2 / bCAP2, TIN1, VBUS2, AIN0, P1.1 |
| P1 [2] | XI, RXD_ / bRXD_, P1.2 |
| P1 [3] | XO, TXD_ / bTXD_, P1.3 |
| P1 [4] | T2_ / bT2_, CAP1_ / bCAP1_, SCS / bSCS, TIN2, UCC1, AIN1, P1.4 |
| P1 [5] | MOSI / bMOSI, PWM1 / bPWM1, TIN3, UCC2, AIN2, P1.5 |
| P1 [6] | MISO / bMISO, RXD1 / bRXD1, TIN4, P1.6 |
| P1 [7] | SCK / bSCK, TXD1 / bTXD1, TIN5, P1.7 |
| P3 [0] | PWM1_ / bPWM1_, RXD / bRXD, P3.0 |
| P3 [1] | PWM2_ / bPWM2_, TXD / bTXD, P3.1 |
| P3 [2] | TXD1_ / bTXD1_, INT0 / bINT0, VBUS1, AIN3, P3.2 |
| P3 [3] | INT1 / bINT1, P3.3 |
| P3 [4] | PWM2 / bPWM2, RXD1_ / bRXD1_, T0 / bT0, P3.4 |
| P3 [5] | T1 / bT1, P3.5 |
| P3 [6] | UDP / bUDP, P3.6 |
| P3 [7] | UDM / bUDM, P3.7 |

On the table from left to right in order of priority, it refers to the order of precedence when a plurality of functional modules compete for the GPIO. For example, when the TXD serial transmission time for P3.1, P3.0 still be used for higher priority PWM1 output.

## 11, external bus

CH552 chip bus is not available to the external signal, the external bus is not supported, but can be accessed xRAM normal chip.

**external total Auxiliary line setting register Device (XBUS_ AUX):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUART0_TX | R0 | UART0 transmission status indication, and 1 represents the process of being sent | 0 |
| 6 | bUART0_RX | R0 | UART0 indicating reception status of 1 indicates the process of being received | 0 |

| | | | | |
|---|---|---|---|---|
| 5 | bSAFE_MOD_ACT | R0 indicates the state security mode, 1 indicates the current mode is safe | | 0 |
| 4 | Retention | RO reserved. | | 0 |
| 3 | GF2 | RW GM flag 2: Users can define their own, can be set or cleared by software | | 0 |
| 2 | bDPTR_AUTO_INC | Enable automatic DPTR RW 1 after the completion of the instruction MOVX_ @ DPTR | | 0 |
| 1 | Retention | RO reserved. | | 0 |
| 0 | DPS | RW dual data pointer DPTR select bit:<br>This bit is 0 DPTR0 is selected; the selected bit is 1 DPTR1 | | 0 |

# 12, timer Timer

## 12.1 Timer0 / 1

Timer0 / 1 is a two 16-bit timer / counter, and is configured by TCON TMOD Timer0 and the Timer1, TCON for timer / counters T0 and T1 of the start control and the external interrupt control overflow interrupt. Each timer is timing unit 16 consists of two 8-bit registers thereof. Timer 0 is the high byte of the counter TH0, TL0 is the low byte; high byte of the timer counter 1 is TH1, the low byte is TL1. Timer 1 can also be used as UART0 baud rate generator.

Table 12.1.1 Timer0 / 1 listing the relevant register

| name | address | description | Reset value |
|---|---|---|---|
| TH1 | 8Dh | Timer1 high byte count | xxh |
| TH0 | 8Ch | Timer0 high byte count | xxh |
| TL1 | 8Bh | Timer1 counter low byte | xxh |
| TL0 | 8Ah | Low byte count Timer0 | xxh |
| TMOD | 89h | Timer0 / 1 mode register | 00h |
| TCON | 88h | Timer0 / 1 Control Register | 00h |

**timing / Counter control 0/1 Storage system Unit (TCON):**

| Place | name access | | description | Reset value |
|---|---|---|---|---|
| 7 | TF1 | RW | Timer1 overflow interrupt flag is automatically cleared after entering the timer interrupt 1 | 0 |
| 6 | TR1 | RW | Timer1 start / stop bits, set to start, set or cleared by software | 0 |
| 5 | TF0 | RW | Automatically cleared after Timer0 overflow interrupt flag, the timer 0 interrupt | 0 |
| 4 | TR0 | RW | Timer0 start / stop bits, set to start, set or cleared by software | 0 |
| 3 | IE1 | RW | INT1 external interrupt 1 request flag is automatically cleared after entering the interrupt | 0 |
| 2 | IT1 | RW | INT1 external interrupt trigger control bit 1, bit 0 of the external interrupts is level-triggered; the bit is 1 External interrupt falling edge triggered | 0 |
| 1 | IE0 | RW | 0 INT0 external interrupt request flag bit is automatically cleared after entering the interrupt | 0 |
| 0 | IT0 | RW | External Interrupt 0 INT0 trigger mode control bit, the bit is 0 is level-triggered external interrupts; the bit is 1 External interrupt falling edge triggered | 0 |

**timing / Counter 0/1 square Type Storage Device (TMOD):**

| Place | name access | | description | Reset value |
|---|---|---|---|---|
| 7 | bT1_GATE | RW | Gate Enable bit, control Timer1 start if affected by external interrupt signal INT1 is. This bit is 0 timer / counter 1 is started and regardless of INT1; this bit is 1 only INT1 pin is high and TR1 to start to 1:00 | 0 |
| 6 | bT1_CT | RW | timing or counting mode selection bit, which is operating in a timing mode 0; the bit is 1 Falling edge of the count mode, used as a clock pin T1 | 0 |

| | | | | |
|---|---|---|---|---|
| 5 | bT1_M1 | RW | timer / counter 1 selects high mode | 0 |
| 4 | bT1_M0 | RW | timer / counter 1 Mode Select Low | 0 |
| 3 | bT0_GATE | RW | Gate Enable bit, start Timer0 control whether affected by external interrupt signal INT0 is. This bit is 0 Timer / counter 0 regardless of whether to initiate the INT0; this bit is 1 only INT0 pin is high and TR0 is set to 1 to start | 0 |
| 2 | bT0_CT | RW | timing or counting mode selection bit, which is operating in a timing mode 0; the bit is 1 Falling edge of the count mode, using the pin as a clock T0 | 0 |
| 1 | bT0_M1 | RW | timer / counter 0 select high mode | 0 |
| 0 | bT0_M0 | RW | timer / counter 0 Mode Select Low | 0 |

Table 12.1.2 bTn_M1 bTn_M0 and operating mode selection Timern (n = 0,1)

| bTn_M1 | bTn_M0 | Timern operating mode (n = 0,1) |
|---|---|---|
| 0 | 0 | 0:13 mode bit timer / counter n, the lower 5 bits of the counting unit and TLn THn composition of three high TLn invalid. Becomes 0 when the count is full, the TFn overflow flag is set, and needs to be reset from the initial value 13 all 1 |
| 0 | 1 | 1:16 mode bit timer / counter n, a counting unit and TLn THn composition. Becomes 0 when the count is full, the TFn overflow flag is set, and needs to be reset from the initial values are all 16-bit 1 |
| 1 | 0 | Mode 2: 8-bit reload timer / counter n, using the counting unit TLn, THn counting unit as a heavy load. Count is changed from 1 to 8 full full 0, the TFn overflow flag is set, and automatically loads the initial value THn from |
| 1 | 1 | Mode 3: If a timer / counter 0, the timer / counter 0 is divided into two parts TL0 and TH0, TL0 as an 8-bit timer / counter, occupies all of the control bits of Timer0; TH0 and do another 8-bit timer use, occupation Timer1 of TR1, TF1 and interrupt resources, and this time Timer1 still available, but can not use the control bit TR1 and overflow flag TF1. If timer / counter 1, then enter mode 3 will stop the timer / counter 1. |

**Timern meter The low byte (TL n ) (N = 0 ,1):**

| Place | name access | | description | Reset value |
|---|---|---|---|---|
| [7: 0] | TLn | RW | Low byte count Timern | xxh |

**Timern meter High byte number (TH n ) (N = 0 ,1):**

| Place | name access | | description | Reset value |
|---|---|---|---|---|
| [7: 0] | THn | RW | High Byte count Timern | xxh |

## 12.2 Timer2

Timer2 is 16-bit auto-reload timer / counter, and configured through T2CON T2MOD register, the timer counter high byte 2 is TH2, the low byte is TL2. Timer2 as UART0 baud rate generator further includes a two-way signal level capture, the capture count is stored in register RCAP2 and T2CAP1.

Table 12.2.1 Timer2 relevant register list

| name | address | description | Reset value |
|---|---|---|---|
| TH2 | CDh | Timer2 counter high byte | 00h |
| TL2 | CCh | Timer2 Counter Low | 00h |
| T2COUNT | CCh | TL2 and TH2 composed of 16 SFR | 0000h |
| T2CAP1H | CFh | Timer2 capture a high byte data (read-only) | xxh |
| T2CAP1L | CEh | Timer2 capture a low-byte data (read only) | xxh |
| T2CAP1 | CEh | T2CAP1L and T2CAP1H composed of 16 SFR | xxxxh |

| | | | |
|---|---|---|---|
| RCAP2H | CBh reload count / capture data register 2 high byte | | 00h |
| RCAP2L | CAh reload count / capture data register 2 low byte | | 00h |
| RCAP2 | CAh | RCAP2L and RCAP2H composed of 16 SFR | 0000h |
| T2MOD | C9h | Timer2 mode register | 00h |
| T2CON | C8h | Timer2 Control Register | 00h |

timing / Counter control register 2 Register ( T2CON):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | TF2 | RW | When bT2_CAP1_EN = 0, Timer2 overflow interrupt flag is, when the count becomes Timer2 from 16 to 1:00 full, the overflow flag is set to 1, the software needs to be cleared is full; when RCLK = 1 or TCLK = 1 when this bit will not be set | 0 |
| 7 | CAP1F | RW | When bT2_CAP1_EN = 1, an interrupt flag is Timer2 capture, by the effective T2 Edge trigger, the software needs to be cleared | 0 |
| 6 | EXF2 | RW | Timer2 external trigger flag, when the valid edge EXEN2 = 1 T2EX triggered by the set, the software needs to be cleared | 0 |
| 5 | RCLK | RW | UART0 receive clock selection, the selected bit is 0 Timer1 overflow pulse generating baud rate; it is 1 for Timer2 overflow pulses generated baud | 0 |
| 4 | TCLK | RW | UART0 transmit clock selection, the selected bit is 0 Timer1 overflow pulse generating baud rate; it is 1 for Timer2 overflow pulses generated baud | 0 |
| 3 | EXEN2 | RW | T2EX trigger enable bit, this bit is ignored T2EX 0; bit to 1 enables the trigger active edge overloaded or when capturing T2EX | 0 |
| 2 | TR2 | RW | Timer2 start / stop bits, set to start, set or cleared by software | 0 |
| 1 | C_T2 | RW | Timer2 clock source select bit, the bit is 0 using the internal clock; the bit is 1 based falling edge pin count T2 | 0 |
| 0 | CP_RL2 | RW | Timer2 function select bit, if RCLK or TCLK is 1, the bit should be forced to zero. This bit is 0 Timer2 timer / event counter, and automatically reload the initial count value when the counter overflows or T2EX level change; this bit to 1 enables capture of Timer2 2 functions to capture the valid edge T2EX | 0 |

timing / 2 mode Send Counter Register ( T2MOD):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bTMR_CLK | RW | Selected fast clock T0 / T1 / T2 timer mode enable fastest clock, the bit is a system using frequency division Fsys not as a count clock; the bit is 0, use frequency-divided clock. This bit has no effect on the selection criteria clock timer | 0 |
| 6 | bT2_CLK | RW | Timer2 internal clock select bit, the bit is 0 is selected from the standard clock, timer / counter mode Fsys / 12, UART0 clock mode Fsys / 4; bit = 1, selected from fast clock, timer / counter mode Fsys / 4 (bTMR_CLK = 0) or Fsys (bTMR_CLK = 1), UART0 clock mode Fsys / 2 (bTMR_CLK = 0) or Fsys (bTMR_CLK = 1) | 0 |
| 5 | bT1_CLK | RW | Timer1 internal clock frequency selection bit, which is selected from 0 standard clock Fsys / 12; 1 is selected from the fast clock Fsys / 4 (bTMR_CLK = 0) or Fsys (bTMR_CLK = 1) | 0 |
| 4 | bT0_CLK | RW | Timer0 internal clock frequency selection bit, which is selected from 0 standard clock Fsys / 12; 1 is selected from the fast clock Fsys / 4 (bTMR_CLK = 0) or Fsys (bTMR_CLK = 1) | 0 |

| | | | | | |
|---|---|---|---|---|---|
| 3 | bT2_CAP_M1 | RW | High Timer2 capture mode Capture mode selection:<br>X0: 01 from falling edge to falling edge: from any direction to an arbitrary direction, i.e. the level change 11: from a rising edge to rising edge | | 0 |
| 2 | bT2_CAP_M0 | RW | Timer2 Capture mode Low | | 0 |
| 1 | T2OE | RW | Timer2 clock output enable bit, which disables the output is 0; bit 1 of the half clock enable output pin T2, Timer2 overflow rate frequency | | 0 |
| 0 | bT2_CAP1_EN | RW | When RCLK = 0, TCLK = 0, CP_RL2 = 1, C_T2 = 0, T2OE = 0 when capturing a mode is enabled, the enable bit capture function captures an active edge of a T2; the bit is disabled 0 1 Capture | | 0 |

**Count overloading / Data Capture 2 Deposit Device (RCAP2):**

| Bit | Name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | RCAP2H | RW | is the high byte of the reload value in the timer / counter mode; is in the capture mode CAP2 captured timer high byte | 00h |
| [7: 0] | RCAP2L | RW | is the low byte of the reload value in the timer / counter mode; is in the capture mode CAP2 captured timer low byte | 00h |

**Timer2 count Number of device (T2CO U NT):**

| Bit | Name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | TH2 | RW | current counter high byte | 00h |
| [7: 0] | TL2 | RW | current counter low byte | 00h |

**1 Timer2 capture data (T 2CAP1 ): Bit**

| Name | access | description | Reset value |
|---|---|---|---|
| [7: 0] T2CAP1H | RO | CAP1 captured timer high byte | xxh |
| [7: 0] T2CAP1L | RO | CAP1 captured timer low byte | xxh |

12.3 PWM function

CH552 provides two 8-bit PWM, PWM can select the default output is low or high polarity, can be dynamically modified PWM output duty cycle is, by integrating a simple RC low-pass filtering the resistor capacitor can obtaining various output voltages, corresponding to the low speed digital to analog converter DAC.

**Output duty = PWM1 PWM_DATA1 / 256, supports a range of 0% to 99.6%. PWM2 output duty = PWM_DATA2 / 256,** supports a range of 0% to 99.6%. In practice, it is recommended to allow PWM output pin PWM output pin and arranged push-pull mode.

12.3.1 PWM1 and PWM2

Table 12.3.1 PWM1 and PWM2 relevant register lists

| name | address | description | Reset value |
|---|---|---|---|
| PWM_CK_SE | 9Eh | Clock Divider PWM setting register | 00h |
| PWM_CTRL | 9Dh | PWM Control Register | 02h |
| PWM_DATA1 | 9Ch | PWM1 data register | xxh |
| PWM_DATA2 | 9Bh | PWM2 data register | xxh |

PWM2 data Register (PWM_DAT A2):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | PWM_DATA2 | RW | PWM2 current data storage,<br>PWM2 output active level duty ratio = PWM_DATA2 / 256 | xxh |

PWM1 data Register (PWM_DAT A1):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | PWM_DATA1 | RW | PWM1 current data storage,<br>PWM1 output active level duty ratio = PWM_DATA1 / 256 | xxh |

PWM control System register (PWM_CTR L ): Bit

| | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bPWM_IE_END | RW | This bit is 1 so that the end of the PWM cycle or buffer empty interrupt MFM | 0 |
| 6 | bPWM2_POLAR | RW | The control PWM2 output polarity, the bit is 0, the default low, there is a high level<br>Effect; the bit is a default high, active low | 0 |
| 5 | bPWM1_POLAR | RW | The control PWM1 output polarity, the bit is 0, the default low, there is a high level<br>Effect; the bit is a default high, active low | 0 |
| 4 | bPWM_IF_END | RW | Clear the PWM cycle end interrupt flag bit, which is 1 means interrupt, write 1 to clear<br>or reload the data PWM_DATA1 | 0 |
| 3 | bPWM2_OUT_EN | RW | PWM2 output enabled, this bit to 1 enables PWM2 output | 0 |
| 2 | bPWM1_OUT_EN | RW | PWM1 output enabled, this bit to 1 enables the output PWM1 | 0 |
| 1 | bPWM_CLR_ALL | RW | This bit is cleared to a count PWM1 and PWM2 and FIFO, the software needs to be cleared | 1 |
| 0 | Retention | RO | reserved. | 0 |

PWM clock divided Frequency setting register ( PWM_C K_SE):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | PWM_CK_SE | Set RW | PWM clock divider divisor | 00h |

12.4 Timer Function

12.4.1 Timer0 / 1

(1) Timer setting T2MOD selected internal clock frequency, if bTn_CLK (n = 0/1) clock corresponding to 0, then the Timer0 / 1

Is Fsys / 12; if bTn_CLK is 1, or a bTMR_CLK = 0 1 Select Fsys / 4 or Fsys as the clock. (2), the working mode setting TMOD the Timer.

0:13 mode bit timer / counter

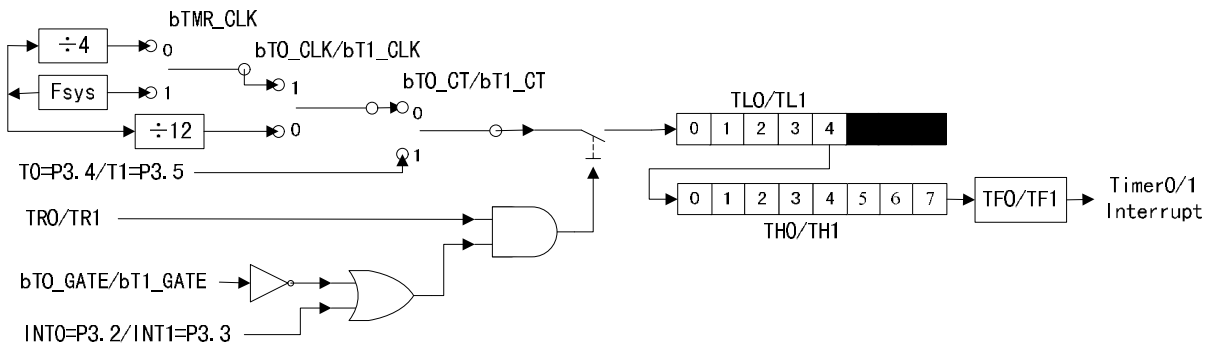


FIG 12.4.1.1 Timer0 / 1 Mode 0

1:16 mode bit timer / counter

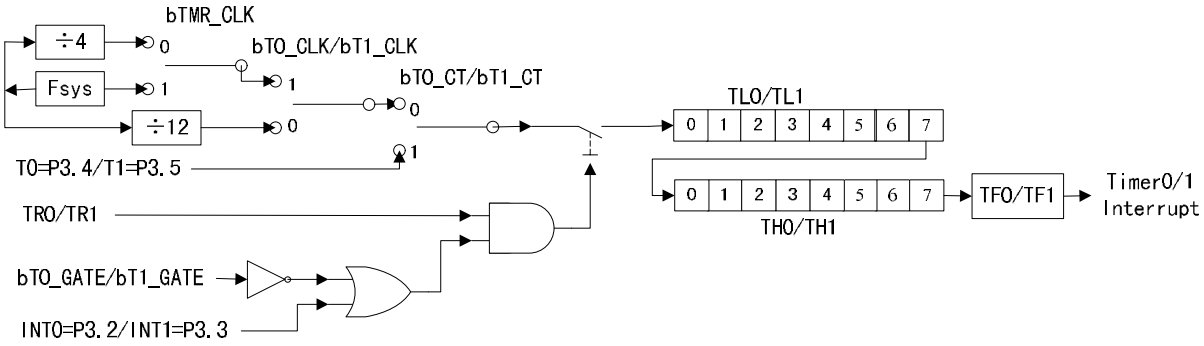



FIG 12.4.1.2 Timer0 / 1 Mode 1

Mode 2: 8 auto-reload timer / counter

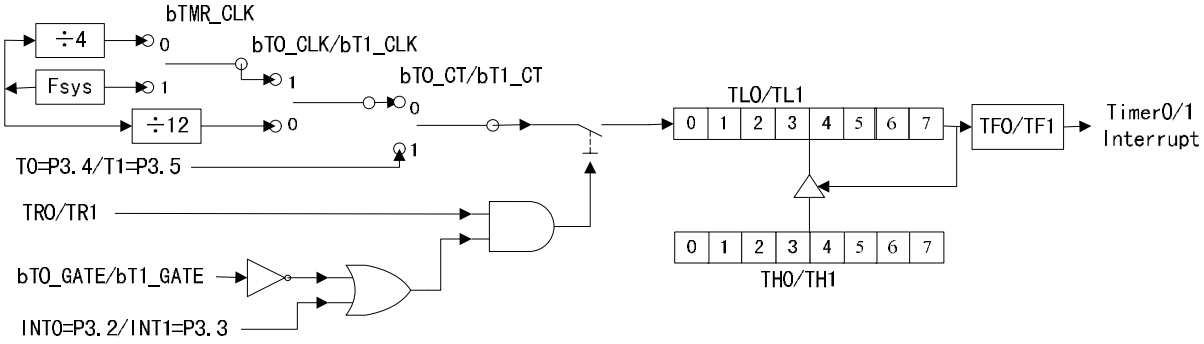



FIG 12.4.1.3 Timer0 / 1 Mode 2

Mode 3: Timer0 into two separate 8-bit Timer / counter, borrow and control bits of Timer1 TR1; TR1 Timer1 replaced by control bits are borrowed whether to activate the mode 3, mode 3 enters Timer1 Timer1 is stopped.

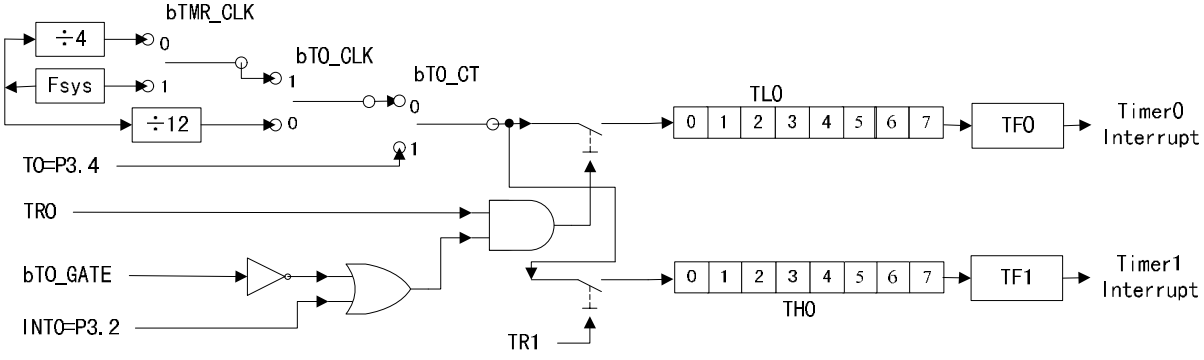



FIG 12.4.1.4 Timer0 mode 3

(3), set the timer / counter and the initial value TLn THn (n = 0/1).

(4) is provided in the TCON bits TRn (n = 0/1) on or stop timer / counter can be (n = 0/1), or inquiry by bit through TFn

Through the interrupt is detected.

### 12.4.2 Timer2

Timer2 16-bit reload timer / counter mode:

(1), set the bit in the RCLK and TCLK T2CON are 0, the non-selected baud rate generator mode. (2), provided in T2CON C_T2 bit 0 is selected using the internal clock, go to step (3); 1 can also be set to select the falling edge of pin T2

As the count clock, skip step (3).

(3), provided T2MOD select Timer internal clock frequency, if bT2_CLK is 0, then the clock Timer2 Fsys / 12; such as

If bT2_CLK is 1, then a 1 or bTMR_CLK = 0 Select Fsys / 4 or Fsys as the clock. (4), provided T2CON CP_RL2 bit to 0 to select the 16-bit reload timer Timer2 / counter functions. (5), and RCAP2H RCAP2L set to reload the timer overflow value is set as the value of the timer TL2 and TH2 (generally with

RCAP2L and RCAP2H same), to a set TR2, open Timer2. (6), or by querying the timer 2 interrupt TF2 can obtain the current timer / counter status.

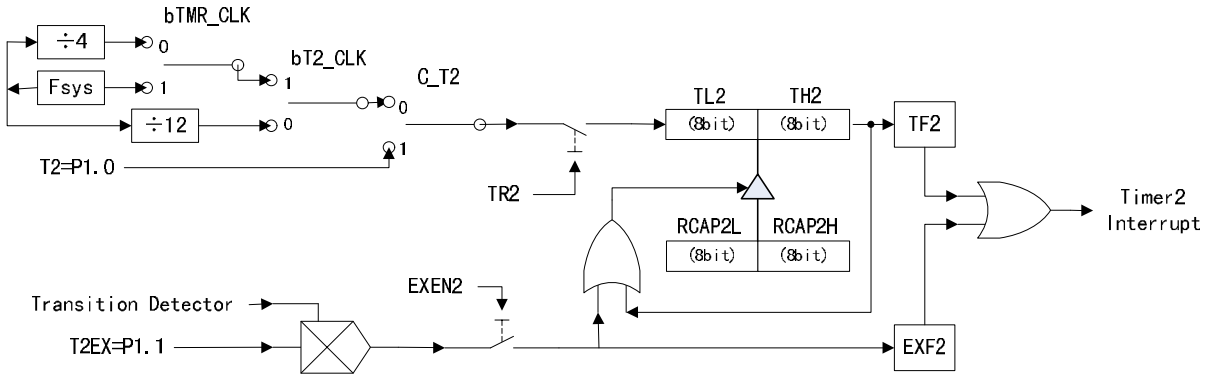



FIG 12.4.2.1 Timer2 16-bit reload timer / counter

Timer2 clock output mode:

Reference 16-bit reload timer / counter mode, and then set the bit in T2OE T2MOD is 1, so that from the output pin T2 TF2 clock frequency divided by two.

Timer2 serial baud rate generator mode 0:

(1), is provided in T2CON C_T2 0 to select the internal clock may be set to 1 to select the falling edge of the clock pin T2, root

It needs to be set in T2CON TCLK and RCLK is one bit or 1 1 wherein selecting the baud rate generator mode. (2), provided T2MOD select Timer internal clock frequency, if bT2_CLK is 0, then the clock Timer2 Fsys / 4; as

If bT2_CLK is 1, then a 1 or bTMR_CLK = 0 Select Fsys / 2 or Fsys clock. (3), and RCAP2H RCAP2L set value for the reload timer overflows, 1 is set TR2, open Timer2.

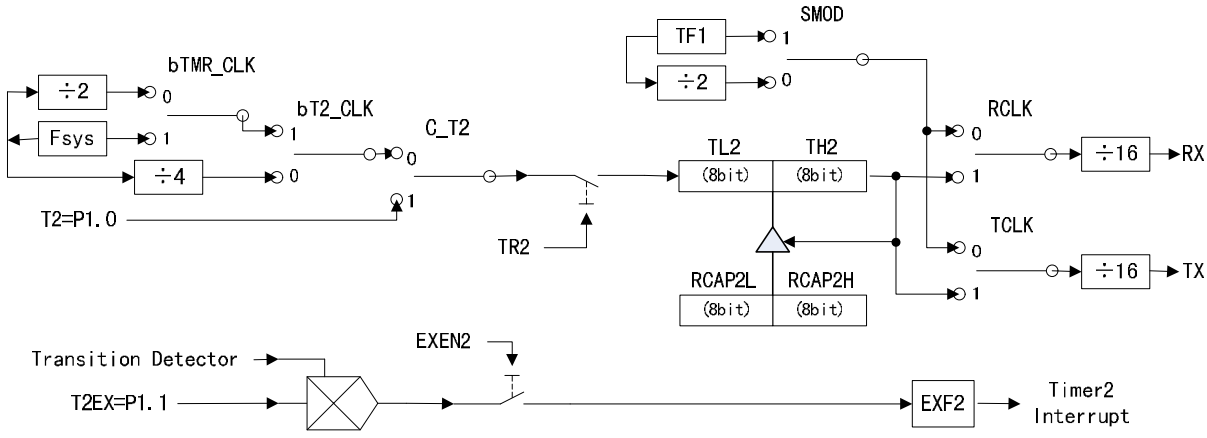



FIG 12.4.2.2 Timer2 UART0 Baud Rate Generator

Timer2 dual channel capture mode:

(1), set the bit in the RCLK and TCLK T2CON are 0, the non-selected baud rate generator mode.

(2), provided in T2CON C_T2 bit 0 is selected using the internal clock, go to step (3); can also be set to select a pin drop T2

Edge as the count clock, skip step (3).

(3), provided T2MOD select Timer internal clock frequency, if bT2_CLK is 0, then the clock Timer2 Fsys / 12; such as

If bT2_CLK is 1, then a 1 or bTMR_CLK = 0 Select Fsys / 4 or Fsys as the clock. (4), and provided T2MOD bT2_CAP_M1 bT2_CAP_M0 selected bit corresponding edge capture mode. (5), a set, selection of T2EX pin Timer2 capture function is CP_RL2 T2CON bit. (6), TL2 and TH2 is set for the value of the timer, set to 1 TR2, open Timer2.

(7), when the capture is completed CAP2, RCAP2L RCAP2H saved time and the count value of TL2 and TH2, and EXF2 set, causing

Interrupt, the difference between the next capture and RCAP2H RCAP2L with the last captured RCAP2L and RCAP2H, signal width is between two valid edges.

(8), if the bit C_T2 T2CON is 0, and the bit bT2_CAP1_EN T2MOD is 1, then the command enables Timer2

Capture of the pin T2, when the CAP1 capturing is complete, T2CAP1L T2CAP1H saved and then the count value TL2 and TH2, and CAP1F set, an interrupt is generated.

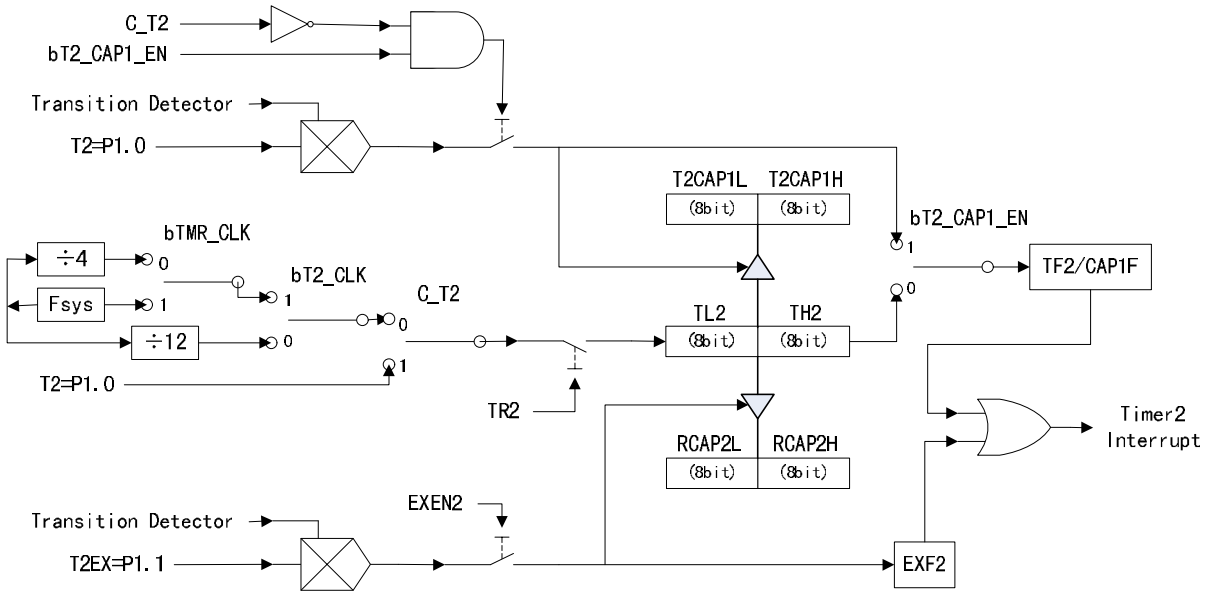



FIG 12.4.2.3 Timer2 capture mode

## 13, UART Universal Asynchronous Receiver Transmitter

### 13.1 UART Profile

CH552 chip provides two serial asynchronous full duplex: UART0 and UART1. CH551 provide UART0 only. MCS51 UART0 standard serial port, which is transmitted and received data access SBUF physically separated by receiving / receive register achieve. SBUF loads the transmit data register is written, for SBUF read operation corresponding to the receive buffer register.

MCS51 serial UART1 is simplified, which receive and send data access SBUF1 are physically separated by receiving / receive register achieve. SBUF1 transmission data write register is loaded, to SBUF1 read operation corresponding to the receive buffer register. Compared UART0 UART1 multiprocessor removed and fixed baud rate communication mode, independent UART1 baud rate generator.

### 13.2 UART Registers

Table 13.2.1 UART-related registers list

| name | address | description | Reset value |
|---|---|---|---|
| SCON | 98h | Control Register UART0 | 00h |
| SBUF | 99h | UART0 data register | xxh |

| | | | |
|---|---|---|---|
| SCON1 | C0h | Control Register UART1 | 40h |
| SBUF1 | C1h | UART1 data register | xxh |
| SBAUD1 | C2h | UART1 baud rate setting register | xxh |

13.2.1 UART0 Register Description

**UART 0 Control register Deposit Device (SC ON):**

| Bit | Name | Access | description | Reset value |
|---|---|---|---|---|
| 7 | SM0 | RW | UART0 operating mode select bit 0, this bit selects 8-bit data is 0 asynchronous communication; the 9-bit data bit asynchronous communication 1 | 0 |
| 6 | SM1 | RW | UART0 operating mode selection bit 1, bit 0 is set to the fixed baud rate; the 1-bit variable baud rate is set, generated by the timer T1 or T2 | 0 |
| 5 | SM2 | RW | UART0 Multiprocessor communication control bits:<br>When Modes 2 and 3 receive data, when 1 SM2 =, if RB8 is 0, then RI is not set, the received valid; if RB8 is 1, then RI is set, the reception is valid; SM2 = 0, regardless RB8 is 0 or 1, are set to receive data bits RI, receiving active; when a mode 1, if SM2 = 1, then only receives a valid stop bit, the reception is valid;<br>When mode 0, SM2 bit must be set to 0 | 0 |
| 4 | REN | RW | UART0 allowed to receive a control bit, which is 0 receive disabled; 1 to this bit allows the receiver | 0 |
| 3 | TB8 | RW | 9th bit transmission data in Mode 2 and 3, TB8 for writing the 9th bit transmission data, a parity bit may be; in a multi-machine communication, is used to represent the host address byte sent or data bytes, TB8 = 0 data, TB8 = 1 address | 0 |
| 2 | RB8 | RW | 9th bit received data, and the mode 2. 3, 9th bit RB8 for storing received data; when the mode 1, if SM2 = 0, then the RB8 for storing the received stop bit; In Mode 0 do not use RB8 | 0 |
| 1 | TI | RW | transmit interrupt flag, a data byte is sent after the set by hardware, software needs to clear zero | 0 |
| 0 | RI | RW | receive interrupt flag bit, a byte of data received valid set by hardware, software needed Clear | 0 |

Table 13.2.1.1 UART0 mode selection

| SM0 | SM1 | description |
|---|---|---|
| 0 | 0 | 0 mode, the shift register mode, the baud rate is fixed Fsys / 12 0 |
| | 1 | 8-bit asynchronous communication mode, baud rate variable, generated by the timer T1 or T2 1 |
| | 2,9 | 0-bit asynchronous communication mode, the baud rate is Fsys / 128 (SMOD = 0) or Fsys / 32 (SMOD = 1) 1 |
| | 3,9 | 1-bit asynchronous communication mode, baud rate variable, generated by the timer T1 or T2 |

In mode 1 and 3, when RCLK = 0 and when TCLK = 0, the UART0 baud rate is generated by the timer T1. T1 should be set to Mode 2 8 with automatic reload timer mode, bT1_CT bT1_GATE and must both be 0, the following categories clock case.

table 13.2.1.2 Generating calculated by T1 UART0 baud

| bTMR_CLK | bT1_CLK | SMOD | description |
|---|---|---|---|
| 1 | 1 | 0 | TH1 = 256 - Fsys / 32 / baud |
| 1 | 1 | 1 | TH1 = 256 - Fsys / 16 / baud |
| 0 | 1 | 0 | TH1 = 256 - Fsys / 4/32 / baud |
| 0 | 1 | 1 | TH1 = 256 - Fsys / 4/16 / baud |

| | | | |
|---|---|---|---|
| X | 0 | 0 | TH1 = 256 - Fsys / 12/32 / baud |
| X | 0 | 1 | TH1 = 256 - Fsys / 12/16 / baud |

In mode 1 and 3, when RCLK = 1 or TCLK = 1, UART0 baud rate is generated by the timer T2. T2 should be set to 16-bit baud rate generator auto-reload mode, C_T2 CP_RL2 and must both be 0, the following categories clock case.

Table 13.2.1.3 UART0 baud rate is generated by the formula T2

| bTMR_CLK | bT2_CLK | description |
|---|---|---|
| 1 | 1 | RCAP2 = 65536 - Fsys / 16 / baud |
| 0 | 1 | RCAP2 = 65536 - Fsys / 2/16 / baud |
| X | 0 | RCAP2 = 65536 - Fsys / 4/16 / baud |

**UART0 data Register (SBU F): Bit**

| | name access | | description | Reset value |
|---|---|---|---|---|
| [7: 0] | SBUF | RW | UART0 data register, including sending and receiving on two physically separate register. Transmitting data corresponding to the write data register to SBUF; SBUF corresponding to read data from the receive data register | xxh |

13.2.2 UART1 Register Description

**UART 1 Control register Deposit Device (SC ON1):**

| Bit | Name | Access | description | Reset value |
|---|---|---|---|---|
| 7 | U1SM0 | RW | UART1 operating mode selection bit, which selects 8-bit asynchronous communication of data is 0; bit selects the 9-bit data of asynchronous communication 1 | 0 |
| 6 | Reserved | RO | reserved. | 1 |
| 5 | U1SMOD | RW | Select UART1 baud rate: 0 slow mode; 1- Quick mode | 0 |
| 4 | U1REN | RW | Allow UART1 receive control bit, the bit is 0 receive disabled; 1 to this bit allows the receiver | 0 |
| 3 | U1TB8 | RW | ninth bit transmission data, when the 9-bit data patterns, TB8 for writing the first data transmission 9, may be a parity bit; in the 8-bit mode, ignoring TB8 | 0 |
| 2 | U1RB8 | RW | 9th bit of the received data, in the 9-bit mode, RB8 for storing a first received data 9; when 8-bit mode, RB8 for storing the received stop bit | 0 |
| 1 | U1TI | RW | transmit interrupt flag, a data byte is sent after the set by hardware, software needs to clear zero | 0 |
| 0 | U1RI | RW | receive interrupt flag bit, a byte of data received valid set by hardware, software needed Clear | 0 |

UART1 baud rate is set by SBAUD1 generated, divided into two types according to U1SMOD selection:

When U1SMOD = 0 when, SBAUD1 = 256 - Fsys / 32 / baud; when U1SMOD = 1, SBAUD1 = 256 - Fsys / 16 / baud rate.

**UART1 data Register (SBU F 1):**

| Place | name access | | description | Reset value |
|---|---|---|---|---|
| [7: 0] | SBUF1 | RW | UART1 data register, including sending and receiving on two physically separate register. SBUF1 corresponding to write data to the transmit data register; SBUF1 corresponding to read data from the receive data register | xxh |

13.3 UART applications

UART0 Application:

(1) Select UART0 baud rate generator may be selected from the timer T1 or T2, and configure counter. (2), starts a timer T1 or T2.

(3), provided the SCON SM0, SM1, SM2 select the operating mode of the serial port 0. REN set to 1, enables the UART0 reception. (4), you can set the serial port interrupt or visit RI and TI interrupt status.

(5), read SBUF achieve serial data transceiver, allowing serial receive baud rate error signal is less than 2%.

UART1 Application:

(1) The baud rate and set the selected U1SMOD SBAUD1.

(2), provided the U1SM0 SCON1 port 1 mode selection. U1REN set to 1, enables the UART1 reception. (3), you can set the serial port 1 interrupt or visit U1RI and U1TI interrupt status.

(4), a reader SBUF1 achieve serial data transceiver, allowing serial receive baud rate error signal is less than 2%.

## 14, a synchronous serial interface SPI

### 14.1 SPI Introduction

CH552 chip provides SPI interface for high-speed synchronous data transfer between peripherals. (1), supports the master mode and the slave master slave mode; (2), and a support mode 0 mode clock mode 3; (3), an optional wire 3 wire full-duplex or half-duplex mode 2; (4), Alternatively transmitted MSB first or LSB lower upper first transmission; (5), the clock frequency is adjustable up to nearly half the system frequency; and (6), built 1 byte 1 byte receive FIFO and transmit FIFO;

(7), from the first byte of the machine support mode preload data for the host to get the first byte of data is returned immediately.

### 14.2 SPI register

Table 14.2.1 SPI associated register list

| name | address | description | Reset value |
|---|---|---|---|
| SPI0_SETUP | FCh | SPI0 setting register | 00h |
| SPI0_S_PRE | FBh | SPI0 slave mode preset data register | 20h |
| SPI0_CK_SE | FBh | SPI0 clock divider setting register | 20h |
| SPI0_CTRL | FAh | Control Register SPI0 | 02h |
| SPI0_DATA | F9h | SPI0 data transceiver register | xxh |
| SPI0_STAT | F8h | Status Register SPI0 | 08h |

**SPI0 Setting register (SPI0_S E TUP)** :

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bS0_MODE_SLV | RW | SPI0 master-slave mode selection bit, which is 0 SPI0 master mode; SPI0 this bit is a mode of machine / device mode from | 0 |
| 6 | bS0_IE_FIFO_OV | RW | slave mode FIFO overflow interrupt enable bit, this bit to 1 enables FIFO Overflow Interrupt; bit is 0 the FIFO overflow interrupt is not generated | 0 |
| 5 | bS0_IE_FIRST | RW | Receiving the first byte of the slave mode complete interrupt enable bit, an interrupt is triggered when the first data byte received from the slave mode to the 1 bit; does not generate an interrupt when this bit 0 is the first byte of the received | 0 |

| | | | | |
|---|---|---|---|---|
| 4 | bS0_IE_BYTE | RW | data byte transfer complete interrupt enable bit, this bit allows complete transmission of 1 byte To interrupt; the bit is 0 byte transfer completion interrupt is not generated | 0 |
| 3 | bS0_BIT_ORDER | RW | bit data byte timing control bits, the MSB bit is 0 the previous high; the bit LSB least significant bit first to a | 0 |
| 2 | Retention | RO | reserved. | 0 |
| 1 | bS0_SLV_SELT | R0 | is selected from the slave mode leaves active state bit, which is 0 indicates that no selected ; This bit is 1, the current state is selected | 0 |
| 0 | bS0_SLV_PRELOAD | R0 | Pre-loading of data from the slave mode status bit, which is 1 indicates that the current in the sheet After the pre-loaded state before the selected valid data has not been transmitted | 0 |

**SPI0 clock Frequency division setting register Device (SPI0 _CK_SE):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | SPI0_CK_SE | | Setting the division ratio of the clock SPI0 RW Host mode | 20h |

**SPI0 slave Mode preset data send Register ( SPI0_S_PRE):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | SPI0_S_PRE | | RW preloaded data transmitted from the first slave mode | 20h |

**SPI0 Control Register (SPI0_C T RL): Bit**

| | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bS0_MISO_OE | RW | SPI0 the MISO output enable control bit, which allows the output to 1; 0 disables the output of the bit | 0 |
| 6 | bS0_MOSI_OE | RW | SPI0 the MOSI output enable control bit, which allows the output to 1; 0 disables the output of the bit | 0 |
| 5 | bS0_SCK_OE | RW | SPI0 The SCK output enable control bit, which allows the output to 1; 0 disables the output of the bit | 0 |
| 4 | bS0_DATA_DIR | RW | SPI0 direction control bit data, the output data bit is 0, as only the write FIFO effective operation, starting a SPI transfer; an input data bit to the write or read FIFO are as active, start a SPI transfer | 0 |
| 3 | bS0_MST_CLK | RW | SPI0 master clock mode control bit, bit 0 of the mode 0, the default idle SCK low level; this bit. 3 is a mode, the default high SCK | 0 |
| 2 | bS0_2_WIRE | RW | SPI0 2-wire half duplex mode enable bit, this bit is 0 3 wire full-duplex mode, including SCK, MOSI, MISO; the bit is a 2-wire half-duplex mode, including SCK, MISO | 0 |
| 1 | bS0_CLR_ALL | RW | This bit is cleared SPI0 1 interrupt flag and FIFO, need to be cleared by software | 1 |
| 0 | bS0_AUTO_IF | RW | Allow the byte enable bit is automatically cleared reception completion interrupt flag by FIFO efficient operation, this bit is automatically cleared one byte received when the FIFO is valid write Complete Interrupt Flag S0_IF_BYTE | 0 |

**SPI0 data A transceiver register (SP I 0_DAT A): Bit**

| | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | SPI0_DATA | FIFO RW | includes two physically separate transmitting and receiving, the read operation corresponding to the contact The FIFO receive data; transmission data corresponding to the write FIFO, the effective read and write operations xxh | |

| | | | | |
|---|---|---|---|---|
| | | | SPI can initiate a transfer | |

**SPI0 Status Register (SPI0_S T AT): Bit**

| | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | S0_FST_ACT | R0 | represents the current state bit is 1, the first byte is received from the slave mode to complete | 0 |
| 6 | S0_IF_OV | RW | Slave mode FIFO overflow flag bit, which is 1 indicates that the FIFO overflow interrupt; the bit is 0, no interrupt. Direct access bit is cleared or write 1 to clear. When bS0_DATA_DIR = 0 when the transmit FIFO empty interrupt trigger; bS0_DATA_DIR = 1 when the receive FIFO is full when triggered by an interrupt | 0 |
| 5 | S0_IF_FIRST | RW | first byte received from the slave mode to complete the interrupt flag bit, which is represented by a Receiving the first byte. Direct access bit is cleared or write 1 to clear | 0 |
| 4 | S0_IF_BYTE | RW | Data byte transfer complete interrupt flag bit, which is represented by a one byte transfer. Direct access bit is cleared by writing a 1 or cleared, or by clearing the FIFO bS0_AUTO_IF = 1 effective operation | 0 |
| 3 | S0_FREE | R0 | SPI0 Idle flag bit, which is 1 indicates that no SPI shift, usually in a neutral period between data bytes | 1 |
| 2 | S0_T_FIFO | R0 | SPI0 transmit FIFO count Valid values are 0 or 1 | 0 |
| 1 | Retention | R0 | Reserved | 0 |
| 0 | S0_R_FIFO | R0 | SPI0 receive FIFO count Valid values are 0 or 1 | 0 |

## 14.3 SPI transport format

SPI Master Mode Mode 0 and Mode 3 supports two transmission formats may be provided by the SPI control register select bit bSn_MST_CLK in SPIn_CTRL, CH552 MISO is always sampled at the rising edge CLK. Data transfer format shown in FIG.

Mode 0: bSn_MST_CLK = 0

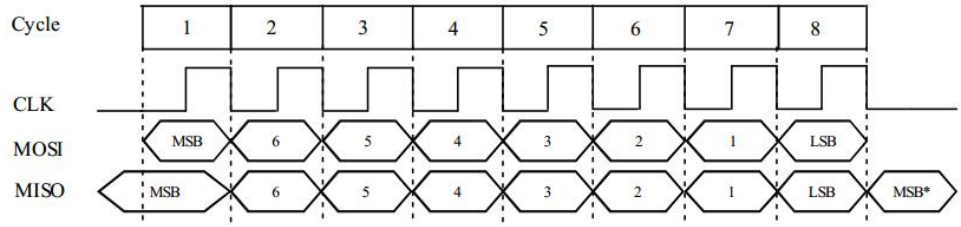



FIG 14.3.1 SPI timing diagram of Mode 0

Mode 3: bSn_MST_CLK = 1

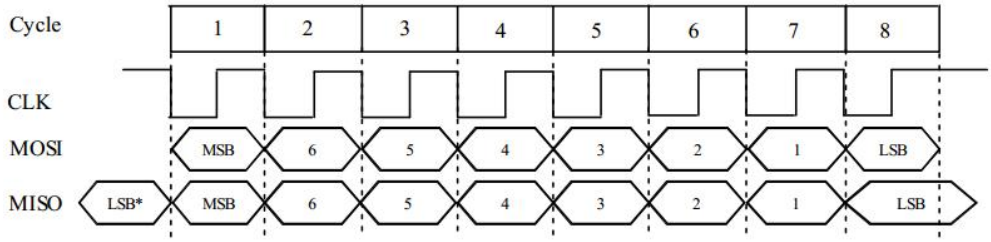



FIG 14.3.2 SPI timing diagram Mode 3

## 14.4 SPI configuration

### 14.4.1 SPI master mode configuration

The SPI master mode, SCK pin output serial clock, chip select output pins can be specified as any I / O pin.

SPI0 configuration steps:

(1), provided SPI clock divider setting register SPI0_CK_SE, arranged SPI clock frequency. (2), provided bS0_MODE_SLV SPI register setting bit 0 SPI0_SETUP is configured to host mode. (3), provided the SPI control register bit bS0_MST_CLK SPI0_CTRL, according to the demand mode is set to 0 or 3. (4), provided the SPI control register bits bS0_SCK_OE SPI0_CTRL and bS0_MOSI_OE is 1, bS0_MISO_OE bit is 0,

Set the port P1 direction bSCK, bMOSI output, bMISO input, an output and a chip select pin.

Data transmission process:

(1), SPI0_DATA write register, write data to be transmitted to the FIFO, automatically starts a SPI transfer. (2) waits for the S0_FREE 1, a transmission is completed, may continue to send the next byte.

Data receiving process:

(1), a write register SPI0_DATA, arbitrary data is written into the FIFO for example 0FFh to initiate a SPI transfer. (2) waits for the S0_FREE 1, a reception completion, can be obtained SPI0_DATA read received data. (3), if previously bS0_DATA_DIR been set, the read operation will start the next SPI transfer, or otherwise disable.

14.4.2 SPI slave mode configuration

Only SPI0 supports slave mode, slave mode, SCK pin is the serial clock for the SPI master receiving connection. (1), provided SPI0 bS0_MODE_SLV register bit set to 1 SPI0_SETUP, configured as a slave mode. (2), provided SPI0 bS0_SCK_OE control register bits and bS0_MOSI_OE SPI0_CTRL 0, to set bS0_MISO_OE

1, a P1 port direction bSCK, bMOSI and bMISO pins and chip select input. When SCS chip select is active (low), MISO output is automatically enabled. Also recommended set MISO pin is high impedance input mode (P1_MOD_OC [6] = 0, P1_DIR_PU [6] = 0), that the MISO output during no chip select is invalid, to facilitate the shared SPI bus. (3), optionally, SPI slave mode setting preset data register SPI0_S_PRE, for the first time is automatically loaded into the chip select buffer

For external output. After eight serial clock, i.e., the first data byte transfer exchange was finished, CH552 external SPI sent by the host to obtain the first byte of data (command code may be), the external preset data obtained SPI master exchange SPI0_S_PRE (possibly a state value). SPI0_S_PRE 7-bit register will be automatically loaded during the low level after SCK SPI chip select to the MISO pin for SPI mode 0, if preset SPI0_S_PRE CH552 bit 7, then the host will be selected in the external SPI SPI chip but yet effective transmission of data, it is possible to obtain the preset value of bit 7 SPI0_S_PRE by querying the MISO pin, so that the value can be obtained by bit 7 SPI0_S_PRE only valid SPI chip select bit.

Data transmission process:

S0_IF_BYTE query or wait for an interrupt, the SPI data after each byte transfer, SPI0_DATA write register, write data to be transmitted to the FIFO. Or wait S0_FREE from 0 to 1, may continue to send the next byte.

Data receiving process:

S0_IF_BYTE query or wait for an interrupt, the SPI data after each byte transfer, SPI0_DATA read register, the received data obtained from the FIFO. Queries S0_R_FIFO can know whether there are remaining byte FIFO.

## 15, analog to digital converter ADC and the voltage comparator (CH551 NA)

### About 15.1 ADC

CH552 chip provides 8-bit analog-digital converter, comprising a voltage comparator and the ADC modules. The converter has four analog input channels, time-sharing can collect, support VCC 0 to the analog input voltage range.

## 15.2 ADC Register

Table 15.2.1 ADC relevant register list

| name | address | description | Reset value |
|---|---|---|---|
| ADC_CTRL | 80h | ADC Control Register | x0h |
| ADC_CFG | 9AH | ADC configuration register | 00h |
| ADC_DATA | 9Fh | ADC data register | xxh |

ADC control register Register (ADC_CTRL):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | CMPO | RO | Voltage comparator result output bit, which is 0 indicates that voltage is lower than the inverting input voltage of the inverting input terminal; bit is one, the positive input voltage is higher than the voltage at the inverting input terminal | x |
| 6 | CMP_IF | RW | voltage comparator result change flag, which is a bit comparison shows voltage The result is a change, direct access bit is cleared | 0 |
| 5 | ADC_IF | RW | ADC conversion complete interrupt flag, the bit is 1 indicates an ADC conversion is complete, direct access bit is cleared | 0 |
| 4 | ADC_START | RW | ADC control start bit which is set to start an ADC conversion, the ADC bit is automatically cleared after the conversion is complete | 0 |
| 3 | CMP_CHAN | RW | voltage comparator inverting input terminal selection: 0-AIN1; 1-AIN3 | 0 |
| 2 | Retention | R0 | Reserved | 0 |
| 1 | ADC_CHAN1 | RW | voltage comparator inverting input terminal and ADC input channel high | 0 |
| 0 | ADC_CHAN0 | RW | voltage comparator inverting input terminal and ADC input channel low | 0 |

And a ADC_CHAN1 ADC_CHAN0 selection voltage comparator and the positive input terminal of ADC channels.

| ADC_CHAN1 | ADC_CHAN0 | Selection voltage comparator inverting input terminal and ADC input channel |
|---|---|---|
| 0 | 0 | AIN0 (P1.1) |
| 0 | 1 | AIN1 (P1.4) |
| 1 | 0 | AIN2 (P1.5) |
| 1 | 1 | AIN3 (P3.2) |

ADC configuration register Register (ADC_CFG):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 4] | Retention | R0 | Reserved | 0000b |
| 3 | ADC_EN | RW | Power control bit ADC module, which indicates the power supply is turned off ADC module 0, go to sleep; 1 indicates the bit is turned on | 0 |
| 2 | CMP_EN | | Power control bits RW voltage comparator, which indicates a voltage close to 0 Power comparator, goes to sleep; 1 indicates the bit is turned on | 0 |
| 1 | Retention | R0 | Reserved | 0 |
| 0 | ADC_CLK | RW | ADC reference clock frequency selection bit, which is slow clock select 0, each ADC 384 need cycles Fosc; the fast clock selection bit is 1, each ADC needs 96 cycles Fosc | 0 |

ADC data register Register (ADC_DATA ): Bit

| | name | access | description | Reset value |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| [7: 0] | ADC_DATA | RO | ADC data sampling results | xxh |

### 15.3 ADC function

ADC sampling mode configuration steps:

(1), provided ADC_EN ADC_CFG register bit is 1, the ADC module opening provided bADC_CLK selected frequency. (2), provided ADC_CTRL register ADC_CHAN1 / 0, to select the input channel.

(3), optional, clear flag ADC_IF. Alternatively, if you are using interrupt mode, you also need this to enable interrupts. (4), provided ADC_CTRL register adc_start, start ADC conversion.

(5), waiting ADC_START becomes 0, or ADC_IF is set (cleared if before), represents the ADC conversion, by

ADC_DATA read data. 255 aliquots of the data value of the input voltage with respect to the power source voltage VCC, e.g., the result data 47, the input voltage approaches described 47/255 VCC voltage. If the supply voltage VCC is not determined, the other can be a measured value determined by the reference voltage, then the calculated ratio of the measured value of the input voltage and the supply voltage VCC. (6), if you set once again at ADC_START ADC conversion can start.

Voltage comparator mode configuration steps:

(1), provided CMP_EN ADC_CFG register bit is 1, the turn-on voltage comparator module. (2), provided ADC_CTRL register ADC_CHAN1 / 0 and CMP_CHAN, selecting positive phase and the inverting input terminal. (3), optional, clear the flag CMP_IF.

(4), any time you can query the status of CMPO bit to get results for the current comparator. (5), if CMP_IF becomes 1, the result of the comparator changes.

Said selected analog input channel, it must be set in the GPIO pins into high impedance mode, or open drain output mode and state output 1 (corresponding to high impedance input), Pn_DIR_PU [x] = 0, and recommendations pull-ups and pull-down resistors off.

## 16, USB controller

## 16.1 USB Controllers

CH552 embedded USB controller and a USB transceiver, the following characteristics:

(1), supports the USB Device device functions, supports USB 2.0 full speed or low speed 12Mbps 1.5Mbps; (2), supports USB control transfer, bulk transfer, interrupt transfer, synchronous / real-time transmission; (3), supports a maximum of 64 bytes packet, built-in FIFO, interrupt support, and DMA.

CH552 the USB-related registers divided into two parts: USB USB endpoint registers and global registers.

### 16.2 global register

Table 16.2.1 USB global register list (gray scale control by the reset bUC_RESET_SIE) Name

| | address | description | Reset value |
|---|---|---|---|
| USB_C_CTRL | 91h | USB type-C channel control registers configured | 0000 0000b |
| USB_INT_FG | D8h | USB interrupt flag register | 0010 0000b |
| USB_INT_ST | D9h | USB Interrupt Status Register (read only) | 00xx xxxxb |
| USB_MIS_ST | DAh | Miscellaneous USB status register (read only) | xx10 1000b |
| USB_RX_LEN | DBh | Receiving USB length register (read only) | 0xxx xxxxb |
| USB_INT_EN | E1h | USB interrupt enable register | 0000 0000b |
| USB_CTRL | E2h | USB control register | 0000 0110b |
| USB_DEV_AD | E3h | USB Device Address Register | 0000 0000b |

**USB Channel configuration control type-C Deposit Device (USB_C_CTRL) :( CH551 NA)**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bVBUS2_PD_EN | RW | This bit is a 10K pull-down resistor internal to enable VBUS2 pin; 0 0 prohibition | |
| 6 | bUCC2_PD_EN | RW | This bit is a pull-down resistor 5.1K can make UCC2 internal pin; 0 prohibition | 0 |
| 5 | bUCC2_PU1_EN | RW | A pull-up resistor This bit controls the selection of the high internal pin UCC2 | 0 |
| 4 | bUCC2_PU0_EN | RW | This bit is a pull-up resistor internal selection control pin low UCC2 | 0 |
| 3 | bVBUS1_PD_EN | RW | This bit is a 10K pull-down resistor internal to enable VBUS1 pin; 0 0 prohibition | |
| 2 | bUCC1_PD_EN | RW | This bit is a pull-down resistor 5.1K can make UCC1 internal pin; 0 prohibition | 0 |
| 1 | bUCC1_PU1_EN | RW | This bit is a pull-up resistor internal selection control pin high UCC1 | 0 |
| 0 | bUCC1_PU0_EN | RW | This bit is a pull-up resistor internal selection control pin low UCC1 | 0 |

UCCn select the internal pin and by bUCCn_PU1_EN bUCCn_PU0_EN pull-up resistor.

| bUCCn_PU1_EN | bUCCn_PU0_EN | Select the internal pull-up resistor pin UCCn |
|---|---|---|
| 0 | 0 | Disable the internal pull-up resistor |
| 0 | 1 | 56KΩ internal pull-up resistors, the current representation provides default USB |
| 1 | 0 | Enables the internal pull-up resistor 22KΩ, the representation may be provided to 1.5A |
| 1 | 1 | 10KΩ enables the internal pull-up resistor, can be provided to 3A represents |

Pull-up resistor and said pull-down resistor is independent of the USB type-C Pn_DIR_PU port direction control and the pullup enable pullup port control register, when a pin is used for USB type-C, it should be prohibited corresponding to the pin pull-up resistor port, high impedance input mode is recommended to enable the pin (or output pin low to avoid the high level).

Details relating to the control and detecting input USB type-C refer to the channel configuration USB type-C Description and routines.

**USB in Interrupt flag register (U S B_INT_ FG):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | U_IS_NAK | RO | indicates that the current bit is a USB NAK transmission during a busy response is received; the Bit 0 indicates a non-received NAK response | 0 |
| 6 | U_TOG_OK | RO | current USB transmission DATA0 / 1 matches the synchronization flag status bit is 1, the The sync data is valid; 0 indicates the bit is not synchronized, the data may be invalid | 0 |
| 5 | U_SIE_FREE | RO | USB protocol processor idle bit, which indicates the busy bit is 0, the USB transfer in progress; this bit is 1 indicates that the USB is idle | 1 |
| 4 | UIF_FIFO_OV | RW | USB FIFO overflow interrupt flag, the bit is 1 indicates FIFO overflow interrupt; the bit is 0 without interruption. Direct access bit is cleared or write 1 to clear | 0 |
| 3 | Retention | RO | reserved. | 0 |
| 2 | UIF_SUSPEND | RW | USB bus suspend or wake-up event interrupt flag bit, which is 1 means interrupt, the interrupt from the USB suspend event or wake-up event trigger; the bit is 0 for no interruptions. Direct access bit is cleared or write 1 to clear | 0 |
| 1 | UIF_TRANSFER | RW | USB transfer complete interrupt flag bit, which is 1 means interrupt, the interrupt is triggered by the completion of a USB transfer; the bit is 0 for no interruptions. Direct access bit is cleared or write 1 to clear | 0 |
| 0 | UIF_BUS_RST | RW | USB bus reset event interrupt flag bit, which is 1 means interrupt, the interrupt is triggered by the USB bus reset event; this bit is 0 for no interruptions. Direct access bit is cleared or write 1 to clear | 0 |

USB Interrupt Status Register (USB_INT_ST):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUIS_IS_NAK | RO | indicates that the current bit is a USB NAK transmission during a busy response is received. With U_IS_NAK | 0 |
| 6 | bUIS_TOG_OK | RO | current USB transmission DATA0 / 1 matches the synchronization flag state, the bit is 1 It indicates synchronization; 0 indicates the bit is not synchronized. With U_TOG_OK | 0 |
| 5 | bUIS_TOKEN1 | RO | current USB transfer transaction identifier token PID high | x |
| 4 | bUIS_TOKEN0 | R0 | current token PID identifies the USB affairs low | x |
| [3: 0] | MASK_UIS_ENDP | RO | current endpoint number of the USB Affairs, 0000 indicating that the endpoint 0; ...; 1111 represents the end point 15 | xxxxb |

bUIS_TOKEN1 and bUIS_TOKEN0 composition MASK_UIS_TOKEN, identifies the current transaction of a USB token PID: 00 represents an OUT packet; represents SOF packet 01; 10 represents IN packet; 11 represents a SETUP packet.

**USB Miscellaneous like The status register (USB_MIS _ST):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 6] | Retention | RO | reserved. | xxb |
| 5 | bUMS_SIE_FREE | RO | USB protocol processor idle bit, which indicates the busy bit is 0, the USB transfer in progress; this bit is 1 indicates that the USB is idle. With U_SIE_FREE | 1 |
| 4 | bUMS_R_FIFO_RDY | RO | USB receiver FIFO data ready status bit, bit 0 indicates that the receiver FIFO is empty; the bit is 1 Receive FIFO Not Empty | 0 |
| 3 | bUMS_BUS_RESET | RO | USB bus reset state bit, which is 0 indicates that no USB bus reset; the bit is 1, are in a USB bus reset | 1 |
| 2 | bUMS_SUSPEND | RO | USB Suspend status bit, bit 0 indicates the currently active USB; 1 indicates the bit is not already some time USB activities, requests pending 0 | |
| [1: 0] | Retention | RO | reserved. | 00b |

**USB receiver long Of the register (USB_R X_LEN) :**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | bUSB_RX_LEN | RO | current USB endpoint number of bytes of the received data | xxh |

**USB in Interrupt Enable Register (USB _INT_E N):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUIE_DEV_SOF | RW | This bit is a SOF packet receive interrupt enable; 0 prohibition | 0 |
| 6 | bUIE_DEV_NAK | RW | This bit is a NAK is received interrupt enable; 0 prohibition | 0 |
| 5 | Retention | RO | reserved. | 0 |
| 4 | bUIE_FIFO_OV | RW | This bit is a FIFO overflow interrupt enable; 0 Close to the enable bit | 0 |
| 3 | Retention | RO | reserved. | 0 |
| 2 | bUIE_SUSPEND | RW | This bit to 1 enables USB bus suspend or interrupt wake-up events; 0 to disable | 0 |
| 1 | bUIE_TRANSFER | RW | This bit can complete interrupt 1 USB transfer so; the bit is 0 ban | 0 |
| 0 | bUIE_BUS_RST | RW | This bit is 1 Enable USB bus reset interrupt event; the bit is 0 ban | 0 |

**USB control System register (USB_CTR L ): Bit**

| | name | access | description | Reset value |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| 7 | Retention | RO reserved. | | 0 |
| 6 | bUC_LOW_SPEED | RW | USB bus signal transmission rate selection bit, which is 0 for full 12Mbps; bit selects the low speed of 1.5Mbps 1 | 0 |
| 5 | bUC_DEV_PU_EN | RW | USB devices, enable and internal pull control bit, which is a USB enabled device and enable transmission of the internal pullup | 0 |
| 5 | bUC_SYS_CTRL1 | RW | USB system control high | 0 |
| 4 | bUC_SYS_CTRL0 | RW | USB control system low | 0 |
| 3 | bUC_INT_BUSY | RW | USB transfer complete interrupt enable bit is automatically paused before the flag is not clear, this bit is an interrupt flag is automatically suspended before UIF_TRANSFER not cleared, it will automatically answer busy NAK; the bit is 0 and do not pause | 0 |
| 2 | bUC_RESET_SIE | RW | USB protocol processor software reset control bit, which is a forced reset and most USB USB protocol processor control registers need to be cleared by software | 1 |
| 1 | bUC_CLR_ALL | RW This bit is 1 Clear USB interrupt flag and FIFO, need to be cleared by software | | 1 |
| 0 | bUC_DMA_EN | RW This bit is a 1 to enable the USB interrupt and DMA DMA; 0 Enable Close | | 0 |

BUC_SYS_CTRL1 a USB system and control assembly bUC_SYS_CTRL0 composition:

| bUC_SYS_CTRL1 | bUC_SYS_CTRL0 | USB control system description |
|---|---|---|
| 0 | 0 | Disable USB device function to close the internal pullup |
| 0 | 1 | USB enabled device function, the internal pull-off, the need to add external pullup |
| 1 | X | USB enabled device function is enabled internal pull-up resistor 1.5KΩ. The pull-up resistor to the pull-down resistor precedence, GPIO mode can also be used |

**USB devices to Address Register (USB_DEV_AD)** :

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUDA_GP_BIT | RW | USB Universal flag: Users can customize the software can be set or cleared | 0 |
| [6: 0] | MASK_USB_ADDR | RW address the USB device | | 00h |

## 16.3 endpoints register

CH552 provides bidirectional terminal endpoints 0,1,2,3,4 five groups, the maximum packet length of 64 bytes are all endpoints. Endpoint Endpoint 0 is the default, support control transmission, transmission and reception of a common 64-byte data buffer. Endpoint 1 and Endpoint 2, each terminal 3 comprises a sending endpoint and a receiving endpoint IN OUT, each have a separate transmission and reception of 64 byte or double byte data buffer 64, to support the control transfer, bulk transfer, interrupt transfer, and Real-time / synchronous transmission.

4 comprises a transmitting endpoint IN endpoint byte data buffer 64 and a receiving endpoint OUT, each have a separate transmitting and receiving support control transfer, bulk transfer, interrupt transfer, and real-time / synchronous transmission.

Each endpoint having a response and transmitting data of OUT transactions and IN transactions, and a control register UEPn_CTRL transmit length register UEPn_T_LEN (n = 0/1/2/3/4), used to set the trigger bits of the synchronization endpoint, the length and the like.

Pull-up resistor may be provided at any time by software as a USB device on the USB bus required is enabled, the USB control register is set when bUC_DEV_PU_EN USB_CTRL in 1, CH552 was the DP according bUD_LOW_SPEED pull pin or the pin connector of the USB bus inside the DM resistance, and enable the USB device functionality.

When the USB bus reset is detected, or suspend the USB bus wake-up event, or when the USB After successfully processing the received data transmission or data, USB protocol handler will set the corresponding interrupt request flag and generates an interrupt. The application can directly query or USB interrupt service routine queries and analysis interrupt flag register USB_INT_FG, the appropriate treatment according to UIF_BUS_RST and UIF_SUSPEND; and, if UIF_TRANSFER effective, you also need to continue to analyze the USB interrupt status register USB_INT_ST, based on the current endpoint number MASK_UIS_ENDP current transaction token and the corresponding PID identification MASK_UIS_TOKEN process. If the preset trigger synchronization bit bUEP_R_TOG OUT affairs of each endpoint, you can U_TOG_OK or bUIS_TOG_OK

Analyzing the currently received data packet matches the bit synchronous triggering the trigger bits of the synchronization endpoint, if the data synchronization, the data is valid; if the data is not synchronized, then the data should be discarded. After each processed USB transmit or receive interrupt should trigger the right to modify the sync bit respective endpoint for the next data packet transmitted synchronization and detects whether the received data packet the next synchronization; Further, by providing the can bUEP_AUTO_TOG automatic trigger bits corresponding synchronization flip successful transmission or reception is successful.

Data length of each of the endpoint is ready to send in the respective buffer, ready to be sent is set independently UEPn_T_LEN; and each endpoint of each received data in the buffer, but the received data length are the length of the USB receiver USB_RX_LEN register may be distinguished based on the current when the USB endpoint number received interrupt.

Table 16.3.1 USB device endpoint list associated registers (gray scale control by the reset bUC_RESET_SIE) Name

| | address | description | Reset value |
|---|---|---|---|
| UDEV_CTRL | D1h | Physical USB device port control register | 10xx 0000b |
| UEP1_CTRL | Endpoint | Control register 1 D2h | 0000 0000b |
| UEP1_T_LEN | Endpoint 1 | D3h transmit length register | 0xxx xxxxb |
| UEP2_CTRL | Endpoint | Control register 2 D4h | 0000 0000b |
| UEP2_T_LEN | Length register | Endpoint 2 transmits D5h | 0000 0000b |
| UEP3_CTRL | Endpoint | Control Register 3 D6h | 0000 0000b |
| UEP3_T_LEN | Endpoint | transmit length register 3 D7h | 0xxx xxxxb |
| UEP0_CTRL | Endpoint | Control Register 0 DCh | 0000 0000b |
| UEP0_T_LEN | DDh transmit | length register Endpoint 0 | 0xxx xxxxb |
| UEP4_CTRL | Endpoint | Control register 4 DEh | 0000 0000b |
| UEP4_T_LEN | 4 transmit | length register endpoint DFh | 0xxx xxxxb |
| UEP4_1_MOD | EAh endpoint | mode control register 4 | 0000 0000b |
| UEP2_3_MOD | EBh endpoint | mode control register 3 | 0000 0000b |
| UEP0_DMA_H | EDh Endpoint | 0 and 4 buffer start address high byte | 0000 00xxb |
| UEP0_DMA_L | Endpoint 0 4 | ECh and the buffer start address low byte | xxxx xxxxb |
| UEP0_DMA | ECh | UEP0_DMA_L and UEP0_DMA_H composed of 16 SFR | 0xxxh |
| UEP1_DMA_H | EFh Endpoint | 1 buffer start address high byte | 0000 00xxb |
| UEP1_DMA_L | EEh Endpoint | 1 buffer start address low byte | xxxx xxxxb |
| UEP1_DMA | EEh | UEP1_DMA_L and UEP1_DMA_H composed of 16 SFR | 0xxxh |
| UEP2_DMA_H | E5h Endpoint | buffer start address high byte | 0000 00xxb |
| UEP2_DMA_L | Endpoint 2 | E4h buffer start address low byte | xxxx xxxxb |
| UEP2_DMA | E4h | UEP2_DMA_L and UEP2_DMA_H composed of 16 SFR | 0xxxh |
| UEP3_DMA_H | Endpoint | E7h buffer start address high byte 3 | 0000 00xxb |
| UEP3_DMA_L | Endpoint | E6h buffer start address low byte 3 | xxxx xxxxb |
| UEP3_DMA | E6h | UEP3_DMA_L and UEP3_DMA_H composed of 16 SFR | 0xxxh |

**USB Assume Preparation of a physical port control send Register ( UDEV_CTRL), by the reset control bUC_RESET_SIE:**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUD_PD_DIS | RW | USB device port UDP / pull-down resistor internal UDM pin disable bit, which is 1 to disable the internal pull-down resistor; bit 0 of the internal pulldown resistor. This bit is not bUSB_IO_EN control mode can also be used to provide the pull-down resistor GPIO | 1 |
| 6 | Retention | RO reserved. | | 0 |
| 5 | bUD_DP_PIN | RO UDP current state of the pin is low represents 0; 1 indicates a high level | | x |
| 4 | bUD_DM_PIN | RO UDM current state of the pin is low represents 0; 1 indicates a high level | | x |
| 3 | Retention | RO reserved. | | 0 |

| | | | | |
|---|---|---|---|---|
| 2 | bUD_LOW_SPEED | RW | USB device physical port speed mode enable bit, 1 bit of the low-speed mode selected is 1.5Mbps; this bit is 0 12Mbps full mode selection | 0 |
| 1 | bUD_GP_BIT | RW | General equipment flag: Users can define their own, can be set or cleared by software | 0 |
| 0 | bUD_PORT_EN | RW | Physical USB device port enable bit, which is 1 can make physical port; bit disables the physical port 0 | 0 |

**Endpoint n Control Register (UEP n_ CTRL) :**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUEP_R_TOG | RW | N USB endpoint receiver (processing SETUP / OUT transaction) of the desired synchronous trigger bit, which is 0 for a desired DATA0; represents the desired DATA1 1 | 0 |
| 6 | bUEP_T_TOG | RW | N USB endpoint transmitter (IN transaction processing) prepared synchronization trigger bit, which is 0 indicates send DATA0; 1 denotes a transmission DATA1 | 0 |
| 5 | Retention | RO reserved. | | 0 |
| 4 | bUEP_AUTO_TOG | RW | Bit synchronization is triggered automatically flip enable control bit, which is represented by a corresponding synchronization trigger automatically inverted position following a successful transmission or reception is successful; 0 indicates no flipping automatically, but can be manually switched. Only supports endpoint 1/2/3 | 0 |
| 3 | bUEP_R_RES1 | Endpoint n RW receiver response to the SETUP / OUT transaction control high | | 0 |
| 2 | bUEP_R_RES0 | Endpoint n RW receiver response to the SETUP / OUT transaction control low | | 0 |
| 1 | bUEP_T_RES1 | N RW endpoint transmitter in response to the high IN transaction control | | 0 |
| 0 | bUEP_T_RES0 | N RW endpoint transmitter in response to the IN transaction control low | | 0 |

The receiver and the bUEP_R_RES1 bUEP_R_RES0 MASK_UEP_R_RES composed of n for the control endpoint responds to the SETUP / OUT transaction: 00 indicates acknowledgment ACK or ready; 01 represents a time-out / no response, the endpoint for implementing the non-real-time / 0 synchronous transmission; 10 shows the response NAK or busy; 11 represents a response STALL or error.

MASK_UEP_T_RES bUEP_T_RES1 and a composition for controlling the endpoint bUEP_T_RES0 n transmitter responds to the IN transaction: 00 response DATA0 / DATA1 or the desired data ready and ACK; 01 a response indicating DATA0 / DATA1 and no response expected, for achieving non- real-time endpoint / 0 synchronous transmission; busy or NAK response indicating 10; 11 or STALL response indicating an error.

**Endpoint n transmit Length register (UEPn_T_L EN):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | bUEPn_T_LEN | RW number of data bytes is provided ready to send USB endpoint n (n = 0/1/3/4) | | xxh |
| | bUEP2_T_LEN | | USB endpoint number set ready to send data byte 2 | 00h |

**4 USB endpoint mode control register Unit (UEP 4_1_MOD):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUEP1_RX_EN | RW This bit is 0 prohibits receiving endpoint 1; 1 enables terminal 1 receives (OUT) | | 0 |
| 6 | bUEP1_TX_EN | RW This bit is 0 Disable Endpoint 1 transmits; 1 enable Endpoint 1 transmits (IN) | | 0 |
| 5 | Retention | RO reserved. | | 0 |
| 4 | bUEP1_BUF_MOD | Endpoint RW data buffer mode control bit 1 | | 0 |
| 3 | bUEP4_RX_EN | R0 4 receives this bit disables endpoint is 0; 1 to enable the receiving terminal 4 (OUT) | | 0 |
| 2 | bUEP4_TX_EN | RW This bit is 0 prohibits transmitting endpoint 4; 1 to enable transmission 4 Endpoint (IN) | | 0 |
| [1: 0] | Retention | RO reserved. | | 00b |

Controlled by the USB endpoint and bUEP4_TX_EN bUEP4_RX_EN composition data buffer mode 0 and 4, with reference to the following table.

Endpoint Table 16.3.2 Buffer Mode 0 and 4

| bUEP4_RX_EN bUEP4_TX_EN | Structure Description: UEP0_DMA to the start address arranged from low to high |
|---|---|

| | | |
|---|---|---|
| 0 | 0 | Endpoint 0 64 single-byte receive and transmit buffers (IN and OUT) |
| 1 | 0 | Endpoint 0 64 single-byte receive and transmit buffers; endpoint 4 single 64-byte receive buffer (OUT) |
| 0 | 1 | Endpoint 0 64 single-byte receive and transmit buffers; endpoint 4 single 64-byte transmit buffer (IN) |
| 1 | 1 | Endpoint 0 64 single-byte receive and transmit buffers; endpoint 4 single 64-byte receive buffer (OUT); endpoint 4 single 64-byte transmit buffer (IN). All 192 bytes arranged as follows:<br>UEP0_DMA + 0 Address: Endpoint 0 duplexer; UEP0_DMA + 64<br>Address: 4 receives endpoint; UEP0_DMA + 128 Address:<br>transmitting endpoint 4 |

**USB 2,3 endpoint control mode register (UEP2_3_MOD):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bUEP3_RX_EN | RW | this bit disables the reception terminal 3 is 0; 1 to enable the receiving end 3 (OUT) | 0 |
| 6 | bUEP3_TX_EN | RW | This bit is 0 prohibits transmission terminal 3; 3 1 enables transmission endpoint (IN) | 0 |
| 5 | Retention | RO | reserved. | 0 |
| 4 | bUEP3_BUF_MOD | | Endpoint RW mode control bit data buffer 3 | 0 |
| 3 | bUEP2_RX_EN | R0 | this bit disables the receiving terminal 2 is 0; 1 to enable the receiving terminal 2 (OUT) | 0 |
| 2 | bUEP2_TX_EN | RW | This bit is 0 prohibits sending endpoints 2; 2 enable transmission of Endpoint 1 (IN) | 0 |
| 1 | Retention | RO | reserved. | 0 |
| 0 | bUEP2_BUF_MOD | | Endpoint RW data buffer mode control bit 2 | 0 |

Control the USB endpoint data buffer mode and 1,2,3 bUEPn_RX_EN bUEPn_TX_EN and by (n = 1/2/3) combinations bUEPn_BUF_MOD, refer to the following table. Wherein the dual mode byte buffer 64, the data transfer according to the USB bUEP _ * _ TOG = 0 before the selected 64-byte buffer, according bUEP _ * _ TOG = 64 bytes 1 selection buffer, automatic switching.

Table 16.3.3 Buffer Mode Endpoint n (n = 1/2/3)

| bUEPn_RX_EN | bUEPn_TX_EN | bUEPn_BUF_MOD | Structure Description: UEPn_DMA to the start address arranged from low to high |
|---|---|---|---|
| 0 | 0 | x | Endpoint is disabled, unused buffer UEPn_DMA |
| 1 | 0 | 0 | Single 64-byte receive buffer (OUT) |
| 1 | 0 | 1 | Dual 64-byte receive buffer, by selecting bUEP_R_TOG |
| 0 | 1 | 0 | Single 64-byte transmit buffer (IN) |
| 0 | 1 | 1 | Dual 64-byte transmit buffer, by selecting bUEP_T_TOG |
| 1 | 1 | 0 | Single-byte receive buffer 64; 64 single-byte transmit buffer |
| 1 | 1 | 1 | Dual 64-byte receive buffer, by selecting bUEP_R_TOG; 64 double-byte transmit buffer, by selecting bUEP_T_TOG. All 256 bytes arranged as follows:<br>UEPn_DMA + 0 Address: bUEP_R_TOG = 0 endpoint receives; UEPn_DMA + 64 Address: bUEP_R_TOG = Endpoint receives 1; UEPn_DMA + 128 Address: bUEP_T_TOG = endpoint sends 0:00; UEPn_DMA + 192 Address: bUEP_T_TOG = Endpoint 1 transmits |

**USB endpoint n Buffer origin site (UEPn_ DMA) (n = 0/1/2/3):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| [7: 0] | UEPn_DMA_H | | Endpoint n RW high byte buffer start address, only lower 2 bits effective, 6 Fixed 0 | 0xh |
| [7: 0] | UEPn_DMA_L | RW | Endpoint n buffer start address low byte | xxh |

Note: the length of the received data buffer> = min (maximum packet length might receive 2 bytes + 64 bytes)

# 17, touch buttons Touch-Key

## 17.1 Touch-Key Profile

CH552 chip capacitor provides a detection module and associated timers having six input channels, to support capacity range 5pF ~ 150pF. Since capacitive can support up to six touch keys, mutual capacitance touch can support up to 15 keys.

## 17.2 Touch-Key Register

Table 17.2.1 Touch-Key associated register list

| name | address | description | Reset value |
|---|---|---|---|
| TKEY_CTRL | C3h | Touch-Key Control Register | x0h |
| TKEY_DATH | C5h | Touch-Key high byte data (read-only) | 00h |
| TKEY_DATL | C4h | Touch-Key low-byte data (read only) | xxh |
| TKEY_DAT | C4h | TKEY_DATL and TKEY_DATH composed of 16 SFR | 00xxh |

**Touch-Ke y Control Register (TKEY_C T RL):**

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bTKC_IF | RO | Timer interrupt flag. If bTKD_CHG = 0 is automatically set at the end of the current timing cycle an interrupt request, when the end of the preparation phase is automatically cleared, or cleared by writing TKEY_CTRL. If bTKD_CHG = 1 is automatically cleared, the interrupt is not requested, the current cycle is skipped, and the next cycle is detected and re-prepared and automatically set at the end of the next cycle of the interrupt request 1 | x |
| [6: 5] | Retention | RO reserved. | | 00b |
| 4 | bTKC_2MS | RW | The capacitance detection period of the timer selection: 0-1mS; 1-2mS. Week period before 87uS preparation stage, the remaining time detection phase. These times are based on the time when Fosc = 24MHz | 0 |
| 3 | Retention | RO reserved. | | 0 |
| 2 | bTKC_CHAN2 | RW touch key input selecting the capacitance detection high | | 0 |
| 1 | bTKC_CHAN1 | RW the capacitance detection touch key input selection bit | | 0 |
| 0 | bTKC_CHAN0 | RW capacitance touch key detecting low input selection | | 0 |

**By the bTKC_CHAN2 ~ BTKC_CHAN0 selected Optional touch button electric Capacitive detector input channel.**

| bTKC_CHAN2 | bTKC_CHAN1 | bTKC_CHAN0 | Selecting the capacitance detection touch key input channels |
|---|---|---|---|
| 0 | 0 | 0 | Close power capacitance detection module, or merely as a period of 1mS independent timer interrupt 2mS |
| 0 | 0 | 1 | TIN0 (P1.0) |
| 0 | 1 | 0 | TIN1 (P1.1) |
| 0 | 1 | 1 | TIN2 (P1.4) |
| 1 | 0 | 0 | TIN3 (P1.5) |
| 1 | 0 | 1 | TIN4 (P1.6) |
| 1 | 1 | 0 | TIN5 (P1.7) |
| 1 | 1 | 1 | Power-on detection module, but the capacitor is not connected to any channel |

Touch-Key Data Register (TKEY_DAT):

| Place | name | access | description | Reset value |
|---|---|---|---|---|
| 7 | bTKD_CHG<br>TKEY_DATH [7] | RO | Touch-Key control change flag. This bit is one, the capacitance is rewritten TKEY_CTRL detection stage, may cause TKEY_DAT data is invalid, and did not mention bTKC_IF end of the current cycle. This bit is set each<br>Preparation phase cycle is automatically cleared when the end, the mask bit of data to be taken | 0 |
| 6 | Retention | RO reserved. | | 0 |
| [5: 0] | TKEY_DATH | RO | Touch-Key high byte of data. Automatically cleared at the end of each timing cycle of the preparation phase; automatic counting stage capacitance detection; data preparation phase remains unchanged, so that the timer interrupt routine read | 00h |
| [7: 0] | TKEY_DATL | RO | Touch-Key low-byte data. Automatically cleared at the end of each timing cycle of the preparation phase; automatic counting stage capacitance detection; data preparation phase remains unchanged, so that the timer interrupt routine read | xxh |

## 17.3 Touch-Key function

Capacitance detecting step:

(1), provided TKEY_CTRL register bTKC_2MS and bTKC_CHAN2 ~ bTKC_CHAN0, the input channel selection period. Is

Selected input channels, it must be set in the GPIO pins into high impedance mode, or open drain output mode and state output 1 (corresponding to high impedance input), Pn_DIR_PU [x] = 0.

(2) cleared bTKC_IF and enable interrupts IE_TKEY wait timer interrupt, or by initiative inquiry into the bTKC_IF interrupt routine. (3), the capacitance detection of the current channel is automatically set preparation phase bTKC_IF interrupt request, while after the next cycle is completed,

TKEY_DAT unchanged and maintain data about 87uS.

(4), entering the interrupt routine, first reads capacitance data from TKEY_DAT the current channel, and the highest bit mask bTKD_CHG, the

Data are relative values, and inversely proportional to the capacitance, when the touch data is smaller than the key depression data is not pressed. (5), provided TKEY_CTRL register bTKC_2MS and bTKC_CHAN2 ~ bTKC_CHAN0, select the next input channel. That

Write automatically cleared bTKC_IF, end interrupt request.

(6), data TKEY_DAT data (4) and the step of reading a previously saved without the key channel, and determines whether the change in capacitance

And if a key is pressed.

(7), a return from interrupt immediately after completion of the capacitance detecting a passage to step (3).

## 18, parameters

**18.1 absolutely Correct The maximum value (equal to or exceed absolute maximum value will likely cause the chip to work Do not Normal or even loss Bad)**

| name | Parameter Description | Minimum | Maximum | unit |
|---|---|---|---|---|
| TA | When the ambient temperature is less than the system frequency 28MHz work Fsys | - 40 | 85 | ℃ |
| TA32M | When the ambient temperature is greater than the system frequency 28MHz work Fsys | --20 | 70 | ℃ |
| TS | The ambient temperature during storage | - 55 | 125 | ℃ |
| VCC | Supply voltage (VCC power supply connected, GND Ground) | - 0.4 | 5.8 | V |
| VIO | In addition to the other input P3.6 / P3.7 or voltage on the output pin | - 0.4 | VCC + 0.4 | V |
| VIOU | The voltage on the P3.6 / P3.7 input or output pin | - 0.4 | V33 + 0.4 | V |

**18.2 Electric Gas parameters 5V (test conditions: TA = 25 ℃, VCC = 5V, Fsys = 6MHz)**

| name | Parameter Description | | Min | Typ | Max | unit |
|---|---|---|---|---|---|---|
| VCC5 | Supply voltage VCC pin | V33 only external capacitor | 3.7 | 5 | 5.5 | V |
| V33 | Internal USB output voltage of the power regulator | | 3.14 | 3.27 | 3.4 | V |

| | | | | | |
|---|---|---|---|---|---|
| ICC24M5 | The total supply current work Fsys = 24MHz | 8 | 11 | | mA |
| ICC6M5 | The total supply current work Fsys = 6MHz | 4 | 6 | | mA |
| ICC750K5 | The total supply current work Fsys = 750KHz | 2 | 3 | | mA |
| ISLP5 | The total supply current after sleep | | 0.1 | 0.2 mA | |
| ISLP5L | VCC = V33 = 5V, and an optional external crystal clock, BLDO3V3_OFF = 1 and off LDO, the total supply current total sleep | | 0.008 | 0.02 | mA |
| IADC5 | ADC analog to digital converter module operating current | | 200 | 800 | uA |
| ICMP5 | The comparator module operating current | | 100 | 500 | uA |
| ITKEY5 | The capacitance detection touch key operation current | | 150 | 250 | uA |
| VIL5 | Low level input voltage | - 0.4 | | 1.2 | V |
| VIH5 | High-level input voltage | 2.4 | | VCC + 0.4 | V |
| VOL5 | Low Output Voltage (12mA current sinking) | | | 0.4 | V |
| VOH5 | High level output voltage (output current 8mA) | VCC-0.4 | | | V |
| VOH5U | P3.6 / P3.7 high-level output voltage (output current 8mA) V33-0.4 | | | | V |
| IIN | No pull-input of the input current | --5 | 0 | 5 | uA |
| IDN5 | Input current with the input pull-down resistor | - 35 | --70 | - 140 | uA |
| IUP5 | Pull-up resistor input of the input current | 35 | 70 | 140 | uA |
| IUP5X | Pull input to the input end is low at a high switching current | 250 | 400 | 600 | uA |
| Vpot | Power-on reset threshold voltage | 2.1 | 2.3 | 2.5 | V |

18.3 Electric Gas parameters 3.3V (test conditions: TA = 25 ℃, VCC = V33 = 3 .3V, Fsys = 6MHz)

| name | Parameter Description | | Min Typ Max unit | | | |
|---|---|---|---|---|---|---|
| VCC3 | VCC pin voltage | V33 shorted to VCC, open USB | 3.0 | 3.3 | 3.6 | V |
| | | V33 shorted to VCC, turn off USB | 2.5 | 3.3 | 3.6 | V |
| ICC16M3 | The total supply current work Fsys = 16MHz | | 4 | 6 | | mA |
| ICC6M3 | The total supply current work Fsys = 6MHz | | 2 | 4 | | mA |
| ICC750K3 | The total supply current work Fsys = 750KHz | | 1 | 2 | | mA |
| ISLP3 | The total supply current after sleep | | | 0.07 | 0.15 | mA |
| ISLP3L | bLDO3V3_OFF = 1 closed LDO, the total supply current total sleep | | | 0.004 | 0.01 | mA |
| IADC3 | ADC analog to digital converter module operating current | | | 150 | 500 | uA |
| ICMP3 | The comparator module operating current | | | 70 | 300 | uA |
| ITKEY3 | The capacitance detection touch key operation current | | | 130 | 200 | uA |
| VIL3 | Low level input voltage | | - 0.4 | | 0.8 | V |
| VIH3 | High-level input voltage | | 1.9 | | VCC + 0.4 | V |
| VOL3 | Low-level output voltage (current sinking 8mA) | | | | 0.4 | V |
| VOH3 | High level output voltage (output current 5mA) | | VCC-0.4 | | | V |
| VOH3U | P3.6 / P3.7 high-level output voltage (output current 8mA) V33-0.4 | | | | | V |
| IIN | No pull-input of the input current | | --5 | 0 | 5 | uA |
| IDN3 | Input current with the input pull-down resistor | | --15 | --30 | - 60 | uA |
| IUP3 | Pull-up resistor input of the input current | | 15 | 30 | 60 | uA |
| IUP3X | Pull input to the input end is low at a high switching current | | 100 | 170 | 250 | uA |
| Vpot | Power-on reset threshold voltage | | 2.1 | 2.3 | 2.5 | V |

18.4 When Order parameter (test conditions: TA = 25 ℃, VCC = 5V or VCC = V 33 = 3.3V, F s ys = 6MHz)

| name | Parameter Description | Min Typ Max unit | | | |
|---|---|---|---|---|---|
| Fxt | Frequency external crystal or clock frequency input XI | 6 | twenty four | 25 | MHz |
| Fosc | V33 = 3V ~ 23.64 by the internal clock frequency after calibration when 3.6V | | twenty four | 24.36 | MHz |
| Fosc27 | V33 = 2.7V ~ 23.28 by the internal clock frequency calibrated at 3V | | twenty four | 24.72 | MHz |
| Fosc25 | Internal clock frequency after V33 = 2.5V calibrated | twenty one | twenty four | 27 | MHz |
| Fpll | After the internal PLL frequency multiplier | twenty four | 96 | 100 | MHz |
| Fusb4x | When using the USB device function, USB sampling clock frequency | 47.04 | 48 | 48.96 | MHz |
| Fsys | Clock frequency of the system frequency (VCC> = 4.9V) | 0.1 | 6 | 32 | MHz |
| | Clock frequency of the system frequency (4.9V> VCC> = 4.0V) | 0.1 | 6 | twenty four | MHz |
| | Clock frequency of the system frequency (4.0V> VCC> = 2.8V) | 0.1 | 6 | 16 | MHz |
| | Clock frequency of the system frequency (VCC <2.8V) | 0.1 | 6 | 12 | MHz |
| Tpor | Power on Reset delay | 9 | 11 | 15 | mS |
| Trst | Active reset signal RST input from the outside width | 70 | | | nS |
| Trdl | Warm Reset Delay | 30 | 45 | 60 | uS |
| Twdc | Calculated watchdog timeout period / timing period 65536 * (0x100 - WD O G_COUNT) / Fsys | | | | |
| Tusp | Automatic detection of USB suspend time | 4 | 5 | 6 | mS |
| Twak | After the chip sleep wake completion time | 1 | 2 | 10 | uS |

19, modify the record

| version | date | Explanation |
|---|---|---|
| V1.0 | 2016.12.20 | Original Issue |
| | | |